Evaluation Board for Small Form Factor (SFF) Through Hole Transceivers

AVAGO TECHNOLOGIES

Application Note 1245

SFF Evaluation Board

The purpose of this Small Form Factor (SFF) through hole evaluation board is to provide the designer with a convenient means to evaluate the performance of 10- or 12-pin SFF fiber optic transceivers such as the HFBR-5921L and HFBR-5923L, as well as future SFF MSA compatible product offerings. This document describes the details of the evaluation printed circuit board (PCB) and the test equipment and methods for evaluating SFF modules. The detailed operation of the SFF modules and test equipment used with this evaluation PCB are not described in this document, but can be found by obtaining the appropriate documents from the reference section.

Document Outline

I. Equipment List

Included:

1. Evaluation PCB
2. SFF 2 x 6 transceiver module(s)

Not Included:

1. 3.3 V DC power supply
2. Fiber optic cables
   - LC to SC (1 M and 50/125 μm or 62.5/125 μm)
   - LC to LC Loopback (<1 M and 50/125 μm or 62.5/125 μm or 9/125 μm)
3. 86100A Agilent Digital Communications Analyzer (DCA)
4. 86103A Agilent Optical/Electrical DCA Plug-In Module Option H43 or H21 (2.125 FC)
5. 86130A Agilent Bit Alyzer 3 Gb/s Bit Error Rate Tester (BERT)
   - Pattern generator, error detector/analyzer
6. Fiber Optic Attenuator (optional)
7. PC (optional)

II. Evaluation PCB Description

Top and bottom views of the evaluation PCB are shown in Figure 1. A description of all of the Input/Output (I/O) interfaces on the PCB is shown in Table 1, all of which are found, on the topside of the PCB. The evaluation PCB is a 4-layer design compatible with high-speed signal I/O rates up to 2.125 GBd.

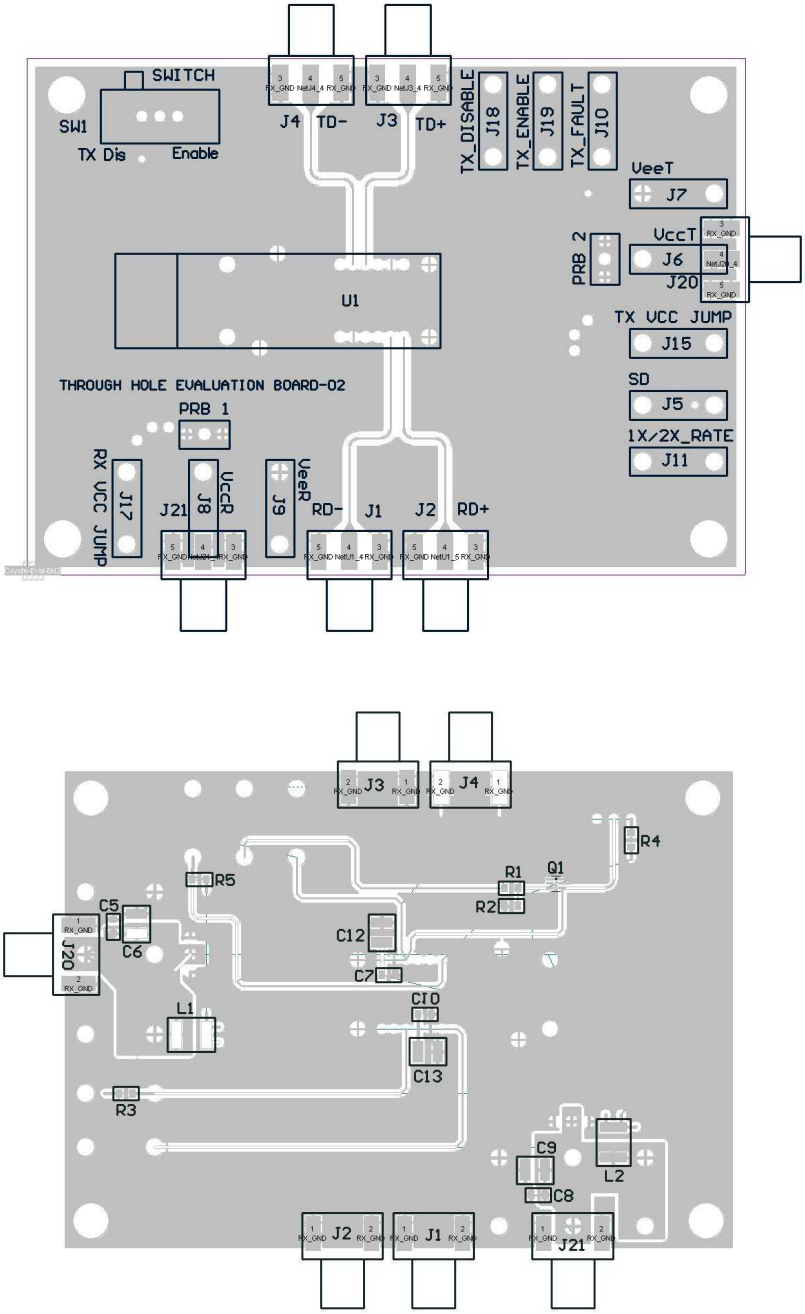


Figure 1. SFF Evaluation Board Top and Bottom View

Table 1 - I/O Description

Reference Designator	Name	Description	Signal Level
J1	RD -	Differential receiver outputs	PECL, Note 1
J2	RD +		
J3	TD +	Differential transmitter inputs (<2.4 V)	PECL, Note 1
J4	TD -		
J5	SD	Signal Detect Output: High indicates sufficient optical power. Low indicates insufficient optical power	LVTTL*
J6	VccT	Transmitter Power	3.3 V
J7	VeeT	Transmitter Ground	GND
J8	VccR	Receiver Power	3.3 V
J9	VeeR	Receiver Ground	GND
J10	TX Fault	Transmitter Fault Output: High output indicates a laser fault, Low indicates normal laser operation	LVTTL* Note 2
J11	1X/2X Rate	Rate Select Pin, Not Connected	
J15	TX VCC JUMP	Jumps Vcc	
J17	RX VCC JUMP		
J18	TX_DISABLE	Not Connected	
J19	TX_ENABLE	Not Connected. Can be used to electrically to switch TX_DISABLE	
J20		Not Connected	
J21		Not Connected	
SW1	TX_DISABLE Switch	Transmitter Disable Input: Enable (low signal) enables the transmitter, Disable position (high signal) disables the transmitter.	LVTTL*
U1	PTH foot print	Module plugs here	

Notes

1. See specific transceiver data sheet for recommended maximums and further information.
2. TX_FAULT available only on 2 x 6 pin module package.

* LVTTL defines a 3.3 voltage level with transitions at 0.8 and 2.0 V.

III. Electro-Optical Test Configuration(s)

The two basic test configurations for evaluating the 10- or 12-pin SFFs are shown in Figure 2 (transmitter) and Figure 3 (receiver or loopback). These test configurations use one evaluation board and the test instruments from the equipment list, such as a Bit-Error-Ratio Tester (BERT) and a Digital Communication Analyzer (DCA). General considerations from the test configuration follow, but more specific details on SFF transceiver testing can be found in the documents listed in the reference section of this document.

Transmitter Configuration:

This configuration is shown in Figure 2. The SFF's optical characteristics can be tested including the eye diagram, jitter, and rise/fall time. A representative eye diagram for an SFF is shown in Figure 4. In this configuration, the receiver is not used, however it is recommended that RD- and RD+ be terminated by 50 Ω matched loads. It is also recommended that low loss, low dispersion, and equal length RF cables be used to connect TD+/- to the test equipment.

Receiver Configuration

This configuration is shown in Figure 3. The SFF's electrical characteristics can be tested including the receiver electrical eye diagram, jitter, and rise/fall time. A representative eye diagram for an SFF is shown in Figure 5.

Results

The following example measurements were made using the configurations illustrated in Figures 2 and 3 respectively.

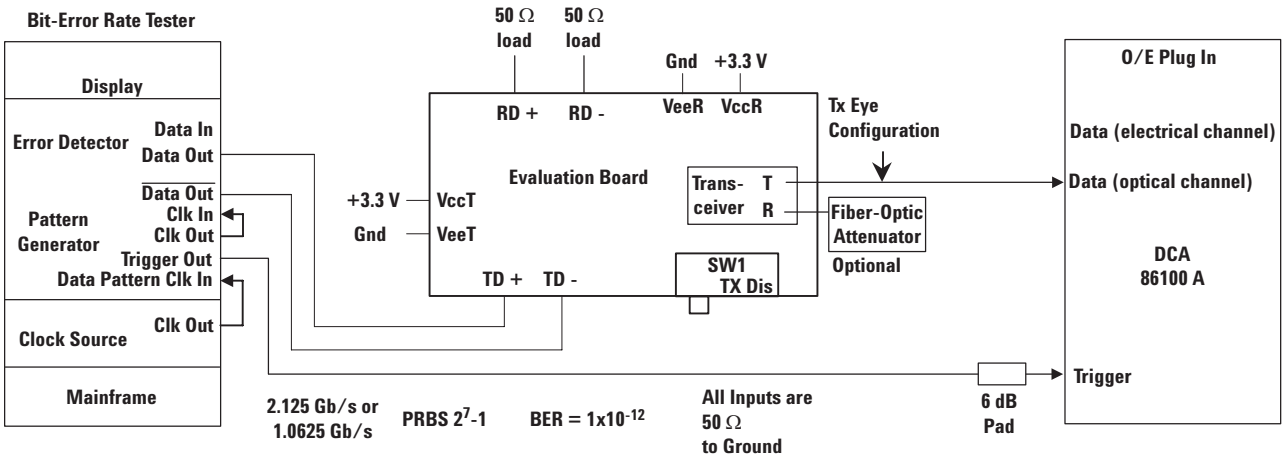


Figure 2. Recommended Transmitter Test Configuration

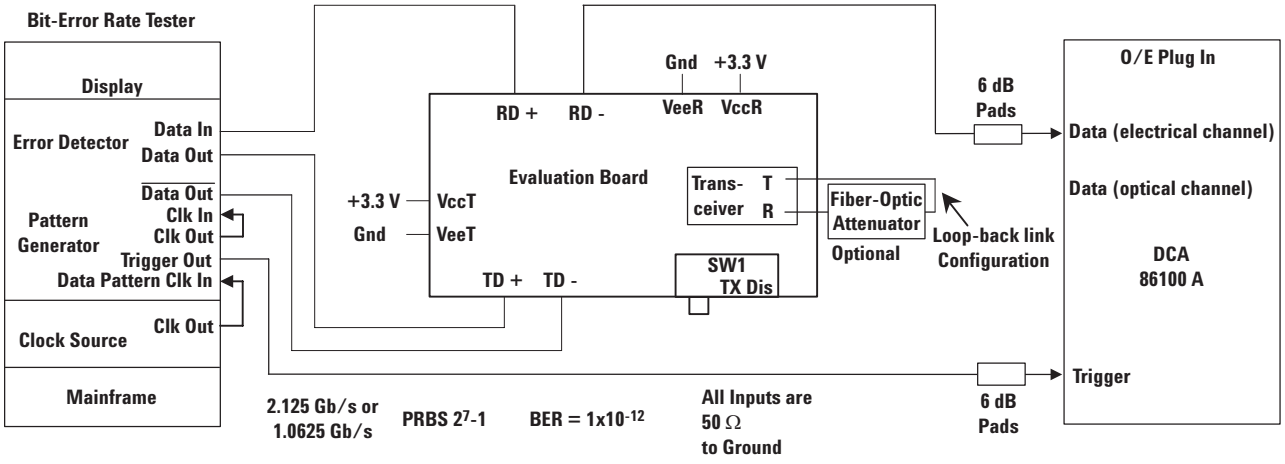


Figure 3. Recommended Receiver Configuration

IV. Evaluation Board Schematic and Bill of Materials

The SFF evaluation PCB electrical schematic is shown in Figure 6 at the end of this document. The user may notice connections on the board which are not represented on this schematic (Figure 6) or pin description (Table 1). This is due to optional functionality of the board. For simplicity and ease of application, only those connections and parts included are described in the schematic and bill of materials (Table 2).

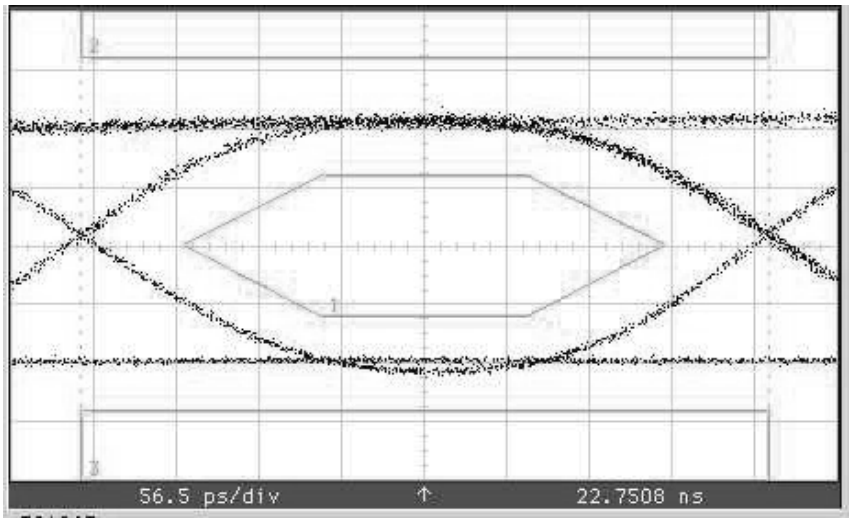


Figure 4. Example Transmitter Eye Diagram

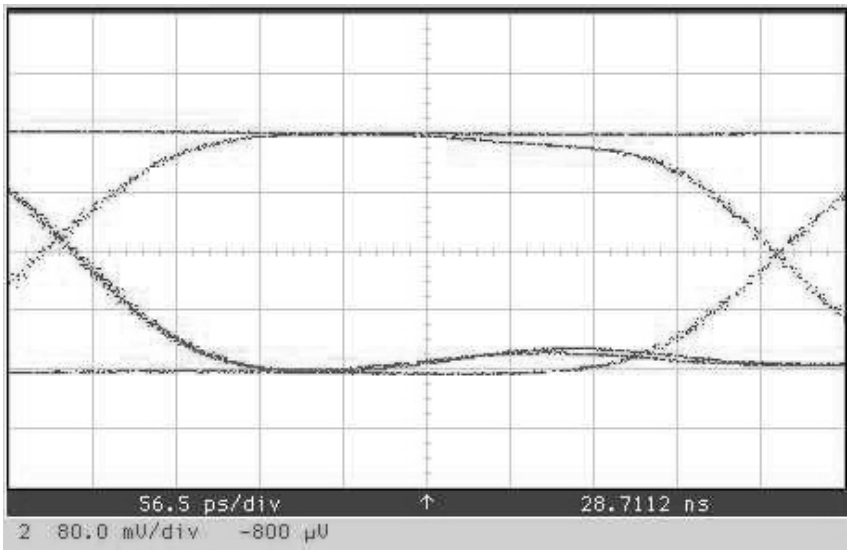
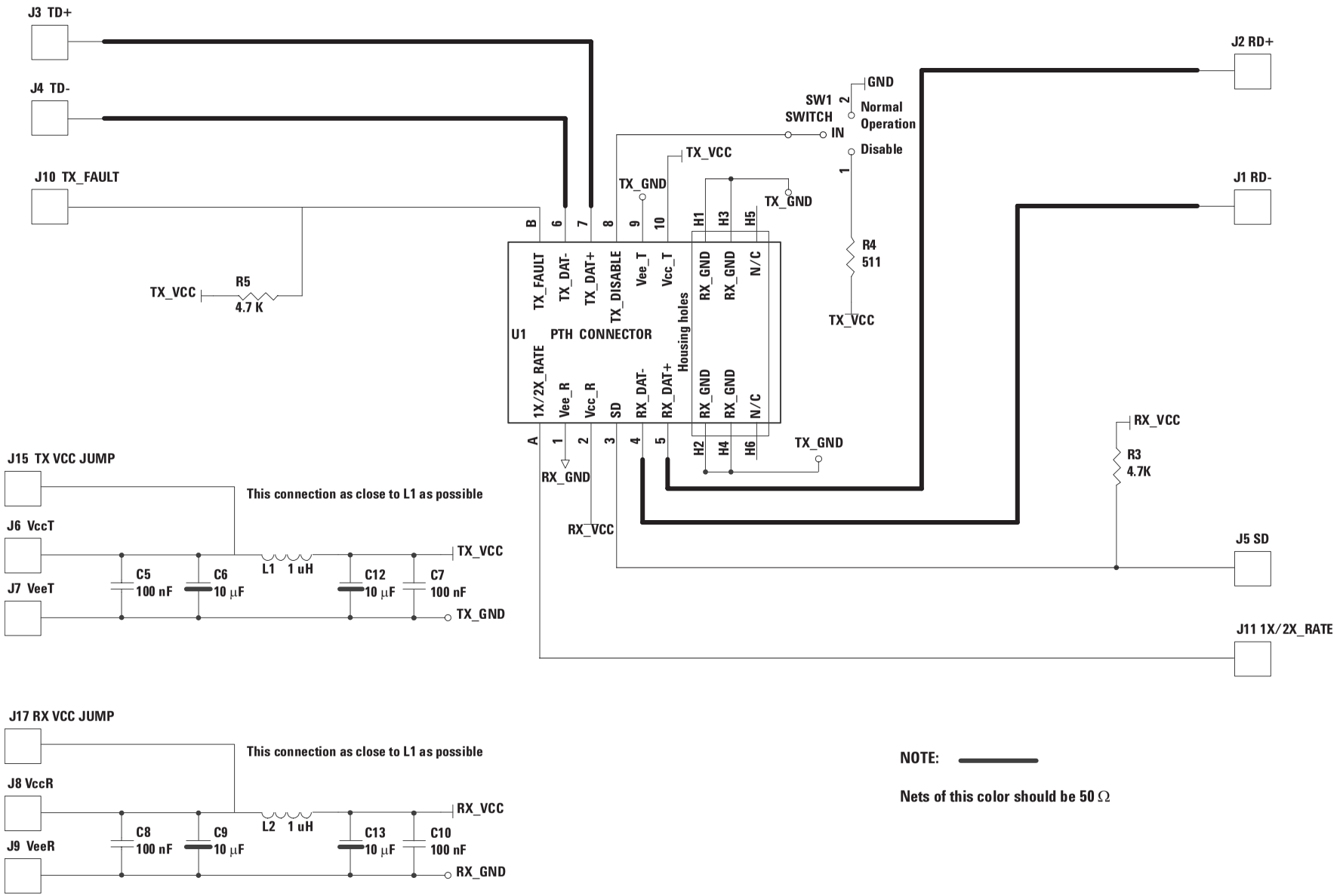


Figure 5. Example Loop Back Receiver Eye Diagram-17 dBm power

Table 2 - SFF Evaluation Board Bill of Materials.

Component	Type	Value	Footprint	Comments
PCB	SFF Evaluation Board			Unpopulated 4 layer circuit board
U1	Surface Mount Socket (20 pin)			AMP 1367073-1
	Case jacks			0 (4off), Advance Interconnect part 1718 or Cambion 450-3704-01-03-00
Q1	Transistor		UMX3N	Rohm dial NPN transistor, not included
	Device jacks			
	Nose jacks			0 (2 off), Cambion part 450-3704-01-03-00
R4	Resistor	511 Ω	0805	
R3,R5	Resistor	4.7 kΩ	0805	Not connected
C5,C7,C8,C10	Capacitor	0.1 μF	0805	10% Tolerance
C6,C9,C12,C13	Capacitor	10 μF	Case code B	Tantalum 20% Tolerance
L1,L2	Inductor	1 μF	1812	
SW1	Switch			Apem 25336NA
J1,J2,J3,J4	End launch SMA jacktab contact			Johnson Components part number 142-0701-851
J5,J10,J11,J18,J19	Jack, 2 mm white			
J6,J8,J15,J17	Jack, 2 mm red			
J7,J9	Jack 2 mm black			



NOTE: ——

Nets of this color should be 50 Ω

Figure 6. SFF Evaluation Board Schematic

VI. References

1. HFBR-59xx Product Data Sheets

2. Avago Technologies' Application Notes (AN)
   – **http://www.avagotech.com**

3. Small Form Factor (SFF) Transceiver Multi-Source Agreement. Revised July 5, 2000. Please contact your local Avago Technologies field sales engineer for a copy of this document.

4. Small Form Factor Pluggable (SFP) Transceiver Multi-Source Agreement. Revised September 14, 2000. Please contact your local Avago Technologies field sales engineer for a copy of this document.

5. Test Equipment User Manuals

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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