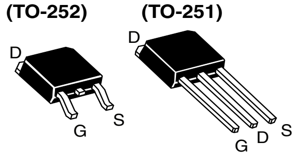
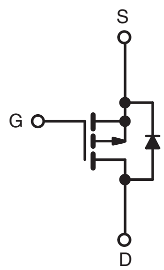
Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	- 400	
$R_{DS(on)}$ (Ω)	V_{GS} = - 10 V	7.0
Q_g (Max.) (nC)	13	
Q_{gs} (nC)	3.2	
Q_{gd} (nC)	5.0	
Configuration	Single	

DPAK (TO-252) **IPAK (TO-251)**





P-Channel MOSFET

FEATURES

- P-Channel
- Surface Mount (IRFR9310, SiHFR9310)
- Straight Lead (IRFU9310, SiHFU9310)
- Advanced Process Technology
- Fast Switching
- Fully Avalanche Rated
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE Available

DESCRIPTION

Third generation power MOSFETs from Vishay utilize advanced processing techniques to achieve low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.
The DPAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU/SiHFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 W are possible in typical surface mount applications.

ORDERING INFORMATION					
Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free and Halogen-free	SiHFR9310-GE3	SiHFR9310TRL-GE3	SiHFR9310TR-GE3	SiHFR9310TRR-GE3	SiHFU9310-GE3
Lead (Pb)-free	IRFR9310PbF	IRFR9310TRLPbF[a]	IRFR9310TRPbF[a]	IRFR9310TRRPbF[a]	IRFU9310PbF
	SiHFR9310-E3	SiHFR9310TL-E3[a]	SiHFR9310T-E3[a]	SiHFR9310TR-E3[a]	SiHFU9310-E3

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)					
PARAMETER			**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage			V_{DS}	- 400	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current	V_{GS} at - 10 V	T_C = 25 °C	I_D	- 1.8	A
		T_C = 100 °C		- 1.1	
Pulsed Drain Current[a]			I_{DM}	- 7.2	
Linear Derating Factor				0.40	W/°C
Single Pulse Avalanche Energy[b]			E_{AS}	92	mJ
Repetitive Avalanche Current[a]			I_{AR}	- 1.8	A
Repetitive Avalanche Energy[a]			E_{AR}	5.0	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	50	W
Peak Diode Recovery dV/dt[c]			dV/dt	- 24	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)[d]	for 10 s			300	

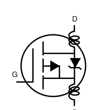
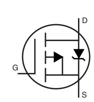
Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Starting T_J = 25 °C, L = 57 mH, R_g = 25 Ω, I_{AS} = - 1.8 A (see fig. 12).
c. $I_{SD} \leq$ - 1.1 A, dI/dt $\leq$ 450 A/μs, $V_{DD} \leq V_{DS}$, $T_J \leq$ 150 °C.
d. 1.6 mm from case.

THERMAL RESISTANCE RATINGS					
PARAMETER	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	-	-	110	°C/W
Maximum Junction-to-Ambient (PCB Mount)[a]	R_{thJA}	-	-	50	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	-	2.5	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 μA		- 400	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = - 1 mA		-	- 0.41	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 μA		- 2.0	-	- 4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 400 V, V_{GS} = 0 V		-	-	- 100	μA
		V_{DS} = - 320 V, V_{GS} = 0 V, T_J = 125 °C		-	-	- 500	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = - 10 V	I_D = - 1.1 A[b]	-	-	7.0	Ω
Forward Transconductance	g_{fs}	V_{DS} = - 50 V, I_D = - 1.1 A		0.91	-	-	S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = - 25 V, f = 1.0 MHz, see fig. 5		-	270	-	pF
Output Capacitance	C_{oss}			-	50	-	
Reverse Transfer Capacitance	C_{rss}			-	8.0	-	
Total Gate Charge	Q_g	V_{GS} = - 10 V	I_D = - 1.1 A, V_{DS} = - 320 V, see fig. 6 and 13[b]	-	-	13	nC
Gate-Source Charge	Q_{gs}			-	-	3.2	
Gate-Drain Charge	Q_{gd}			-	-	5.0	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 200 V, I_D = - 1.1 A, R_g = 21 Ω, R_D = 180 Ω, see fig. 10[b]		-	11	-	ns
Rise Time	t_r			-	10	-	
Turn-Off Delay Time	$t_{d(off)}$			-	25	-	
Fall Time	t_f			-	24	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact[c]		-	4.5	-	nH
Internal Source Inductance	L_S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	- 1.9	A
Pulsed Diode Forward Current[a]	I_{SM}			-	-	- 7.6	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = - 1.1 A, V_{GS} = 0 V[b]		-	-	- 4.0	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = -1.1 A, dI/dt = 100 A/μs[b]		-	170	260	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	640	960	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.

c. This is applied for IPAK, L_S of DPAK is measured between lead and center of die contact.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

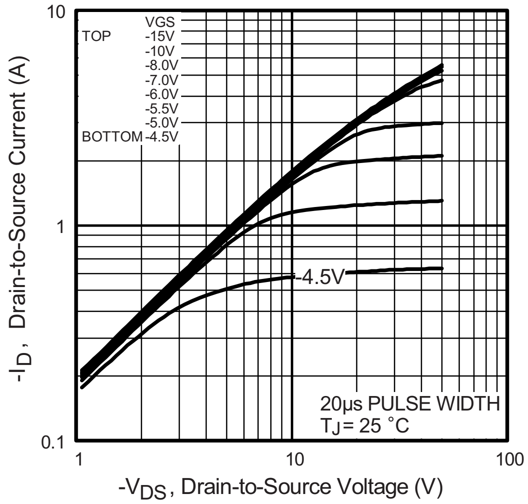


Fig. 1 - Typical Output Characteristics

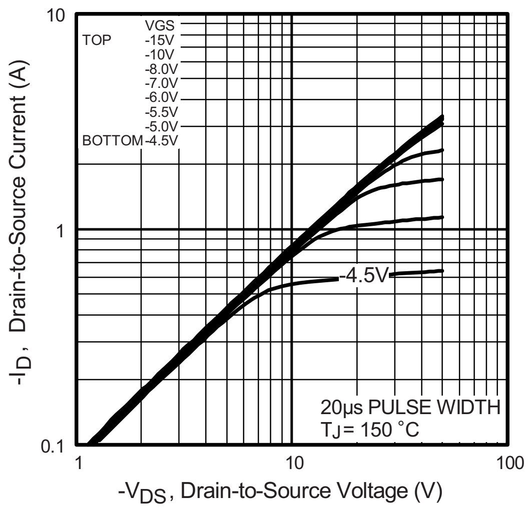


Fig. 2 - Typical Output Characteristics

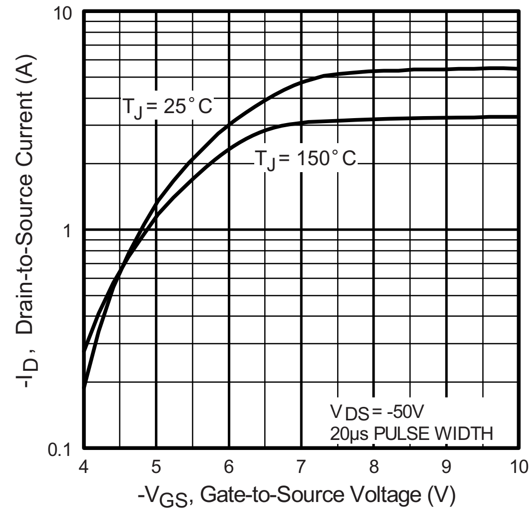


Fig. 3 - Typical Transfer Characteristics

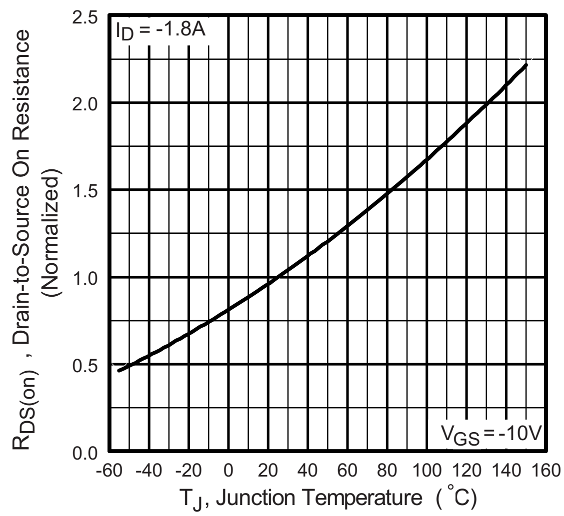


Fig. 4 - Normalized On-Resistance vs. Temperature

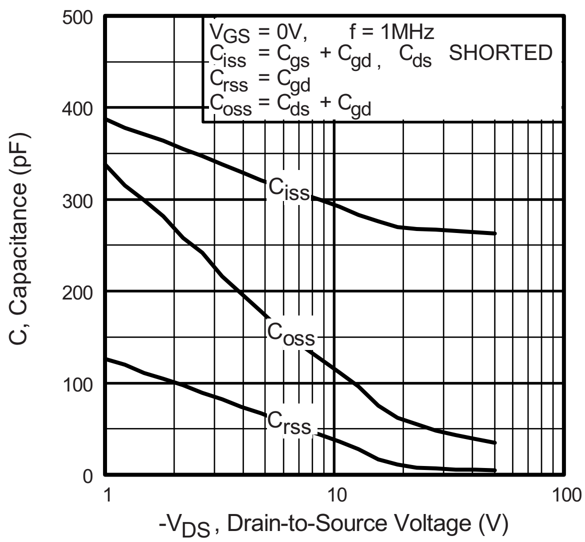


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

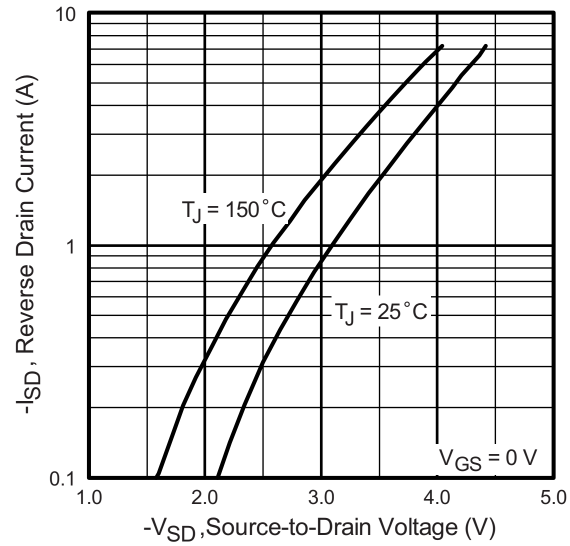


Fig. 7 - Typical Source-Drain Diode Forward Voltage

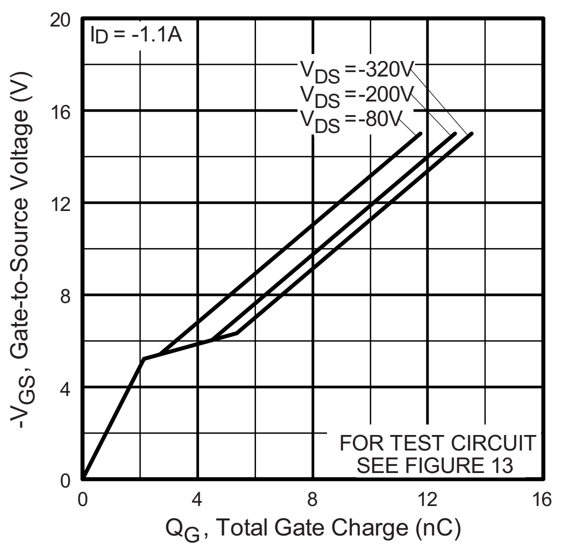


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

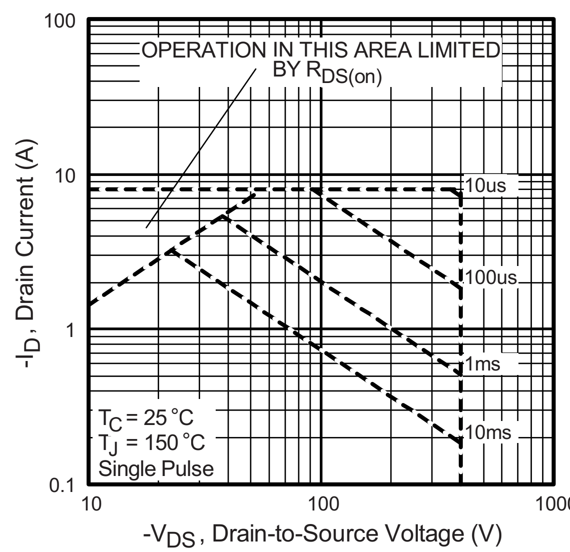


Fig. 8 - Maximum Safe Operating Area

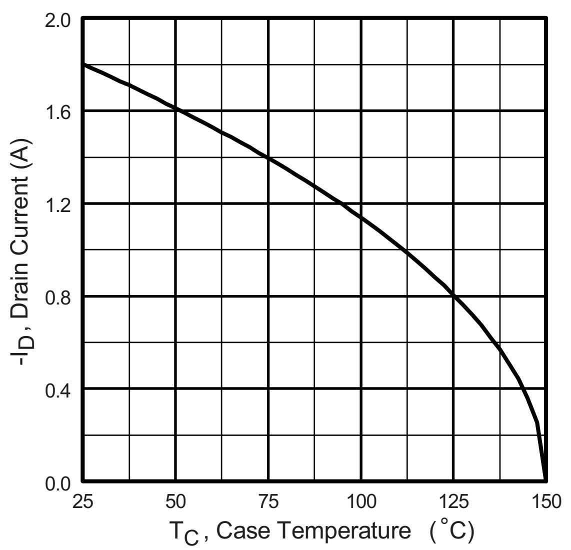


Fig. 9 - Maximum Drain Current vs. Case Temperature

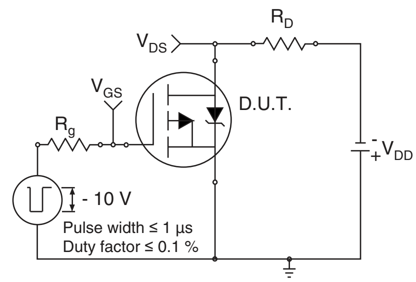


Fig. 10a - Switching Time Test Circuit

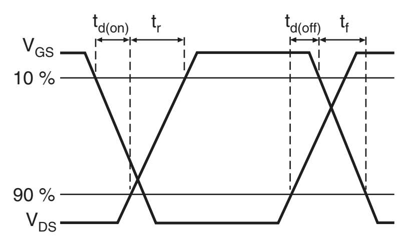


Fig. 10b - Switching Time Waveforms

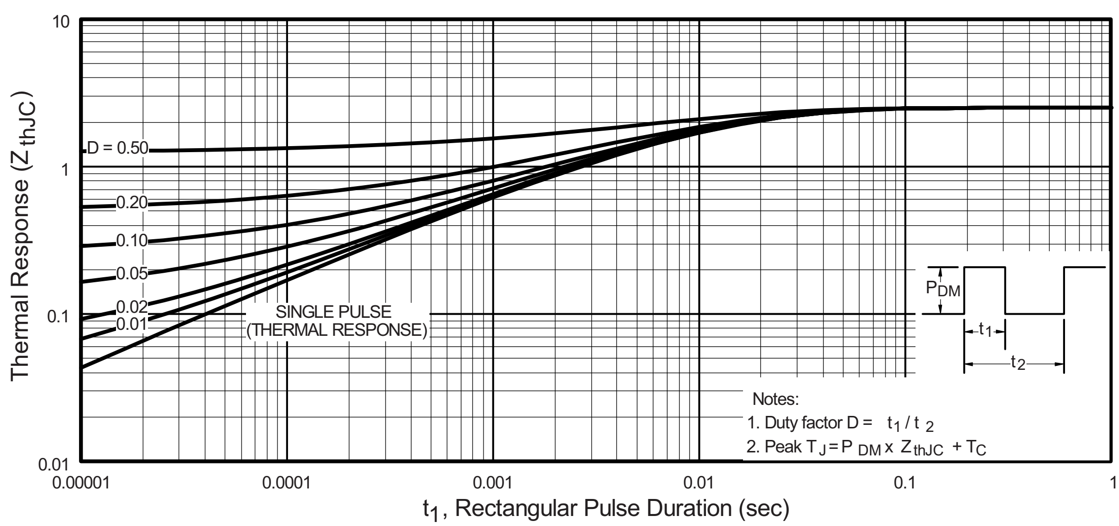


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

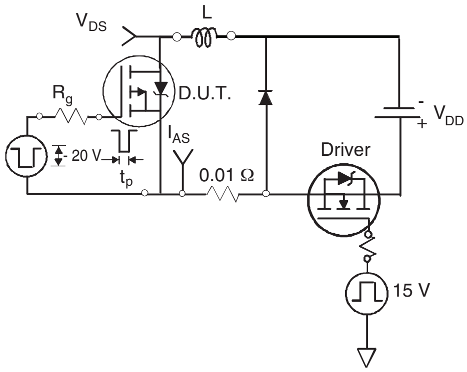


Fig. 12a - Unclamped Inductive Test Circuit

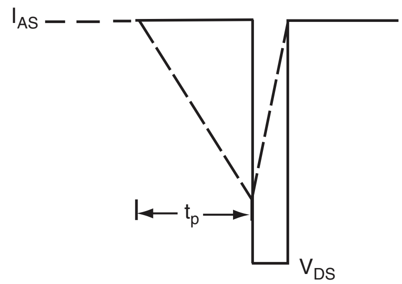


Fig. 12b - Unclamped Inductive Waveforms

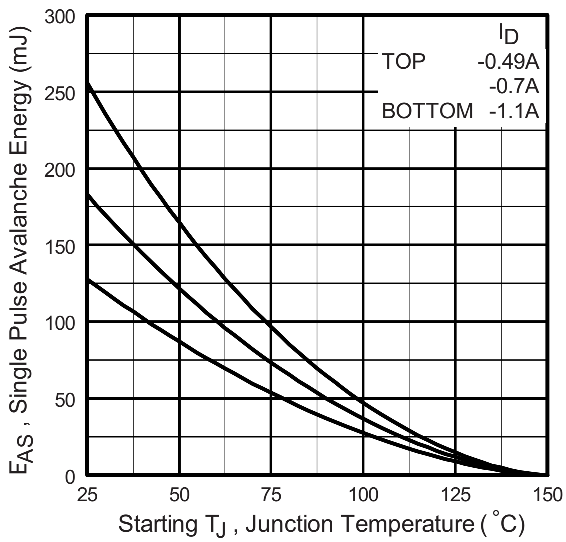


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

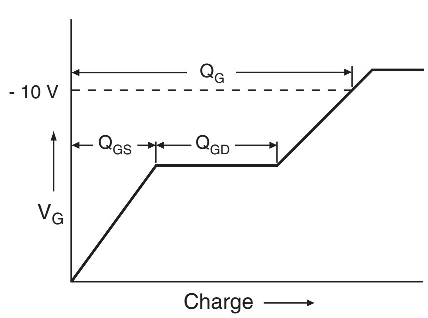


Fig. 13a - Basic Gate Charge Waveform

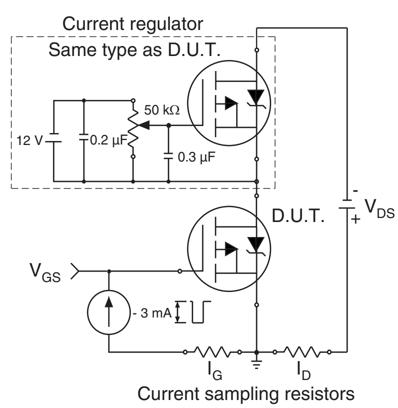
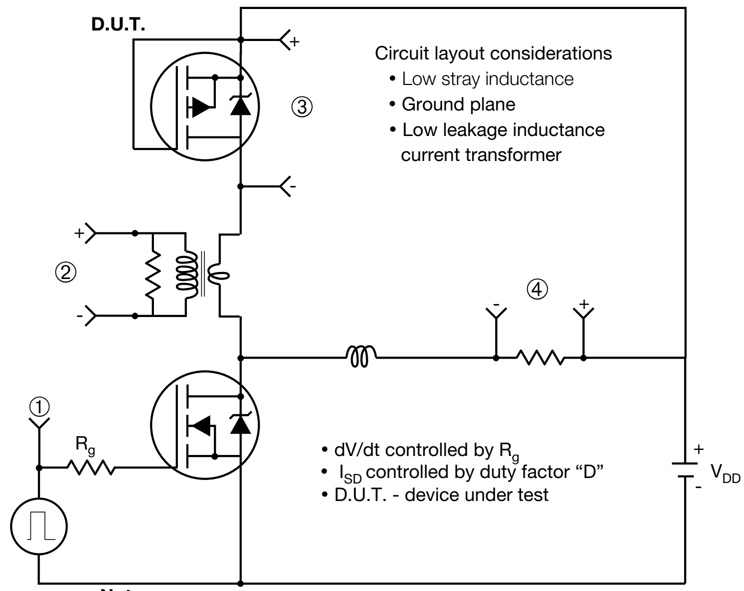


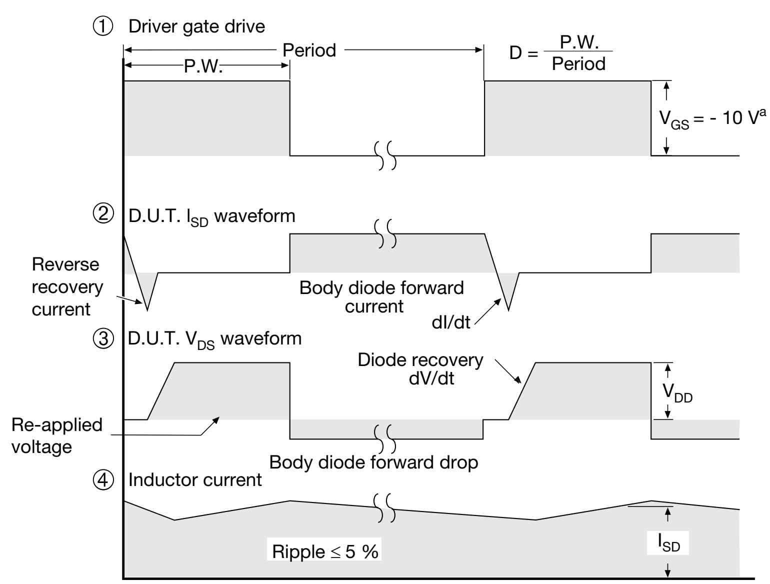
Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

• Compliment N-Channel of D.U.T. for driver



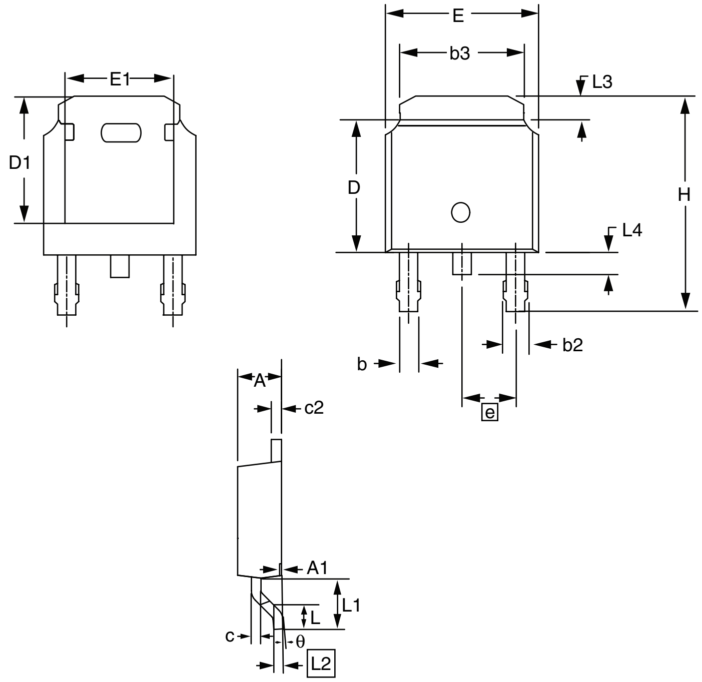
Note

a. V_{GS} = - 5 V for logic level and - 3 V drive devices

Fig. 14 - For P-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91284.

TO-252AA (HIGH VOLTAGE)

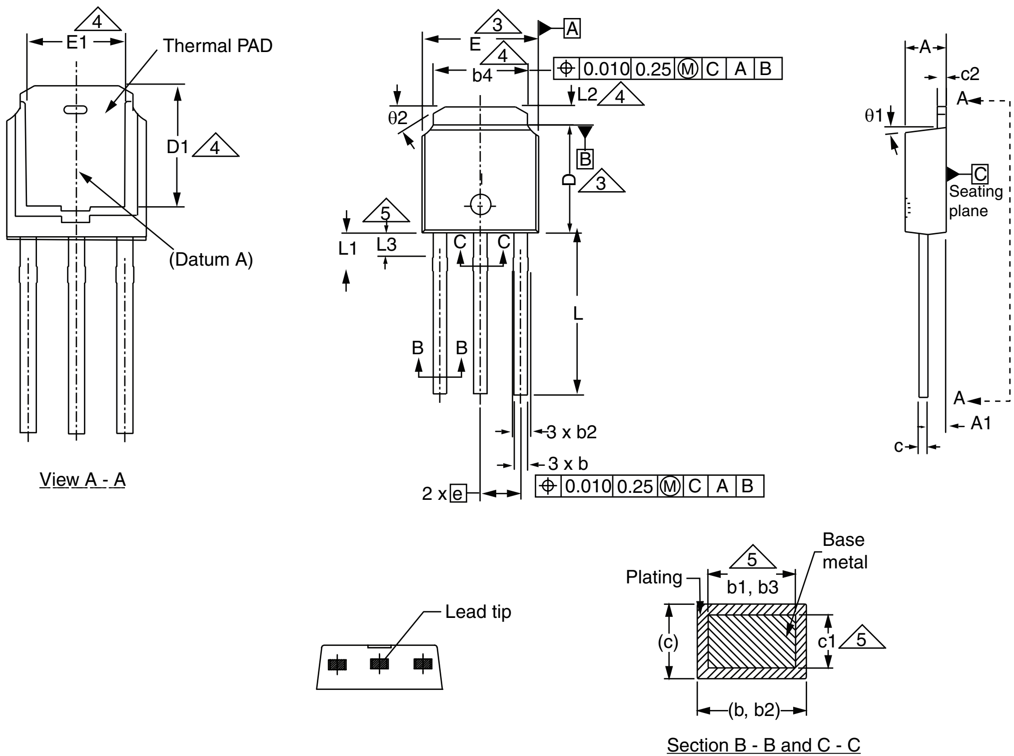


	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
E	6.40	6.73	0.252	0.265
L	1.40	1.77	0.055	0.070
L1	2.743 REF		0.108 REF	
L2	0.508 BSC		0.020 BSC	
L3	0.89	1.27	0.035	0.050
L4	0.64	1.01	0.025	0.040
D	6.00	6.22	0.236	0.245
H	9.40	10.40	0.370	0.409
b	0.64	0.88	0.025	0.035
b2	0.77	1.14	0.030	0.045
b3	5.21	5.46	0.205	0.215
e	2.286 BSC		0.090 BSC	
A	2.20	2.38	0.087	0.094
A1	0.00	0.13	0.000	0.005
c	0.45	0.60	0.018	0.024
c2	0.45	0.58	0.018	0.023
D1	5.30	-	0.209	-
E1	4.40	-	0.173	-
θ	0'	10'	0'	10'
ECN: S-81965-Rev. A, 15-Sep-08 DWG: 5973				

Notes

1. Package body sizes exclude mold flash, protrusion or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 0.10 mm per side.
2. Package body sizes determined at the outermost extremes of the plastic body exclusive of mold flash, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
3. The package top may be smaller than the package bottom.
4. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.10 mm total in excess of "b" dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.

TO-251AA (HIGH VOLTAGE)



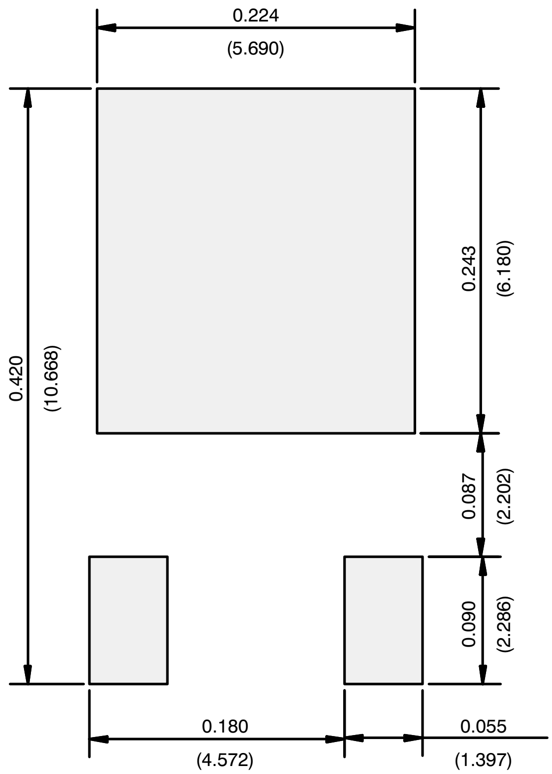
DIM.	MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.	DIM.	MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.
A	2.18	2.39	0.086	0.094	D1	5.21	-	0.205	-
A1	0.89	1.14	0.035	0.045	E	6.35	6.73	0.250	0.265
b	0.64	0.89	0.025	0.035	E1	4.32	-	0.170	-
b1	0.65	0.79	0.026	0.031	e	2.29 BSC		2.29 BSC	
b2	0.76	1.14	0.030	0.045	L	8.89	9.65	0.350	0.380
b3	0.76	1.04	0.030	0.041	L1	1.91	2.29	0.075	0.090
b4	4.95	5.46	0.195	0.215	L2	0.89	1.27	0.035	0.050
c	0.46	0.61	0.018	0.024	L3	1.14	1.52	0.045	0.060
c1	0.41	0.56	0.016	0.022	θ1	0'	15'	0'	15'
c2	0.46	0.86	0.018	0.034	θ2	25'	35'	25'	35'
D	5.97	6.22	0.235	0.245					

ECN: S-82111-Rev. A, 15-Sep-08
DWG: 5968

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension are shown in inches and millimeters.
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.13 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
4. Thermal pad contour optional with dimensions b4, L2, E1 and D1.
5. Lead dimension uncontrolled in L3.
6. Dimension b1, b3 and c1 apply to base metal only.
7. Outline conforms to JEDEC outline TO-251AA.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.