PI90LV02/PI90LVT02

SOTiny™ LVDS High-Speed Differential Line Receiver

Features

- Meets or Exceeds the Requirements of ANSI TIA/EIA-644-1995 Standard
- Signaling rates up to 400 Mbps
- Interfaces to LVDS, LVPECL
- Bus-Terminal ESD exceeds 10kV
- Differential Input Voltage Threshold less than 100mV
- Typical Propagation Delay Times of 2.6ns
- Typical Power Dissipation of 40mW @200 MHz
- Low Voltage TTL (LVTTL) Level is 5V Tolerant
- Open-Circuit Fail Safe
- Output are High Impedance with V_{CC} <1.5V
- Integrated 110-ohm Line Termination Resistor (PI90LVT02)
- Operates from a 3.3V supply
- Input common-mode voltage range 0V–3.2V
- Industrial Temperature Operating Range: –40°C to 85°C
- Packaging (Pb-free & Green available):
  - 5-pin space-saving SOT23 (T)

Description

The PI90LV02 and PI90LVT02 are single differential line receivers that use low-voltage differential signaling (LVDS) to support data rates up to 400 Mbps. These products are designed for applications requiring high-speed, low-power consumption, low-noise generation, and a small package.

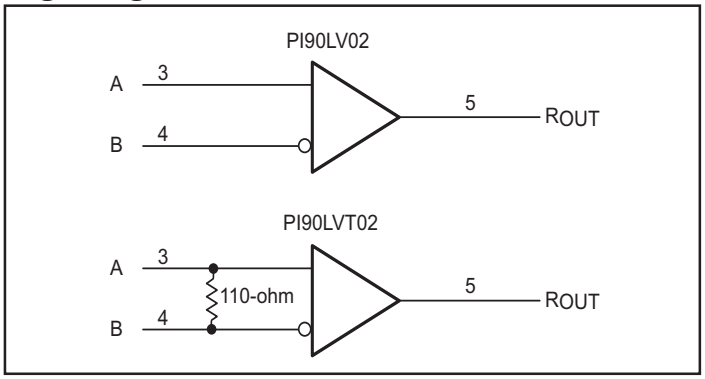
A differential input signal (350mV) is translated by the device to a 3.3V CMOS output level. The PI90LVT02 integrates the terminating resistor while the PI90LV02 requires an external resistor.

Applications

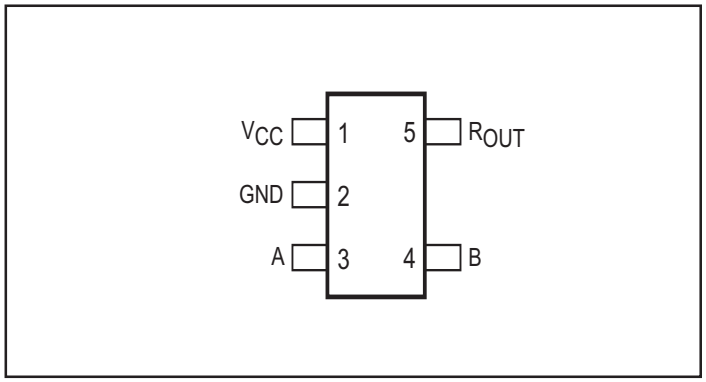
Applications include point-to-point and multi-drop baseband data transmissions over impedance media of approximately 100-ohms. The transmission media can be printed circuit board traces, backplanes, or cables.

The PI90LV02 and PI90LVT02 and companion line drivers (PI90LV01 and PI90LVB01) provide new alternatives to RS-232, PECL, and ECL devices for high-speed, point-to-point interface applications.

Logic Diagram



Pinout



Function Table

Inputs	Outputs
$V_{ID} = V_A - V_B$	R_{OUT}
V_{ID} >50mV	H
–50mV < V_{ID} < 50mV	?
$V_{ID} \leq$ –50mV	L
Open	H

H = high level
L = low level
? = indeterminate

Absolute Maximum Ratings Over Operating Free-Air Temperature

(unless otherwise noted)†

Supply Voltage Range, V_{CC}(1)	–0.5V to 4V
Voltage Range (A, B , or R_{OUT})	–0.5 to V_{CC}+0.5V
ESD rating (HBM, 1.5K-ohms, 100pF)	≥10KV
Continuous total power dissipation	See dissipation rating table
Storage Temperature Range	–65°C to 150°C
Lead Temperature 1.6 mm (1/16 inch) from case for 10 seconds	250°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability.

Notes:
1. All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

Dissipation Rating Table

Package	T_A £ 25°C Power Rating	Derating Factor Above T_A = 25°C**	T_A = 85°C Power Rating
5-Pin SOT-23 (T)	385mW	3.1mW/°C	200mW

**This is the inverse of the junction-to-ambient thermal resistance when board-mounted (low-K) and with no air flow.

Recommended Operating Conditions

	Min.	Nom.	Max.	Units
Supply Voltage, V_{CC}	3.0	3.3	3.6	V
Magnitude of differential input voltage, $\|V_{ID}\|$	0.1		0.6	
Common-Mode Input Voltage, V_{IC} (See Figure 6)	0		$2.0 - \frac{\|V_{ID}\|}{2}$	
			V_{CC} –0.8	
Operating free-air temperature, T_A	–40		85	°C

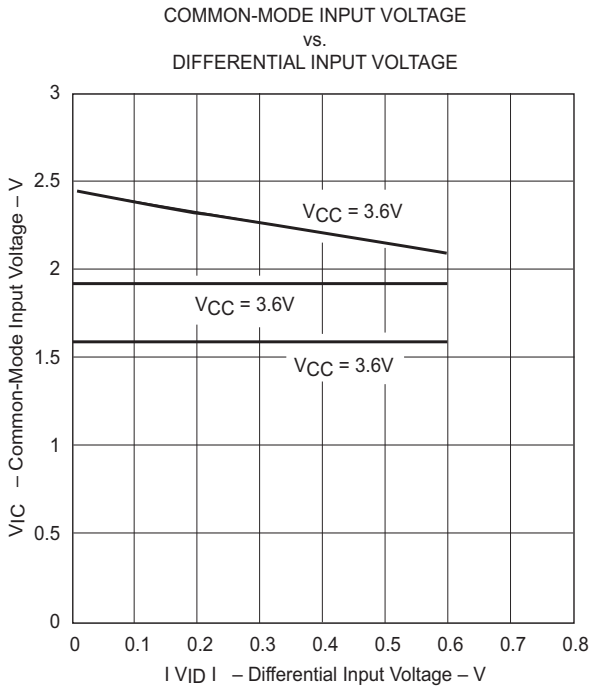


Figure 1. V_{IC} vs. V_{ID} and V_{CC}

Electrical Characteristics, V_{CC} = 3V to 3.6V (Over Recommended Operating Conditions, unless otherwise noted).

Symbol	Parameter		Test Conditions	Min.	Typ.(1)	Max.	Units
V_{ITH+}	Positive-going differential input voltage threshold		See Figure 2, & Table 1			100	mV
$V_{ITH–}$	Negative-going differential input voltage threshold			–100			
V_{OH}	High-level output voltage		I_{OH} = –8mA	2.4	3		V
V_{OL}	Low-level output voltage		I_{OL} = 8mA		0.25	0.4	
I_{CC}	Supply current		No load, Steady state		4	7	mA
I_I	Input current (A or B inputs)	LV02	V_I = 0V			±20	µA
		LVT02	V_I = 0V, Other input open			±40	
		LV02	V_I = 2.4V or V_{CC} –0.8	–1.2			
		LVT02	V_I = 2.4V, Other input open	–2.4			
I_{ID}	High-level input current ($I_{IA} – I_{IB}$)	LV02	V_{IA} = 0V, V_{IB} = 0.1V V_{IA} = 2.4V, V_{IB} = 2.3V			±2	
		LVT02	V_{IA} = 2.4V, V_{IB} = 2.3V	1.5	1.8	2.2	mA
$I_{I(OFF)}$	Power-off input current (A or B inputs)	LV02	V_{CC} = 0V, V_I = 2.4V			20	µA
		LVT02	V_{CC} = 0V, V_I = 2.4V, Other input open			40	

Receiver Switching Characteristics, V_{CC} = 3V to 3.6V (Over Recommended Operating Conditions, unless noted).

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Units
t_{PLH}	Propagation delay time, low-to-high level output	C_L = 10pF, See Figure 3	1.3	2.1	3.2	ns
t_{PHL}	Propagation delay time, high-to-low level output		1.3	2.0	3.2	
t_r	Output signal rise time			0.7	1.4	
t_f	Output signal fall time			0.7	1.4	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)(2)			0.1	0.5	
t_{PZH}	Propagation delay time, high-level-to-high-impedance output	See Figure 4		1.5	3.1	
t_{PZL}	Propagation delay time, low-level-to-low-impedance output			4.0	6.0	
t_{PHZ}	Propagation delay time, high-impedance-to-high-level output			2.5	3.5	
t_{PLZ}	Propagation delay time, low-impedance-to-high-level output			6.0	7.6	

Notes:
1. All typical values are at 25°C and with a 3.3V supply
2. $t_{sk(p)}$ is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.

Parameter Measurement Information

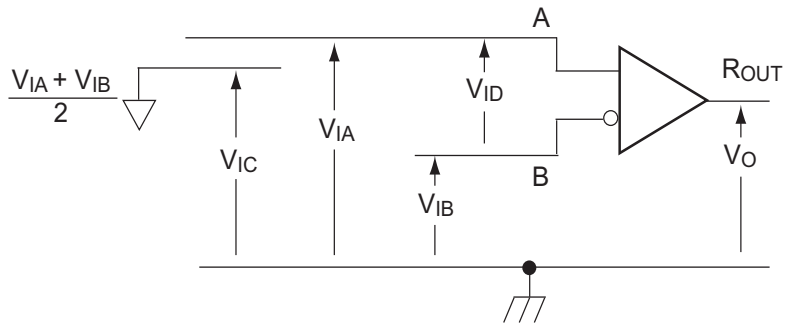
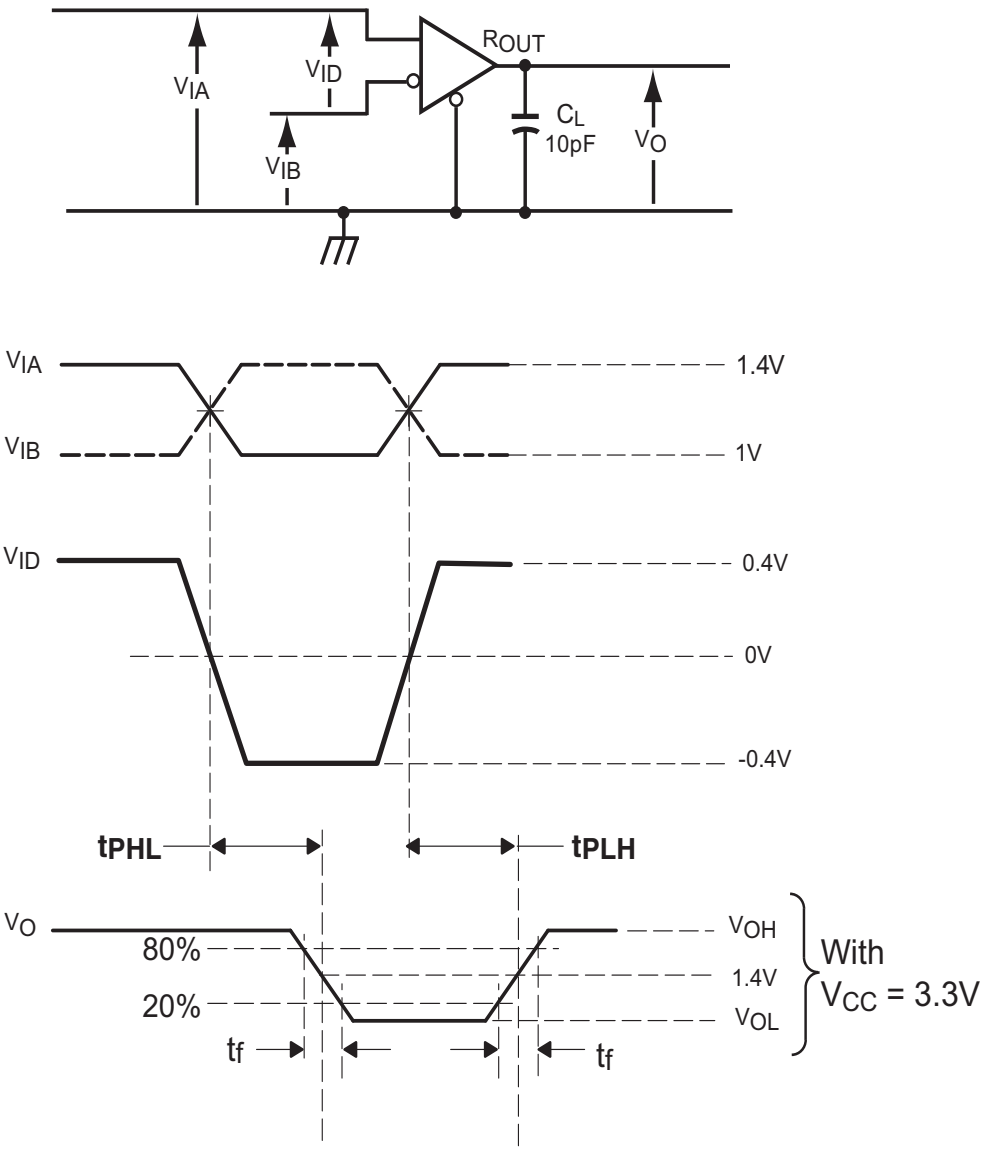


Figure 2. Receiver Voltage Definitions

Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages

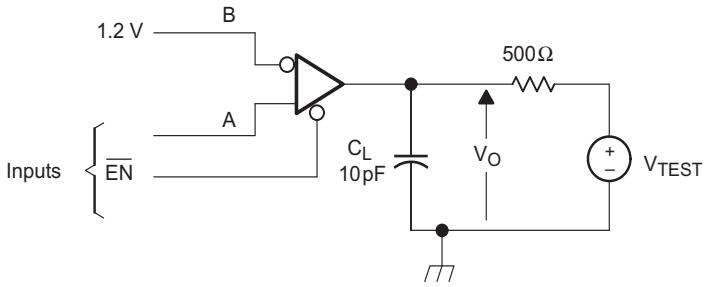
Applied Voltages (V)		Resulting Differential Input Voltage (mV)	Resulting Common-Mode Input Voltage (V)
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.25	1.20	50	1.2
1.15	1.20	–50	1.2
2.4	2.35	50	2.35
2.3	2.35	–50	2.35
0.05	0	50	0.05
0	0.05	–50	0.05
1.5	0.9	600	1.2
0.9	1.5	–600	1.2
2.4	1.8	600	2.1
1.8	2.4	–600	2.1
0.6	0	600	0.3
0	0.6	–600	0.3



Note A: All input pulses are supplied by a generator having the following characteristics: t_r or t_f £ 1ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ±0.2ns. C_L includes instrumentation and fixture capacitance within 0.06m of the D.U.T.

Note B: To verify input max signalling rate, the input signal transition time (tr/tf) should not exceeds 1.25ns.

Figure 3. Timing Test Circuit and Waveforms



NOTE A: All input pulses are supplied by a genertor having the following characteristics: t_r or t_f £ 1ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse wide = 500 ±10ns. CL includes instrumentation and fixture capacitance within 0.06m of the D.U.T.

NOTE B: To verify input max signalling rate, the input signal transition time (tr/tf) should not exceeds 1.25ns.

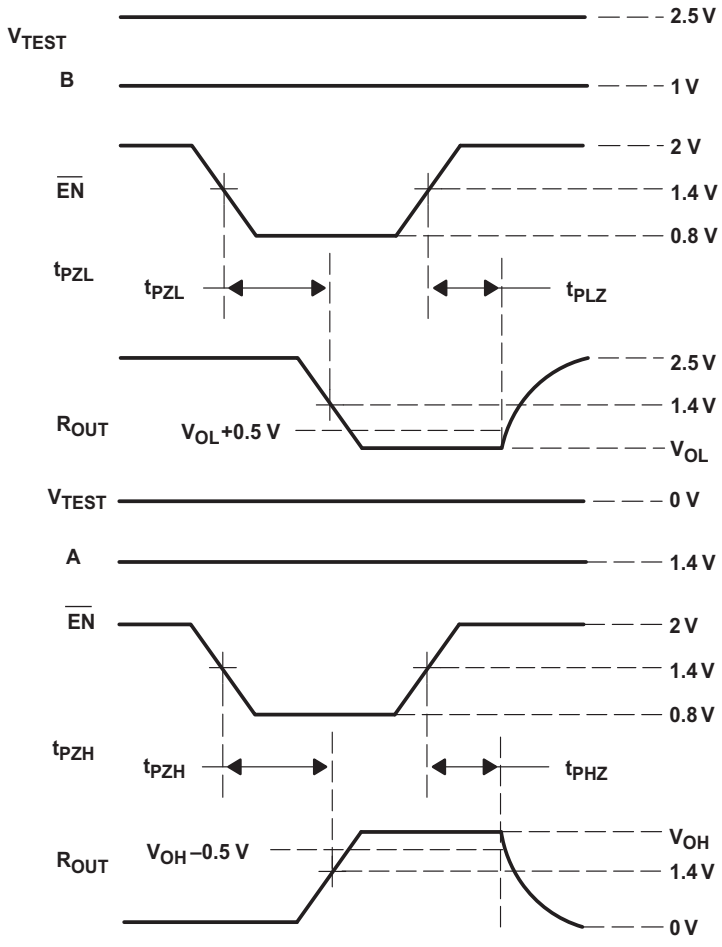


Figure 4. Enable/Disable Time Test Circuit and Waveforms

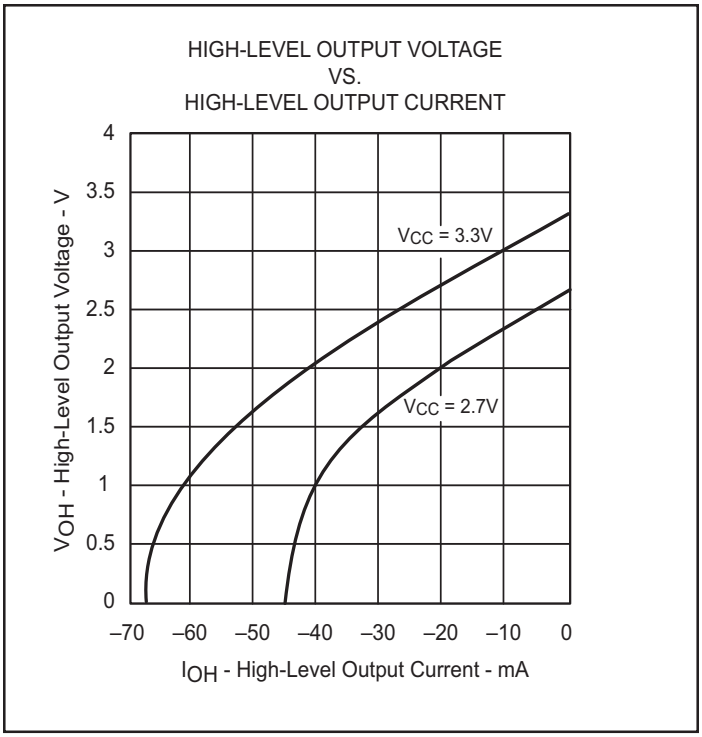


Figure 5

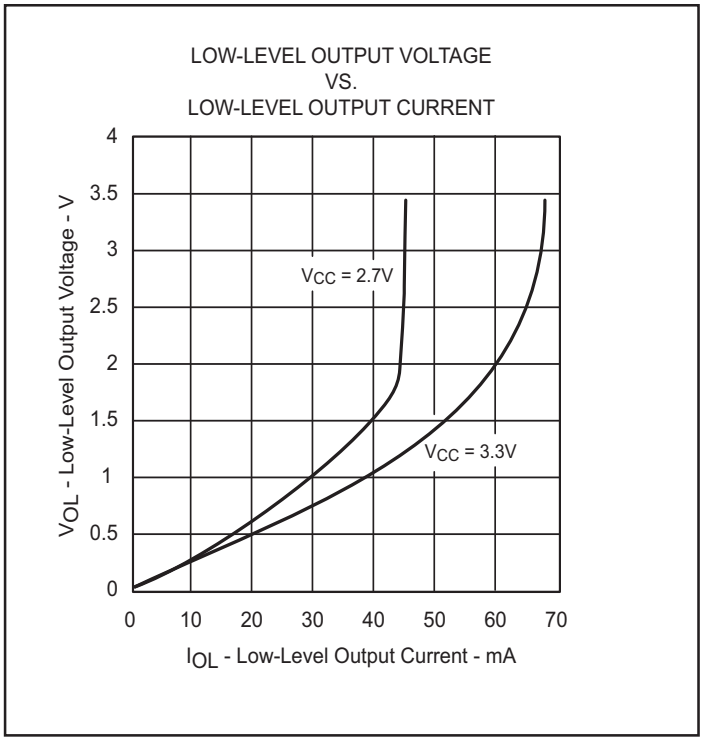


Figure 6

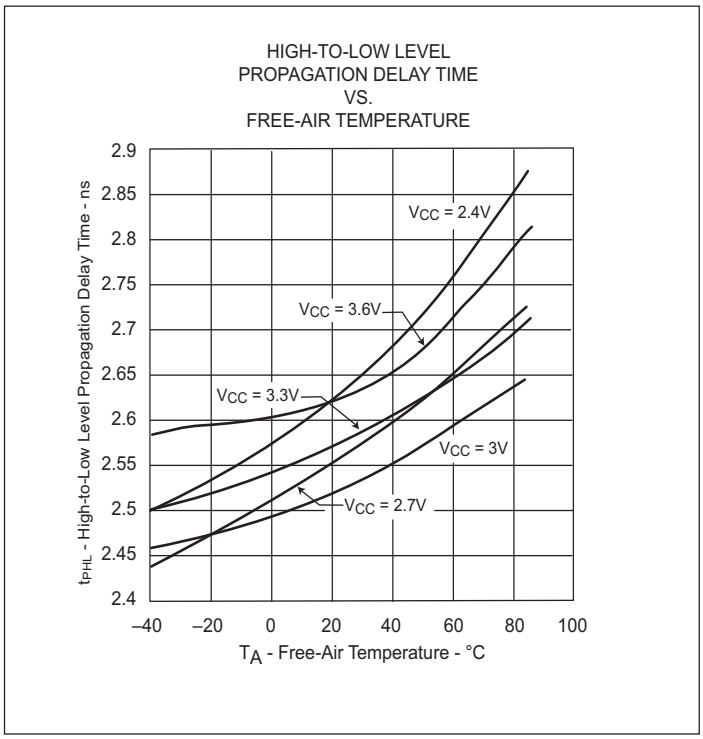


Figure 7

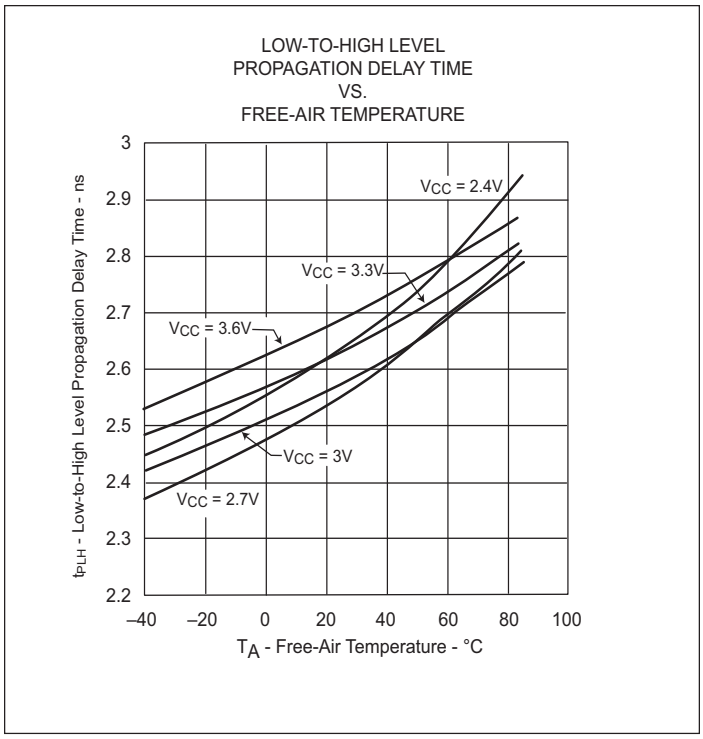
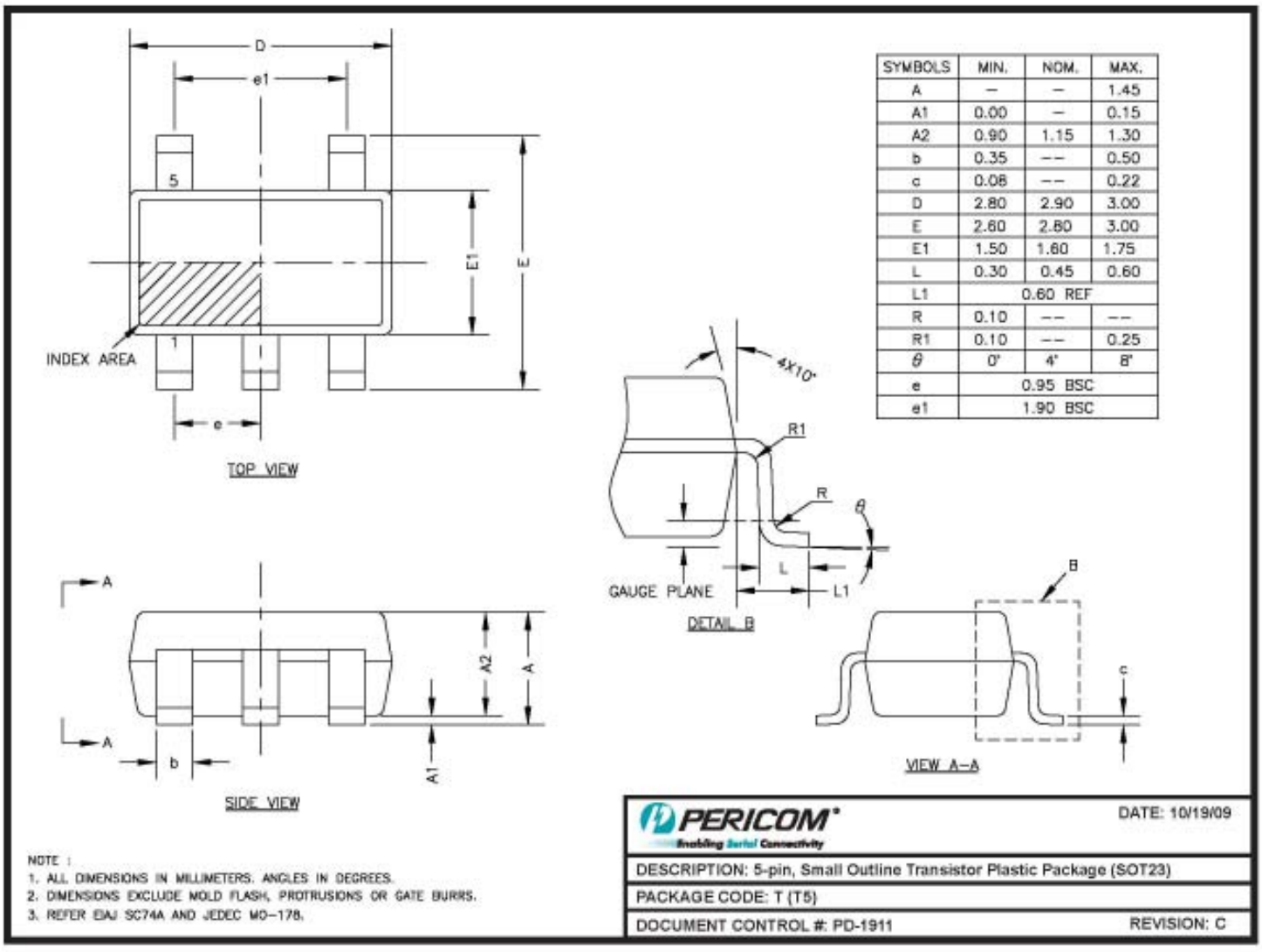


Figure 8



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.45
A1	0.00	–	0.15
A2	0.90	1.15	1.30
b	0.35	––	0.50
c	0.08	––	0.22
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.60	1.75
L	0.30	0.45	0.60
L1	0.60 REF		
R	0.10	––	––
R1	0.10	––	0.25
θ	0°	4°	8°
e	0.95 BSC		
e1	1.90 BSC		

09-0130

Notes:

1. For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information

Ordering Code	Package Code	Package Description	Top Marking
PI90LV02TEX	T	Pb-free & Green, 5-pin, SOT23	L5
PI90LVT02TEX	T	Pb-free & Green, 5-pin, SOT23	L6

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green
3. X = Tape and reel