

*POWER MANAGEMENT SYSTEM DEVICE*

# RN5T568C-E4

*Product Specifications*

**Rev1.1**

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**RICOH**

RICOH Electronic Devices Co., Ltd.

This specification is subject to change without notice.

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## 1. Outline

This IC is the power management IC for GPS-PND/STB/POS/Panel Computer and so on. It integrates four high-efficiency step-down DCDC converters, seven low dropout regulators, power control logic, I2C-Bus Interface, voltage detections, thermal shut-down, and etc.

## 2. Feature

- System
  - ✓ I2C-Bus interface @3.4MHz and 400kHz
  - ✓ Detector Function (System/IO, UVLO, DETVSB)
  - ✓ Thermal Shutdown Function
  - ✓ Watchdog timer
  - ✓ Power on key input for System's power up
  - ✓ Power on reset output for CPU
  - ✓ Flexible power-on/off sequence by OTP
  - ✓ Flexible DCDCx and LDOx default-on/off control by OTP
- High Efficiency Step-down DC/DC Converters
  - ✓ DC/DC1    0.6-3.5V            Max 3000mA
  - ✓ DC/DC2    0.6-3.5V            Max 3000mA
  - ✓ DC/DC3    0.6-3.5V            Max 2000mA
  - ✓ DC/DC4    0.6-3.5V            Max 2000mA
  - ✓ Soft-start circuit
- Low Drop Voltage Regulators
  - ✓ LDO1        0.9-3.5V            Max 300mA
  - ✓ LDO2        0.9-3.5V            Max 300mA
  - ✓ LDO3        0.6-3.5V            Max 300mA
  - ✓ LDO4        0.9-3.5V            Max 200mA
  - ✓ LDO5        0.9-3.5V            Max 200mA
  - ✓ LDORTC1    1.2-3.5V            Max 30mA (AlwaysOn, For coin battery)
  - ✓ LDORTC2    0.9-3.5V            Max 10mA (AlwaysOn)
  - ✓ Over current Protection and Short circuit Protection.
- 4ch-GPIO
  - ✓ Supports interrupt function (level/edge) for input signals
  - ✓ Outputs power-on signal for external devices
  - ✓ Power on/off input for System's power up/down
  - ✓ DCDCx and LDOx can be controlled by external input
  - ✓ GPIO2 can output LDORTC2
  - ✓ GPIO0 and GPIO1 have maximum 15mA sink for LED.
  - ✓ GPIOx have Output C32KOUT of internal clock for external devices.
- Interrupt Controller (INTC)
- Package     QFN0707-48 (0.5mm pitch)
- Process      CMOS

● OTP selected list

	OTP Function	Setting	Explanation:
System OTP Setting	I2CSLV	2: 32h	The settings of I2C slave address (A3-A1).
	SLEEPPOL	0: Non-Inversion	SLEEP pin polarity selection ( Default High active )
	PWRONPOL	0: Non-Inversion	PWRON pin polarity selection ( Default High active )
	VINDAC	4: 3.0V	System Voltage Detection for Power-ON permit.
	VINHYSSEL	1: 200mV	Hysteresis Voltage for VINDET ( System Voltage Detection for Power-ON permit )
	VINRRESET	1: ERSTB	VINDAC/VINHYS Reset selection
	IODAC	1: 1.60V	VDDIO Voltage Detection ( Power OFF factor )
	PREVINDAC	6 :3.5(↑)/3.4(↓)	System Voltage Pre-Detection ( Interrupt output )
	OVTEMP	0: 105/85°C	initial temperature of Overheat Detection(Interrupt output)

	OTP Function	Setting	Explanation:
GPIO OTP setting	GPIO3POL	0: Non-Inversion	GPIO3 input's polarity ( Default High Active )
	GPIO2POL	0: Non-Inversion	GPIO2 input's polarity ( Default High Active )
	GPIO1POL	0: Non-Inversion	GPIO1 input's polarity ( Default High Active )
	GPIO0POL	0: Non-Inversion	GPIO0 input's polarity ( Default High Active )

	OTP Function	Setting	OTP Function	Setting	Explanation		
Sequence, DCDC, LDO OTP settings	LDORTC1AWON	1: AlwaysOn	LRTC DAC	3.30V	LDORTC1 Always-ON or I2C Control / Initial VOUT		
	LDORTC1ONSLOT	0: Enable	L5DAC	3.30V	The setting of initial ON/OFF for RTCLDO1 ( Select "0:Enable" for AlwaysON )		
	LDO5ONSLOT	0: Enable	L4DAC	3.30V	The setting of LDO5 Pin Control / Initial VOUT		
	LDO4ONSLOT	0: Enable	L3DAC	2.50V	The setting of LDO4 Pin Control / Initial VOUT		
	LDO3ONSLOT	0: Enable	L2DAC	3.30V	The setting of LDO3 Pin Control / Initial VOUT		
	LDO2ONSLOT	0: Enable	L1DAC	1.80V	The setting of LDO2 Pin Control / Initial VOUT		
	LDO1ONSLOT	0: Enable			The setting of LDO1Pin Control / Initial VOUT		
	DC4ONSLOT	0: Enable	DD4DAC	1.80V	DD4LIM	1: 2.3A	Pin control /VOUT /Limit Current
	DC3ONSLOT	0: Enable	DD3DAC	1.20V	DD3LIM	1: 2.3A	Pin control /VOUT /Limit Current
	DC2ONSLOT	0: Enable	DD2DAC	1.10V	DD2LIM	1: 3.2A	Pin control /VOUT /Limit Current
	DC1ONSLOT	0: Enable	DD1DAC	1.10V	DD1LIM	1: 3.2A	Pin control /VOUT /Limit Current

### 3. Block Diagram

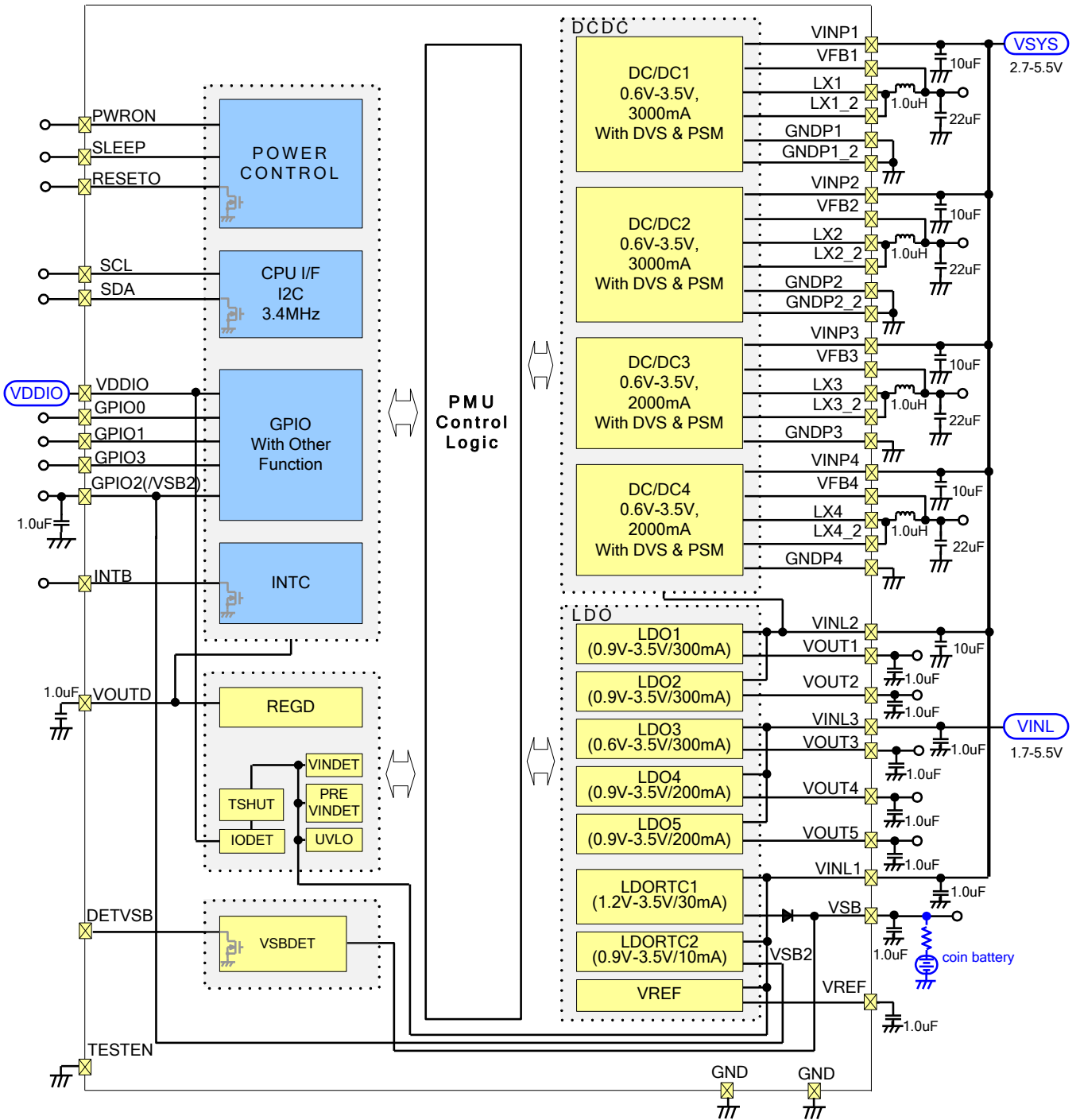


Fig 3-1 Block Diagram

## 4. Electrical Characteristics

### 4.1 Absolute Maximum Ratings

Exposure to the condition exceeded absolute maximum ratings may cause the permanent damages and affect the reliability and safety of both device and systems using the device. The functional operations cannot be guaranteed beyond specified values in the recommended conditions.

Symbol	Parameter	Condition	Min	Max	Units
V <sub>PS1</sub>	Power Supply Voltage 1	VINP1-4, VINL1-3pin	-0.3	6.0	V
V <sub>PS2</sub>	Power Supply Voltage 2	VDDIO pin	-0.3	4.5	V
V <sub>INPUT</sub>	Input Voltage Range	PWRON, SLEEP pin	-0.3	VINL1 + 0.3	V
		SDA, SCL pin	-0.3	4.5	V
		GPIO0-1 pin	-0.3	VINL1 + 0.3 / VDDIO + 0.3	V
		GPIO2-3 pin	-0.3	VINL1 + 0.3	V
V <sub>OUTPUT</sub>	Output Voltage Range	RESETO, INTB,GPIO2-3 pin	-0.3	VINL1 + 0.3	V
		GPIO0-1 pin	-0.3	VINL1 + 0.3 / VDDIO + 0.3	V
		DETVSB pin	-0.3	VSB* + 0.3	V
T <sub>stg</sub>	Storage Temperature	-	-55	125	degrees C
PD	Package Allowable Dissipation	QFN0707-48(0.5mm pitch) T <sub>a</sub> = 25 degrees C	0	3700	mW

\*VSB : LDORTC1\_Output or Coin Battery

Table 4-1 Absolute Maximum Ratings

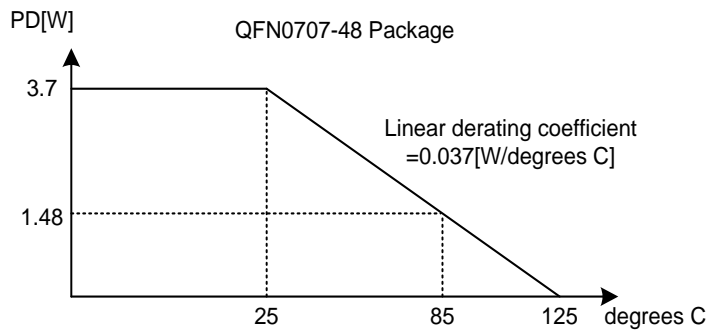


Fig 4-1 Maximum Package Allowable Dissipation

## 4.2 Recommendation of Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
VSYS	Power Supply Voltage	VINP1-4, VINL1-2 pin *1	2.7	3.6	5.5	V
VINL	Power Supply Voltage	VINL3 pin *2	1.7	3.6	5.5	V
VDDIO	Power Supply Voltage	VDDIO pin (VSYS > VDDIO)	1.7	1.8	3.4	V
VSB	Power Supply Voltage	VSB pin	1.45	3.1	3.4	V
*GND*	Ground	GND		0		V
Ta	Temperature of Operation	-	-40		85	degrees C

Note\*1:VINP1-4 and VINL2 must be equal to VINL1.

However, if POWROFF state, VINP1-4 and VINL2 is possible to power-off  
(Only Parts Mode and then Input pin level must be GND.)

Note\*2:VINL3 must be less than or equal to VINL1.

Table 4-2 Recommendation of Operating Conditions



## 4.3 I/O Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
<i>VINL1 NMOS Input Pin: PWRON, SLEEP, GPIO0, GPIO1, GPIO2, GPIO3</i>						
VIL	Low level input voltage				0.4	V
VIH	High level input voltage		1.4		VINL1	V
<i>VINL1 Nch Open Drain output Pin : RESET0</i>						
VOL	Low level output voltage	Iout = 2mA			0.4	V
Vto	Tolerant				VINL1	V
<i>VINL1 CMOS input/output Pin : GPIO0, GPIO1, GPIO2, GPIO3</i>						
VIL	Low level input voltage				VINL1*0.2	V
VIH	High level input voltage		VINL1*0.8		VINL1	V
VOL	Low level output voltage	Iout = 4mA			0.4	V
VOH	High level output voltage	Iout = -4mA	VINL1-0.4			V
<i>VINL1 Nch Open Drain output Pin : INTB, GPIO0, GPIO1, GPIO2, GPIO3</i>						
VOL	Low level output voltage	Iout = 4mA			0.4	V
Vto	Tolerant				VINL1	V
<i>VINL1 Nch Open Drain output Pin: GPIO0, GPIO1 (for LED)</i>						
VOL	Low level output voltage	Iout = 15mA			0.4	V
Vto	Tolerant				VINL1	V
<i>VSB Nch Open Drain output Pin: DETVSB</i>						
VOL	Low level output voltage	Iout = 1mA			0.2	V
Vto	Tolerant				VSB	V

Symbol	Parameter	Condition	Min	Typ	Max	Units
<i>VOUTD CMOS input Pin (Schmitt Input): SCL</i>						
VIL	Low level input voltage				VOUTD *0.3	V
VIH	High level input voltage		VOUTD *0.7		3.4	V
$\Delta V_I$	Hysteresis		VOUTD *0.1			V
<i>VOUTD CMOS input/output Pin(Schmitt Input / Nch Open Drain output) : SDA</i>						
VIL	Low level input voltage				VOUTD *0.3	V
VIH	High level input voltage		VOUTD *0.7		3.4	V
$\Delta V_I$	Hysteresis		VOUTD *0.1			V
VOL	Low level output voltage	Iout = 3mA			0.4	V
<i>VDDIO CMOS input/output Pin : GPIO0, GPIO1</i>						
VIL	Low level input voltage				VDDIO*0.2	V
VIH	High level input voltage		VDDIO*0.8		VDDIO	V
VOL	Low level output voltage	Iout = 4mA			0.4	V
VOH	High level output voltage	Iout = -4mA	VDDIO-0.4			V

\*VOUTD : REGD\_Output (1.8V)

Table 4-3 I/O Electrical Characteristics

## 4.4 Consumption Current

Operating Conditions (unless otherwise specified)  $T_a = 25$  degrees C,  $V_{IN} = 3.6V$ , No-load

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{ST}$	Standby current	PowerOff (Note*1)		15		$\mu A$
$I_{OP}$	Operating current	PowerOn (Note*1)		350		$\mu A$
$I_{SLP}$	Sleep current	Sleep (Note*1)		100		$\mu A$

Table 4-4 Consumption Current

Note\*1) Each condition is below. (It is possible to change the enabled LDO/DCDC at PowerOn/Sleep.)

	PowerOFF	PowerON	Sleep
LDO1	-	○	-
LDO2	-	○	-
LDO3	-	○	○
LDO4	-	○	○
LDO5	-	○	-
LDORTC1	○	○	○
LDORTC2	-	-	-
VREF	○	○	○
DCDC1	-	○	-
DCDC2	-	○	○(ECO)
DCDC3	-	-	-
DCDC4	-	-	-
UVLO	○	○	○
VINDET	○	○	○
IODET	○	○	○
PREVINDET	○	○	○
VSBDDET	○	○	○
TSHUT	○	○	○
REGD	○	○	○
Internal Logic	○	○	○

## 5. Package information

### 5.1 Pin Configuration

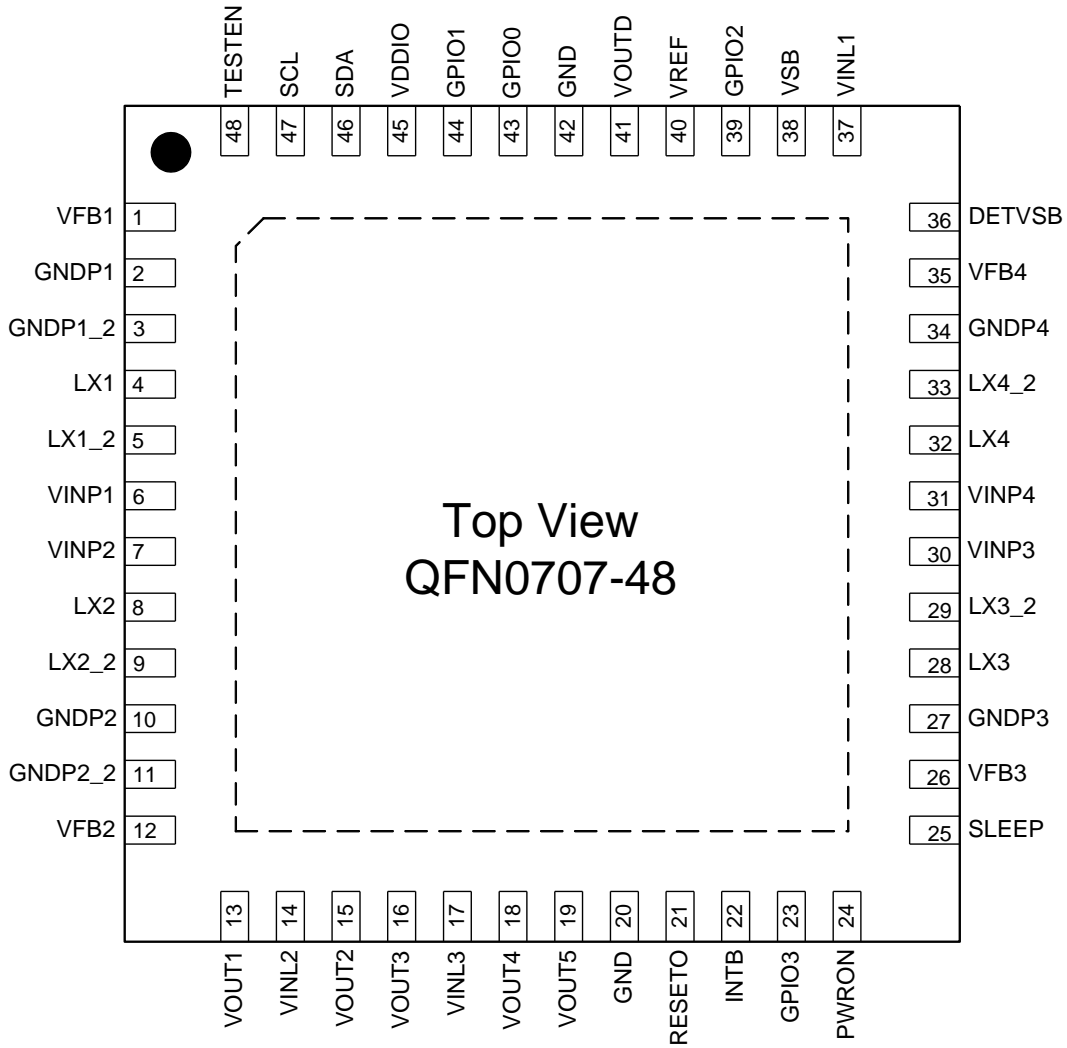
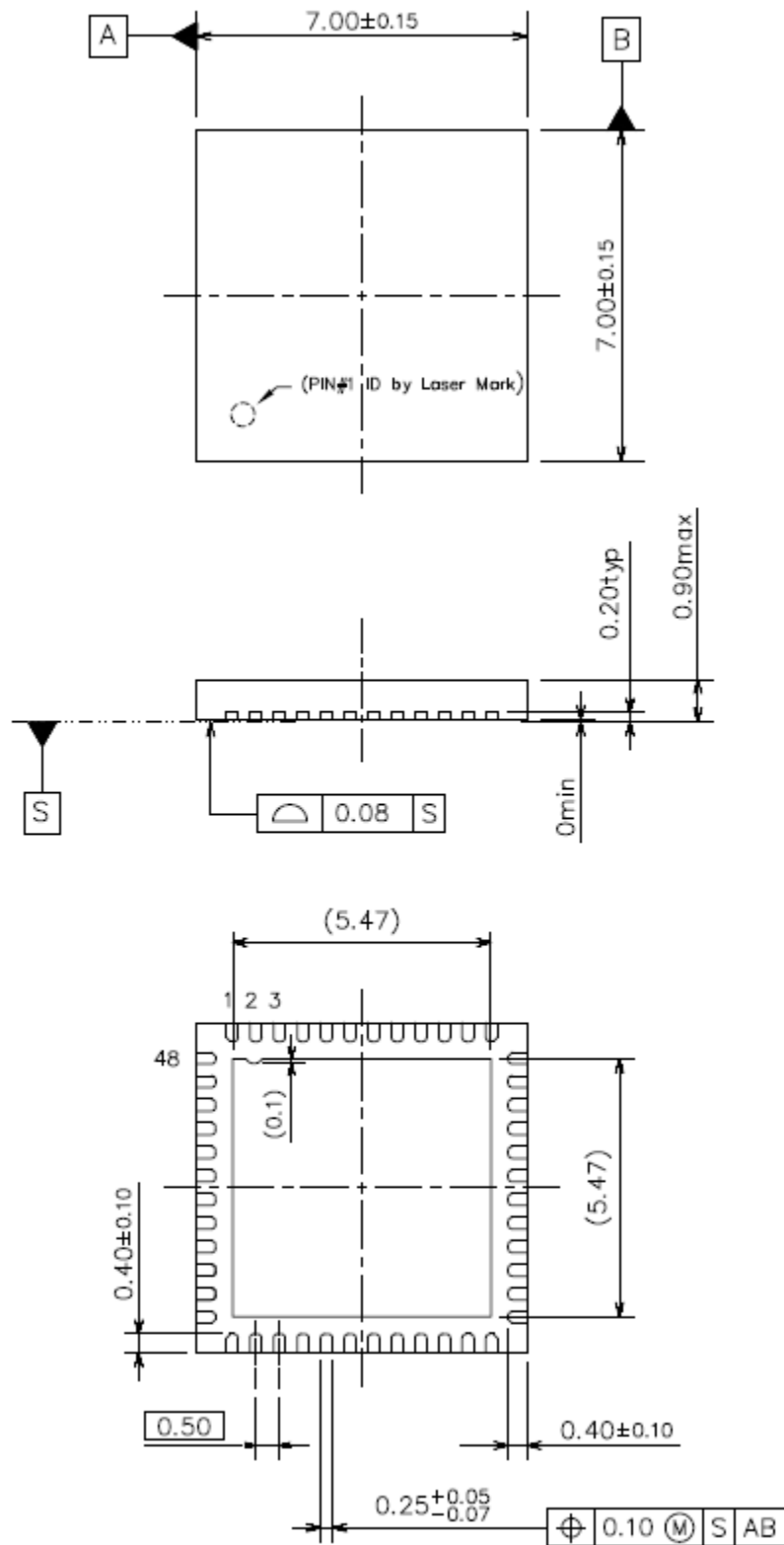


Fig 5-1 Pin Configuration

5.2 QFN0707-48 Package



UNIT: mm

Fig 5-2 Package Diagram (QFN0707-48pin, 0.5mm pitch)

## 6. Pin Description

No.	Pin Name	Function	I/O (*1)	D/A (*2)	Reset State (*3)		Note
1	VFB1	DC/DC1 Output voltage feedback input	I/O	A			
2	GNDP1	GND for DC/DC1	-	G			
3	GNDP1_2	GND for DC/DC1	-	G			
4	LX1	DC/DC1 switch output	O	A			
5	LX1_2	DC/DC1 switch output	O	A			
6	VINP1	Power supply for DC/DC	-	P			
7	VINP2	Power supply for DC/DC2	-	P			
8	LX2	DC/DC2 switch output	O	A			
9	LX2_2	DC/DC2 switch output	O	A			
10	GNDP2	GND for DC/DC2	-	G			
11	GNDP2_2	GND for DC/DC2	-	G			
12	VFB2	DC/DC2 Output voltage feedback input	I/O	A			
13	VOU1	LDO1 output	O	A			
14	VINL2	Power supply for LDO1,2 and DCDC analog	-	P			
15	VOU2	LDO2 output	O	A			
16	VOU3	LDO3 output	O	A			
17	VINL3	Power supply for LDO3,4 and LDO5	-	P			
18	VOU4	LDO4 output	O	A			
19	VOU5	LDO5 output	O	A			
20	GND	GND for Logic circuit,analog circuit, IO and etc	-	G			
21	RESETO	Host Reset output	O	D	O	Low	NOD
22	INTB	Interrupt request output	O	D	O	Hi-z	NOD
23	GPIO3	General purpose I/O Note*	I/O	D	*4	*4	*4
24	PWRON	External power on signal input	I	D	I	-	1.4V to VINL1
25	SLEEP	Stand-by mode control signal input	I	D	I	-	1.4V to VINL1
26	VFB3	DC/DC3 Output voltage feedback input	I/O	A			
27	GNDP3	GND for DC/DC3	-	G			
28	LX3	DC/DC3 switch output	O	A			
29	LX3_2	DC/DC3 switch output	O	A			
30	VINP3	Power supply for DC/DC3	-	P			
31	VINP4	Power supply for DC/DC4	-	P			
32	LX4	DC/DC4 switch output	O	A			
33	LX4_2	DC/DC4 switch output	O	A			
34	GNDP4	GND for DC/DC4	-	G			
35	VFB4	DC/DC4 Output voltage feedback input	I/O	A			
36	DETVSB	Voltage detection VSB output (Nch-opendrain)	O	D	O	-	NOD
37	VINL1	Power supply for LDORTC1,2, VREF, DET, IO and etc	-	P			
38	VSU	LDORTC1 output	O	A			
39	GPIO2(VSU2)	General purpose I/O Note*	I/O	D	*4	*4	*4
40	VREF	Bypass capacitor connecting pin	O	A			
41	VOU4D	Capacitor connection for built-in Regulator	O	A			
42	GND	GND for Logic circuit,analog circuit, IO and etc	-	G			
43	GPIO0	General purpose I/O Note*	I/O	D	*4	*4	*4
44	GPIO1	General purpose I/O Note*	I/O	D	*4	*4	*4
45	VDDIO	Power supply for CPU IF	-	P			
46	SDA	I2C-Bus Data input/Output	I/O	D	I	-	Schmitt,NOD
47	SCL	I2C-Bus Clock input	I	D	I	-	CMOS
48	TESTEN	For TEST (Connect to GND)	I	D	I	PD	CMOS Schmitt

Note\*1: I:Input, O:Output

Note\*2: A:Analog, D:Digital, P:Power, G:Ground

Note\*3: Reset State: RESETO=Low.

Note\*4: GP00-GP03: "Input" or "Output" is selectable by OTP. Input/Output type (CMOS or NMOS or Analog or Nch Open Drain Output) is selectable by OTP. Refer to the chapter of GPIO for detail.

Table 6-1 Pin Description

## 7. Power Control

This PMU has the power-on/off sequence that can be flexibly set by OTP. The default on/off, timing, and voltage of DCDCx and LDOx are programmable. In addition, GPIO0-GPIO3 pins output the power-on/off signal to external LDO/DCDC by the setting of OTP.

### 7.1 State Machine Diagram

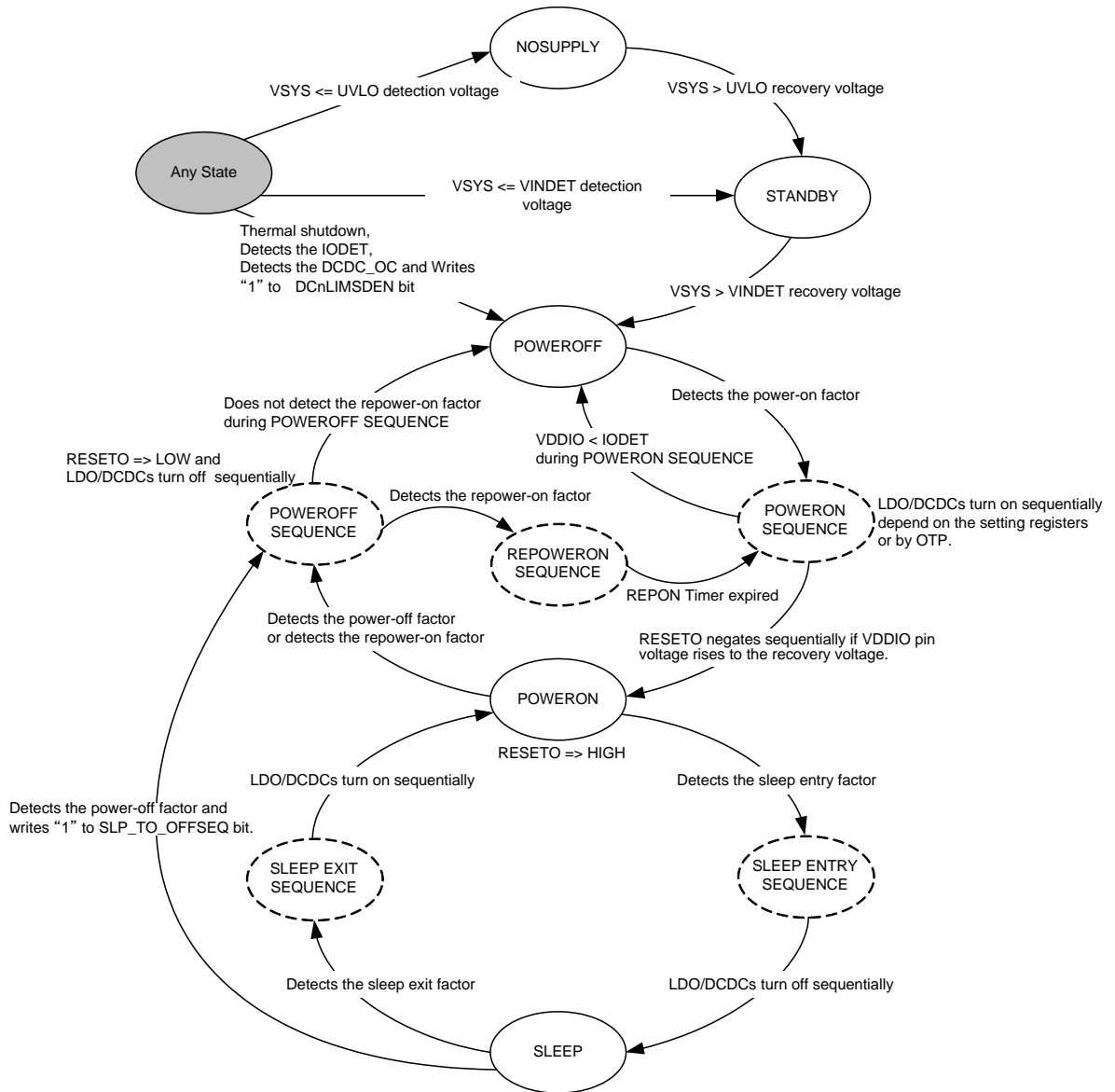


Fig 7-1 Power Control State Machine Diagram

## 7.2 State Machine Description

The state machine will step through the following statuses:

### **NOSUPPLY**

The power supply to VSYS falls below the UVLO detection voltage.

### **STANDBY**

The power supply to VSYS rises above the UVLO recovery voltage, followed by LDORTC1 turns on.

### **POWEROFF**

The power supply to VSYS rises above the VINDET recovery voltage.

This PMU is always monitoring the power-on factor, and if the factor is detected, it will start the power-on sequence.

### **POWERON SEQUENCE**

LDO/DCDCs turn on sequentially according to a pre-programmed order by OTP. And RESETO will be pulled up high sequentially if VDDIO pin voltage rises to the recovery voltage. Even if VDDIO pin voltage falls below the IODET detection voltage during POWERON SEQUENCE state, it will change to POWEROFF state.

### **POWERON**

RESETO is pulled up high. CPU can control this PMU through some control pins or I2C Interface. In this state, this PMU is always monitoring the power-off or the repower-on factors.

### **POWEROFF SEQUENCE**

This PMU will change to this state by detecting the power-off factor in POWERON state. In this state, RESETO pin is output low level and all LDO/DCDCs turn off sequentially in reverse order of power-on sequence.

### **REPOWERON SEQUENCE**

This PMU will change to this state by detecting the repower-on factor. RESETO pin is output low level, and all LDO/DCDCs turn off sequentially in reverse order of power-on sequence. After turn-off is completed, repower-on timer starts, and it will change to POWERON SEQUENCE state when repower-on timer expired.

### **SLEEP ENTRY / EXIT SEQUENCE**

This PMU will change to this state by detecting the deep sleep entry/exit factor. LDO/DCDCs turn off/on sequentially and enter or exit SLEEP. Refer to SLEEP ENTRY / EXIT SEQUENCE section.

### **SLEEP**

This PMU will change to this state through SLEEP ENTRY SEQUENCE. In this state, it operates the low power consumption.

### **Shutdown**

If this PMU detects conditions shown below, this PMU will change to NOSUPPLY state or STANDBY state or POWEROFF state regardless of the current state

- Low input voltage under the UVLO detection voltage
- Low input voltage under the VINDET detection voltage
- Low input voltage under the IODET detection voltage  
(Shutdown operation is disabled during POWERON/OFF and REPOWERON SEQUENCE.)
- Abnormal temperature
- Over current of DCDCx  
(Shutdown operation is disabled during POWERON/OFF SEQUENCE.)

### 7.3 Power On Sequence

This PMU's power is turned on by detecting the power-on factor at the POWEROFF state.  
 The default settings of the resources as shown below are programmable.  
 The slot duration can be selected in 0.5ms and 2ms by OTP.

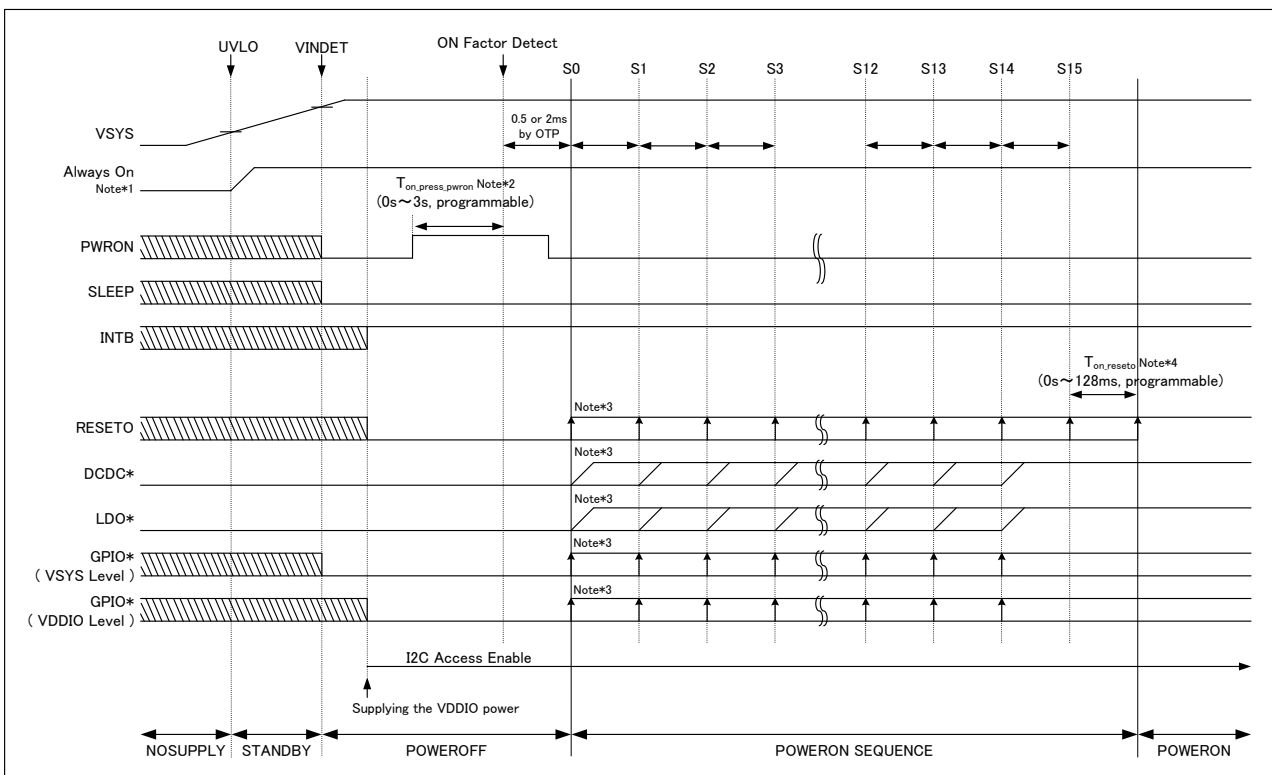
[Controllable resources]

DCDC1-4, LDO1-5, RESETO, PS00-3(GPIO0-3)

[Power-on factor]

PWRON: High level input more than certain time to PWRON pin.  
 ON\_EXTIN(GPIO\*): High input to ON\_EXTIN pin.

Note : This PMU powers on/off according to the on/off sequence. The interrupt is output when these pins are asserted.  
 The power-on/off history is stored by the history register.



Note\*1: Always On is VREF/REGD. Only LDORTC2 default on/off is programmable by OTP.

LDORTC1 power-on timing is programmable either always-on or power-on sequence on by OTP.

Note\*2: Initial values of register can be configured by OTP. (0sec/100us/20ms/128ms/1sec/2sec/3sec)

Note\*3: DCDCx/LDOx/GPIOx power-on timing is programmable by OTP. (S0 to S14)

RESETO release timing is programmable by OTP. (S0 to S15)

Selected slot of DCDCx/LDOx/GPIOx must be set before RESETO release slot.

Note\*4: RESETO has extra time (0sec/32ms/64ms/128ms) by OTP when it is programmed S15.

Note\*: PWRON polarity is programmable by OTP.

Fig 7-2 Power-on Sequence

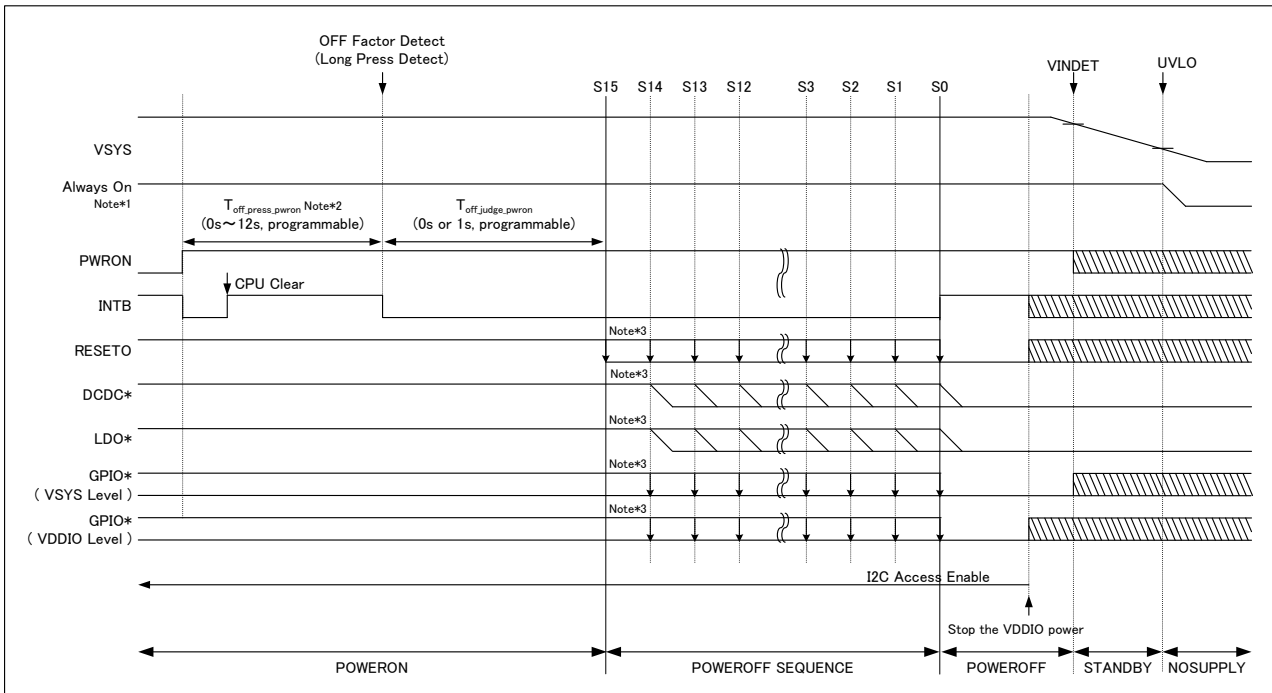


## 7.4 Power Off Sequence

This PMU's power is turn off by detecting the power-off factor at the POWERON or SLEEP state.

[Power-off factor]

- Long power on key press: High level input more than certain time to PWRON pin.
- Watchdog timer: The internal watchdog timer expires.
- <SWPWROFF> register: The CPU writes a dedicated register.
- N\_OE(GPIO\*): High level input more than certain time to N\_OE pin.
- PSHOLD(GPIO\*): Low input to PSHOLD pin.



Note\*1: Always On is VREF/REGD. Only LDORTC2 default on/off is programmable by OTP.

LDORTC1 power-on timing is programmable either always-on or power-on sequence on by OTP.

Note\*2: This value can be selected by register. (0sec/1sec/2sec/4sec/6sec/8sec/10sec/12sec)

Note\*3: The power-off timing reverse order of the power-on sequence.

Selected slot of DCDCx/LDOx/GPIOx must set after RESETO assert slot.

Fig 7-3 Power-off Sequence

### 7.5 Sleep Entry/Exit Sequence

This PMU is changed to the SLEEP state by detecting the sleep-entry factor at the PWRON and PWRON SEQUENCE state.

The state change timing of some resources as shown below is programmable.

[Controllable resources]

- Active/Sleep Control: DCDC1-4, LDO1-5, PSO0-3(GPIO0-3)
- Output Voltage Control: DCDC1-4, LDO1-5

And, this PMU is changed to the PWRON state by detecting the Sleep-exit factor at the SLEEP state. The state change timing of some resources is performed in reverse order of the sleep-entry sequence.

[Sleep-entry factor]

- SLEEP: High input to SLEEP pin.
- <SLPENT> register: The CPU writes a dedicated register.

[Sleep-exit factor]

- SLEEP: Low input to SLEEP pin.
- <SLPEXIT> register: The CPU writes a dedicated register.

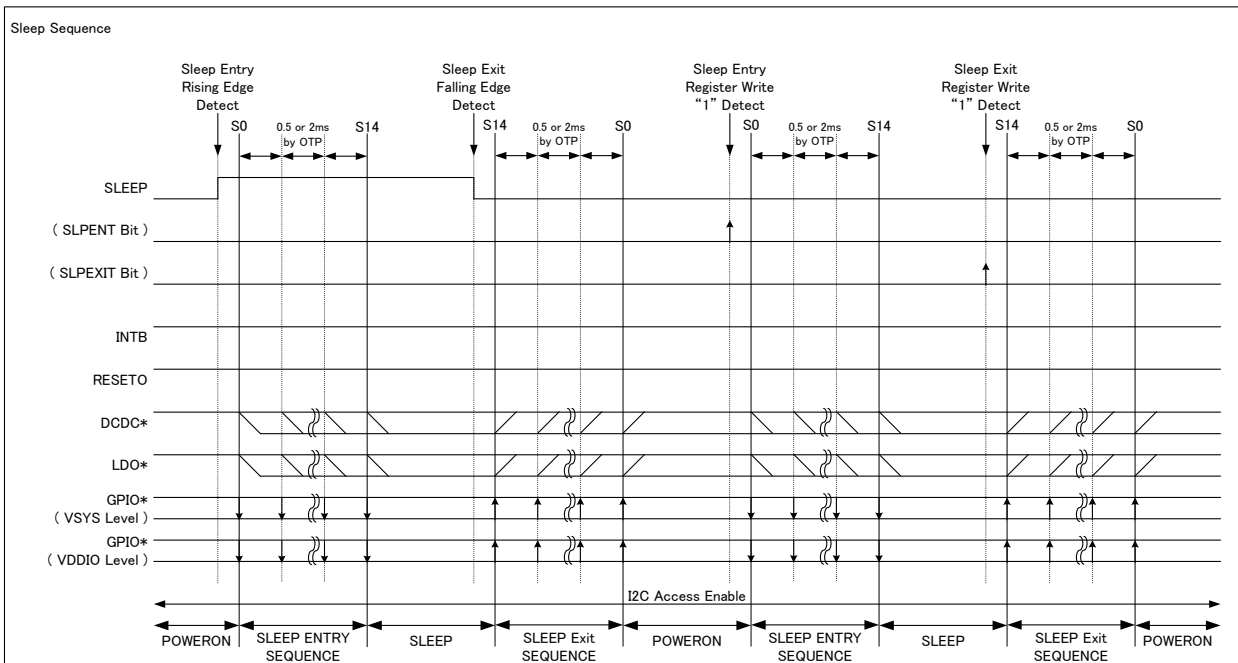
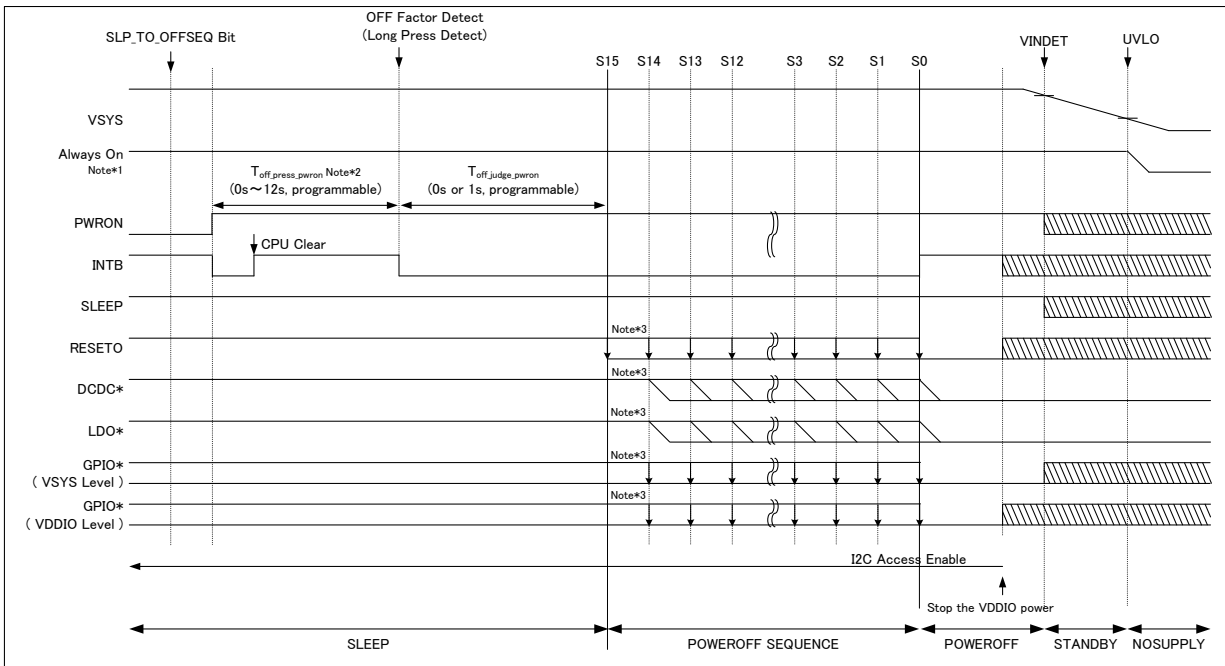


Fig 7-4 Sleep Entry/Exit Sequence

This PMU is changed to the PWOFF SEQUENCE state by detecting PWRON long press at the SLEEP state. It is necessary to write the <SLP\_TO\_OFFSEQ> register in advance.

The state change timing of some resources is performed in reverse order of the power-on sequence.



Note\*1: Always On is VREF/REGD. Only LDORTC2 default on/off is programmable by OTP.

LDORTC1 power-on timing is programmable either always-on or power-on sequence on by OTP.

Note\*2: This value can be selected by register. (0sec/1sec/2sec/4sec/6sec/8sec/10sec/12sec)

Note\*3: The power-off timing is in reverse order of the power-on sequence.

Fig 7-5 Sleep to Power-off Sequence

## 7.6 Repower-on Sequence

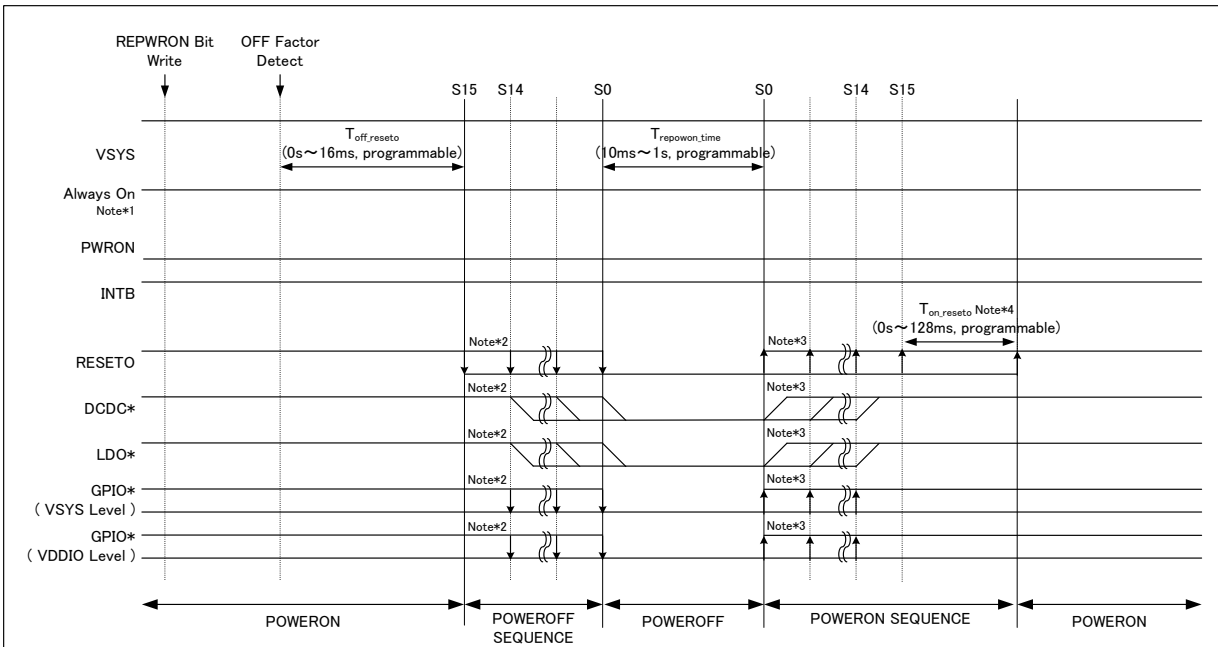
Once the repower-on factor is detected, this PMU executes the power-on sequence after executing the power-off sequence without the power-on factor.

This PMU does not change to POWERON state, when VDDIO pin voltage falls below the IODET detection voltage or repower-on timer is not expired. repower-on timer is selectable 10ms-1s. It is the waiting time for the all regulator's output capacitor to discharge.

[Repower-on factor]

- Long power on key press: High level input more than certain time to PWRON pin.
  - Watchdog timer: The internal watchdog timer expires.
  - <SWPWROFF> register: The CPU writes a dedicated register.
  - N\_OE(GPIO\*): High level input more than certain time to N\_OE pin.
  - HRESET(GPIO\*): High level input to HRESET pin.
- After power off by detecting HRESET, this PMU repower-on regardless of setting value of REPWRON bit.

The state transition time from finishing the repower-on sequence to POWERON SEQUENCE state can be controlled by repower-on timer.



Note\*1: Always On is VREF/REGD. Only LDORTC2 default on/off is programmable by OTP.

LDORTC1 power-on timing is programmable either always-on or power-on sequence on by OTP.

Note\*2: The power-off timing reverse order of the power-on sequence.

Note\*3: DCDCx/LDOx/GPIOx power-on timing is programmable by OTP(S0 to S14).

Note\*4: RESETO has extra time (0/32/64/128ms) by OTP when it is programmed S15.

Fig 7-6 Repower-on Sequence

### 7.7 Shutdown Factor

The following factors trigger a shutdown, and each state is transitioned to NOSUPPLY State/STANDBY State/POWEROFF State.

The transition to POWERON State is enabled when each recovery condition for each shutdown factor is met.

	Shutdown Factor	State of Transition	Recovery Condition from Shutdown
1	UVLO detection	NOSUPPLY	UVLO release
2	VINDET detection	STANDBY	VINDET release
3	Temperature's abnormal detection	POWEROFF	Temperature's normal detection
4	DCDCx current limit detection Note*1	POWEROFF	DCDCx current normal detection
5	IODET(VDDIO monitor) detection*2	POWEROFF	IODET release

Note\*1: This PMU shuts down if over-current continues for 2ms.

Shutdown operation is disabled during POWERON/OFF SEQUENCE.

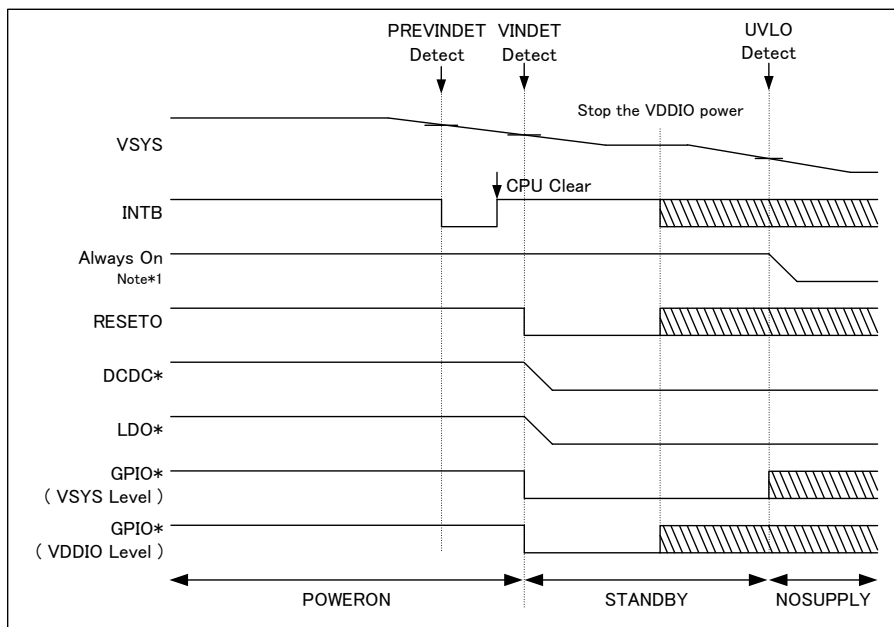
Note\*2: Shutdown operation is disabled during POWERON/OFF SEQUENCE, REPOWERON SEQUENCE.

Table 7-1 Shutdown Factor & Recovery Condition

### 7.8 Shutdown Sequence

This PMU is forcibly powered off when the shutdown factor is detected. All LDO/DCDCs are turned off at once. Until the shutdown condition is recovered, this PMU does not accept the power-on factors. For the reset condition of register, refer to the register map.

#### 7.8.1 Shutdown Sequence (VINDET, UVLO)

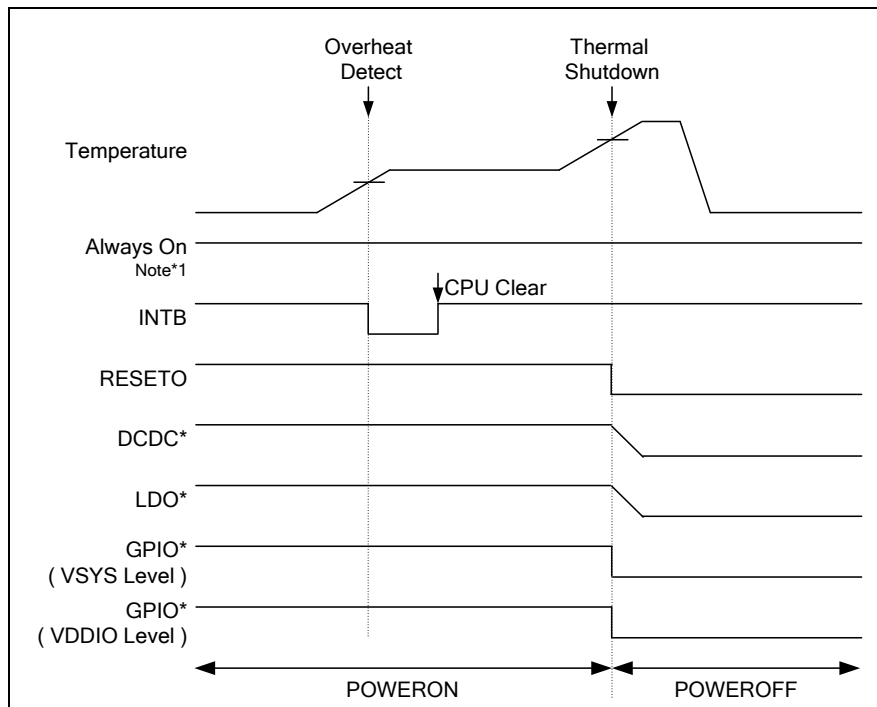


Note\*1: Always On is VREF/REGD. Only LDORTC2 default on/off is programmable by OTP.

LDORTC1 power-on timing is programmable either always-on or power-on sequence on by OTP.

Fig 7-7 Shutdown Sequence (VINDET, UVLO detection)

### 7.8.2 Shutdown Sequence (Abnormal temperature)

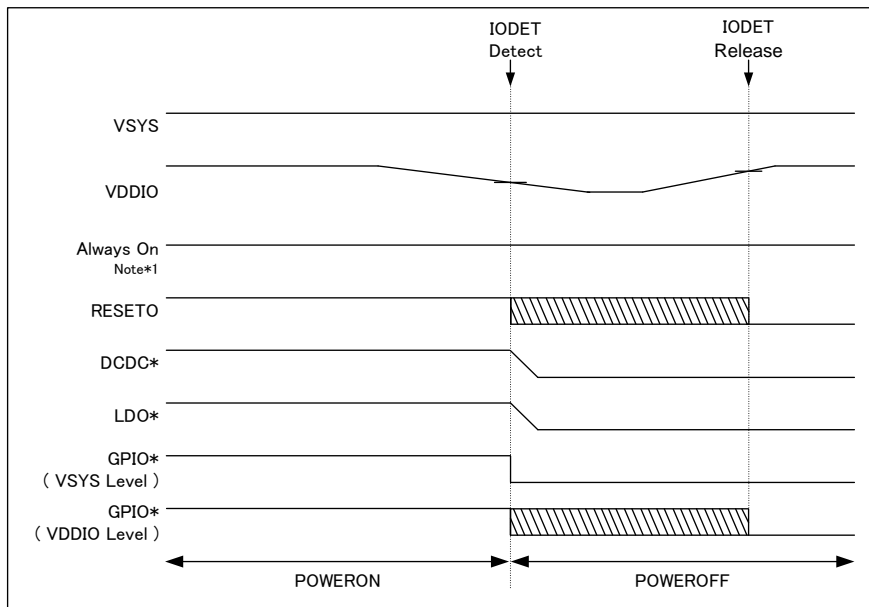


Note\*1: Always On is VREF/REGD. Only LDORTC2 default on/off is programmable by OTP.

LDORTC1 power-on timing is programmable either always-on or power-on sequence on by OTP.

Fig 7-8 Shutdown Sequence (Abnormal temperature)

### 7.8.3 Shutdown Sequence (IODET)



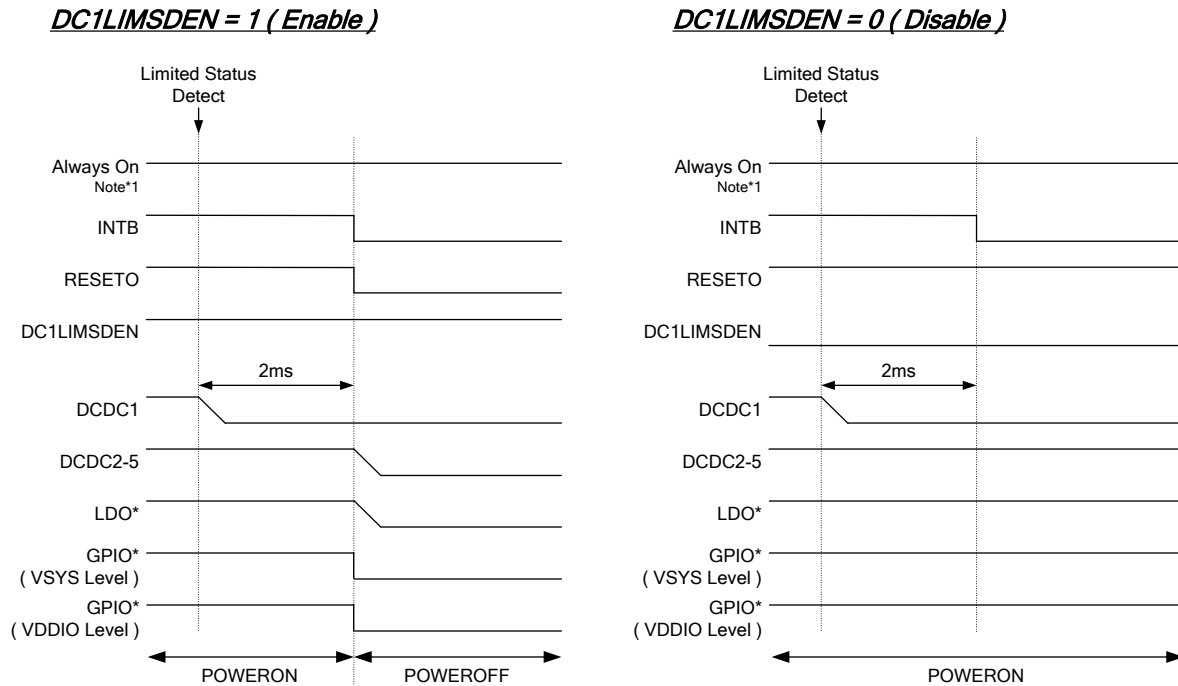
Note\*1: Always On is VREF/REGD. Only LDORTC2 default on/off is programmable by OTP.

LDORTC1 power-on timing is programmable either always-on or power-on sequence on by OTP.

Note\*2: IODET is invalid when VDDIO is not selected as the power supply of both GPIO0 and GPIO1.

Fig 7-9 Shutdown Sequence (IODET)

**7.8.4 Shutdown Sequence (DCDCx current limit detection)**



Note\*1: Always On is VREF/REGD. Only LDORTC2 default on/off is programmable by OTP.  
 LDORTC1 power-on timing is programmable either always-on or power-on sequence on by OTP.

Fig 7-10 Shutdown Sequence (DCDC1 current limit detection)

**7.9 Power-on/off History**

This PMU has the register which monitors the power-on/off factor. After this PMU powers on, CPU can recognize the power-on factor and power-off factor by reading PONHIS register and POFFHIS register.

The power-on factors as below are stored when the power-on sequence starts.

PWRON / ON\_EXTIN(GPIO\*) / HRESET(GPIO\*)

The power-off /repower-on factors stored when the power-off sequence starts.

Long power on key press / Watchdog / SWPWROFF / N\_OE(GPIO\*) / PSHOLD(GPIO\*) / HRESET(GPIO\*)

The shutdown factors as below are stored immediately before the power-off.

TSHUT / VINDET / IODET / DCDC current limit

The repower-on factors as below are stored when the power-off sequence is finished

Repower-on

---

## 7.10 Watchdog Timer Function

This PMU integrates a watchdog timer in order to power off the system when the CPU becomes hung-up. If the CPU does not access the WATCHDOG register until the watchdog timer expired, this PMU output interrupt. And then if the CPU does not clear the interrupt within 1sec, this PMU is transition to POWEROFF SEQUENCE.

A watchdog timer expiring time is programmable from 1 to 128 seconds with a default value of 128 seconds by dedicated register.

## 7.11 Power Control Block Interrupt Request

Power control block provides the interrupt requests to INTC block by the following pin input change or the transition state detection:

- PWRON pin input
  - Outputs the interrupt when PWRON pin input signal changes (See next section).  
    Selectable both-edge/level interrupt type (Default level).
  - Outputs 2nd interrupt after PWRON pin input signal changes (See next section).  
    The interrupt is falling-edge type. If it is not cleared, this PMU powers off.
- Abnormal temperature detection
  - Outputs the interrupt when overheat detection circuit detects the abnormal temperature.  
    Selectable both-edge/level interrupt type (Default level).
- Watchdog timer overflow
  - Outputs the interrupt when the watchdog timer expires.
- PREVINDET (Pre detection)
  - Outputs the interrupt when PREVINDET detects the pre detection voltage.  
    Selectable both-edge/level interrupt type (Default level).

The initial state of all the interrupt request signals from power control block is disabled.

It is necessary to set the interrupt enable bit of each interrupt factor if the interrupt request output to INTC block is permitted. Even if the interrupt output is disabled, CPU can read the each interrupt factor by PWRIRQ register.

For the details of interrupt, refer to the interrupt controller (INTC).



### 7.12 PWRON Long Press Operation

This PMU can output two interrupts by changing the PWRON pin input signal during POWERON state. If CPU does not clear the 2nd interrupt, this PMU changes to the POWEROFF state. For other detailed operations, refer to the appendix.

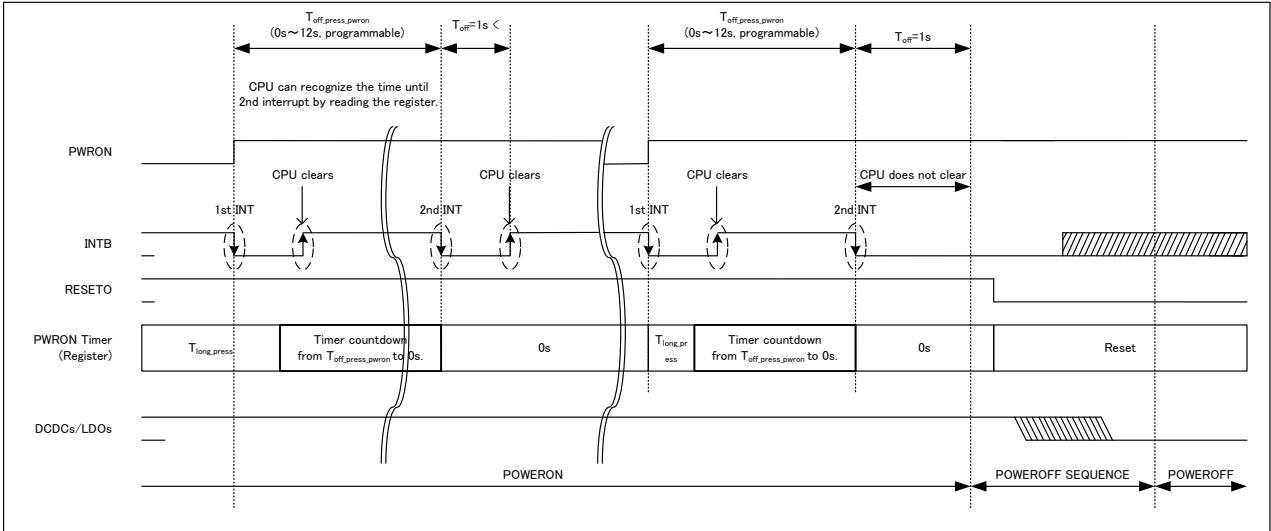


Fig 7-11 PWRON Long Press Operation

### 7.13 Power-on Signal Output by GPIO0-3

This PMU can output the power-on signal from GPIO0-3 pin. This function is selected by OTP. The signals output by GPIO0-3 are asserted sequentially according to a pre-programmed order by OTP. For example, these signals are used for operating external regulators. On SLEEP Entry/Exit sequence, these signals are programmable by the register.

## 7.14 Voltage Detector

### ■ UVLO

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
$V_{Release}$	UVLO Threshold Voltage	VINL1 Voltage Rising		2.30		V
$V_{Detect}$	UVLO Threshold Voltage	VINL1 Voltage Falling	-10%	2.20	+10%	V
$V_{Hys}$	UVLO Hysteresis			100		mV

•  $VINL1 < V_{Detect}$  : Transition to NOSUPPLY state.

### ■ VINDET

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
$V_{Release}$	VINDET Threshold Voltage	VINL1 Voltage Rising		2.90		V
$V_{Detect}$	VINDET Threshold Voltage	VINL1 Voltage Falling	-3%	2.70	+3%	V
$V_{Hys}$	VINDET Hysteresis			200		mV

•  $VINL1 < V_{Detect}$  : Transition to STANDBY state or NOSUPPLY state.

•  $V_{Detect}$  voltage is selected by OTP and register.

### ■ PREVINDET

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
$V_{Release}$	PREVINDET Threshold Voltage	VINL1 Voltage Rising		2.85		V
$V_{Detect}$	PREVINDET Threshold Voltage	VINL1 Voltage Falling	-3%	2.80	+3%	V
$V_{Hys}$	PREVINDET Hysteresis			50		mV

•  $VINL1 < V_{Detect}$  : Generate interrupt to INTB.

•  $V_{Detect}$  voltage is selected by OTP and register.

### ■ IODET

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
$V_{Release}$	IODET Threshold Voltage	VDDIO Voltage Rising		1.65		V
$V_{Detect}$	IODET Threshold Voltage	VDDIO Voltage Falling	-3%	1.60	+3%	V
$V_{Hys}$	IODET Hysteresis			50		mV

•  $V_{Detect}$  voltage is selected by OTP and register.

■ VSBDET

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
V <sub>Release</sub>	VSBDET Threshold Voltage	VSB Voltage Rising		2.8		V
V <sub>Detect</sub>	VSBDET Threshold Voltage	VSB Voltage Falling	2.13	2.3	2.47	V
V <sub>Hys</sub>	VSBDET Hysteresis			500		mV

After VSB output (LDORTC1) rises, DETVSB signal turns to “H” after 400ms from the detection voltage is detected. DETVSB is Nch-opendrain output pin.

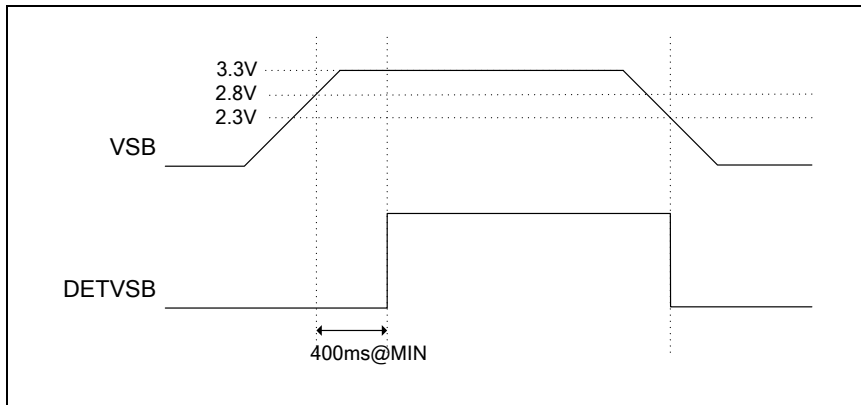


Fig 7-12 Voltage Detection timing

**7.15 Overheat Detection Block**

■ Overheat Detection

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
T <sub>Detect</sub>	Detection Temperature	-	-	135 125 115 105	-	Degrees C
T <sub>Recover</sub>	Recover Temperature	-	T <sub>Detect</sub> -20			Degrees C

- Chip Temperature > T<sub>Detect</sub> : Generate interrupt to INTB.
- T<sub>Detect</sub> temperature is selected by OTP and register.

■ Thermal Shutdown

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
T <sub>Detect</sub>	Detection Temperature	-	-	140	-	Degrees C
T <sub>Recover</sub>	Recover Temperature	-	110			Degrees C

- Chip Temperature > T<sub>Detect</sub> : Transition to POWEROFF state.

## 8. Regulators

### 8.1 Regulators Table

Symbol	DCDC1	DCDC2	DCDC3	DCDC4
Initial Output Voltage	0.6-3.5V	0.6-3.5V	0.6-3.5V	0.6-3.5V
Maximum Output Current	3000mA	3000mA	2000mA	2000mA
External Inductor	1.0 $\mu$ H	1.0 $\mu$ H	1.0 $\mu$ H	1.0 $\mu$ H
External Capacitor	22 $\mu$ F	22 $\mu$ F	22 $\mu$ F	22 $\mu$ F
Output Control	I2C	I2C	I2C	I2C

Table 8-1 Regulator Table (DC/DC)

Symbol	LDO1	LDO2	LDO3	LDO4
Initial Output Voltage	0.9-3.5V	0.9-3.5V	0.6-3.5V	0.9-3.5V
Maximum Output Current	300mA	300mA	300mA	200mA
External Capacitor	1 $\mu$ F	1 $\mu$ F	1 $\mu$ F	1 $\mu$ F
Output Control	I2C	I2C	I2C	I2C

Symbol	LDO5	LDORTC1	LDORTC2	
Initial Output Voltage	0.9-3.5V	1.2-3.5V	0.9-3.5V	
Maximum Output Current	200mA	30mA	10mA	
External Capacitor	1 $\mu$ F	1 $\mu$ F	1 $\mu$ F	
Output Control	I2C	Always-On/I2C	Always-On/I2C	

Table 8-2 Regulator Table (LDO)

## 8.2 DCDC Electrical Characteristics

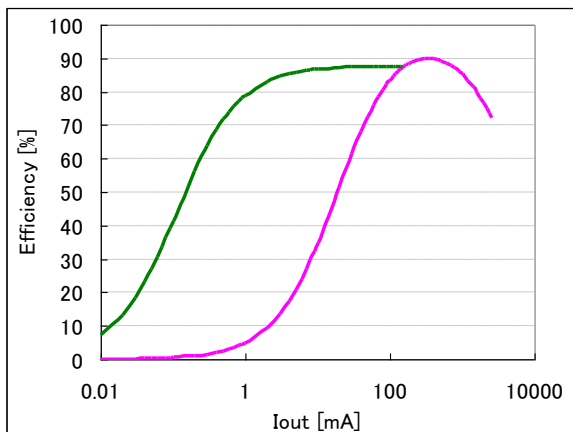
### 8.2.1 DCDC1-2 Electrical Characteristics

Operating Conditions (unless otherwise specified)  $-40 \text{ degrees C} < T_a < 85 \text{ degrees C}$

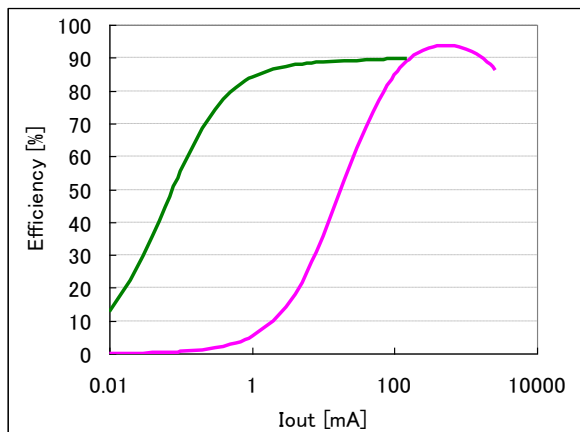
Symbol	Parameter	Condition	Min	Typ	Max	Units	
$V_{IN}$	Input voltage range	-	2.7	3.6	5.5	V	
$V_{OUT}$	Output voltage range	-	0.6	1.2	3.5	V	
	Voltage setting step width	-		12.5		mV	
$V_{accu}$	Output voltage accuracy	$1\text{mA} < I_{OUT} < I_{omax}$ Auto/PSM/PWM Mode	$V_{OUT} < 1.0\text{V}$	-20	0	20	mV
			$1.0 \leq V_{OUT}$	-2	0	2	%
$V_{rip}$	Output ripple voltage	Auto Mode $I_{out}=1\text{mA}$		25		mV	
		PWM Mode		-10	10	mV	
$F_{osc}$	Switching frequency	PWM Mode		1.8		MHz	
$I_{out\_max}$	Maximum output current	Auto/PWM Mode $V_{OUT} < 3.5\text{V}, V_{IN} = V_{OUT} + 1\text{V}$		1000		mA	
		Auto/PWM Mode $V_{OUT} < 2.4\text{V}, V_{IN} = V_{OUT} + 1.1\text{V}$		2000		mA	
		Auto/PWM Mode $V_{OUT} < 1.5\text{V}, V_{in} > 2.8\text{V}$		3000		mA	
		PSM Mode		10		mA	
$I_{lim1}$	Limit current		3200			mA	
$V_{peak}$	Output transition response	$10 \rightarrow 400\text{mA} @ \Delta T = 1.0\mu\text{s}$ , $V_{in} = 3.6\text{V}, V_{OUT} = 1.2\text{V}$			5	%	
$I_{ss}$	Consumption current	Auto Mode	$I_{OUT} = 0\text{mA}$	45		$\mu\text{A}$	
		PSM Mode	$I_{OUT} = 0\text{mA}$	25		$\mu\text{A}$	
$C_{in}$	Input Capacitor			10		$\mu\text{F}$	
$C_{out}$	Output Capacitor	Output Capacitor		22		$\mu\text{F}$	
$L$	External Inductor			1.0		$\mu\text{H}$	

Table 8-3 DCDC1-2 Electrical Characteristic

※ $V_{in}=3.6\text{V}, V_{out}=1.2\text{V}, f=1.8\text{MHz}, L=1.0\mu\text{H}$



※ $V_{in}=5.0\text{V}, V_{out}=3.3\text{V}, f=1.8\text{MHz}, L=1.0\mu\text{H}$



-PWMFIX  
-AUTO

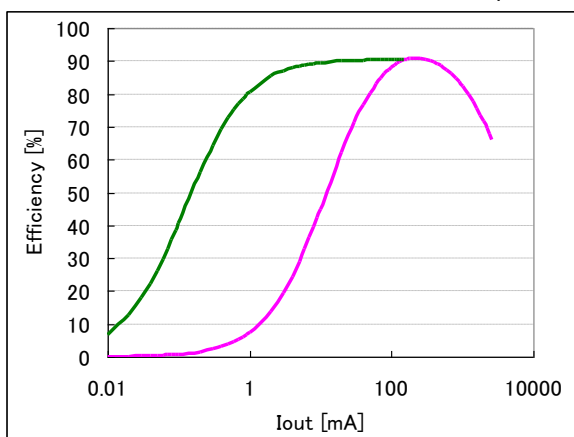
8.2.2 DCDC3-4 Electrical Characteristics

Operating Conditions (unless otherwise specified)  $-40 \text{ degrees C} < T_a < 85 \text{ degrees C}$

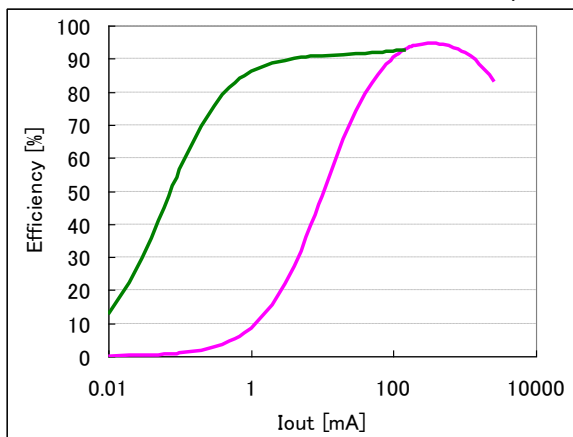
Symbol	Parameter	Condition	Min	Typ	Max	Units	
$V_{IN}$	Input voltage range	-	2.7	3.6	5.5	V	
$V_{OUT}$	Output voltage range	-	0.6	1.2	3.5	V	
	Voltage setting step width	-		12.5		mV	
$V_{accu}$	Output voltage accuracy	$1\text{mA} < I_{OUT} < I_{omax}$ Auto/PSM/PWM Mode	$V_{OUT} < 1.0\text{V}$	-20	0	20	mV
			$1.0 \leq V_{OUT}$	-2	0	2	%
$V_{rip}$	Output ripple voltage	Auto Mode $I_{out}=1\text{mA}$		25		mV	
		PWM Mode		-10	10	mV	
$F_{osc}$	Switching frequency	PWM Mode		1.8		MHz	
$I_{out\_max}$	Maximum output current	Auto/PWM Mode $V_{OUT} < 3.5\text{V}, V_{IN} = V_{OUT} + 1\text{V}$		500		mA	
		Auto/PWM Mode $V_{OUT} < 3.1, V_{IN} = V_{OUT} + 1.1\text{V}$		1000		mA	
		Auto/PWM Mode $V_{OUT} < 1.5\text{V}, V_{in} > 2.9\text{V}$		2000		mA	
		PSM Mode		10		mA	
$I_{lim1}$	Limit current		2300			mA	
$V_{peak}$	Output transition response	$10 \rightarrow 400\text{mA} @ \Delta T = 1.0\mu\text{s}$ , $V_{in} = 3.6\text{V}, V_{OUT} = 1.2\text{V}$			5	%	
$I_{ss}$	Consumption current	Auto Mode	$I_{OUT} = 0\text{mA}$	45		$\mu\text{A}$	
		PSM Mode	$I_{OUT} = 0\text{mA}$	25		$\mu\text{A}$	
$C_{in}$	Input Capacitor			10		$\mu\text{F}$	
$C_{out}$	Output Capacitor	Output Capacitor		22		$\mu\text{F}$	
$L$	External Inductor			1.0		$\mu\text{H}$	

Table 8-4 DCDC3-4 Electrical Characteristic

※ $V_{in}=3.6\text{V}, V_{out}=1.2\text{V}, f=1.8\text{MHz}, L=1.0\mu\text{H}$



※ $V_{in}=5.0\text{V}, V_{out}=3.3\text{V}, f=1.8\text{MHz}, L=1.0\mu\text{H}$



-PWMFIX  
-AUTO

**8.2.3 RAMP Control Operation**

This function starts by setting DC\*DAC register. The ramp rate is controllable by DC\*SR bit.

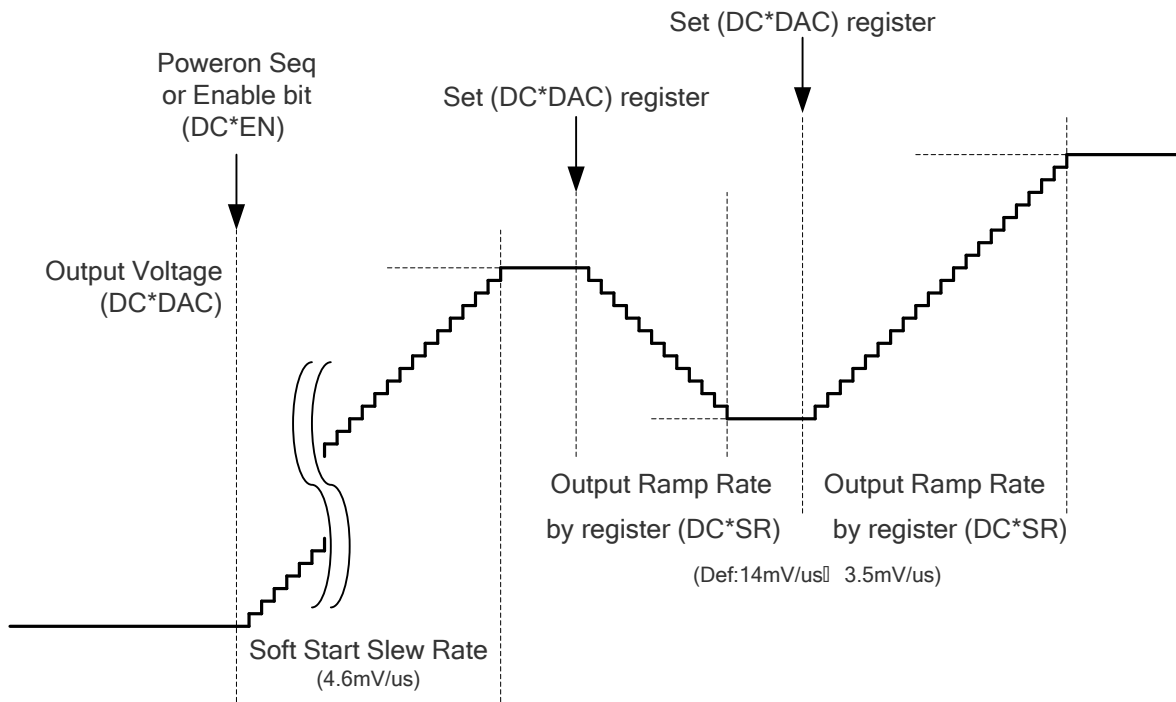


Fig 8-1 Ramp up/down Control Timing Chart

## 8.3 LDO Electrical Characteristics

### 8.3.1 LDO1-2 Electrical Characteristics

Operating Conditions (unless otherwise specified)  $V_{in}=3.6V$ ,  $C_{out}=1.0\mu F$ ,  $T_a = 25$  degrees C

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{IN}$	Input Voltage Range	-	2.7	3.6	5.5	V
$V_{OUT}$	Output Voltage Range	$50\mu A < I_{OUT} < I_{OUTMAX}$	0.9		3.5	V
	Voltage setting step width			50		mV
$V_{accu}$	Output Voltage Accuracy	$V_{OUT}=\text{all output range}$ $I_{out}=1mA$	-1.5		1.5	%
$I_{OUTMAX}$	Output Current	-			300	mA
$I_{LIM}$	Limit Current		350			mA
$V_{diff}$	Dropout Voltage	$V_{out\ setting} = V_{IN}$ , $I_{OUT} = I_{OUTMAX}$			0.2	V
$V_{line}$	Line Regulation	$2.7 < V_{in} < 5.5V$ , $I_{OUT}=1mA$			0.2	%/V
$V_{load}$	Load Regulation	$100\mu A < I_{out} < I_{outmax}$			30	mV
$V_{TR}$	Transient Response	$I_{OUT}=100\mu A \leftrightarrow I_{OUTMAX} / 2$		10		mV
RR	Ripple Rejection	$f=217 \sim 1kHz$ , $I_{OUT} = I_{OUTMAX} / 2$ $V_{diff} > 0.6V$		70		dB
$O_{Noise}$	Output Noise	$I_{OUT} = I_{OUTMAX} / 2$ $BW=10Hz-100kHz$ , $V_{out}=1.2V$		25		$\mu V_{rms}$
$I_{SS}$	Supply Current	$I_{OUT}=0mA$		100		$\mu A$
$I_{OFF}$	Standby current	$I_{OUT}=0mA$			1	$\mu A$
$T_r$	Rising time	$V_{OUT} \times 0.9$ , $I_{OUT}=0mA$			500	$\mu s$
$T_f$	Falling time	$V_{OUT} \times 0.1$ , $I_{OUT}=0mA$			500	$\mu s$
$C_{out}$	Output Capacitor			1.0		$\mu F$

Table 8-5 LDO1-2 Electrical Characteristic



**8.3.2 LDO3 Electrical Characteristics**Operating Conditions (unless otherwise specified)  $V_{in}=3.6V$ ,  $C_{out}=1.0\mu F$ ,  $T_a = 25$  degrees C

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{IN}$	Input Voltage Range	-	1.7	3.6	5.5	V
$V_{OUT}$	Output Voltage Range	$50\mu A < I_{OUT} < I_{OUTMAX}$	0.6		3.5	V
	Voltage setting step width			50		mV
$V_{accu}$	Output Voltage Accuracy	$V_{OUT}=\text{all output range}$ $I_{out}=1mA$	-1.5		1.5	%
$I_{OUTMAX}$	Output Current	-			300	mA
$I_{LIM}$	Limit Current		350			mA
$V_{diff}$	Dropout Voltage	$V_{out}$ setting = $V_{IN}$ , $I_{OUT}= I_{OUTMAX}$			0.3	V
$V_{line}$	Line Regulation	$1.7 < V_{in} < 5.5V$ , $I_{OUT}=1mA$			0.2	%/V
$V_{load}$	Load Regulation	$100\mu A < I_{out} < I_{outmax}$			30	mV
$V_{TR}$	Transient Response	$I_{OUT}=100\mu A \leftrightarrow I_{OUTMAX} / 2$		40		mV
RR	Ripple Rejection	$f=217\sim 1kHz$ , $I_{OUT}= I_{OUTMAX} / 2$ $V_{diff} > 0.6V$		60		dB
$O_{Noise}$	Output Noise	$I_{OUT}= I_{OUTMAX} / 2$ BW=10Hz-100kHz $V_{out}=1.2V$		60		$\mu V_{rms}$
$I_{SS}$	Supply Current	$I_{OUT}=0mA$		20		$\mu A$
$I_{OFF}$	Standby current	$I_{OUT}=0mA$			1	$\mu A$
$T_r$	Rising time	$V_{OUT} \times 0.9$ , $I_{OUT}=0mA$			500	us
$T_f$	Falling time	$V_{OUT} \times 0.1$ , $I_{OUT}=0mA$			500	us
$C_{out}$	Output Capacitor			1.0		$\mu F$

Table 8-6 LDO3 Electrical Characteristic

**8.3.3 LDO4-5 Electrical Characteristics**Operating Conditions (unless otherwise specified)  $V_{in}=3.6V$ ,  $C_{out}=1.0\mu F$ ,  $T_a = 25$  degrees C

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{IN}$	Input Voltage Range	-	1.7	3.6	5.5	V
$V_{OUT}$	Output Voltage Range	$50\mu A < I_{OUT} < I_{OUTMAX}$	0.9		3.5	V
	Voltage setting step width			50		mV
$V_{accu}$	Output Voltage Accuracy	$V_{OUT}=\text{all output range}$ $I_{out}=1mA$	-1.5		1.5	%
$I_{OUTMAX}$	Output Current	-			200	mA
$I_{LIM}$	Limit Current		250			mA
$V_{diff}$	Dropout Voltage	$V_{out}$ setting = $V_{IN}$ , $I_{OUT}= I_{OUTMAX}$			0.4	V
$V_{line}$	Line Regulation	$2.7 < V_{in} < 5.5V$ , $I_{OUT}=1mA$			0.2	%/V
$V_{load}$	Load Regulation	$100\mu A < I_{out} < I_{outmax}$			30	mV
$V_{TR}$	Transient Response	$I_{OUT}=100\mu A \leftrightarrow I_{OUTMAX} / 2$		40		mV
RR	Ripple Rejection	$f=217\sim 1kHz$ , $I_{OUT}= I_{OUTMAX} / 2$ $V_{diff} > 0.6V$		60		dB
$O_{Noise}$	Output Noise	$I_{OUT}= I_{OUTMAX} / 2$ BW=10Hz-100kHz $V_{out}=1.2V$		50		$\mu V_{rms}$
$I_{SS}$	Supply Current	$I_{OUT}=0mA$		20		$\mu A$
$I_{OFF}$	Standby current	$I_{OUT}=0mA$			1	$\mu A$
$T_r$	Rising time	$V_{OUT} \times 0.9$ , $I_{OUT}=0mA$			500	us
$T_f$	Falling time	$V_{OUT} \times 0.1$ , $I_{OUT}=0mA$			500	us
$C_{out}$	Output Capacitor			1.0		$\mu F$

Table 8-7 LDO4-5 Electrical Characteristic

**8.3.4 LDORTC1 Electrical Characteristics**Operating Conditions (unless otherwise specified)  $V_{IN}=3.6V$ ,  $C_{OUT}=1.0\mu F$ ,  $T_a = 25$  degrees C

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{IN}$	Input Voltage Range	-	2.2	3.6	5.5	V
$V_{OUT}$	Output Voltage Range	$50\mu A < I_{OUT} < I_{OUTMAX}$	1.2		3.5	V
	Voltage setting step width			50		mV
$V_{accu}$	Output Voltage Accuracy	$V_{OUT}=\text{all output range}$ $I_{OUT}=1mA$	-1.5		1.5	%
$I_{OUTMAX1}$	Output Current				30	mA
$I_{OUTMAX2}$		$4.5V < V_{IN} < 5.5V$			100	mA
$V_{diff}$	Dropout Voltage	$V_{out\ setting} = V_{IN}$ , $I_{OUT} = I_{OUTMAX1}$			0.8	V
$I_{LIM}$	Limit Current		110			mA
$V_{diff}$	Dropout Voltage	$V_{out\ setting} = V_{IN}$ , $I_{OUT} = I_{OUTMAX}$			0.2	V
$I_{SS}$	Supply Current	$I_{OUT}=0mA$		2		$\mu A$
$I_{OFF}$	Standby current	$I_{OUT}=0mA$			1	$\mu A$
$C_{OUT}$	Output Capacitor			1.0		$\mu F$

Table 8-8 LDORTC1 Electrical Characteristic

**8.3.5 LDORTC2 Electrical Characteristics**Operating Conditions (unless otherwise specified)  $V_{in}=3.6V$ ,  $C_{out}=1.0\mu F$ ,  $T_a = 25$  degrees C

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{IN}$	Input Voltage Range	-	2.2	3.6	5.5	V
$V_{OUT}$	Output Voltage Range	$50\mu A < I_{OUT} < I_{OUTMAX}$	0.9		3.5	V
	Voltage setting step width			50		mV
$V_{accu}$	Output Voltage Accuracy	$V_{OUT}=\text{all output range}$ $I_{out}=1mA$	-1.5		1.5	%
$I_{OUTMAX}$	Output Current	-			10	mA
$I_{LIM}$	Limit Current		20			mA
$V_{diff}$	Dropout Voltage	$V_{out}$ setting = $V_{IN}$ , $I_{OUT}= I_{OUTMAX}$			0.2	V
$I_{SS}$	Supply Current	$I_{OUT}=0mA$		1		$\mu A$
$I_{OFF}$	Standby current	$I_{OUT}=0mA$			1	$\mu A$
$C_{out}$	Output Capacitor			1.0		$\mu F$

Table 8-9 LDORTC2 Electrical Characteristic

## 9. MODE

This PMU has two Modes selected by OTP.

MODE	Pin					
	GPIO0	GPIO1	GPIO2	GPIO3	SLEEP	PWRON
Normal	selectable				SLEEP	PWRON
Parts	DCDC1 EXON	DCDC2 EXON	DCDC3 EXON	DCDC4EXON and LDO3EXON	LDO1EXON and LDO4EXON	LDO2EXON and LDO5EXON

Table 9-1 Modes and function of pins

### 9.1 Normal MODE

The function of GPIO0-3 pins can be respectively selected by OTP. Note\*

The function of SLEEP and PWRON pins are respectively decided SLEEP and PWRON.

Note\*: For details of the function of GPIO\* pins, refer to GPIO.

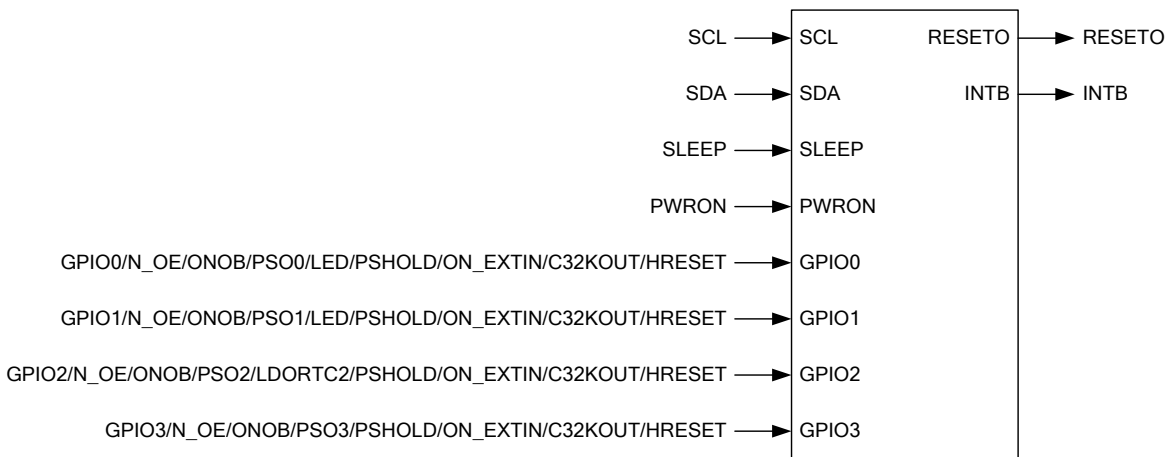


Fig 9-1 The function of pins in Normal mode

**9.2 Parts MODE**

ON/OFF of DCDC1-4 and LDO1-5 can be controlled by pin.  
 GPIO0 pin can control ON/OFF of DCDC1.  
 GPIO1 pin can control ON/OFF of DCDC2.  
 GPIO2 pin can control ON/OFF of DCDC3.  
 GPIO3 pin can control ON/OFF of DCDC4 and LDO3.  
 SLEEP pin can control ON/OFF of LDO1 and LDO4.  
 PWRON pin can control ON/OFF of LDO2 and LDO5.

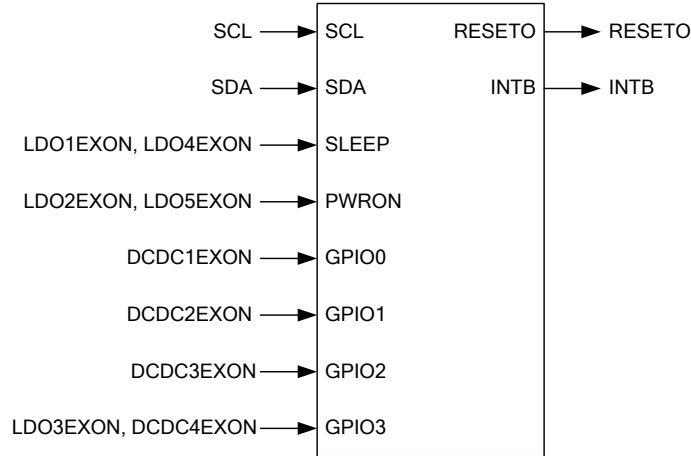


Fig 9-2 The function of pins in Parts mode

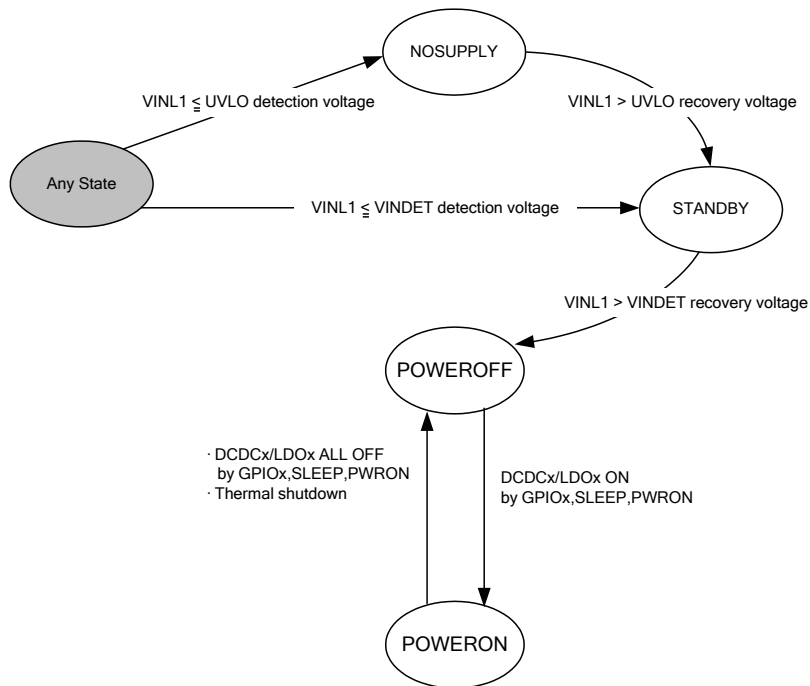
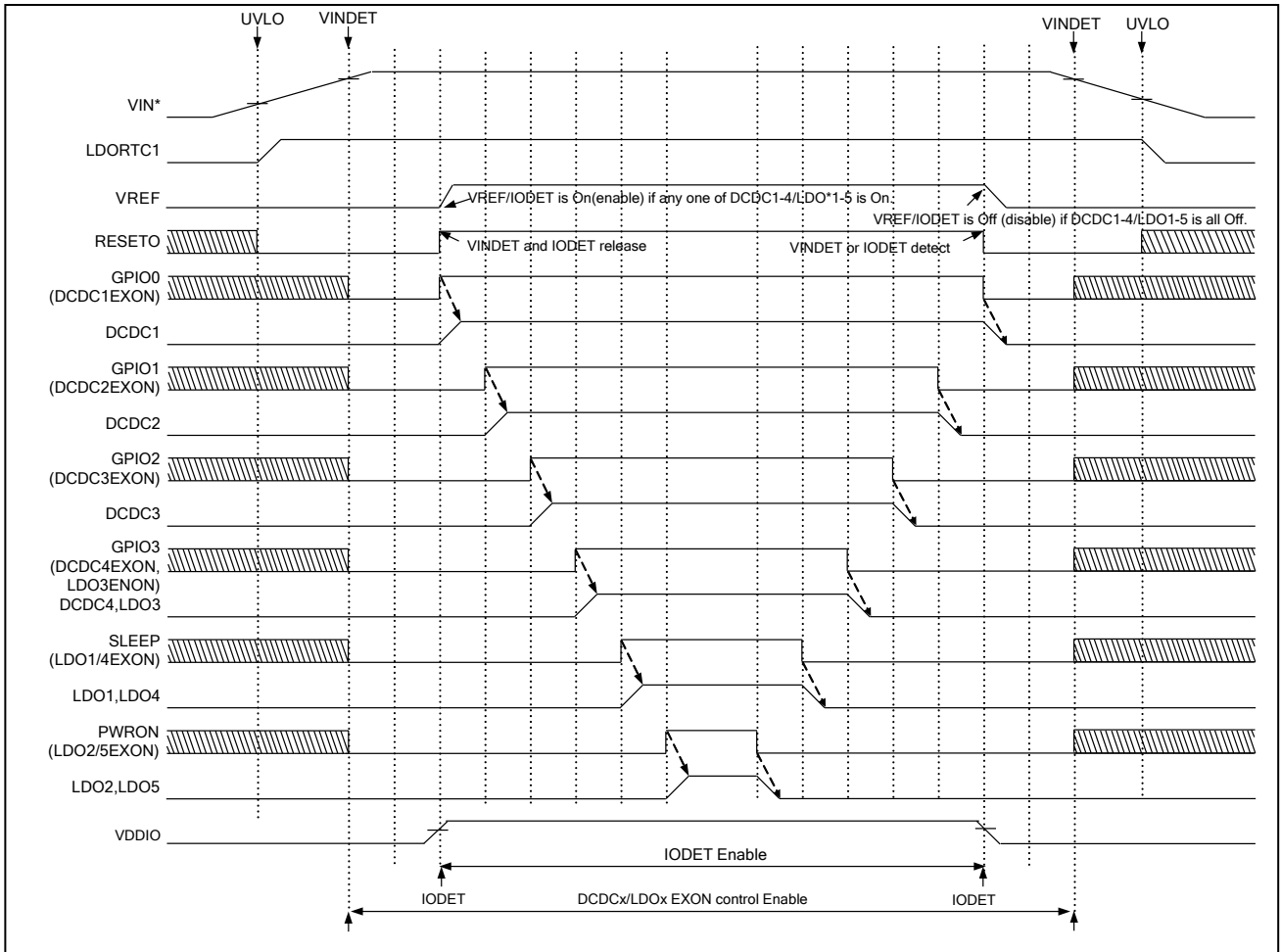


Fig 9-3 State Machine Diagram in Parts mode



Note\*: Each resource turns off by writing the enable bit (LDO\*EN/DC\*EN bit) to "0".

LDO\*EN/DC\*EN bit:

LDO1-5EN: 44h bit [4:0]

DC1-4EN: 2Ch/2Eh/30h/32h bit0

Fig 9-4 Power On/Off function in Parts mode

## 10. GPIO

This PMU supports four channels of general purpose input/output.  
GPIO0-3 pins have the function selected by OTP as shown below.

Name	Function	Input,*1,*2	Output,*1,*2	Power,*3	GPIO			
					0	1	2	3
N_OE	External power off	N	-	VSYS	○	○	○	○
GPIO0	General purpose I/O	C or N	C or N	VSYS or VDDIO	○	-	-	-
GPIO1	General purpose I/O	C or N	C or N	VSYS or VDDIO	-	○	-	-
GPIO2	General purpose I/O	C or N	C or N	VSYS	-	-	○	-
GPIO3	General purpose I/O	C or N	C or N	VSYS	-	-	-	○
ONOB	PWRON pin monitor	-	N	VSYS	○	○	○	○
PSO0	Power-on signal output function	-	C or N	VSYS or VDDIO	○	-	-	-
PSO1	Power-on signal output function	-	C or N	VSYS or VDDIO	-	○	-	-
PSO2	Power-on signal output function	-	C or N	VSYS	-	-	○	-
PSO3	Power-on signal output function	-	C or N	VSYS	-	-	-	○
LDORTC2	LDORTC2 output	-	A	-	-	-	○	-
LED	LED function	-	N	VSYS	○	○	-	-
PSHOLD	PSHOLD (power-on hold) function	N	-	VSYS	○	○	○	○
ON_EXTIN	External input for on factor	N	-	VSYS	○	○	○	○
**EXON	External LDO*/DCDC* on/off input	N	-	VSYS	*4	*4	*4	*4
C32KOUT	32 kHz clock output function	-	C or N	VSYS or VDDIO	○	○	○	○
HRESET	Hard RESET input	N	-	VSYS	○	○	○	○

Note\*1: Explanation of column of "Input" and "Output" :

A : Analog Output.

C : CMOS Input/Output.

N : NMOS Input(VSYS only)/ Nch Open Drain Output.

Note\*2: CMOS or Nch is selectable by OTP.

Note\*3: VSYS or VDDIO is selectable by OTP.

Note\*4: Refer to the chapter of Mode.

Table 10-1 The function of GPIO0-3 pins



N\_OE function(GPIO0-3 pins)

Power-off factor.  
 Programmable polarity of input signal by OTP.

GPIO function (GPIO0-3 pins)

Can be controlled the direction by IOSEL register (output or input).  
 Output mode:  
 Each output circuit is programmed CMOS or Nch open drain by OTP.  
 Input mode:  
 Programmable polarity of input signal by OTP.  
 Programmable interrupt detection, edge or level by GPEDGE1,2 register.  
 (For the details of interrupt, refer to the interrupt controller and GPIO).

ONOB function (GPIO0-3 pins)

Output Low when PWRON pin is pressed.

PSO function (GPIO0-3 pins)

Power-on signal output function.  
 Programmable output timing in the POWERON/POWEROFF sequence by OTP.  
 Programmable output timing in SLEEP\_ENTRY/EXIT sequence by the register.

LDORTC2 output function (GPIO2 pins)

Output LDORTC2.

LED function (GPIO0-1 pins)

Programmable Power On/Off mode or Register mode by register.  
 Programmable type of flicker by register in Register mode. Note\*

Note\*: For details of type of flicker by register, refer to GP\*\_LEDMODE register.

Mode	Power State	Type of Flicker
Power On/Off Mode	Power On	Always Turn-on
	Power Off	Always Turn-off
Register Mode	Power On	Depend on GP*_LEDFUNC register

Table 10-2 Type of flicker

PSHOLD input function (GPIO0-3 pins)

Power-on hold and power-off factor.  
 Hold power-on even if power-on factor de-asserts, when PSHOLD asserts less than 500ms since RESET0 is released. Note\*  
 Power-off when PSHOLD de-asserts in power-on. Note\*  
 Programmable polarity of input signal by OTP.

Note\*: For details of power-on/power-off by PSHOLD, refer to Appendix.

ON\_EXTIN input function (GPIO0-3 pins)

Power-on factor.

Programmable polarity of input signal by OTP.

\*\*EXON input function(GPIO0-3 pins)

DCDC1-4, LDO1-5 on/off control signals.

Refer to the chapter of Mode.

32 kHz clock output function (GPIO0-3 pins)

Output 32 kHz clock.

HRESET function(GPIO0-3 pins)

Reset (Power Off - Repower ON) factor.

Programmable polarity of input signal by OTP.

## 11. I2C-Bus interface

This PMU uses I2C-Bus system for CPU connection through two wires. Connection and transfer system of I2C-Bus are described in the following sections.

### 11.1 I2C-Bus Operation

Within the procedure of I2C-Bus, unique situations arise which are defined as start and stop conditions.

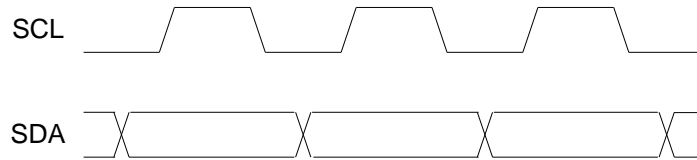


Fig 11-1 I2C-Bus Data Transmission

An "H" to "L" transition on SDA line while SCL is "H" indicates a start condition. An "L" to "H" transition on SDA line while SCL is "H" defines a stop condition. Start and stop conditions are always generated by master. (Refer to the figure below). The bus is considered to be busy after start condition. The bus is considered to be free again a certain time after the stop condition.

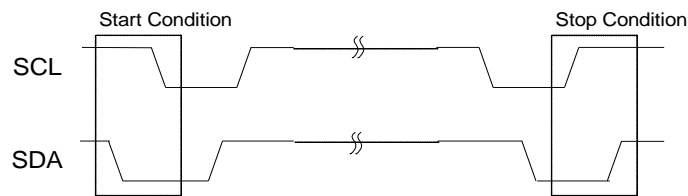


Fig 11-2 I2C-Bus Start and Stop Condition

## 11.2 AC Characteristics of I2C-Bus

Operating Conditions (unless otherwise specified) V<sub>OUTD</sub> = 1.8V, T<sub>a</sub> = 25 degrees C, C<sub>b</sub> = 400pF max

Symbol	Parameter	Condition	Min	Typ	Max	Units
f <sub>SCL</sub>	SCL Clock Frequency	-			400	kHz
t <sub>BUF</sub>	Bus Free Time Between a Precedent and Start	-	1.3		-	us
t <sub>LOW</sub>	SCL Clock "L" Time	-	1.3		-	us
t <sub>HIGH</sub>	SCL Clock "H" Time	-	0.6		-	us
t <sub>SU;STA</sub>	Start Condition Setup Time	-	0.6		-	us
t <sub>HD;STA</sub>	Start Condition Hold Time	-	0.6		-	us
t <sub>SU;STO</sub>	Stop Condition Setup Time	-	0.6		-	us
t <sub>HD;DAT</sub>	Data Hold Time	-	0			us
t <sub>SU;DAT</sub>	Data Setup Time	-	100 (*1)		-	ns
t <sub>R</sub>	Rising Time of SCL and SDA (Input)	-			300	ns
t <sub>F</sub>	Falling Time of SCL and SDA (Input)	-			300	ns
t <sub>SP</sub>	Suppressing Pulse Width	-	0		50	ns

- Fast Speed Mode

Operating Conditions (unless otherwise specified) V<sub>OUTD</sub> = 1.8V, T<sub>a</sub> = 25 degrees C, C<sub>b</sub> = 100pF max

Symbol	Parameter	Condition	Min	Typ	Max	Units
f <sub>SCL</sub>	SCL Clock Frequency	-			3.4	MHz
t <sub>LOW</sub>	SCL Clock "L" Time	-	160		-	ns
t <sub>HIGH</sub>	SCL Clock "H" Time	-	60		-	ns
t <sub>SU;STA</sub>	Start Condition Setup Time	-	160		-	ns
t <sub>HD;STA</sub>	Start Condition Hold Time	-	160		-	ns
t <sub>SU;STO</sub>	Stop Condition Setup Time	-	160		-	ns
t <sub>HD;DAT</sub>	Data Hold Time	-	0		70	ns
t <sub>SU;DAT</sub>	Data Setup Time	-	10		-	ns
t <sub>RCL</sub> , t <sub>FCL</sub>	Rising and Falling Time of SCL	-	10		40	ns
t <sub>RDA</sub> , t <sub>FDA</sub>	Rising and Falling Time of SDA	-	20		80	ns
t <sub>SP</sub>	Suppressing Pulse Width	-	0		10	ns

- Hs Mode

C<sub>b</sub>: Capacitive load for each bus line

Table 11-1 I2C-Bus AC Characteristics

Note\*: All the above-mentioned values are corresponding to V<sub>IH</sub> min and V<sub>IL</sub> max level.

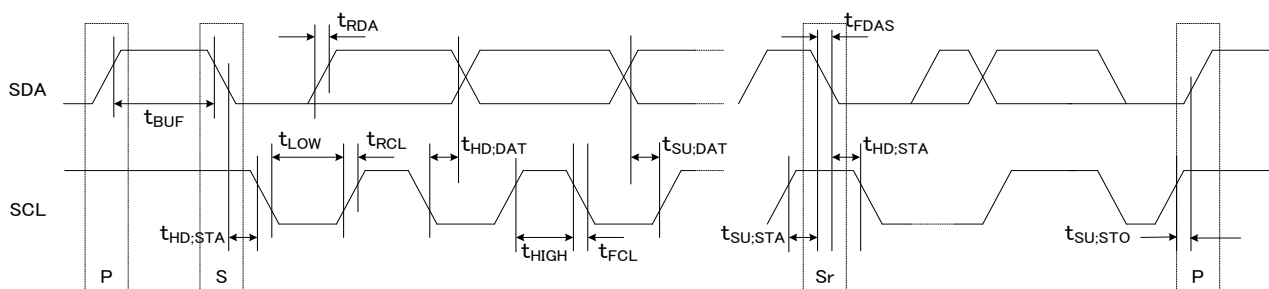


Fig 11-3 I2C-Bus Interface Timing Chart

### 11.3 I2C-Bus Data Transmission and its Acknowledge

After start condition, data is transmitted by 1byte (8bits). The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit.

Data transmission with acknowledge is obligatory. The acknowledge-related clock pulse is generated by the master. The transmitter releases SDA line during the acknowledge clock pulse.

The receiver must pull down SDA line during the acknowledge clock pulse so that SDA line remains stable “L” during the “H” period of the acknowledge clock pulse.

If a master–receiver is involved in a transfer, it must signal the end of the data to the slave-transmitter by not generating acknowledge on the last byte that was clocked out of the slave. The slave-transmitter must release the data line to allow the master to generate a stop condition.

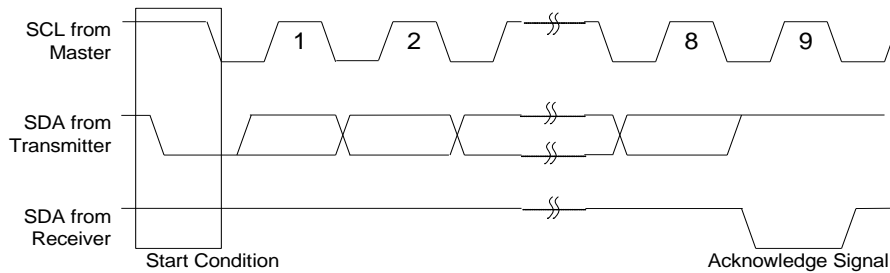


Fig 11-4 I2C-Bus Data Transmission and Acknowledge

### 11.4 I2C-Bus Slave Address

After start condition, a slave address is sent. The address is 7-bit long followed by an 8<sup>th</sup> bit which is data direction bit (Read/Write). The slave address of This PMU is programmable by OTP.

	A7	A6	A5	A4	A3	A2	A1
Setting value	0	1	1	0	0 Note*	1 Note*	0 Note*

A7~A1: Slave address

Note\*: A3~A1 of the slave address are programmable by OTP.

Table 11-2 Slave Address of This PMU

**11.5 I2C-Bus Data Transmission Read Format (Fast Speed mode)**

In order to read the internal register data:

- Specify an internal address pointer (8bit).
- Generate the repeated start condition to change the data transmission direction to read.

With a start of read mode, automatic increment in address pointers will be made. Read-mode is repeated until stop condition is initiated.

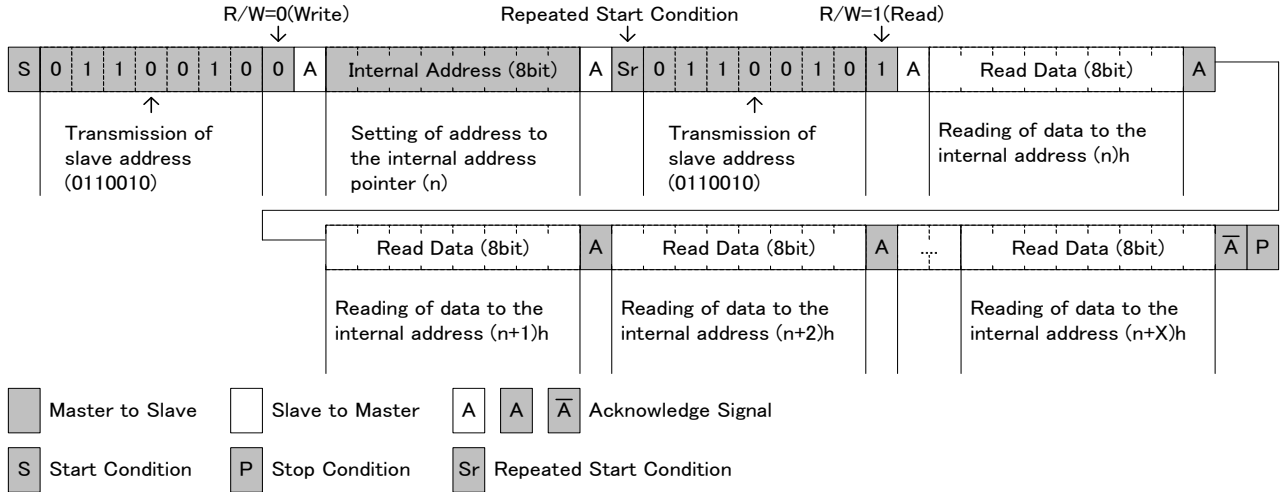


Fig 11-5 I2C-Bus Data Transmission Read Format

**11.6 I2C-Bus Data Transmission Write Format (Fast Speed mode)**

The transmission format for the slave address allocated to each IC is defined by I2C-Bus standard. However transmission method of address information of each IC is not defined. This PMU transmits command data. For the data transmission, please transmit MSB first from master and following data in sequence.

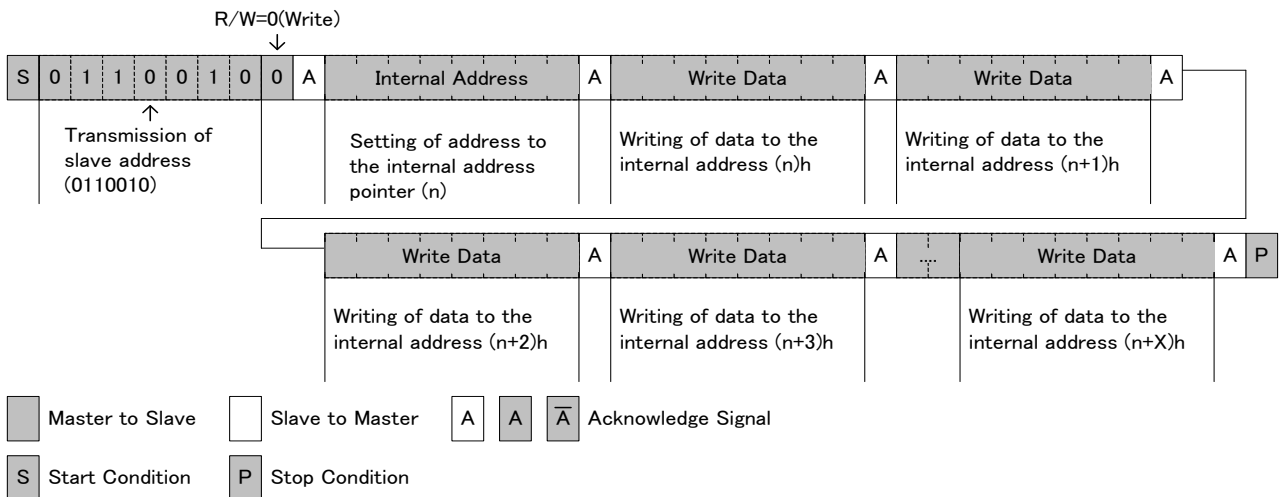


Fig 11-6 I2C-Bus Data Transmission Write Format

The format which supports the power I2C is shown below.

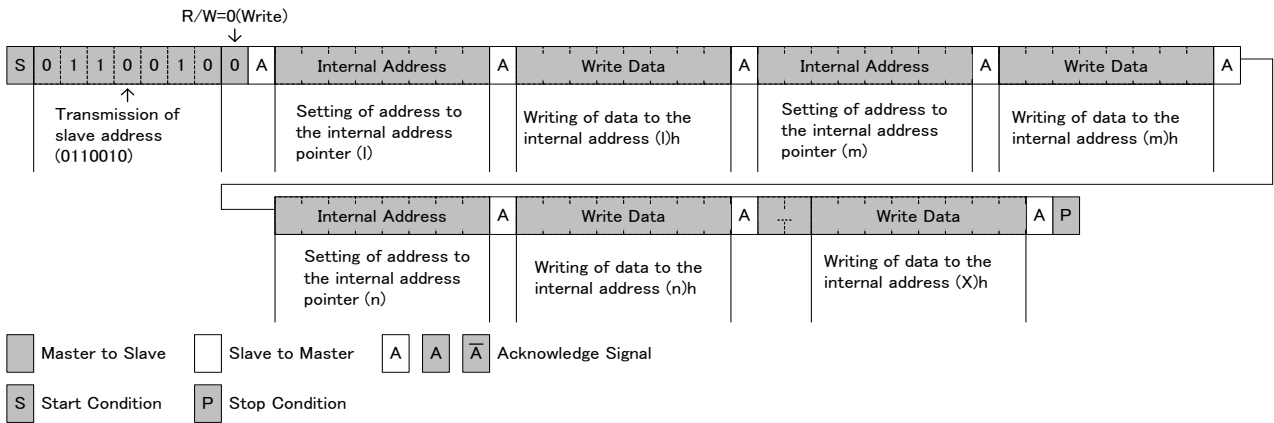


Fig 11-7 I2C-Bus Data Transmission Write Format (Power I2C)

### 11.7 I2C-Bus Internal Register Write-in Timing (Fast Speed mode)

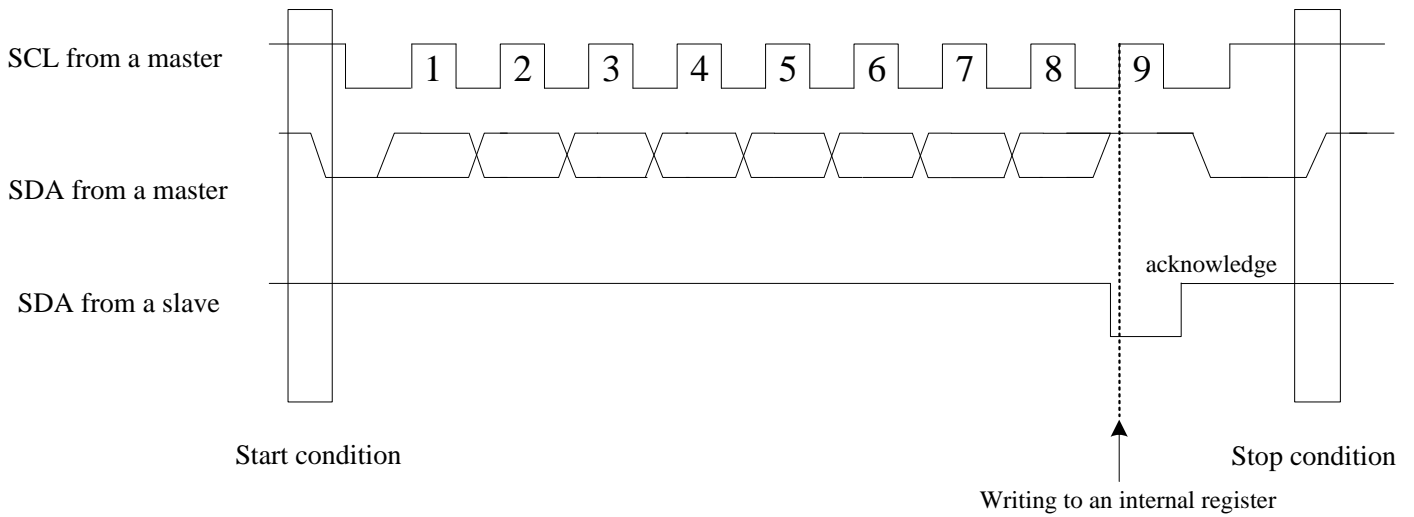


Fig 11-8 I2C-Bus Internal Register Write-in Timing

**11.8 I2C-Bus Data Transmission Read Format (Hs mode)**

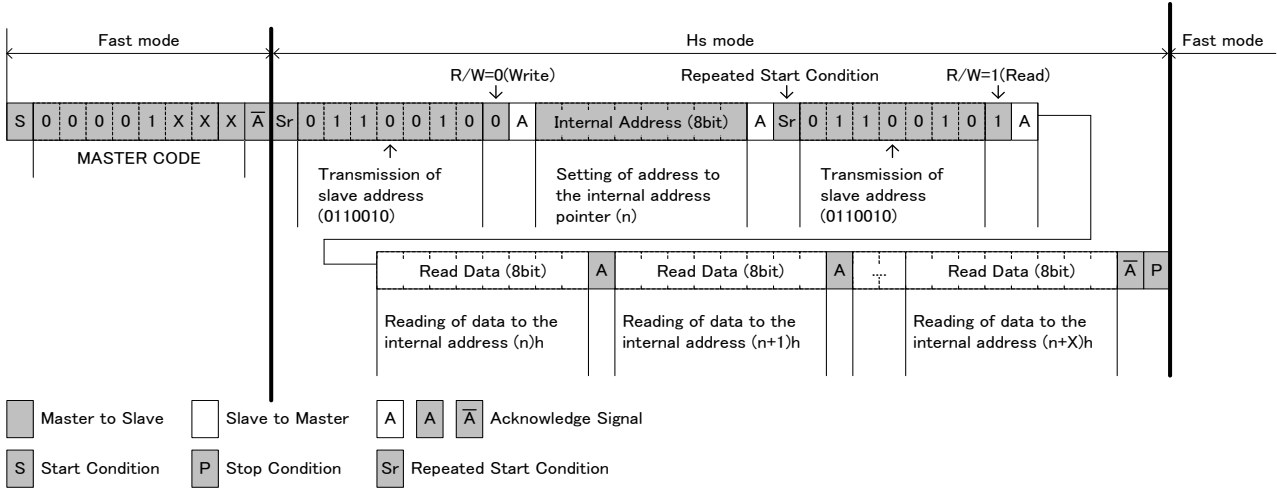
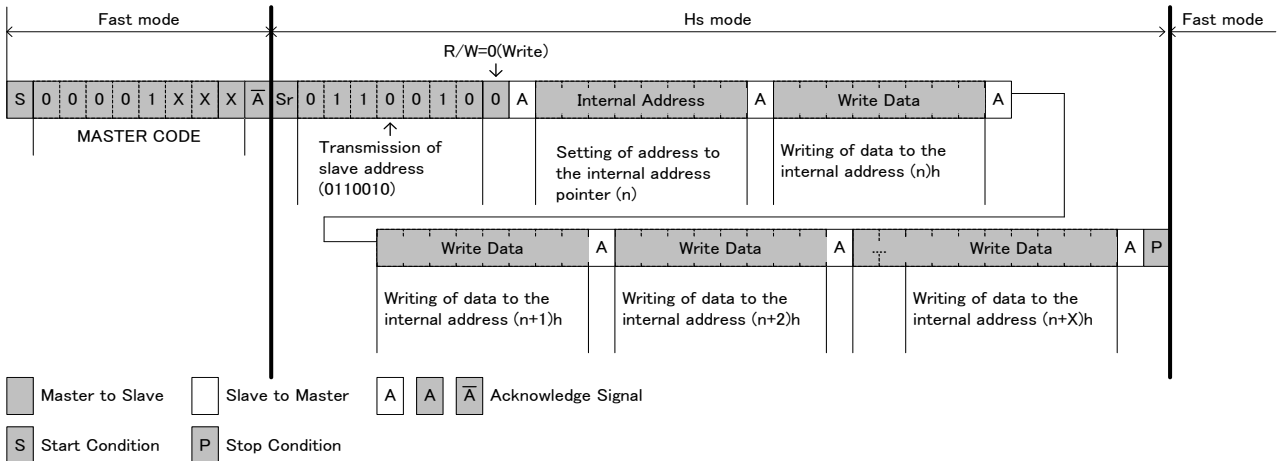


Fig 11-9 I2C-Bus Data Transmission Read Format (Hs mode)

**11.9 I2C-Bus Data Transmission Write Format (Hs mode)**



Note\*: Should have the interval of 100us or more at writing and reading the same address.

Fig 11-10 I2C-Bus Data Transmission Write Format (Hs mode)



## 12. Interrupt Controller (INTC)

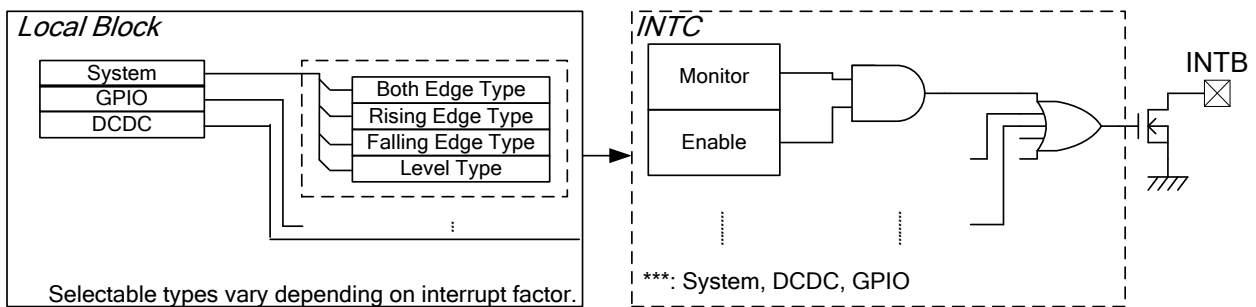
This PMU has an interrupt controller.

CPU can read all the permitted interrupt request flags coming from different functional blocks. When an interrupt occurs, CPU is informed by asserting INTB pin. CPU can identify block and factor which output interrupt by reading Monitor register of INTC and Local Block.

Monitor register is read-only. OR gate signal of each permitted interrupt request flag will be output from INTB pin.

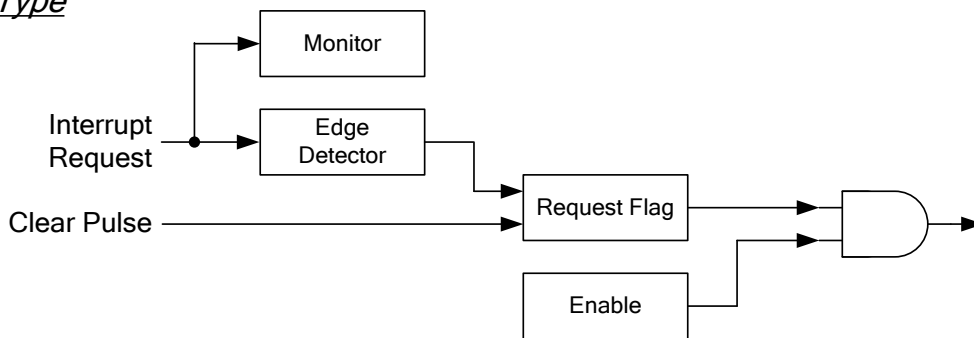
CPU can figure out the current state of this PMU by reading Monitor register at power-on. To enable interrupt output through INTB pin, it is necessary to write "1" in Enable register.

### 12.1 Interrupt Controller Block Diagram



#### Local Block

##### Edge Type



##### Level Type

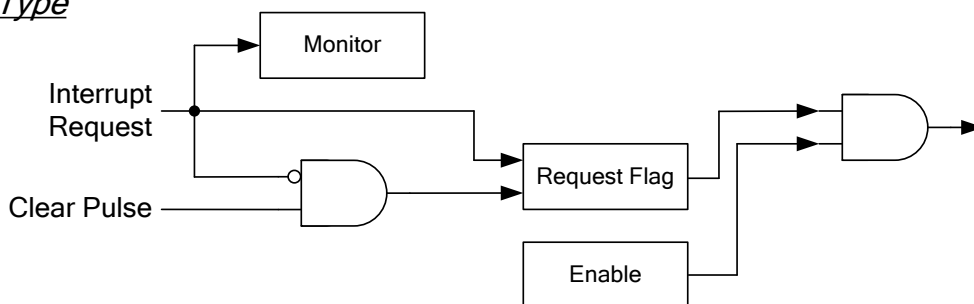


Fig 12-1 INTC Block Diagram

# 13. Registers

## 13.1 Registers Map

RSTB: Transition to PWROFF state or Shutdown factor detection

ERSTB: UVLO detection

Note\*1: Do not set "1" to - bits. Do not write "1" or "0" to undefined registers.

Note\*2: The default value of green hatch registers are set by OTP.

Note\*3: The default value of yellow hatch registers are set by OTP and initial value of the other register.

Block	Address	Symbol Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default	Reset	
SYSTEM	00	LSIVER	R	LSIVER[7:0]								01h	---	
	01	OTPVER	R	OTPVER[7:0]								by OTP	---	
	02	IODAC	R/W	IODAC[5:0]								by OTP	RSTB	
	03	VINDAC	R/W	VNRRESET	---	---	VINHYS	---	VINDAC[2:0]			by OTP	ERSTB(VNRRESET), ERSTB(RSTB(Other))	
	04	---	R/W	---	---	---	---	---	---	---	---	00h	RSTB	
	05	OUT32KEN	R/W	---	---	---	OUT32KEN3	OUT32KEN2	OUT32KEN1	OUT32KEN0	---	by OTP	RSTB	
I2C	06	CPUCNT	R/W	---	---	---	---	---	---	INCB	POWERI2C	00h	RSTB	
Power Control	07	PSWR	R/W	RRESET	PSWR[6:0]								00h	ERSTB
	08	---	R	---	---	---	---	---	---	---	---	by OTP	---	
	09	PONHIS	R	---	---	---	---	ON_EXTIN_PON	---	REPWR_PON	PWRON_PON	00h	ERSTB	
	0A	POFFHIS	R	N_OE_POFF	DCLIM_POFF	WDG_POFF	CPU_POFF	IODET_POFF	VINDET_POFF	TSHUT_POFF	PWRON_POFF	00h	ERSTB	
	0B	WATCHDOG	R/W	---	---	---	---	WDOG_SLPEN	WDOGEN	WDOGTIM[1:0]		03h	RSTB	
	0C	WATCHDOGCNT	R	WATCHDOGCNT[7:0]								---	RSTB	
	0D	PWRFUNC	R/W	---	---	SLP_TO_OFFSEQ	---	---	---	OFFSEQ_SEL	---	00h	RSTB	
	0E	SLPCNT	W	---	---	---	SLPEXIT	SLPENT	---	---	SWPWRON	00h	RSTB	
	0F	REPCNT	R/W	---	---	OFF_RESETQ[1:0]	---	---	---	REPWRTIM[1:0]	REPWRON	00h	RSTB	
	10	PWRONTIMSET	R/W	DIS_OFF_PWRON_TIM	OFF_PRESS_PWRON[2:0]			OFF_JUDGE_PWRON	ON_PRESS_PWRON[2:0]			by OTP	RSTB	
	11	NOETIMSETCNT	R/W	---	---	---	---	DIS_OFF_NOE_TIM	OFF_JUDGE_NOE	OFF_PRESS_NOE[1:0]		05h	RSTB	
	12	PWRIREN	R/W	---	EN_WDOG	EN_NOE_OFF	EN_PWRON_OFF	EN_OVTEMP	EN_PRVINDT	EN_EXTIN	EN_PWRON	00h	RSTB	
	13	PWRIRQ	R/W	---	IR_WDOG	IR_NOE_OFF	IR_PWRON_OFF	IR_OVTEMP	IR_PRVINDT	IR_EXTIN	IR_PWRON	---	RSTB	
	14	PWRMON	R	---	---	---	---	MON_OVTEMP	MON_PRVINDT	MON_EXTIN	MON_PWRON	---	RSTB	
	15	PWRIRSEL	R/W	---	---	---	---	SEL_OVTEMP	SEL_PRVINDT	SEL_EXTIN	SEL_PWRON	0Fh	RSTB	
	16	DC1_SLOT	R/W	DC10NSLOT[3:0]				DC1SLPSLOT[3:0]				by OTP	RSTB	
	17	DC2_SLOT	R/W	DC20NSLOT[3:0]				DC2SLPSLOT[3:0]				by OTP	RSTB	
	18	DC3_SLOT	R/W	DC30NSLOT[3:0]				DC3SLPSLOT[3:0]				by OTP	RSTB	
	19	DC4_SLOT	R/W	DC40NSLOT[3:0]				DC4SLPSLOT[3:0]				by OTP	RSTB	
	1A	---	---	---	---	---	---	---	---	---	---	00h	---	
	1B	LDO1_SLOT	R/W	LDO10NSLOT[3:0]				LDO1SLPSLOT[3:0]				by OTP	RSTB	
	1C	LDO2_SLOT	R/W	LDO20NSLOT[3:0]				LDO2SLPSLOT[3:0]				by OTP	RSTB	
	1D	LDO3_SLOT	R/W	LDO30NSLOT[3:0]				LDO3SLPSLOT[3:0]				by OTP	RSTB	
	1E	LDO4_SLOT	R/W	LDO40NSLOT[3:0]				LDO4SLPSLOT[3:0]				by OTP	RSTB	
	1F	LDO5_SLOT	R/W	LDO50NSLOT[3:0]				LDO5SLPSLOT[3:0]				by OTP	RSTB	
	20	---	---	---	---	---	---	---	---	---	---	00h	---	
	21	---	---	---	---	---	---	---	---	---	---	00h	---	
	22	---	---	---	---	---	---	---	---	---	---	00h	---	
	23	---	---	---	---	---	---	---	---	---	---	00h	---	
	24	---	---	---	---	---	---	---	---	---	---	00h	---	
	25	PSO0_SLOT	R/W	PSO00NSLOT[3:0]				PSO0SLPSLOT[3:0]				by OTP	RSTB	
	26	PSO1_SLOT	R/W	PSO10NSLOT[3:0]				PSO1SLPSLOT[3:0]				by OTP	RSTB	
27	PSO2_SLOT	R/W	PSO20NSLOT[3:0]				PSO2SLPSLOT[3:0]				by OTP	RSTB		
28	PSO3_SLOT	R/W	PSO30NSLOT[3:0]				PSO3SLPSLOT[3:0]				by OTP	RSTB		
29	---	---	---	---	---	---	---	---	---	---	00h	---		
2A	LDORTC1_SLOT	R/W	LDORTC10NSLOT[3:0]				LDORTC1SLPSLOT[3:0]				by OTP	RSTB		
2B	---	R/W	---	---	---	---	---	---	---	---	00h	---		

**POWER MANAGEMENT SYSTEM DEVICE**

Block	Address	Symbol Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default	Reset		
DCDC	2C	DC1CTL	R/W	DC1MODE_SLP[1:0]		DC1MODE[1:0]				DC1DIS	DC1EN	by other bit or OTP	RSTB, ERSTB(only DC1DIS)		
	2D	DC1CTL2	R/W	reserved		DC1SR[1:0]			DC1LIM[1:0]		DC1LIMSDEN	by other bit or OTP	RSTB		
	2E	DC2CTL	R/W	DC2MODE_SLP[1:0]		DC2MODE[1:0]				DC2DIS	DC2EN	by other bit or OTP	RSTB, ERSTB(only DC2DIS)		
	2F	DC2CTL2	R/W	reserved		DC2SR[1:0]			DC2LIM[1:0]		DC2LIMSDEN	by other bit or OTP	RSTB		
	30	DC3CTL	R/W	DC3MODE_SLP[1:0]		DC3MODE[1:0]				DC3DIS	DC3EN	by other bit or OTP	RSTB, ERSTB(only DC3DIS)		
	31	DC3CTL2	R/W	reserved		DC3SR[1:0]			DC3LIM[1:0]		DC3LIMSDEN	by other bit or OTP	RSTB		
	32	DC4CTL	R/W	DC4MODE_SLP[1:0]		DC4MODE[1:0]				DC4DIS	DC4EN	by other bit or OTP	RSTB, ERSTB(only DC4DIS)		
	33	DC4CTL2	R/W	reserved		DC4SR[1:0]			DC4LIM[1:0]		DC4LIMSDEN	by other bit or OTP	RSTB		
	34	---	---	---	---	---	---	---	---	---	---	---	00h	---	
	35	---	---	---	---	---	---	---	---	---	---	---	00h	---	
	36	DC1DAC	R/W					DC1DAC[7:0]					by OTP	RSTB	
	37	DC2DAC	R/W					DC2DAC[7:0]					by OTP	RSTB	
	38	DC3DAC	R/W					DC3DAC[7:0]					by OTP	RSTB	
	39	DC4DAC	R/W					DC4DAC[7:0]					by OTP	RSTB	
	3A	---	---	---	---	---	---	---	---	---	---	---	00h	---	
	3B	DC1DAC_SLP	R/W					DC1DAC_SLP[7:0]					by other bit or OTP	RSTB	
	3C	DC2DAC_SLP	R/W					DC2DAC_SLP[7:0]					by other bit or OTP	RSTB	
	3D	DC3DAC_SLP	R/W					DC3DAC_SLP[7:0]					by other bit or OTP	RSTB	
	3E	DC4DAC_SLP	R/W					DC4DAC_SLP[7:0]					by other bit or OTP	RSTB	
	3F	---	---	---	---	---	---	---	---	---	---	---	00h	---	
	40	DCIREN	R/W					EN_DC4LIM	EN_DC3LIM	EN_DC2LIM	EN_DC1LIM		00h	RSTB	
	41	DCIRQ	R/W					IR_DC4LIM	IR_DC3LIM	IR_DC2LIM	IR_DC1LIM		00h	RSTB	
	42	DCIRMON	R					MON_DC4LIM	MON_DC3LIM	MON_DC2LIM	MON_DC1LIM		*	RSTB	
	43	---	---	---	---	---	---	---	---	---	---	---	00h	---	
	LDO	44	LDOEN1	R/W					LDO5EN	LDO4EN	LDO3EN	LDO2EN	LDO1EN	by other bit or OTP	RSTB
		45	LDOEN2	R/W			LDORTC2EN	LDORTC1EN						by OTP	RSTB
		46	LDDIS1	R/W				LDO5DIS	LDO4DIS	LDO3DIS	LDO2DIS	LDO1DIS		1Fh	ERSTB
		47	---	---	---	---	---	---	---	---	---	---	---	00h	---
		48	---	---	---	---	---	---	---	---	---	---	---	00h	---
		49	---	---	---	---	---	---	---	---	---	---	---	00h	---
		4A	---	---	---	---	---	---	---	---	---	---	---	00h	---
		4B	---	---	---	---	---	---	---	---	---	---	---	00h	---
		4C	LDO1DAC	R/W					LDO1DAC[6:0]					by OTP	RSTB
		4D	LDO2DAC	R/W					LDO2DAC[6:0]					by OTP	RSTB
		4E	LDO3DAC	R/W					LDO3DAC[6:0]					by OTP	RSTB
		4F	LDO4DAC	R/W					LDO4DAC[6:0]					by OTP	RSTB
		50	LDO5DAC	R/W					LDO5DAC[6:0]					by OTP	RSTB
		51	---	---	---	---	---	---	---	---	---	---	---	00h	---
		52	---	---	---	---	---	---	---	---	---	---	---	00h	---
53		---	---	---	---	---	---	---	---	---	---	---	00h	---	
54		---	---	---	---	---	---	---	---	---	---	---	00h	---	
55		---	---	---	---	---	---	---	---	---	---	---	00h	---	
56		LDORTC1DAC	R/W					LDORTC1DAC[6:0]					by OTP	RSTB	
57		LDORTC2DAC	R/W					LDORTC2DAC[6:0]					by OTP	RSTB	
58		LDO1DAC_SLP	R/W					LDO1DAC_SLP[6:0]					by OTP	RSTB	
59		LDO2DAC_SLP	R/W					LDO2DAC_SLP[6:0]					by OTP	RSTB	
5A		LDO3DAC_SLP	R/W					LDO3DAC_SLP[6:0]					by OTP	RSTB	
5B		LDO4DAC_SLP	R/W					LDO4DAC_SLP[6:0]					by OTP	RSTB	
5C		LDO5DAC_SLP	R/W					LDO5DAC_SLP[6:0]					by OTP	RSTB	
5D		---	---	---	---	---	---	---	---	---	---	---	00h	---	
5E		---	---	---	---	---	---	---	---	---	---	---	00h	---	
5F	---	---	---	---	---	---	---	---	---	---	---	00h	---		
60-9F	---	---	---	---	---	---	---	---	---	---	---	00h	---		
GPIO	90	IOSEL	R/W					IO03	IO02	IO01	IO00		00h	RSTB	
	91	IOOUT	R/W					IOOUT03	IOOUT02	IOOUT01	IOOUT00		00h	RSTB	
	92	GPEDGE1	R/W	EDGE03[1:0]		EDGE02[1:0]		EDGE01[1:0]		EDGE00[1:0]			00h	RSTB	
	93	---	---	---	---	---	---	---	---	---	---	---	00h	---	
	94	EN_GPIR	R/W					EN_GP03IR	EN_GP02IR	EN_GP01IR	EN_GP00IR		00h	RSTB	
	95	IR_GPR	R/W					IR_GP03R	IR_GP02R	IR_GP01R	IR_GP00R		00h	RSTB	
	96	IR_GPF	R/W					IR_GP03F	IR_GP02F	IR_GP01F	IR_GP00F		00h	RSTB	
	97	MON_IOIN	R					MON_IOIN03	MON_IOIN02	MON_IOIN01	MON_IOIN00		*	---	
	98	GPLED_FUNC	R/W		GP1_LEDMODE	GP1_LEDFUNC[1:0]		GP0_LEDMODE	GP0_LEDFUNC[1:0]				by OTP	RSTB	
	99	---	R/W										00h	RSTB	
9A	---	R/W										00h	RSTB		
9B	---	---	---	---	---	---	---	---	---	---	---	00h	---		
INTC	9C	INTPOL	R/W								INTPOL	00h	RSTB		
	9D	INTEN	R/W				GPIO_IREN			DCDC_IREN	SYSTEM_IREN	00h	RSTB		
SYSTEM OPTION	9E	INTMON	R			WDG_IRM	GPIO_IRM			DCDC_IRM	SYSTEM_IRM	*	---		
	9F	---	---	---	---	---	---	---	---	---	---	00h	---		
SYSTEM OPTION	B0	PREVINDAC	R/W						PREVINDACH	PREVINDAC[1:0]		by OTP	ERSTB		
	B1	---	---	---	---	---	---	---	---	---	---	00h	---		
	B2	---	---	---	---	---	---	---	---	---	---	00h	---		
	B3	---	---	---	---	---	---	---	---	---	---	00h	---		
	B4	---	---	---	---	---	---	---	---	---	---	00h	---		
	B5	---	---	---	---	---	---	---	---	---	---	00h	---		
	B6	---	---	---	---	---	---	---	---	---	---	00h	---		
	B7	---	---	---	---	---	---	---	---	---	---	00h	---		
	B8	---	---	---	---	---	---	---	---	---	---	00h	---		
	B9	---	---	---	---	---	---	---	---	---	---	00h	---		
	BA	---	---	---	---	---	---	---	---	---	---	00h	---		
	BB	---	---	---	---	---	---	---	---	---	---	00h	---		
	BC	OVTEMP	R/W								OVTEMP[1:0]	by OTP	ERSTB		
BD	---	---	---	---	---	---	---	---	---	---	00h	---			
BE	---	---	---	---	---	---	---	---	---	---	00h	---			
BF	---	---	---	---	---	---	---	---	---	---	00h	---			
C0-FF	---	---	---	---	---	---	---	---	---	---	---	00h	---		

## 13.2 SYSTEM

### 13.2.1 LSIVER: LSI Version Register (Address 00h)

Bit	7	6	5	4	3	2	1	0
Symbol	LSIVER							
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	1

Bit 7 ~ Bit 0: LSIVER

This register indicates LSI version.

### 13.2.2 OTPVER: OTP Version Register (Address 01h)

Bit	7	6	5	4	3	2	1	0
Symbol	OTPVER							
R/W	R	R	R	R	R	R	R	R
Default	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP

Bit 6 ~ Bit 0: OTPVER

This register indicates OTP version.

### 13.2.3 IODAC: IODET Detection Voltage Setting Register (Address 02h)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	IODAC[5:0]					
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP

Bit 5 ~ Bit 0: IODAC bit

Setting the detection voltage to IODET

#### The detection voltage table of IODET (Step = 50mV)

IODAC[5:0]	Detection voltage [V]
000000 (00h)	Prohibit
~	Prohibit
001100(0Ch)	1.40(↓)
~	~
010000(10h)	1.60(↓)
~	~
101000(28h)	2.80(↓)
~	~
110000(30h)	3.20(↓)
~	Prohibit
111111(3Fh)	Prohibit

The default voltage can be set up the following values by OTP.

1.4V, 1.6V, 1.85V, 2.1V, 2.35V, 2.6V, 2.85V, 3.1V

**13.2.4 VINDAC: VINDET Detection Voltage Setting Register (Address 03h)**

Bit	7	6	5	4	3	2	1	0
Symbol	VINR RESET	-	-	VINHYS	-	VINDAC[2:0]		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	By OTP	0	0	By OTP	0	By OTP	By OTP	By OTP

**Bit 7: VINRRESET bit**

Select the reset condition for VINHYS bit and VINDAC bit.

“0”: RSTB

“1”: ERSTB

**Bit 4: VINHYS bit**

Setting the hysteresis voltage to VINDET

“1”: 200mV

“0”: 500mV

**Bit 2 ~ Bit 0: VINDAC bit**

Setting the detection voltage to VINDET

**The detection voltage table of VINDET (Step = 100mV)**

VINDAC[2:0]	Detection voltage [V]
000 (0h)	2.6(↓)
001 (1h)	2.7(↓)
010 (2h)	2.8(↓)
011 (3h)	2.9(↓)
100 (4h)	3.0(↓)
101 (5h)	3.1(↓)
110 (6h)	3.2(↓)
111 (7h)	3.3(↓)

The default voltage can be set up all of the above register values by OTP.

**13.2.5 OUT32KEN: C32KOUT Control Register (Address 05h)**

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	OUT32KEN3	OUT32KEN2	OUT32KEN1	OUT32KEN0	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	By OTP	By OTP	By OTP	By OTP	0

**Bit 4: OUT32KEN3 bit**

Select the clock output control bit from GPIO3(C32KOUT3) pin. (OTP Option)

“0”: Disable

“1”: Enable

**Bit 3: OUT32KEN2 bit**

Select the clock output control bit from GPIO2(C32KOUT2) pin. (OTP Option)

“0”: Disable

“1”: Enable

**Bit 2: OUT32KEN1 bit**

Select the clock output control bit from GPIO1(C32KOUT1) pin. (OTP Option)

“0”: Disable

“1”: Enable

**Bit 1: OUT32KEN0 bit**

Select the clock output control bit from GPIO0(C32KOUT0) pin. (OTP Option)

“0”: Disable

“1”: Enable

### 13.3 I2C

#### 13.3.1 CPUCNT: CPUIF Control Register (Address 06h)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	INCB	POWER I2C
R/W	R	R	R	R	R	R	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit 1: INCB bit

Setting I2C R/W format (Automatic increment in address pointers)

“0”: Enable (Automatic increment)

“1”: Disable

Bit 0: POWERI2C bit

Setting power I2C format

“0”: Disable

“1”: Enable

## 13.4 Power Control

### 13.4.1 PSWR: Power Supply Watch Register (Address 07h)

Bit	7	6	5	4	3	2	1	0
Symbol	RRESET	PSWR						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Note\*: This register is reset by UVLO.

#### Bit 7 RRESET bit

Select the reset condition of registers which is reset by RSTB during POWEROFF state.

By setting this bit to "1", all registers are not reset. Writing to this bit is prohibited in Parts Mode.

0: Reset

1: Not reset. (The reset condition is same as ERSTB.)

#### Bit 6 ~ Bit 0: PSWR bit

This register is reset to "00h" by UVLO. After this PMU powers on, CPU writes some unique value except for "00h".

Then CPU can recognize whether the register data of the power supply is maintained.



**13.4.2 PONHIS: Power-on History Register (Address 09h)**

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	ON_EXTIN PON	-	REPWR PON	PWRON PON
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	Undefined	0	Undefined	Undefined

CPU can recognize the power-on factor by reading this register.  
The power-on factor is set when the power-on sequence starts.

Bit 3 ON\_EXTINPON bit

Indicates that the power-on has occurred by detecting ON\_EXTIN asserts

Bit 1 REPWRPON bit

Indicates that the repower-on has occurred by the power-off with setting REPWRON bit to 1  
Same as repower-on by HRESET.

Bit 0 PWRONPON bit

Indicates that the power-on has occurred by detecting PWRON asserts

**13.4.3 POFFHIS: Power-off History Register (Address 0Ah)**

Bit	7	6	5	4	3	2	1	0
Symbol	N_OE POFF	DCLIM POFF	WDG POFF	CPU POFF	IODET POFF	VINDET POFF	TSHUT POFF	PWRON POFF
R/W	R	R	R	R	R	R	R	R
Default	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

CPU can recognize the power-off factor by reading this register.

The power-off factors is set when the power-off sequence starts or the forcibly powers off.

Bit 7 N\_OEPOFF bit

Indicates that the power-off has occurred by N\_OE asserts or HRESET asserts.

Bit 6 DCLIMPOFF bit

Indicates that the power-off has occurred detecting the overcurrent of DCDC1-4 by the current limit circuit.

Bit 5 WDGPOFF bit

Indicates that the power-off has occurred by the watchdog function

Bit 4 CPUPOFF bit

Indicates that the power-off has occurred by follows.

- SWPWROFF bit setting.
- PSHOLD(GPIO\*) is low.
- PSHOLD(GPIO\*) is timeout.

Bit 3 IODETPOFF bit

Indicates that the power-off has occurred by IODET asserts.

Bit 2 VINDETPOFF bit

Indicates that the forced power-off has occurred by detecting the low power condition in VINDET circuit

Bit 1 TSHUTPOFF bit

Indicates that the forced power-off has occurred by detecting an abnormal temperature in the thermal shutdown circuit

Bit 0 PWRONPOFF bit

Indicates that the power-off has occurred by PWRON assert.

**13.4.4 WATCHDOG: Watchdog Timer Setting Register (Address 0Bh)**

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	WDOG SLPEN	WDOG EN	WDOG TIM	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	1	1

The count value of watchdog timer is cleared by accessing (R/W) to this register.

**Bit 3: WDOGSLPEN bit**

Valid/Invalid the watchdog timer during SLEEP state

0: Invalid (Stop the countdown)

1: Valid (Kept the countdown and generated the interrupt after expiring the timer)

**Bit 2: WDOGEN bit**

Enable/Disable the power-off function by the watchdog timer.

Writing to this bit is prohibited in Parts Mode.

0: Disable

1: Enable

This bit can restrict the writing by OTP. It is whether it is possible to rewrite.

**Bit 1 ~ Bit 0: WDOGTIM bit**

Set the access monitoring time from CPU by watchdog timer.

WDOGTIM[1:0]	Timeout
00	1 sec
01	8 sec
10	32 sec
11	128 sec (default)

**13.4.5 WATCHDOGCNT: Watchdog Timer Count Register (Address 0Ch)**

Bit	7	6	5	4	3	2	1	0
Symbol	WATCHDOGCNT							
R/W	R	R	R	R	R	R	R	R
Default	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

**Bit 7 ~ Bit 0: WATCHDOGCNT bit**

Read the count value of watchdog timer

The read value of this register is determined by the setting of WDOGTIM bits as indicated below.

WDOGTIM[1:0]	WATCHDOGCNT Read value
00	25 msec / 1bit
01	50 msec / 1bit
10	200 msec / 1bit
11	800 msec / 1bit

Example: If the value = 10h (16d) and WDOGTIM bits = 11b,

the power-off sequence starts by watchdog after the (16 \* 800 msec + 1 sec).

Note\*: In order to prevent malfunction of reading operation, read this register twice or more continuously, and if both count value data match, they are determined as the value is read accurately.

**13.4.6 PWRFUNC: Power Control Function Register (Address 0Dh)**

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	SLP_TO_ OFFSEQ	-	-	-	OFFSEQ_ SEL	-
R/W	R	R	R/W	R	R	R	R/W	R
Default	0	0	0	0	0	0	0	0

**Bit 5: SLP\_TO\_OFFSEQ bit**

This PMU changes to POWEROFF SEQUENCE state by detecting PWRON longpress during SLEEP state. Writing to this bit is prohibited in Parts Mode .

0: Invalid

1: Valid

**Bit 1: OFFSEQ\_SEL bit**

Power-off sequence timing select bit. Writing to this bit is prohibited in Parts Mode.

0: By ONSLOT registers.

1: At Slot\_15.

**13.4.7 SLPCNT: Sleep Control Register (Address 0Eh)**

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	SLPEXIT	SLPENT	-	-	-	SWPWR OFF
R/W	W	W	W	W	W	W	W	W
Default	0	0	0	0	0	0	0	0

**Bit 5: SLPEXIT bit**

During SLEEP state, this PMU changes to SLEEP EXIT SEQUENCE state by writing "1" in this bit. Writing to this bit is prohibited in Parts Mode.

**Bit 4: SLPENT bit**

During POWERON state, this PMU changes to SLEEP ENTRY SEQUENCE state by writing "1" in this bit. Writing to this bit is prohibited in Parts Mode.

**Bit 0: SWPWROFF bit**

During POWERON state, this PMU changes to POWEROFF SEQUENCE state by writing "1" in this bit.

**13.4.8 REPCNT: Repower-on Control Register (Address 0Fh)**

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	OFF_RESETO		-	REPWRTIM		RE PWRON
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit 5 ~ Bit 4: OFF\_RESETO bit

Setting time asserted RESETO pin. Writing to this bit is prohibited in Parts Mode.

OFF_RESETO[1:0]	Time
00	0ms (default)
01	2ms
10	8ms
11	16ms

Bit 2 ~ Bit 1: REPWRTIM bit

Setting time between the power-off sequence finishes and the power-on sequence starts.

REPWRTIM[1:0]	Time
00	10 ms (default)
01	100 ms
10	500 ms
11	1000 ms

Bit 0: REPWRON bit

By setting this bit to "1", this PMU powers on after the power-off without the power-on factors. Writing to this bit is prohibited in Parts Mode.

0: Disable

1: Enable

**13.4.9 PWRONTIMSET: PWRON Timer Setting Register (Address 10h)**

Bit	7	6	5	4	3	2	1	0
Symbol	DIS_OFF_ PWRON_TIM	OFF_PRESS_PWRON			OFF_JUDGE_ PWRON	ON_PRESS_PWRON		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	1	1	1	by OTP	by OTP	by OTP

**Bit 7: DIS\_OFF\_PWRON\_TIM bit**

Clear and initializing the PWRON off\_press timer value and over-flow flag.

- 0: Enable
- 1: Disable

**Bit 6 ~ Bit 4: OFF\_PRESS\_PWRON bit**

Setting of PWRON off\_press timer.

Writing to this bit is prohibited in Parts Mode.

OFF_PRESS_PWRON[2:0]	Timeout
000	0 sec
001	1 sec
010	2 sec
011	4 sec (default)
100	6 sec
101	8 sec
110	10 sec
111	12 sec

**Bit 3: OFF\_JUDGE\_PWRON bit**

Setting of PWRON judge timer.

Writing to this bit is prohibited in Parts Mode.

OFF_JUDGE_PWRON	Timeout
0	0 sec
1	1 sec (default)

**Bit 2 ~ Bit 0: ON\_PRESS\_PWRON bit**

Setting of PWRON on\_press timer.

Writing to this bit is prohibited in Parts Mode.

ON_PRESS_PWRON[2:0]	Timeout
000	0 ms
001	20 ms
010	128 ms
011	1 sec
100	2 sec
101	3 sec
110	Prohibit
111	Prohibit

The default time can be set up the following values by OTP.

0ms, 20ms, 1s, 3s

**13.4.10 NOETIMSET: N\_OE Timer Setting Register (Address 11h)**

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	DIS_OFF_ NOE_TIM	OFF_JUDGE _NOE	OFF_PRESS_NOE	
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	1	0	1

**Bit 3: DIS\_OFF\_NOE\_TIM bit**

Clear and initializing the N\_OE off\_press timer value and over-flow flag.

0: Enable

1: Disable

**Bit 2: OFF\_JUDGE\_NOE bit**

Setting of N\_OE judge timer

Writing to this bit is prohibited in Parts Mode.

Note\*: It is possible to write this bit by writing "1" in DIS\_OFF\_NOE\_TIM bit

OFF_JUDGE_NOE	Timeout
0	0 sec
1	1 sec (default)

**Bit 1 ~ Bit 0: OFF\_PRESS\_NOE bit**

Setting of N\_OE off\_press timer.

Writing to this bit is prohibited in Parts Mode.

Note\*: It is possible to write this bit by writing "1" in DIS\_OFF\_NOE\_TIM bit

OFF_PRESS_NOE[1:0]	Timeout
00	128 ms
01	1 sec (default)
10	2 sec
11	3 sec

**13.4.11 PWIREN: Power Control Interrupt Factor Output Enable Register (Address 12h)**

Bit	7	6	5	4	3	2	1	0
Symbol	-	EN_WDOG	EN_NOE_OFF	EN_PWRO_N_OFF	EN_OVTEMP	EN_PRVINDT	EN_EXTIN	EN_PWRON
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

**Bit 6: EN\_WDOG bit**

Enable outputs of the interrupt request in the watchdog timer.

“0”: Disable

“1”: Enable

Note\*: Writing to this bit is prohibited in Parts Mode.

**Bit 5: EN\_NOE\_OFF bit**

Enable outputs of the interrupt request in the NOE timer.

“0”: Disable

“1”: Enable

Note\*: Power-off by long-press doesn't depend on EN\_NOE\_OFF bit setting.

**Bit 4: EN\_PWRON\_OFF bit**

Enable outputs of the interrupt request in the PWRON timer.

“0”: Disable

“1”: Enable

Note\*: Power-off by long-press doesn't depend on EN\_PWRON\_OFF bit setting.

**Bit 3: EN\_OVTEMP bit**

Enable outputs of the interrupt request when detecting overheat temperature.

“0”: Disable

“1”: Enable

**Bit 2: EN\_PRVINDT bit**

Enable output of the interrupt request when the power supply to VSYS below the VINDET detection voltage.

“0”: Disable

“1”: Enable

**Bit 1: EN\_EXTIN bit**

Enable outputs of the interrupt request when ON\_EXTIN pin input signal changes.

“0”: Disable

“1”: Enable

**Bit 0: EN\_PWRON bit**

Enable outputs of the interrupt request when PWRON pin input signal changes.

“0”: Disable

“1”: Enable



**13.4.12 PWRIRQ: Power Control Interrupt Factor Register (Address 13h)**

Bit	7	6	5	4	3	2	1	0
Symbol	-	IR_ WDOG	IR_ NOE_OFF	IR_PWRON _OFF	IR_ OVTEMP	IR_ PRVINDT	IR_ EXTIN	IR_ PWRON
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Note\*: Each bit can be cleared by writing “0”, but cannot be set by writing “1”.

Bit 6: IR\_ WDOG bit

Store the interrupt request factor in the watchdog timer.

“0”: None

“1”: Requested

Bit 5: IR\_ NOE\_OFF bit

Store the interrupt request factor in the NOE timer.

“0”: None

“1”: Requested

Bit 4: IR\_ PWRON\_OFF bit

Store the interrupt request factor in the PWRON timer.

“0”: None

“1”: Requested

Bit 3: IR\_ OVTEMP bit

Store the interrupt request factor in the detecting overheat temperature.

“0”: None

“1”: Requested

Bit 2: IR\_ PRVINDT bit

Store the interrupt request factor in the power supply to VSYS below the VINDET detection voltage.

“0”: None

“1”: Requested

Bit 1: IR\_ EXTIN bit

Store the interrupt request factor when ON\_EXTIN pin input signal changes.

“0”: None

“1”: Requested

Bit 0: IR\_ PWRON bit

Store the interrupt request factor when PWRON pin input signal changes.

“0”: None

“1”: Requested

**13.4.13 PWRMON: Power Control Interrupt Factor Monitoring Register (Address 14h)**

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	MON_ OVTEMP	MON_ PRVINDT	MON_ EXTIN	MON_ PWRON
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	Undefined	Undefined	Undefined	Undefined

Bit 3: MON\_ OVTEMP bit

Monitor the detection state of overheat circuit.

“0”: Normal temperature

“1”: Abnormal temperature

Bit 2: MON\_ PRVINDT bit

Monitor PREVINDET detection signal.

“0”: Over PREVINDET release voltage

“1”: Under PREVINDET detection voltage

Bit 1: MON\_ EXTIN bit

Monitor ON\_EXTIN signal.

“0”: ON\_EXTIN deassert

“1”: ON\_EXTIN assert

Bit 0: MON\_ PWRON bit

Monitor PWRON signal.

“0”: PWRON is released

“1”: PWRON is held down

**13.4.14 PWRIRSEL: Power Control Interrupt Type Setting Register (Address 15h)**

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	SEL_ OVTEMP	SEL_ PRVINDT	SEL_ EXTIN	SEL_ PWRON
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	1	1	1	1

For the details of interrupt, refer to the chapter of the interrupt controller (INTC).

Bit 3: SEL\_ OVTEMP bit

Select the type of the interrupt by the overheat temperature detection.

Bit 2: SEL\_ PRVINDT bit

Select the type of the interrupt by Pre-VINDET detection signal.

Bit 1: SEL\_ EXTIN bit

Select the type of the interrupt by ON\_EXTIN input signal changes.

Bit 0: SEL\_ PWRON bit

Select the type of the interrupt by PWRON input signal changes.

SEL_ ***	Type
0	Level
1	Both-edge

**13.4.15 \*\*\*\_SLOT: Power-On/Off And Sleep Entry/Exit Sequence Setting Register (Address 16h ~ 2Ah)**

(\*\*\*=DC1-4, LDO1-5, LDORTC1, PSO0-3)

**DC1\_SLOT (16h)**

Bit	7	6	5	4	3	2	1	0
Symbol	DC1ONSLLOT				DC1SLPSLOT			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	by OTP	by OTP	by OTP	by OTP	1	1	1	1

**DC2\_SLOT (17h)**

Bit	7	6	5	4	3	2	1	0
Symbol	DC2ONSLLOT				DC2SLPSLOT			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	by OTP	by OTP	by OTP	by OTP	1	1	1	1

**DC3\_SLOT (18h)**

Bit	7	6	5	4	3	2	1	0
Symbol	DC3ONSLLOT				DC3SLPSLOT			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	by OTP	by OTP	by OTP	by OTP	1	1	1	1

**DC4\_SLOT (19h)**

Bit	7	6	5	4	3	2	1	0
Symbol	DC4ONSLLOT				DC4SLPSLOT			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	by OTP	by OTP	by OTP	by OTP	1	1	1	1

**LDO1\_SLOT (1Bh)**

Bit	7	6	5	4	3	2	1	0
Symbol	LDO1ONSLLOT				LDO1SLPSLOT			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	by OTP	by OTP	by OTP	by OTP	1	1	1	1

**LDO2\_SLOT (1Ch)**

Bit	7	6	5	4	3	2	1	0
Symbol	LDO2ONSLLOT				LDO2SLPSLOT			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	by OTP	by OTP	by OTP	by OTP	1	1	1	1

**LDO3\_SLOT (1Dh)**

Bit	7	6	5	4	3	2	1	0
Symbol	LDO3ONSLLOT				LDO3SLPSLOT			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	by OTP	by OTP	by OTP	by OTP	1	1	1	1

**LDO4\_SLOT (1E)**

Bit	7	6	5	4	3	2	1	0
Symbol	LDO4ONSLLOT				LDO4SLPSLOT			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	by OTP	by OTP	by OTP	by OTP	1	1	1	1

**LDO5\_SLOT (1F)**

Bit	7	6	5	4	3	2	1	0
Symbol	LDO5ONSLLOT				LDO5SLPSLOT			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	by OTP	by OTP	by OTP	by OTP	1	1	1	1

PSO0\_SLOT (25h)

Bit	7	6	5	4	3	2	1	0
Symbol	PSO0ONSLOT				PSO0SLPSLOT			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	by OTP	by OTP	by OTP	by OTP	1	1	1	1

PSO1\_SLOT (26h)

Bit	7	6	5	4	3	2	1	0
Symbol	PSO1ONSLOT				PSO1SLPSLOT			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	by OTP	by OTP	by OTP	by OTP	1	1	1	1

PSO2\_SLOT (27h)

Bit	7	6	5	4	3	2	1	0
Symbol	PSO2ONSLOT				PSO2SLPSLOT			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	by OTP	by OTP	by OTP	by OTP	1	1	1	1

PSO3\_SLOT (28h)

Bit	7	6	5	4	3	2	1	0
Symbol	PSO3ONSLOT				PSO3SLPSLOT			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	by OTP	by OTP	by OTP	by OTP	1	1	1	1

LDORTC1\_SLOT (2Ah)

Bit	7	6	5	4	3	2	1	0
Symbol	LDORTC1ONSLOT				LDORTC1SLPSLOT			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	by OTP	by OTP	by OTP	by OTP	1	1	1	1

Bit 7 ~ Bit 4: **\*\*\*ONSLOT** bit (\*\*\*=DC1-4, LDO1-5, LDORTC1, PSO0-3)

Setting the on/off timing of power-on/off sequence

Bit 3 ~ Bit 0: **\*\*\*SLPSLOT** bit (\*\*\*=DC1-4, LDO1-5, LDORTC1, PSO0-3)

Setting the on/off timing of sleep entry/exit sequence

The following restrictions exist.

If the value of DC1-4/LDO1-5ONSLOT registers is Fh, the control of DCDCx/LDOxEXON pins are disabled in Parts Mode.

***SLOT[3:0]	Power-on/off sequence time slot number	Sleep entry/exit sequence time slot number
0000		Slot _0
0001		Slot _1
0010		Slot _2
0011		Slot _3
0100		Slot _4
~		~
1010		Slot _10
1011		Slot _11
1100		Slot _12
1101		Slot _13
1110		Slot _14
1111	Default Off	The state in POWERON state is maintained

## 13.5 DCDC

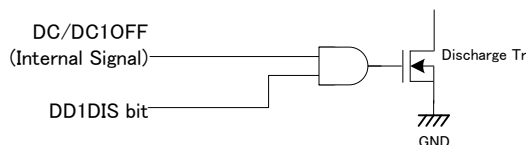
### 13.5.1 DC1CTL: DCDC1 Control Register (Address 2Ch)

Bit	7	6	5	4	3	2	1	0
Symbol	DC1MODE_SLP[1:0]	DC1MODE[1:0]			-	-	DC1DIS	DC1EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	1	By OTP

Bit 7 ~ 6: DC1MODE\_SLP[1 :0] bit  
 DCDC1 mode setting bit at the SLEEP state

Bit 5 ~ 4: DC1MODE[1 :0] bit  
 DCDC1 mode setting bit at the POWERON state  
 "00": Auto mode  
 "01": PWM mode  
 "10": PSM mode  
 "11": Auto mode

Bit 1: DC1DIS bit  
 DCDC1 discharge control bit  
 "0": Off  
 "1": On (This bit is invalid when DCDC1 state is on.)



Bit 0: DC1EN bit  
 DCDC1 enable bit  
 "0": Disable  
 "1": Enable

The initial value of this register depends on the initial value of DC1ONSLOT register and Mode setting. The initial value of DC1ONSLOT register and Mode setting are set by OTP.

·Normal Mode

DC1ONSLOT = Fh: DC1EN = 0b

DC1ONSLOT = 0h-Eh: DC1EN = 1b

·Parts Mode

DC1EN = 1b

**13.5.2 DC1CTL2: DCDC1 Control2 Register (Address 2Dh)**

Bit	7	6	5	4	3	2	1	0
Symbol	(reserved)		DC1SR[1:0]		-	DC1LIM[1:0]		DC1LIMSDEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	By OTP	By OTP	0	0	0	By OTP	By OTP	By OTP

Bit 7 ~ Bit 6: reserved bit

Note\*: This bits are reserved. Writing this bits are prohibited.

Bit 5 ~ Bit 4: DC1SR bit

DCDC1 ramp rate of output voltage setting bit

DC1SR[1:0]	Voltage Slope
00	14 mV / us (default)
01	7 mV / us
10	3.5 mV / us
11	Prohibited

Note\*: Writing this register is prohibited during the ramp control.

Bit 2 ~ Bit 1: DC1LIM bit

DCDC1 minimum current limit setting bit

DC1LIM[1:0]	Current limit
00	No Limit
01	3.2A
10	3.7A
11	4.0A

The default current can be set up all of the above register values by OTP.

Bit 0: DC1LIMSDEN bit

Enable shutdown function from the current limit detection of DCDC1.

The current limit detection is to continue exceeding limit current during 2ms.

“0”: Disable

“1”: Enable

The initial value of this register depends on Mode setting. Mode setting is set by OTP.

·Normal Mode

DC1LIMSDEN = 1b

·Parts Mode

DC1LIMSDEN = 0b

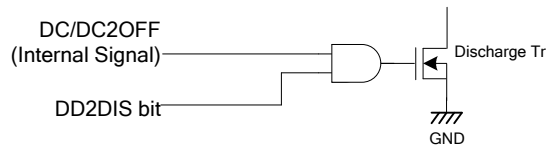
**13.5.3 DC2CTL: DCDC2 Control Register (Address 2Eh)**

Bit	7	6	5	4	3	2	1	0
Symbol	DC2MODE_SLP[1:0]		DC2MODE[1:0]		-	-	DC2DIS	DC2EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	1	By OTP

Bit 7 ~ 6: DC2MODE\_SLP[1 :0] bit  
 DCDC2 mode setting bit at the SLEEP state

Bit 5 ~ 4: DC2MODE[1 :0] bit  
 DCDC2 mode setting bit at the POWERON state  
 "00": Auto mode  
 "01": PWM mode  
 "10": PSM mode  
 "11": Auto mode

Bit 1: DC2DIS bit  
 DCDC2 discharge control bit  
 "0": Off  
 "1": On (This bit is invalid when DCDC2 state is on.)



Bit 0: DC2EN bit  
 DCDC2 enable bit  
 "0": Disable  
 "1": Enable

The initial value of this register depends on the initial value of DC2ONSLOT register and Mode setting. The initial value of DC2ONSLOT register and Mode setting are set by OTP.

- Normal Mode
  - DC2ONSLOT = Fh: DC2EN = 0b
  - DC2ONSLOT = 0h-Eh: DC2EN = 1b
- Parts Mode
  - DC2EN = 1b

**13.5.4 DC2CTL2: DCDC2 Control2 Register (Address 2Fh)**

Bit	7	6	5	4	3	2	1	0
Symbol	(reserved)		DC2SR[1:0]		-	DC2LIM[1:0]		DC2 LIMSDEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	By OTP	By OTP	0	0	0	By OTP	By OTP	By OTP

Bit 7 ~ Bit 6: reserved bit

Note\*: This bits are reserved. Writing this bits are prohibited.

Bit 5 ~ Bit 4: DC2SR bit

DCDC2 ramp rate of output voltage setting bit

DC2SR[1:0]	Voltage Slope
00	14 mV / us (default)
01	7 mV / us
10	3.5 mV / us
11	Prohibited

Note\*: Writing this register is prohibited during the ramp control.

Bit 2 ~ Bit 1: DC2LIM bit

DCDC2 minimum current limit setting bit

DC2LIM[1:0]	Current limit
00	No Limit
01	3.2A
10	3.7A
11	4.0A

The default current can be set up all of the above register values by OTP.

Bit 0: DC2LIMSDEN bit

Enable shutdown function from the current limit detection of DCDC2.

The current limit detection is to continue exceeding limit current during 2ms.

“0”: Disable

“1”: Enable

The initial value of this register depends on Mode setting. Mode setting is set by OTP.

· Normal Mode

DC2LIMSDEN = 1b

· Parts Mode

DC2LIMSDEN = 0b



**13.5.5 DC3CTL: DCDC3 Control Register (Address 30h)**

Bit	7	6	5	4	3	2	1	0
Symbol	DC3MODE_SLP[1:0]		DC3MODE[1:0]		-	-	DC3DIS	DC3EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	1	By OTP

Bit 7 ~ 6: DC3MODE\_SLP[1 :0] bit

DCDC3 mode setting bit at the SLEEP state

Bit 5 ~ 4: DC3MODE[1 :0] bit

DCDC3 mode setting bit at the POWERON state

“00”: Auto mode

“01”: PWM mode

“10”: PSM mode

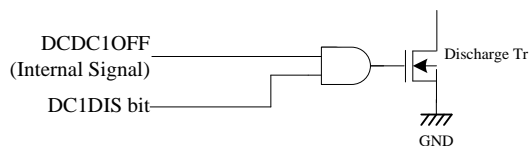
“11”: Auto mode

Bit 1: DC3DIS bit

DCDC3 discharge control bit

“0”: Off

“1”: On (This bit is invalid when DCDC3 state is on.)



Bit 0: DC3EN bit

DCDC3 enable bit

“0”: Disable

“1”: Enable

The initial value of this register depends on the initial value of DC3ONSLOT register and Mode setting. The initial value of DC3ONSLOT register and Mode setting are set by OTP.

·Normal Mode

DC3ONSLOT = Fh: DC3EN = 0b

DC3ONSLOT = 0h-Eh: DC3EN = 1b

·Parts Mode

DC3EN = 1b

**13.5.6 DC3CTL2: DCDC3 Control2 Register (Address 31h)**

Bit	7	6	5	4	3	2	1	0
Symbol	(reserved)		DC3SR[1:0]		-	DC3LIM[1:0]		DC3LIMSDEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	By OTP	By OTP	0	0	0	By OTP	By OTP	By OTP

Bit 7 ~ Bit 6: reserved bit

Note\*: This bits are reserved. Writing this bits are prohibited.

Bit 5 ~ Bit 4: DC3SR bit

DCDC3 ramp rate of output voltage setting bit

DC3SR[1:0]	Voltage Slope
00	14 mV / us (default)
01	7 mV / us
10	3.5 mV / us
11	Prohibited

Note\*: Writing this register is prohibited during the ramp control.

Bit 2 ~ Bit 1: DC3LIM bit

DCDC3 minimum current limit setting bit

DC3LIM[1:0]	Current limit
00	No Limit
01	2.3A
10	2.8A
11	3.2A

The default current can be set up all of the above register values by OTP.

Bit 0: DC3LIMSDEN bit

Enable shutdown function from the current limit detection of DCDC3.

The current limit detection is to continue exceeding limit current during 2ms.

“0”: Disable

“1”: Enable

The initial value of this register depends on Mode setting. Mode setting is set by OTP.

·Normal Mode

DC3LIMSDEN = 1b

·Parts Mode

DC3LIMSDEN = 0b

**13.5.7 DC4CTL: DCDC4 Control Register (Address 32h)**

Bit	7	6	5	4	3	2	1	0
Symbol	DC4MODE_SLP[1:0]		DC4MODE[1:0]		-	-	DC4DIS	DC4EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	1	By OTP

Bit 7 ~ 6: DC4MODE\_SLP[1:0] bit

DCDC4 mode setting bit at the SLEEP state

Bit 5 ~ 4: DC4MODE[1:0] bit

DCDC4 mode setting bit at the POWERON state

“00”: Auto mode

“01”: PWM mode

“10”: PSM mode

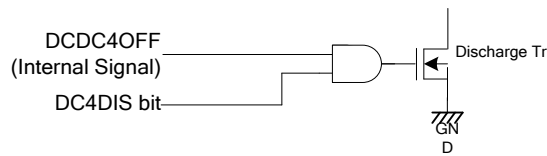
“11”: Auto mode

Bit 1: DC4DIS bit

DCDC4 discharge control bit

“0”: Off

“1”: On (This bit is invalid when DCDC4 state is on.)



Bit 0: DC4EN bit

DCDC4 enable bit

“0”: Disable

“1”: Enable

The initial value of this register depends on the initial value of DC4ONSLOT register and Mode setting. The initial value of DC4ONSLOT register and Mode setting are set by OTP.

·Norma Mode

DC4ONSLOT = Fh: DC4EN = 0b

DC4ONSLOT = 0h-Eh: DC4EN = 1b

·Parts Mode

DC4EN = 1b

**13.5.8 DC4CTL2: DCDC4 Control2 Register (Address 33h)**

Bit	7	6	5	4	3	2	1	0
Symbol	(reserved)		DC4SR[1:0]		-	DC4LIM[1:0]		DC4LIMSDEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	By OTP	By OTP	0	0	0	By OTP	By OTP	By OTP

Bit 7 ~ Bit 6: reserved bit

Note\*: This bits are reserved. Writing this bits are prohibited.

Bit 5 ~ Bit 4: DC4SR bit

DCDC4 ramp rate of output voltage setting bit

DC4SR[1:0]	Voltage Slope
00	14 mV / us (default)
01	7 mV / us
10	3.5 mV / us
11	Prohibited

Note\*: Writing this register is prohibited during the ramp control.

Bit 2 ~ Bit 1: DC4LIM bit

DCDC4 minimum current limit setting bit

DC4LIM[1:0]	Current limit
00	No Limit
01	2.3A
10	2.8A
11	3.2A

The default current can be set up all of the above register values by OTP.

Bit 0: DC4LIMSDEN bit

Enable shutdown function from the current limit detection of DCDC4.

The current limit detection is to continue exceeding limit current during 2ms.

“0”: Disable

“1”: Enable

The initial value of this register depends on Mode setting. Mode setting is set by OTP.

·Normal Mode

DC4LIMSDEN = 1b

·Parts Mode

DC4LIMSDEN = 0b

**13.5.9 DC1DAC: DCDC1 Output Voltage Control Register (Address 36h)**

Bit	7	6	5	4	3	2	1	0
Symbol	DC1DAC[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0	0

**13.5.10 DC2DAC: DCDC2 Output Voltage Control Register (Address 37h)**

Bit	7	6	5	4	3	2	1	0
Symbol	DC2DAC[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0	0

**13.5.11 DC3DAC: DCDC3 Output Voltage Control Register (Address 38h)**

Bit	7	6	5	4	3	2	1	0
Symbol	DC3DAC[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0	0

**13.5.12 DC4DAC: DCDC4 Output Voltage Control Register (Address 39h)**

Bit	7	6	5	4	3	2	1	0
Symbol	DC4DAC[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0	0

**The output voltage table of DCDC1~4 (Step=12.5mV)**

DCnDAC[7:0]	Output voltage [V]
0000000 (00h)	0.6000
~	~
0011000 (18h)	0.9000
~	~
1011100 (5Ch)	1.7500
~	~
11101000 (E8h)	3.5000
~	Prohibit
11111111 (FFh)	Prohibit

The default voltage can be set up from 0.6V to 3.5V at 50mV/step by OTP.

**13.5.13 DC1DAC\_SLP: DCDC1 Output Voltage Control Register in Sleep (Address 3Bh)**

Bit	7	6	5	4	3	2	1	0
Symbol	DC1DAC_SLP[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0	0

**13.5.14 DC2DAC\_SLP: DCDC2 Output Voltage Control Register in Sleep (Address 3Ch)**

Bit	7	6	5	4	3	2	1	0
Symbol	DC2DAC_SLP[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0	0

**13.5.15 DC3DAC\_SLP: DCDC3 Output Voltage Control Register in Sleep (Address 3Dh)**

Bit	7	6	5	4	3	2	1	0
Symbol	DC3DAC_SLP[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0	0

**13.5.16 DC4DAC\_SLP: DCDC4 Output Voltage Control Register in Sleep (Address 3Eh)**

Bit	7	6	5	4	3	2	1	0
Symbol	DC4DAC_SLP[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0	0

**The output voltage table of DCDC1~4 (Step=12.5mV)**

DCnDAC_SLP[7:0]	Output voltage [V]
0000000 (00h)	0.6000
~	~
0011000 (18h)	0.9000
~	~
1011100 (5Ch)	1.7500
~	~
11101000 (E8h)	3.5000
~	Prohibit
11111111 (FFh)	Prohibit

The default voltage is set to the value of the DC1-4DAC register.

**13.5.17 DCIREN: DCDC Interrupt Enable Register (Address 40h)**

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	EN_ DC4LIM	EN_ DC3LIM	EN_ DC2LIM	EN_ DC1LIM
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit 3 ~ Bit 0: EN\_DCnLIM bit (n=1, 2, 3, 4)

DCDCn current limit interrupt enable bit

“0”: Disable

“1”: Enable

**13.5.18 DCIRQ: DCDC Interrupt Flag Register (Address 41h)**

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	IR_ DC4LIM	IR_ DC3LIM	IR_ DC2LIM	IR_ DC1LIM
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Note\*: Each bit can be cleared by writing “0”, but cannot be set by writing “1”.

Bit 3 ~ Bit 0: IR\_DCnLIM bit (n=1, 2, 3, 4)

DCDCn current limit flag bit

“0”: None

“1”: Requested

**13.5.19 DCIRMON: DCDC Interrupt Monitor Register (Address 42h)**

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	MON_ DC4LIM	MON_ DC3LIM	MON_ DC2LIM	MON_ DC1LIM
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit 3 ~ Bit 0: MON\_DCnLIM bit (n=1, 2, 3, 4)

DCDCn current limit interrupt monitor bit

“0”: Undetected

“1”: Detected

## 13.6 LDO

### 13.6.1 LDOEN1: LDOs On / Off Control Register (Address 44h)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	LDO5EN	LDO4EN	LDO3EN	LDO2EN	LDO1EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	By OTP	By OTP	By OTP	By OTP	By OTP

Bit 4 ~ Bit 0: LDO<sub>n</sub>EN bit (n=1, 2, 3, 4, 5)

LDO<sub>n</sub> on/off control bit

“0”: Off

“1”: On

The initial value of this register depends on the initial value of LDO<sub>n</sub>ONSLOT register, the mode setting. The initial value of LDO<sub>n</sub>ONSLOT register, the mode setting are set by OTP.

·Normal Mode

LDO<sub>n</sub>ONSLOT = Fh: LDO<sub>n</sub>EN = 0b

LDO<sub>n</sub>ONSLOT = 0h-Eh: LDO<sub>n</sub>EN = 1b

·Parts Mode

LDO<sub>n</sub>EN = 1b



**13.6.2 LDOEN2: LDOs On / Off Control Register (Address 45h)**

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	LDORTC2 EN*1	LDORTC1 EN*2	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	By OTP	By OTP	0	0	0	0

Bit 5 ~ Bit 4: LDO<sub>n</sub>EN bit (n= RTC,RTC2)

LDO<sub>n</sub> on/off control bit

“0”: Off

“1”: On

Note\*1: Writing to this bit is prohibited when GPIO2 pin is not set as LDORTC2 output.

Note\*2: The initial value of this register depends on the initial value of LDORTC1ONSL0T register, Mode setting and Always-on setting.

The initial value of LDO<sub>n</sub>ONSL0T register, Mode setting and Always-on setting are set by OTP.

· Always-on

LDORTC1EN = 1b (without dependence on Mode setting)

· Normal Mode

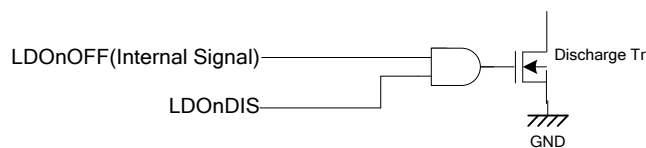
LDORTC1ONSL0T = Fh: LDORTC1EN = 0b

LDORTC1ONSL0T = 0h-Eh: LDORTC1EN = 1b

**13.6.3 LDODIS: LDOs On / Off Control Register (Address 46h)**

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	LDO5DIS	LDO4DIS	LDO3DIS	LDO2DIS	LDO1DIS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	1	1	1	1	1

Bit 4 ~ Bit 0: LDO<sub>n</sub>DIS bit (n=1, 2, 3, 4, 5)  
 LDO<sub>n</sub> discharge Tr on/off control bit  
 "0": Off  
 "1": On (This bit is invalid when LDO<sub>n</sub> state is on.)



**13.6.4 LDO1DAC: LDO1 Output Voltage Control Register (Address 4Ch)**

Bit	7	6	5	4	3	2	1	0
Symbol	-	LDO1DAC						
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0

**13.6.5 LDO2DAC: LDO2 Output Voltage Control Register (Address 4Dh)**

Bit	7	6	5	4	3	2	1	0
Symbol	-	LDO2DAC						
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0

**The output voltage table of LDO1~2 (Step=50mV)**

LDO <sub>n</sub> DAC[6:0]	Output voltage [V]
0000000 (00h)	0.900
0000010 (02h)	0.950
~	~
0100100 (24h)	1.800
~	~
1101000 (68h)	3.500
~	Prohibit
1111110 (7Eh)	Prohibit

The default voltage can be set up from 0.9V to 3.5V at 50mV/step by OTP.

**13.6.6 LDO3DAC: LDO3 Output Voltage Control Register (Address 4Eh)**

Bit	7	6	5	4	3	2	1	0
Symbol	-	LDO3DAC						
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0

**The output voltage table of LDO3 (Step=50mV)**

LDO3DAC[6:0]	Output voltage [V]
0000000 (00h)	0.600
0000010 (02h)	0.650
~	~
0110000 (30h)	1.800
~	~
1110100 (74h)	3.500
~	Prohibit
1111110 (7Eh)	Prohibit

The default voltage can be set up from 0.6V to 3.5V at 50mV/step by OTP.

**13.6.7 LDO4DAC: LDO4 Output Voltage Control Register (Address 4Fh)**

Bit	7	6	5	4	3	2	1	0
Symbol	-	LDO4DAC						
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0

**13.6.8 LDO5DAC: LDO5 Output Voltage Control Register (Address 50h)**

Bit	7	6	5	4	3	2	1	0
Symbol	-	LDO5DAC						
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0

**The output voltage table of LDO4~5 (Step=50mV)**

LDO <sub>n</sub> DAC[6:0]	Output voltage [V]
0000000 (00h)	0.900
0000010 (02h)	0.950
~	~
0100100 (24h)	1.800
~	~
1101000 (68h)	3.500
~	Prohibit
1111110 (7Eh)	Prohibit

The default voltage can be set up from 0.9V to 3.5V at 50mV/step by OTP.

**13.6.9 LDORTCDAC: LDORTC Output Voltage Control Register (Address 56h)**

Bit	7	6	5	4	3	2	1	0
Symbol	-	LDORTCDAC						
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0

**The output voltage table of LDORTC (Step=50mV)**

LDORTCDAC[6:0]	Output voltage [V]
0000000 (00h)	1.200
0000010 (02h)	1.250
~	~
0011000 (18h)	1.800
~	~
1011100 (5Ch)	3.500
~	Prohibit
1111110 (7Eh)	Prohibit

The default voltage can be set up from 1.2V to 3.5V at 50mV/step by OTP.

**13.6.10 LDORTC2DAC: LDORTC2 Output Voltage Control Register (Address 57h)**

Bit	7	6	5	4	3	2	1	0
Symbol	-	LDORTC2DAC						
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0

**The output voltage table of LDORTC2 (Step=50mV)**

LDORTC2DAC[6:0]	Output voltage [V]
0000000 (00h)	0.900
0000010 (02h)	0.950
~	~
0100100 (24h)	1.800
~	~
1101000 (68h)	3.500
~	Prohibit
1111110 (7Eh)	Prohibit

The default voltage can be set up from 0.9V to 3.5V at 50mV/step by OTP.

**13.6.11 LDO1DAC\_SLP: LDO1 Output Voltage Control Register in Sleep (Address 58h)**

Bit	7	6	5	4	3	2	1	0
Symbol	-	LDO1DAC_SLP[6:0]						
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0

**13.6.12 LDO2DAC\_SLP: LDO2 Output Voltage Control Register in Sleep (Address 59h)**

Bit	7	6	5	4	3	2	1	0
Symbol	-	LDO2DAC_SLP[6:0]						
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0

**The output voltage table of LDO1~2 (Step=50mV)**

LDO <sub>n</sub> DAC_SLP[6:0]	Output voltage [V]
0000000 (00h)	0.900
0000010 (02h)	0.950
~	~
0100100 (24h)	1.800
~	~
1101000 (68h)	3.500
~	Prohibit
1111110 (7Eh)	Prohibit

The default voltage is set to the value of the LDO<sub>n</sub>DAC register.

**13.6.13 LDO3DAC\_SLP: LDO3 Output Voltage Control Register in Sleep (Address 5Ah)**

Bit	7	6	5	4	3	2	1	0
Symbol	-	LDO3DAC_SLP[6:0]						
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0

**The output voltage table of LDO3 (Step=50mV)**

LDO3DAC_SLP[6:0]	Output voltage [V]
0000000 (00h)	0.600
0000010 (02h)	0.650
~	~
0110000 (30h)	1.800
~	~
1110100 (74h)	3.500
~	Prohibit
1111110 (7Eh)	Prohibit

The default voltage is set to the value of the LDO3DAC register.

**13.6.14 LDO4DAC\_SLP: LDO4 Output Voltage Control Register in Sleep (Address 5Bh)**

Bit	7	6	5	4	3	2	1	0
Symbol	-	LDO4DAC_SLP[6:0]						
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0

**13.6.15 LDO5DAC\_SLP: LDO5 Output Voltage Control Register in Sleep (Address 5Ch)**

Bit	7	6	5	4	3	2	1	0
Symbol	-	LDO5DAC_SLP[6:0]						
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0

**The output voltage table of LDO4~5 (Step=50mV)**

LDO <sub>n</sub> DAC_SLP[6:0]	Output voltage [V]
0000000 (00h)	0.900
0000010 (02h)	0.950
~	~
0100100 (24h)	1.800
~	~
1101000 (68h)	3.500
~	Prohibit
1111110 (7Eh)	Prohibit

The default voltage is set to the value of the LDO<sub>n</sub>DAC register.

## 13.7 GPIO

### 13.7.1 IOSEL: GPIO Direction Setting Register (Address 90h)

IOSEL register can set the input/output of GPIO pin. Writing “0” in the register, the corresponding pin becomes input pin, and becomes output pin when writing “1”.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	IO03	IO02	IO01	IO00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit	Symbol	R/W	Function	1	0	Initial value
3	IO03	R/W	GPI03 Direction Setting bit	Output	Input	0
2	IO02	R/W	GPI02 Direction Setting bit	Output	Input	0
1	IO01	R/W	GPI01 Direction Setting bit	Output	Input	0
0	IO00	R/W	GPI00 Direction Setting bit	Output	Input	0

Note\*1: IO03 – IO00 are invalid when PSO mode.

※ PSO ... Power-on Signal Output for the external devices.

### 13.7.2 IOOUT: GPIO Output Signal Register (Address 91h)

IOOUT register can set “L” or “Hi-Z” of GPIO pin when GP pin is set as output.

By writing “0” in IOOUT register, the corresponding pin outputs “L” and becomes “Hi-Z” by writing “1”.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	IOOUT03	IOOUT02	IOOUT01	IOOUT00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit	Symbol	R/W	Function	1	0	Initial value
3	IOOUT03	R/W	GPI03 Output Setting bit	H	L	0
2	IOOUT02	R/W	GPI02 Output Setting bit	H	L	0
1	IOOUT01	R/W	GPI01 Output Setting bit	H	L	0
0	IOOUT00	R/W	GPI00 Output Setting bit	H	L	0

Note\*1: Valid only in the output mode.

Note\*2: When the output circuit is set as Nch open drain by OTP, the output of GP pin becomes not “H” but “Hi-Z”.



**13.7.3 GPEDGE1: GPIO Interrupt Detection Type Setting Register (Address 92h)**

GPEDGE register can set GPIO interrupt detection type.

Bit	7	6	5	4	3	2	1	0
Symbol	EDGE03		EDGE02		EDGE01		EDGE00	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit	Symbol	R/W	Function	1	0	Initial value
7-6	EDGE03	R/W	GPI03 Interrupt Detection Type Setting bit	As below		00
5-4	EDGE02	R/W	GPI02 Interrupt Detection Type Setting bit	As below		00
3-2	EDGE01	R/W	GPI01 Interrupt Detection Type Setting bit	As below		00
1-0	EDGE00	R/W	GPI00 Interrupt Detection Type Setting bit	As below		00

EDGE*[1:0]	Detection Function
00	Level (default)
01	Rising Edge
10	Falling Edge
11	Both Edge

**13.7.4 EN\_GPIR: Interrupt Enable Register (Address 94h)**

Writing "1" enables the interrupt request.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	EN_ GP03IR	EN_ GP02IR	EN_ GP01IR	EN_ GP00IR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit	Symbol	R/W	Function	1	0	Initial value
3	EN_GP03IR	R/W	GPI03 interrupt enable bit	Enable	Disable	0
2	EN_GP02IR	R/W	GPI02 interrupt enable bit	Enable	Disable	0
1	EN_GP01IR	R/W	GPI01 interrupt enable bit	Enable	Disable	0
0	EN_GP00IR	R/W	GPI00 interrupt enable bit	Enable	Disable	0

**13.7.5 IR\_GPR: Rising Edge Interrupt Request Register (Address 95h)**

In the rising edge or both edge mode, IR\_GPR register can monitor the interrupt request of rising edge.

The register is cleared by writing "0" in the corresponding bit, but cannot be set by writing "1".

The function above-mentioned is operated in level mode as well.

However, it cannot be cleared while the interrupt request signal is "H".

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	IR_ GP03R	IR_ GP02R	IR_ GP01R	IR_ GP00R
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit	Symbol	R/W	Function	1	0	Initial value
3	IR_GP03R	R/W	GPI03 Rising Edge Interrupt Request bit	Requested	None	0
2	IR_GP02R	R/W	GPI02 Rising Edge Interrupt Request bit	Requested	None	0
1	IR_GP01R	R/W	GPI01 Rising Edge Interrupt Request bit	Requested	None	0
0	IR_GP00R	R/W	GPI00 Rising Edge Interrupt Request bit	Requested	None	0

**13.7.6 IR\_GPF: Falling Edge Interrupt Request Register (Address 96h)**

In the falling edge or both edge mode, IR\_GPF can monitor the interrupt request of falling edge. It is cleared by writing "0" corresponding bit, but cannot be set by writing "1".

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	IR_ GP03F	IR_ GP02F	IR_ GP01F	IR_ GP00F
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit	Symbol	R/W	Function	1	0	Initial value
3	IR_GP03F	R/W	GPI03 Falling Edge Interrupt Request bit	Requested	None	0
2	IR_GP02F	R/W	GPI02 Falling Edge Interrupt Request bit	Requested	None	0
1	IR_GP01F	R/W	GPI01 Falling Edge Interrupt Request bit	Requested	None	0
0	IR_GP00F	R/W	GPI00 Falling Edge Interrupt Request bit	Requested	None	0

**13.7.7 MON\_IOIN: GPIO Input Signal Read Register (Address 97h)**

MON\_IOIN register can monitor the debounced signal from GP pin.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	MON_ IOIN03	MON_ IOIN02	MON_ IOIN01	MON_ IOIN00
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	Undefined	Undefined	Undefined	Undefined

Bit	Symbol	R/W	Function	1	0	Initial value
3	MON_IOIN03	R	GPI03 input status bit	H	L	-
2	MON_IOIN02	R	GPI02 input status bit	H	L	-
1	MON_IOIN01	R	GPI01 input status bit	H	L	-
0	MON_IOIN00	R	GPI00 input status bit	H	L	-

**13.7.8 GPLED\_FUNC: LED Function Setting Register (Address 98h)**

When set to LED function, GPIO0 and GPIO1 can be changed type of flicker for LED.

Bit	7	6	5	4	3	2	1	0
Symbol	-	GP1_LED MODE	GP1_LEDFUNC[1:0]		-	GP0_LED MODE	GP0_LEDFUNC[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	By OTP	0	0	0	By OTP	0	0

Bit	Symbol	R/W	Function	1	0	Initial value
6	GP1_LEDMODE	R/W	GP1 LED_MODE Select bit	As below		OTP
5-4	GP1_LEDFUNC	R/W	GP1 Type of Flicker Select bit			0
2	GP0_LEDMODE	R/W	GP0 LED_MODE Select bit	As below		OTP
1-0	GP0_LEDFUNC	R/W	GP0 Type of Flicker Select bit			0

LED Mode (GP*_LEDMODE bit)	Power On/Off status or Flicker Control (GP*_LEDFUNC bit)	GPIO	
		Mode	Type of Flicker
0	Power Off	POWERON/OFF function	Off
	Power On	POWERON/OFF function	Always Turn-On
1	00b	LED function	Off
	01b	LED function	1Hz Flicker (25% Turn-on)
	10b	LED function	4Hz Flicker (25% Turn-on)
	11b	LED function	Always Turn-on

## 13.8 INTC

### 13.8.1 INTPOL: Interrupt Polarity Register (Address 9Ch)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	INTPOL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit 0: INTPOL bit

INTB pin polarity

“0”: Low-active

“1”: High-active

### 13.8.2 INTEN: Interrupt Output Control Register (Address 9Dh)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	GPIO IREN	-	-	DCDC IREN	SYSTEM IREN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit 4: GPIOIREN bit

GPIO interrupt enable

“0”: Disable

“1”: Enable

Bit 1: DCDCIREN bit

DCDC interrupt enable

“0”: Disable

“1”: Enable

Bit 0: SYSTEMIREN bit

SYSTEM interrupt enable

“0”: Disable

“1”: Enable

**13.8.3 INTMON: Interrupt Monitor Register (Address 9Eh)**

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	WDG IRM	GPIO IRM	-	-	DCDC IRM	SYSTEM IRM
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit 5: WDGIRM bit

Watchdog interrupt flag monitor

"0": None

"1": Requested

Bit 4: GPIOIRM bit

GPIO interrupt flag monitor

"0": None

"1": Requested

Bit 1: DCDCIRM bit

DCDC interrupt flag monitor

"0": None

"1": Requested

Bit 0: SYSTEMIRM bit

SYSTEM interrupt flag monitor

"0": None

"1": Requested

## 13.9 SYSTEM OPTION

### 13.9.1 PREVINDAC: PREVINDET Detection Voltage Setting Register (Address B0h)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	PREVIN DACH	PREVIN DAC[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	By OTP	By OTP	By OTP

#### Bit 2: PREVINDACH bit

Setting the detection voltage to PREVINDET

#### Bit 1 ~ Bit 0: PREVINDAC bit

Setting the detection voltage to PREVINDET

#### The detection voltage table of PREVINDET

PREVINDACH	PREVINDAC[1:0]	Detection voltage [V]
0	00 (0h)	2.75(↑)/2.7(↓)
0	01 (1h)	2.85(↑)/2.8(↓)
0	10 (2h)	2.95(↑)/2.9(↓)
0	11 (3h)	3.05(↑)/3.0(↓)
1	00 (0h)	3.30(↑)/3.2(↓)
1	01 (1h)	3.40(↑)/3.3(↓)
1	10 (2h)	3.50(↑)/3.4(↓)
1	11 (3h)	3.60(↑)/3.5(↓)

The default voltage can be set up by OTP.

### 13.9.2 OVTEMP: Overheat Detection Temperature Setting Register (Address BCh)

This register sets the detection temperature for Overheat temperature.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	OVTEMP[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	By OTP	

#### Bit 1~0: OVTEMP[1:0] bit

Setting the detection temperature of overheat detection.

OVTEMP[1:0]	Temperature [degrees C] (Detection / Recovery)
00 (0h)	105 / 85
01 (1h)	115 / 95
10 (2h)	125 / 105
11 (3h)	135 / 115

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