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QorIQ T1024 Reference Design Board Quick Start

1 Introduction

The T1024 reference design board (RDB) system is a hardware board, having a Freescale QorIQ T1024 processor with two e5500 cores and speed up to 1.4 GHz.

For the T1024 RDB system, the prototype part number is XT1024RDB-PC and the production part number is T1024RDB-PC.

Contents

2 Related documentation

The table below lists and explains the additional documents that you can refer to, for more information about T1024RDB.

Some of the documents listed below may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local field applications engineer or sales representative.

Table 1. Useful references

Document	Description
QorIQ T1024, T1014 Data Sheet (T1024EC)	Provides specific data regarding bus timing, signal behavior, and AC, DC, and thermal characteristics, as well as other design considerations.
QorIQ T1024 Reference Manual (T1024RM)	Provides a detailed description on T1024 QorIQ multicore processor, and on some of its features, such as memory map, serial interfaces, power supply, chip features, and clock information. The T1024 QorIQ processor combines two 64-bit ISA Power Architecture® processor cores with high-performance datapath acceleration logic and network peripheral bus interfaces, required for networking and telecommunications. This chip can be used in applications, such as routers, switches, Internet access devices, firewall and other packet filtering processors, and general-purpose embedded computing. Its high-level integration offers significant performance benefits and greatly helps to simplify board design.
T1024 Product Brief (T1024PC)	Provides an overview of the T1024 features and usage examples of T1024.
QorIQ T1024 Reference Design Board User Guide (T1024RDBPCUG)	Describes the features and operation of T1024 performance reference platform, which supports QorIQ Power Architecture® processors.

NOTE

For more information on T1024RDB, see T1024RDB Product Summary Page

3 Preparing board

The figure below shows the UART serial port of the T1024RDB-PC.

Figure 1. T1024RDB serial ports location

To prepare a T1024RDB-PC board for use, set the default configuration as: CPU: 1.4 GHz and DDR: 1600 MT/s. The steps to prepare a T1024RDB-PC board are as follows:

1. Attach an RS-232 cable (RJ45 to DB9 cable) between the T1024RDB UART0 port (the upper RJ45 port) and serial port of the host computer.
2. Open a serial connection on the host computer to communicate with the T1024RDB.
3. Configure the host computer's serial port with the following settings:
   - Data rate: 115200 bit/s
   - Number of data bits: 8
   - Parity: None

- Number of stop bits: 1
- Flow control: Hardware/None

4. Press the power button on the lower left hand corner of the motherboard.

The board boots up and shows the U-Boot console messages as illustrated below:

```
U-Boot 2014.07QorIQ-SDK-V1.7+g659b6a2 (Mar 17 2015 - 11:03:18)
CPU0:  T1024E, Version: 1.0, (0x85480010)
Core:  e5500, Version: 2.1, (0x80241021)
Single Source Clock Configuration
Clock Configuration:
       CPU0:1400 MHz, CPU1:1400 MHz,
       CCB:400  MHz,
       DDR:800  MHz (1600 MT/s data rate) (Asynchronous), IFC:100  MHz
       QE:200  MHz
       FMAN1: 700 MHz
       QMAN:  400 MHz
L1:    D-cache 32 KiB enabled
       I-cache 32 KiB enabled
Reset Configuration Word (RCW):
       0000000: 0810000e 00000000 00000000 00000000
       0000010: 4a800001 80000012 ec027000 21000000
       0000020: 00000000 00000000 00000000 00030810
       0000030: 00000000 0b005a08 00000000 00000006
Board: T1024RDB, Board rev: 0x03 CPLD ver: 0x05, boot from NOR vBank0
SERDES Reference Clocks:
SD1_CLK1=156.25MHZ, SD1_CLK2=100.00MHZ
I2C:   ready
SPI:   ready
DRAM:  Initializing....using SPD
Detected UDIMM 18KSF51272AZ-1G6K1
4 GiB (DDR3, 64-bit, CL=11, ECC on)
       DDR Chip-Select Interleaving Mode: CS0+CS1
Flash: 128 MiB
L2:    256 KiB enabled
Corenet Platform Cache: 256 KiB enabled
Using SERDES1 Protocol: 149 (0x95)
NAND:  1024 MiB
MMC:   FSL_SDHC: 0
QE Firmware 'Microcode version 0.0.1 for T1024 r1.0' for 1024 V1.0
QE: uploading microcode 'Microcode for T1024 r1.0' version 0.0.1
EEPROM: NXID v1
PCIe1: Root Complex, no link, regs @ 0xfe240000
PCIe1: Bus 00 - 00
PCIe2: Root Complex, no link, regs @ 0xfe250000
PCIe2: Bus 01 - 01
PCIe3: Root Complex, no link, regs @ 0xfe260000
PCIe3: Bus 02 - 03
In:    serial
Out:   serial
Err:   serial
Net:   Fman1: Uploading microcode version 107.4.2
       FM1@DTSEC3, FM1@DTSEC4 [PRIME], FM1@TGEC1
Hit any key to stop autoboot:  0
```

The Linux system auto boots and shows the following messages on the login screen:

```
t1024rdb
login: root
root@t1024rdb:~#
```

4 T1024RDB system board interface

The figure below shows the top view of the T1024RDB system board interface.

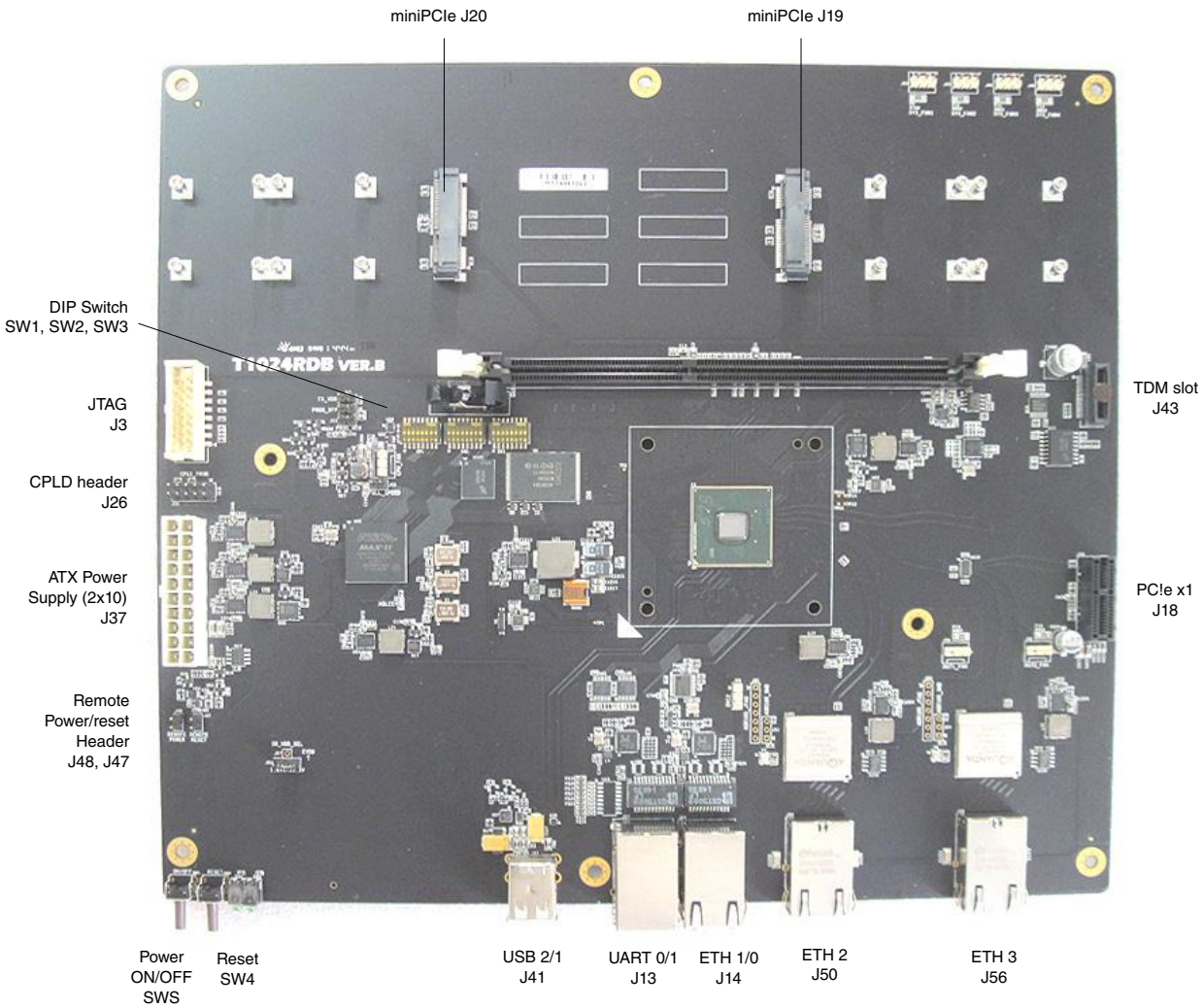

Figure 2. T1024RDB system board interface

4.1 Block diagram

The figure below shows the high-level block diagram of the T1024RDB.

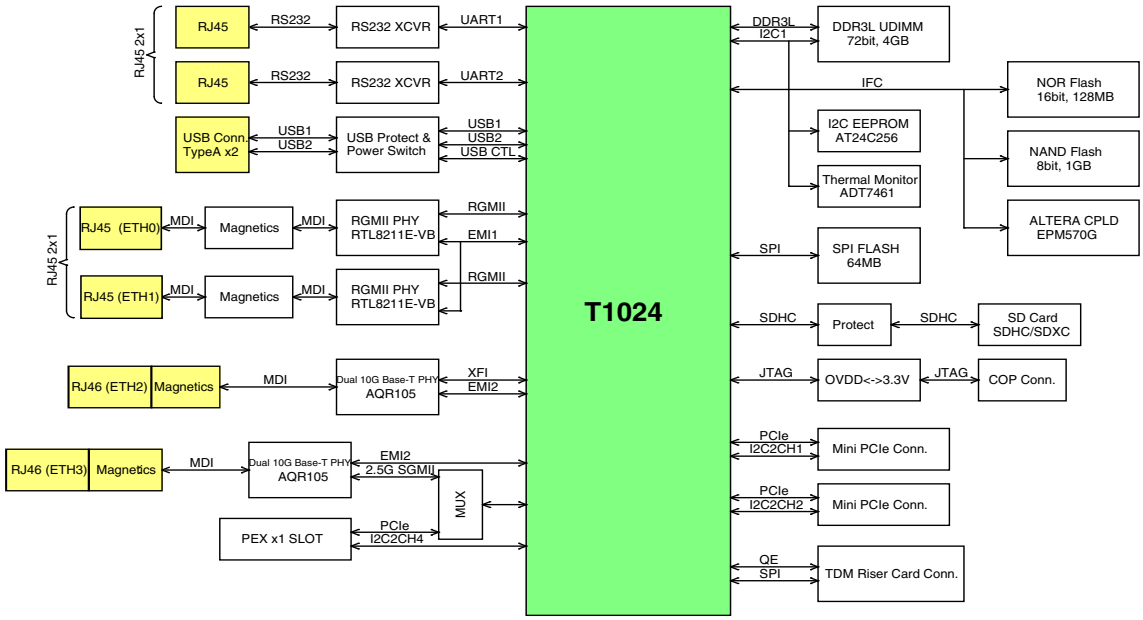

Figure 3. T1024RDB Block diagram

4.2 Features

Some key features of the T1024RDB are:

- Freescale QorIQ processing platform
  - QorIQ T1024 processor with two e5500 cores, 1.4 GHz
- Memory subsystem
  - DDR3L
    - 1 DIMM slot; supports 2 GB per DIMM
    - Supports DDR3 1600 UDIMM/RDIMM
  - NOR flash
    - 128 MB 16-bit NOR flash, MICRON: JS28F00AM29EWHA
  - NAND flash
    - 1 GB NAND flash, MICRON: MT29F8G08ABBCAH4:C
  - SD connector interface
- PCIe
  - One PCIe-x1 connector
  - Two mini PCIe connectors
- USB 2.0
  - One dual USB slot, connected to USB PHY
- Ethernet
  - ETH0 - ETH1: Connected to two independent RGMII PHYs - RTL8211E
  - ETH2: Connected to AQR105, 10GBase-T port
  - ETH3: 2.5G SGMII, connected to AQR105
- UART
  - Supports two UARTs, up to 115200 bit/s for console display; uses dual RJ45 slot for the two UARTs ports

4.3 Working modes

There are two working modes in the T1024RDB-PC. The following tables represents the configurations for 10GBase-T and 2.5G SGMII working modes:

Working mode	Image in Flash	SW3 [1:8] On = 0	SerDes Protocal	ETH0	ETH1	ETH2	ETH3	PCIe Slot
10GBase-T	Bank 0 (Default)	00100001	0x95	1G/100M	1G/100M	10G/ 2.5G/1G	Disable	Enable
2.5G SGMII	Bank4	01101001	0x135	1G/100M	Disable	Disable	2.5G	Disable

Working mode	SerDes Protocal	Lane A	Lane B	Lane C	Lane D	EC1	EC2
10GBase-T	0x95	XFI (MAC1)	PEXc	PEXb	PEXa	MAC4	MAC3
2.5G SGMII	0x135	Aurora	SGMII (MAC3)	PEXb	PEXa	MAC4	N/A

Follow the instructions to change the DIP settings to switch from the default 10G port to the 2.5G port:

- For 2.5G SGMII: Turn off the board, switch from bank0 to bank4 to use RCW 0x135, set SW3[5] = OFF(1) and SW3[2] = OFF(1)
- For 10GBase-T: Turn off the board, switch from bank4 to bank0 to use RCW 0x95, and set SW3[5] = ON(0) and SW3[2] = ON(0)

NOTE

Ignore the above switch settings for SW3[5] and SW3[2], when board is turned on while switching to bank0 using `cpld reset` or switching to bank4 using `cpld reset altbank`.

4.4 Port map

The tables below shows how the Ethernet port can be mapped to Linux, U-Boot, and label on the 1U box.

Table 2. Ethernet port mapping for SerDes 0x95 protocol

Label on 1U box	Port in U-Boot	Port in Linux	FMan address	Comments
ETH0	FM1@DTSEC4	fm1-mac4	0xffe4e6000	1G RGMII (RTL8211E)
ETH1	FM1@DTSEC3	fm1-mac3	0xffe4e4000	1G RGMII (RTL8211E)
ETH2	FM1@TGEC1	fm1-mac1	0xffe4e0000	10GBase-T (AQR105)

Table 3. Ethernet port mapping for SerDes 0x135 protocol

Label on 1U box	Port in U-Boot	Port in Linux	FMan address	Comments
ETH0	FM1@DTSEC4	fm1-mac4	0xffe4e6000	1G RGMII (RTL8211E)

Table continues on the next page...

Table 3. Ethernet port mapping for SerDes 0x135 protocol (continued)

ETH3	FM1@DTSEC3	fm1-mac3	0xffe4e4000	2.5G SGMII (AQR105)

5 Default boot mode

In T1024RDB, the boot loader, by default, executes from the NOR flash bank 0.

6 Flash image layout

Start address	End address	Image	Maximum size
0xEFF40000	0xEFFFFFFF	U-Boot (current bank)	768 KB
0xEFF20000	0xEFF3FFFF	U-Boot environment (current bank)	128 KB
0xEFF00000	0xEFF1FFFF	FMan microcode (current bank)	128 KB
0xEFE00000	0xEFE3FFFF	QUICC Engine firmware (current bank)	256 KB
0xED300000	0xEFEFFFFF	rootfs (alternate bank)	43 MB
0xEC800000	0xEC8FFFFF	Hardware device tree (alternate bank)	1 MB
0xEC020000	0xEC7FFFFF	Linux.uImage (alternate bank)	7 MB+875 KB
0xEC000000	0xEC01FFFF	RCW (alternate bank)	128 KB
0xEBF40000	0xEBFFFFFF	U-Boot (alternate bank)	768 KB
0xEBF20000	0xEBF3FFFF	U-Boot environment (alternate bank)	128 KB
0XEBF00000	0xEBF1FFFF	FMan microcode (alternate bank)	128 KB
0xEBE00000	0xEBE3FFFF	QUICC Engine firmware (alternate bank)	256 KB
0xE9300000	0xEBEFFFFF	rootfs (current bank)	43 MB
0XE8800000	0xE88FFFFF	Hardware device tree (current bank)	1 MB
0xE8020000	0xE86FFFFF	Linux.uImage (current bank)	7 MB+875 KB
0xE8000000	0xE801FFFF	RCW (current bank)	128 KB

7 Switch settings

This section defines the default switch settings and other boot source settings.

NOTE

The default switch settings may not match the ones given in the Quick Start guide, see *T1024RDB Reference Manual* for additional information.

7.1 Default switch settings (NOR flash boot)

NOR flash boot is the default boot mode. To boot from the NOR flash, the dual inline package (DIP) switches should be configured, as shown in the tables below:

NOTE

ON and OFF are represented on the board as 0 and 1, respectively.

Table 4. DIP switch settings for XFI 10G working mode

DIP switch	Switch binary value	1	2	3	4	5	6	7	8
SW1	0001 0011	ON	ON	ON	OFF	ON	ON	OFF	OFF
SW2	1011 1111	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
SW3	0010 0001	ON	ON	OFF	ON	ON	ON	ON	OFF

Follow the steps given below to change the DIP switch settings to 2.5G mode:

- Turn off the T1024RDB-PC board.
- Change switch settings as given in the below table.
- Turn on the T1024RDB-PC board.

Table 5. DIP switch settings for 2.5G SGMII working mode

DIP switch	Switch binary value	1	2	3	4	5	6	7	8
SW1	0001 0011	ON	ON	ON	OFF	ON	ON	OFF	OFF
SW2	1011 1111	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
SW3	0110 1001	ON	OFF	OFF	ON	OFF	ON	ON	OFF

7.2 Other boot source settings

To boot from the NAND flash, DIP switches should be configured, as shown in the table below:

DIP switch	Switch binary value	1	2	3	4	5	6	7	8
SW1	1000 1000	OFF	ON	ON	ON	OFF	ON	ON	ON
SW2	1011 1111	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
SW3	0111 0001	ON	OFF	OFF	OFF	ON	ON	ON	OFF

To boot from the SPI flash, DIP switches should be configured, as shown in the table below:

DIP switch	Switch binary value	1	2	3	4	5	6	7	8
SW1	0010 0010	ON	ON	OFF	ON	ON	ON	OFF	ON
SW2	1011 1111	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
SW3	0110 0001	ON	OFF	OFF	ON	ON	ON	ON	OFF

To boot from the SD card, DIP switches should be configured, as shown in the table below:

DIP switch	Switch binary value	1	2	3	4	5	6	7	8
SW1	0010 0000	ON	ON	OFF	ON	ON	ON	ON	ON
SW2	0011 1111	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF
SW3	0110 0001	ON	OFF	OFF	ON	ON	ON	ON	OFF

7.3 Switch detailed description

The table below describes the switches in detail.

NOTE

ON and OFF are represented on the board as 0 and 1, respectively.

Switch	PoR configururation	Signal name	Signal meaning	Setting
SW1[1]	cfg_rcw_src0	IFC_AD8	000100111: NOR boot mode	RCW source: • 010011011: Hard-coded RCW for JTAG debug • 000100111: NOR boot mode • 10001000: NAND boot mode
SW1[2]	cfg_rcw_src1	IFC_AD9		
SW1[3]	cfg_rcw_src2	IFC_AD10		
SW1[4]	cfg_rcw_src3	IFC_AD11		
SW1[5]	cfg_rcw_src4	IFC_AD12		
SW1[6]	cfg_rcw_src5	IFC_AD13		
SW1[7]	cfg_rcw_src6	IFC_AD14		
SW1[8]	cfg_rcw_src7	IFC_AD15		
SW2[1]	cfg_rcw_src8	IFC_CLE		

Table continues on the next page...

Switch	PoR configururation	Signal name	Signal meaning	Setting
				• 001000101: SPI boot mode • 001000000: SD boot mode
SW2[2]	cfg_ifc_te	IFC_TE		OFF (1): IFC drives logic 0 for TE assertion.
SW2[3]	cfg_pll_config_sel_b	IFC_A18	Reserved	Reserved
SW2[4]	cfg_por_ainit	IFC_A19	Reserved	Reserved
SW2[5]	cfg_svr0	IFC_A16	Reserved	Reserved
SW2[6]	cfg_svr1	IFC_A17	Reserved	Reserved
SW2[7]	cfg_dram_type	IFC_A21		OFF (1): T1024 uses DDR3L (1.35V)
SW2[8]	cfg_rsp_dis	IFC_AVD	Reserved	Reserved
SW3[1]	cfg_eng_use0	IFC_WE_N		OFF (1): SYSCLK clock source ON (0): Single-clock source using diff_sys_clk
SW3[2]	cfg_eng_use1	IFC_OE_N		ON (0): Choose 10G working mode OFF (1): Choose 2.5G working mode
SW3[3]	cfg_eng_use2	IFC_WP_N		Reserved
SW3[4]		BOOT_FLASH_SEL		ON (0): Select NOR fash on CS0 OFF (1): Select NAND flash as CS0
SW3[5]		CFG_VBANK0	Alter flash bank	000: NOR flash bank 0 select, VBank0 contains the 10G working mode image 100: NOR flash bank 4 select, VBank4 contains the 2.5G SGMII working mode image
SW3[6]		CFG_VBANK1		
SW3[7]		CFG_VBANK2		
SW3[8]		TEST_SEL_N		

8 Programming flash (without U-Boot)

To program flash for the first time (without U-Boot), perform the following steps:

1. In U-Boot source code, add below line into *boards.cfg*, and run "`make T1024RDB_SPIFLASH_config`" to create `U-Boot_spi.bin`.
2. Set DIP switches as given below:
   - SW1: 0001 0011 (after CPLD v1.2, NOR boot mode can connect JTAG)

- SW2: 1011 1111
- SW3: 1110 0001

NOTE

In Single Clock mode, JTAG cannot work to connect CPU.

3. Run `T1024RDB_RCW_override.cfg` in CCS, to override RCW.
4. Run `T1024RDB_core_init.tcl` in the CodeWarrior IDE with Halt mode to configure DDR SDRAM.
5. Download RAM U-Boot `U-Boot-spi.bin` to 0x00200000, and set PC reg to 0x00200000.
6. Run with the CodeWarrior IDE.
7. After entering U-Boot command, stop the CodeWarrior software.
8. Memory download fman_ucode at 0x100000, download RCW at 0x200000, download U-Boot.bin at 0x1000000.
9. Run the CodeWarrior software again.
10. In U-Boot, execute the following commands:

    Erase all

```
cp.b 100000 eff00000 8000
cp.b 200000 e8000000 100
cp.b 1000000 eff40000 c0000
```

11. Power down, set DIP switches as follows:
    - SW1: 0001 0011
    - SW2: 1011 1111
    - SW3: 0110 0001
12. Turn power on, and the system will enter the U-Boot environment.

9 SDK build details

NOTE

See the latest SDK 1.7 documentation for information on building toolchain, RCW, boot loader, Linux, and the root file system for the T1024RDB-PC.

10 Revision history

The table below summarizes revisions to this document.

Table 6. Revision history

Revision	Date	Description
Rev 0	04/2015	Initial Public release

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