

## 100V Micropower Dual Voltage Monitor

### FEATURES

- **Wide Operating Range: 3.5V to 100V**
- **Wide Monitoring Range: 1.75V to 98V**
- **Quiescent Current: 7 $\mu$ A**
- **Adjustable Threshold Range**
- **Internal High Value Resistive Dividers**
- $\pm 1.4\%$  (Max) Threshold Accuracy Over Temperature
- Polarity Selection
- 100V Rated Outputs
- Selectable Built-In Hysteresis
- 20-Lead SW and 16-Lead 3mm  $\times$  3mm QFN Packages

### APPLICATIONS

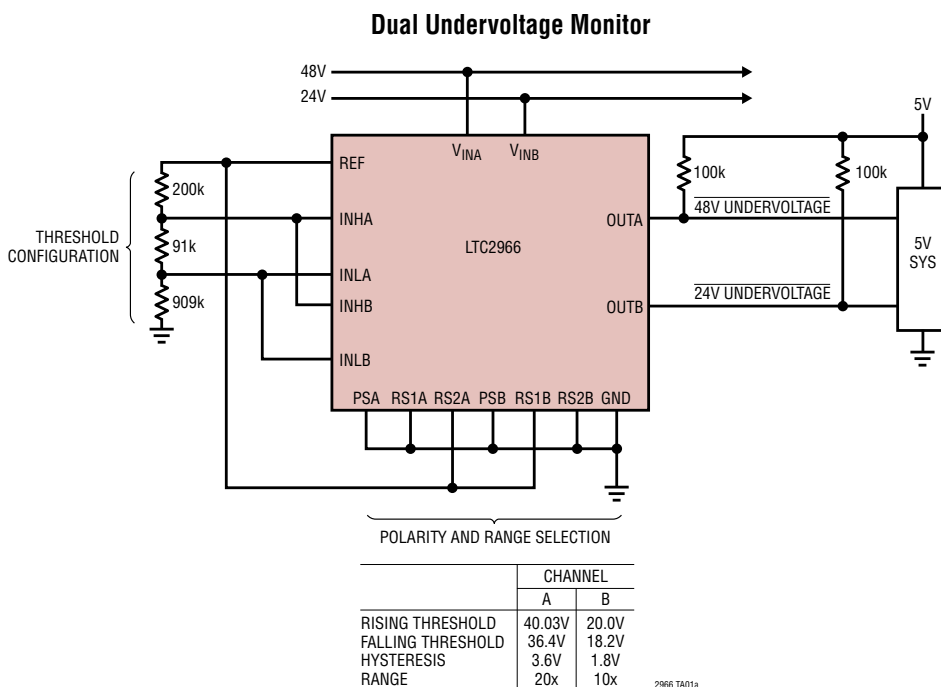
- Portable Equipment
- Battery-Powered Equipment
- Telecom Systems
- Automotive/Industrial Electronics

### DESCRIPTION

The **LTC<sup>®</sup>2966** is a low current, high voltage dual channel voltage monitor. Internal high value resistors sense the input monitor pins providing a compact and low power solution for voltage monitoring. Each channel includes two comparator reference inputs (INH/INL) to allow configuration of a high and low threshold using an external resistive divider biased from the on-chip reference. Range selection pins are provided for each channel to set the internal resistive dividers for 5x, 10x, 20x and 40x scaling. The thresholds are scaled according to the range selection settings. Additionally, either INH or INL can be grounded to enable built-in hysteresis. Polarity selection pins allow each output to be inverted. The outputs are 100V capable and include a 500k pull-up resistor to an internal supply.

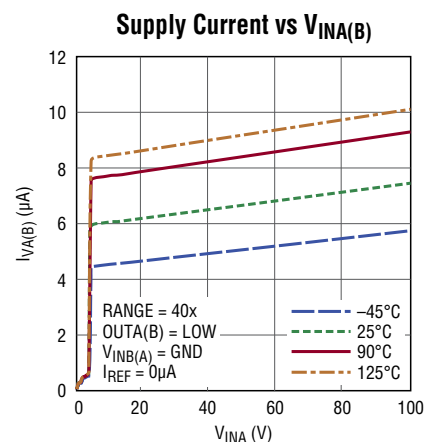
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### TYPICAL APPLICATION



V <sub>IN</sub> MONITOR RANGE	RANGE SELECTION
1.75V* to 12.25V	5x
3.5V to 24.5V	10x
7V to 49V	20x
14V to 98V	40x

\* Requires either V<sub>INA</sub> or V<sub>INB</sub> > 3.5V



2966fc



# ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{INA} = V_{INB} = 12\text{V}$ ,  $RS1/RS2 = \text{GND}$ ,  $PS = \text{GND}$ ,  $INH = 1.2\text{V}$ ,  $INL = \text{GND}$  (Notes 1, 2).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IN}$	Input Supply Operating Range	$V_{INA}$ or $V_{INB}$	●	3.5	100	V
$V_{MON}$	$V_{IN}$ Monitor Range	(Note 3)	●	1.75	98	V
$I_{VA}$	$V_{INA}$ Input Supply Current	$V_{INA} = 100\text{V}$ , $V_{INB} = \text{GND}$ , 40x $V_{INA} = \text{GND}$ , $V_{INB} = 100\text{V}$ , 40x	● ●	3 7	15 ±50	μA nA
$I_{VB}$	$V_{INB}$ Input Supply Current	$V_{INB} = 100\text{V}$ , $V_{INA} = \text{GND}$ , 40x $V_{INB} = \text{GND}$ , $V_{INA} = 100\text{V}$ , 40x $V_{INB} = 100\text{V}$ , $V_{INA} = 5\text{V}$ , 40x	● ● ●	3 7 2	15 ±50 4	μA nA μA
$V_{UVLO}$	Undervoltage Lockout	$V_{INA}$ or $V_{INB}$ Rising	●		3	V
	Undervoltage Lockout Hysteresis	$V_{INA}$ and $V_{INB}$ Falling		70		mV

## Comparator Reference Input: INHA, INHB, INLA, INLB

V <sub>CM</sub>	Comparator Common Mode Voltage		●	0.35	2.45	V	
V <sub>ERR</sub>	V <sub>IN</sub> Error Voltage at 96V	INH = V <sub>REF</sub> , 40x 0.35V ≤ INH ≤ 2.4V, 40x	● ●	±250 ±250	±1360 ±400	mV mV	
	V <sub>IN</sub> Error Voltage at 48V	INH = V <sub>REF</sub> , 20x 0.35V ≤ INH ≤ 2.4V, 20x	● ●	±100 ±100	±630 ±150	mV mV	
	V <sub>IN</sub> Error Voltage at 24V	INH = V <sub>REF</sub> , 10x 0.35V ≤ INH ≤ 2.4V, 10x	● ●	±35 ±35	±315 ±75	mV mV	
	V <sub>IN</sub> Error Voltage at 12V	INH = V <sub>REF</sub> , 5x 0.35V ≤ INH ≤ 2.4V, 5x	● ●	±15 ±15	±155 ±35	mV mV	
V <sub>OS</sub>	Comparator Offset Voltage	INH = 0.35V, 10x	●	±1.9	±3	mV	
AV <sub>ERR</sub>	Internal Resistive Divider Range Error	INH = 2.4V, Range = 5x, 10x, 20x, 40x	●		±0.4	%	
V <sub>HYS</sub>	Comparator Built-in Hysteresis	INH = GND, INL Rising INL = GND, INH Falling	● ●	14 –30	22 –22	30 –14	mV mV
V <sub>HYTH</sub>	Built-in Hysteresis Enable Threshold		●	100	175	mV	
t <sub>PD</sub>	V <sub>IN</sub> to OUT Comparator Propagation Delay	Overdrive = 10%, OUT Falling, 10x INH = GND, INL = 1.2V	●	40	80	μs	
I <sub>IN(LKG)</sub>	Input Leakage Current (INH, INL)	V = 1.2V, I-Grade V = 1.2V, H-Grade	● ●	±0.1 ±0.1	±1 ±10	nA nA	

## Reference: REF

$V_{REF}$	Reference Output Voltage	$I_{REF} \leq 100\mu\text{A}$ , $V_{IN} \geq 3.5\text{V}$	●	2.378	2.402	2.426	V
Noise	Reference Output Noise	100Hz to 100kHz			140		μV <sub>RMS</sub>

## Control Inputs: RS1A, RS2A, RS1B, RS2B, PSA, PSB

$V_{TH}$	Select Input Threshold		●	0.4	1.4		V
$I_{LKG}$	Input Leakage Current	$V = 2.4\text{V}$	●		±100		nA

## Status Outputs: OUTA, OUTB

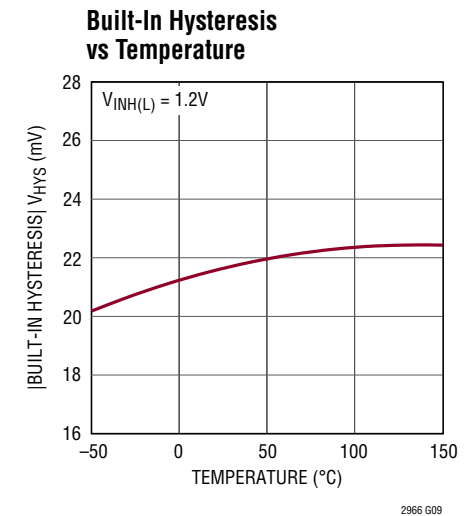
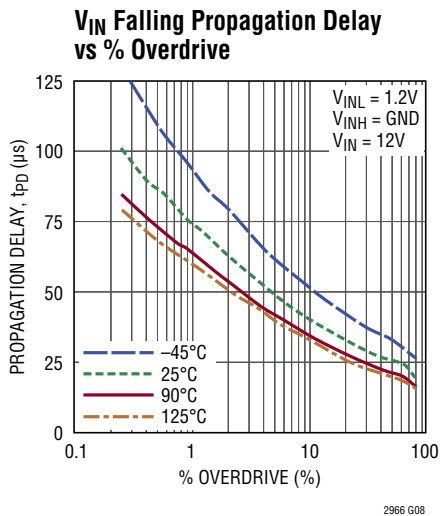
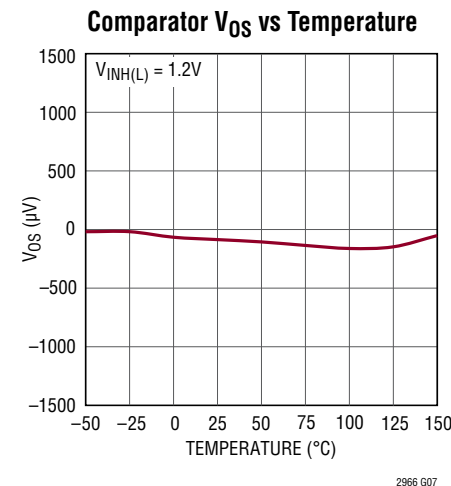
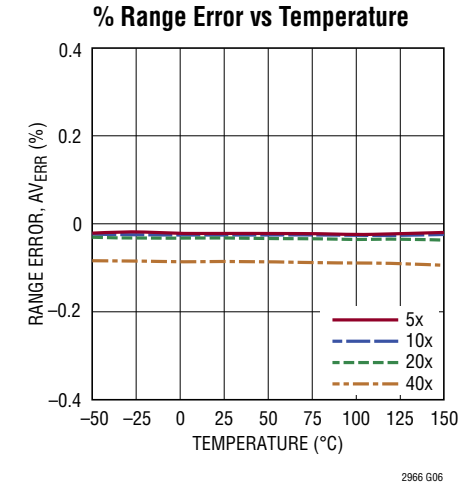
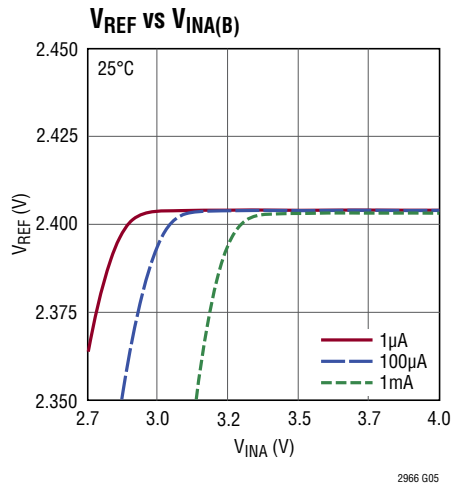
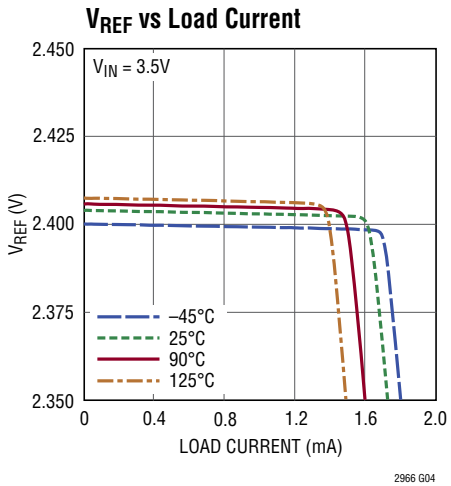
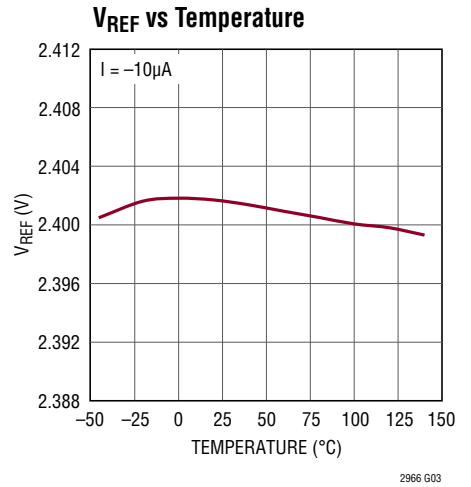
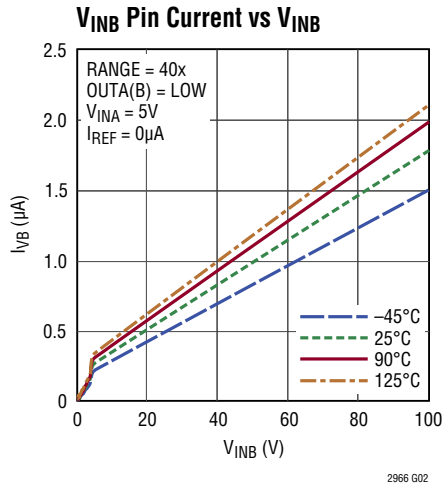
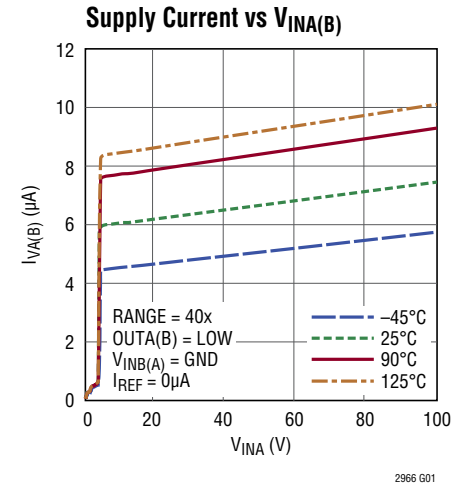
$V_{OL}$	Voltage Output Low	$V_{IN} = 1.25\text{V}$ , $I = 10\mu\text{A}$ $V_{IN} = 3.5\text{V}$ , $I = 500\mu\text{A}$	● ●			100 400	mV mV
$V_{OH}$	Voltage Output High	$V_{IN} = 3.5\text{V}$ , $I = -1\mu\text{A}$ $V_{IN} \geq 4.5\text{V}$ , $I = -1\mu\text{A}$	● ●	2 2.5	2.375 3	2.75 4	V V
$I_{OH}$	Output Current High	$V = \text{GND}$ , $V_{IN} = 3.5\text{V}$	●	-15	-7.5	-5	μA
$I_{O(LKG)}$	Leakage Current, Output High	$V = 100\text{V}$ , $V_{IN} = 6\text{V}$	●			±250	nA

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

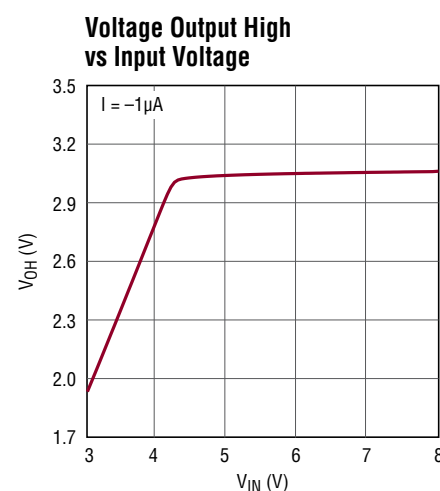
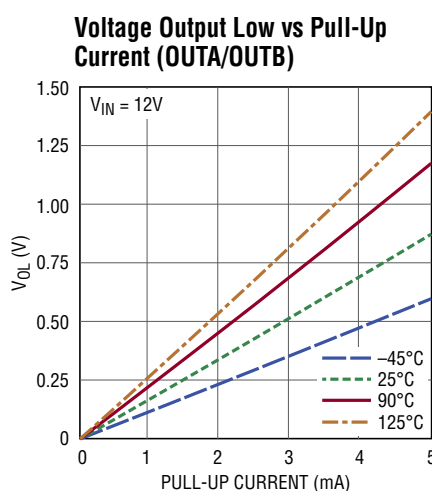
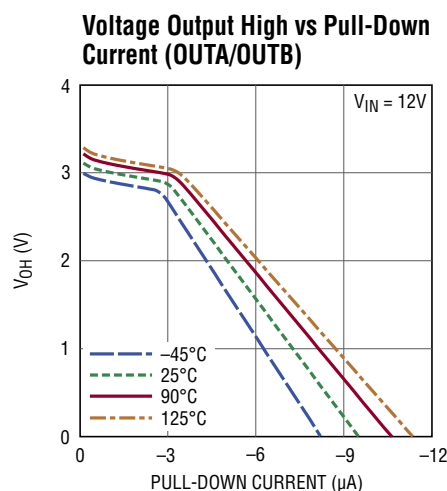
**Note 2:** All currents into pins are positive; all voltages are referenced to GND unless otherwise noted.

**Note 3:** Requires either  $V_{INA}$  or  $V_{INB} > 3.5\text{V}$ .

# TYPICAL PERFORMANCE CHARACTERISTICS



## TYPICAL PERFORMANCE CHARACTERISTICS



## PIN FUNCTIONS

**Exposed Pad (UD16 Only):** Exposed pad may be left floating or connected to device ground.

**GND:** Device Ground.

**INHA:** Channel A High Comparator Reference Input. Voltage on this pin is multiplied by the configured range setting to set the  $V_{INA}$  high or rising threshold. Keep within valid voltage range,  $V_{CM}$ , or tie to GND to configure built-in hysteresis where high threshold for  $V_{INA}$  becomes  $INLA + V_{HYS}$  scaled according to the RS pin configuration.

**INHB:** Channel B High Comparator Reference Input. Voltage on this pin is multiplied by the configured range setting to set the  $V_{INB}$  high or rising threshold. Keep within valid voltage range,  $V_{CM}$ , or tie to GND to configure built-in hysteresis where high threshold for  $V_{INB}$  becomes  $INLB + V_{HYS}$  scaled according to the RS pin configuration.

**INLA:** Channel A Low Comparator Reference Input. Voltage on this pin is multiplied by the configured range setting to set the  $V_{INA}$  low or falling threshold. Keep within valid voltage range,  $V_{CM}$ , or tie to GND to configure built-in hysteresis where low threshold becomes  $INHA - V_{HYS}$

scaled according to the RS pin configuration. Otherwise,  $INHA - INLA$  sets the hysteresis of the Channel A comparator. Oscillation will occur if  $INLA > INHA$  unless built-in hysteresis is enabled.

**INLB:** Channel B Low Comparator Reference Input. Voltage on this pin is multiplied by the configured range setting to set the  $V_{INB}$  low or falling threshold. Keep within valid voltage range,  $V_{CM}$ , or tie to GND to configure built-in hysteresis where low threshold becomes  $INHB - V_{HYS}$  scaled according to the RS pin configuration. Otherwise,  $INHB - INLB$  sets the hysteresis of the Channel B comparator. Oscillation will occur if  $INLB > INHB$  unless built-in hysteresis is enabled.

**OUTA:** Channel A Comparator Output. OUTA consists of a high voltage active pull-down and a gated, resistive (500k $\Omega$ ) pull-up to an internally generated supply between 3.5V and 5V depending on input supply voltage. Blocking circuitry at the pin allows the pin to be resistively pulled up to voltages as high as 100V without back conducting onto the internal supply of the part. Polarity with respect to the  $V_{INA}$  pin is configured using the polarity select pin, PSA. OUTA pulls low when the part is in UVLO.

## PIN FUNCTIONS

**OUTB:** Channel B Comparator Output. OUTB consists of a high voltage active pull-down and a gated, resistive (500k $\Omega$ ) pull-up to an internally generated supply between 3.5V and 5V depending on input supply voltage. Blocking circuitry at the pin allows the pin to be resistively pulled up to voltages as high as 100V without back conducting onto the internal supply of the part. Polarity with respect to the  $V_{INB}$  pin is configured using the polarity select pin, PSB. OUTB pulls low when the part is in UVLO.

**PSA:** Channel A Polarity Selection. Connect to REF or a voltage  $>V_{TH}$  to configure comparator output to be inverting with respect to  $V_{INA}$ . Otherwise connect pin to GND to configure comparator output to be noninverting with respect to  $V_{INA}$ .

**PSB:** Channel B Polarity Selection. Connect to REF or a voltage  $>V_{TH}$  to configure comparator output to be inverting with respect to  $V_{INB}$ . Otherwise connect pin to GND to configure comparator output to be noninverting with respect to  $V_{INB}$ .

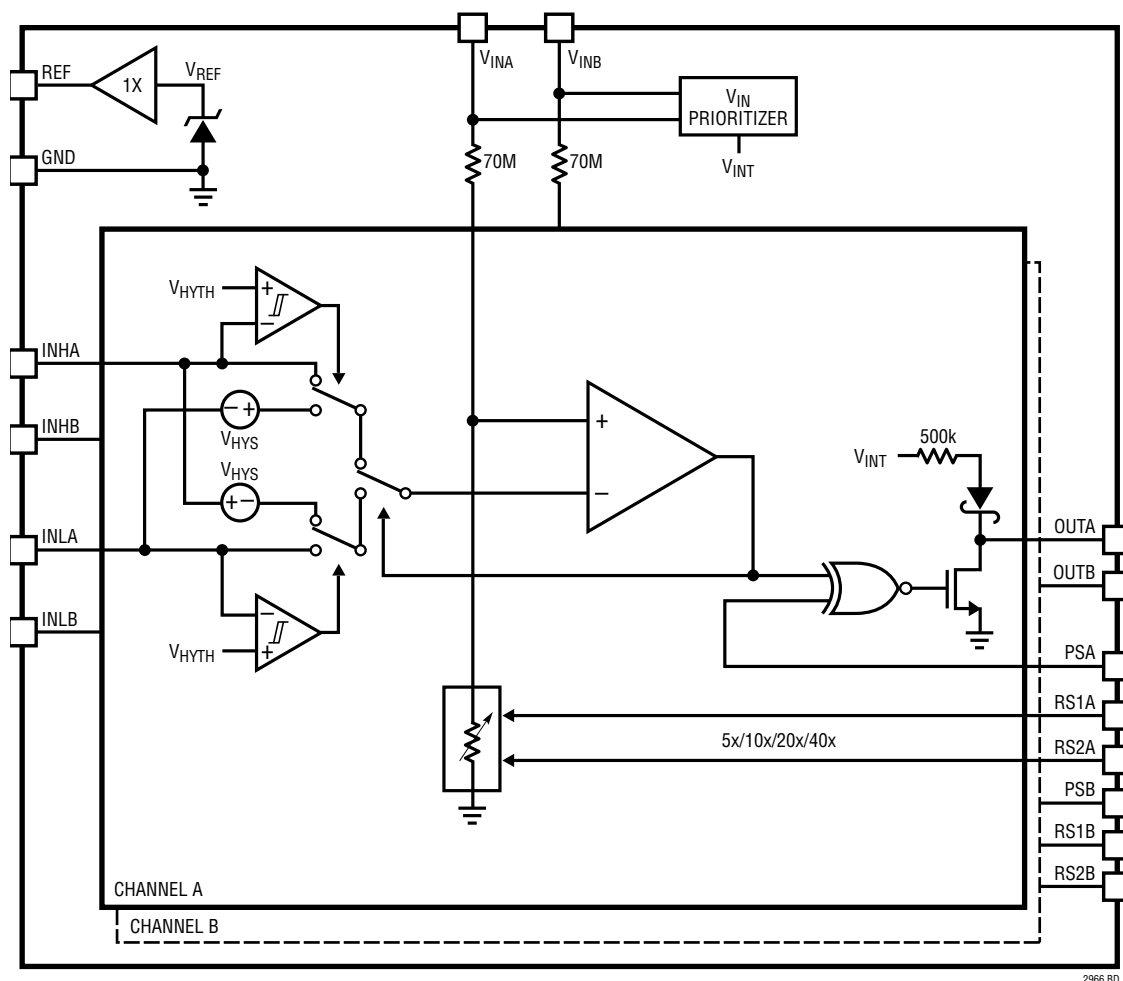
**REF:** Reference Output.  $V_{REF}$  with respect to GND. Use a maximum of 1nF to bypass unless damping resistor is used.

**RS1A-RS2A:** Channel A Range Select Input. RS1A-RS2A select 5x, 10x, 20x or 40x range for Channel A. Connect to REF or GND to configure the pin. (See Table 1)

**RS1B-RS2B:** Channel B Range Select Input. RS1B-RS2B select 5x, 10x, 20x or 40x range for Channel B. Connect to REF or GND to configure the pin. (See Table 1)

**$V_{INA}$ ,  $V_{INB}$ :** Voltage Monitor and Supply Inputs. An internal high value resistive divider is connected to the pin. The greater of  $V_{INA}$  and  $V_{INB}$  is used to generate an internal voltage rail with priority given to  $V_{INA}$ . If both  $V_{INA}$  and  $V_{INB}$  fall below the UVLO threshold minus hysteresis, the outputs are pulled low. If  $V_{INB} < V_{INA} < 1.2V$ , the logic state of the outputs cannot be guaranteed.

# BLOCK DIAGRAM



2966 BD

## OPERATION

The LTC2966 is a micropower dual channel voltage monitor with a 100V maximum operating voltage. Each channel is comprised of an internal high value resistive divider and a comparator with a high voltage output. A reference voltage is provided to allow the thresholds of each channel to be set independently. This configuration has the advantage of being able to monitor very high voltages with very little current draw while threshold configuration is done using low value resistors at low voltages.

The two channels of the LTC2966 provide independent monitoring capabilities for multiple voltages or work in conjunction to set up an undervoltage/overvoltage monitor. Integration of a resistive divider for high voltage sensing makes the LTC2966 a compact and low power solution for generating voltage status signals to a monitoring system.

A built-in buffered reference gives the monitor flexibility to operate independently from a high voltage supply without the requirement of additional low voltage biasing. The reference provides an accurate voltage from which a resistive divider to ground configures the threshold voltage for the internal comparators. In addition, the REF pin can be used as a logic high voltage for the range and polarity select pins.

The input voltage threshold at  $V_{IN}$  is determined by the voltage on the INH and INL pins which are scaled by the attenuation internal resistive divider. In the LTC2966 the attenuation of the internal divider is configured using two range select pins, RS1 and RS2 to select 5x, 10x, 20x or 40x for each channel. Use Table 1 to determine the correct configuration for a desired range setting. The polarity select pins, (PSA/PSB), configure the corresponding OUT pin to be inverting or noninverting with respect to  $V_{IN}$  allowing the part to be configured for monitoring overvoltage and undervoltage conditions with either polarity output.

Table 1.

$V_{IN}$ MONITOR RANGE	RANGE SELECTION	RS1	RS2
1.75V* to 12.25V	5x	L	L
3.5V to 24.5V	10x	H	L
7V to 49V	20x	L	H
14V to 98V	40x	H	H

\*Requires either  $V_{INA}$  or  $V_{INB} > 3.5V$ .

The INH pin determines the high or rising edge threshold for  $V_{IN}$  in each channel. If the monitored voltage connected to  $V_{INA}$  rises to the scaled INHA voltage then the OUT pin is pulled high assuming PSA is ground. Likewise, the INL pin determines the low or falling edge threshold for  $V_{IN}$  in each channel. If  $V_{INA}$  falls to the scaled INLA voltage then the OUT pin is pulled low assuming PSA is ground. The amount of hysteresis referred to  $V_{IN}$  is the difference in voltage between INH and INL scaled according to the RS pin configuration. INH and INL have an allowable voltage range,  $V_{CM}$ . Figure 1 shows the allowable monitor voltage at  $V_{IN}$  for each range as a function of comparator reference input voltage (INL, INH).

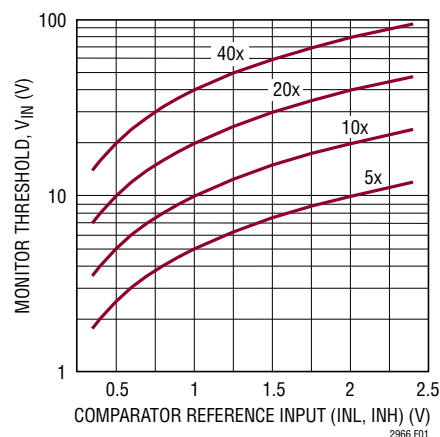
Typically, an external resistive divider biased from REF is used to generate the INH and INL pin voltages. A built-in hysteresis feature requiring only two resistors can be enabled on either the  $V_{IN}$  rising edge by grounding INH or on the falling edge by grounding INL. For example, it is appropriate to ground INH to activate rising edge hysteresis if an accurate falling voltage threshold is required for undervoltage detection. Conversely, it is appropriate to ground INL for falling edge built-in hysteresis if an accurate overvoltage threshold is required. Do not ground both INH and INL. Oscillation occurs if  $V_{INL} > V_{INH}$  unless INH built-in hysteresis is enabled.



## OPERATION

The high voltage OUT pins have the capability to be pulled up to a user defined voltage as high as 100V with an external resistor. The LTC2966 also includes an internal 500k pull-up resistor to an internal voltage between 3.5V and 5V depending on input supply voltage. (See  $V_{OH}$  in Electrical Characteristics) Wire-OR functionality is implemented by connecting OUTA and OUTB with appropriate monitor configuration.

Supply current is drawn from the higher of  $V_{INA}$  or  $V_{INB}$  with priority given to  $V_{INA}$ . If both  $V_{IN}$  pins fall below the UVLO threshold then both OUT pins are pulled low regardless of the PS pin state.



**Figure 1. Monitor Threshold vs Comparator Reference Inputs**

## APPLICATIONS INFORMATION

### Threshold Configuration

Each LTC2966 channel (A/B) monitors the voltage applied to the corresponding  $V_{IN}$  input. A comparator senses the  $V_{IN}$  pin on one of its inputs through the internal resistive divider. The other input is connected to INH/INL that is in turn biased with external resistive dividers off of the REF pin as shown in Figure 2a and 2b. The  $V_{IN}$  rising and falling thresholds are determined by:

$$V_{IN(RISE)} = RANGE \cdot V_{INH}$$

$$V_{IN(FALL)} = RANGE \cdot V_{INL}$$

Where RANGE is the configured range of the internal resistive divider. In order to set the threshold for the LTC2966, choose an appropriate range setting for the desired  $V_{IN}$  voltage threshold such that the INH and INL voltages are within the specified common mode range,  $V_{CM}$ . For example, if a falling threshold of 18V is desired for monitoring a 24V power supply then a range greater than 10x is allowed. However, to maximize the accuracy of the  $V_{IN}$  threshold the smallest acceptable range is used, 10x in this case. To implement 2V of hysteresis referred to  $V_{IN}$  this means:

$$V_{INH} = 2V, V_{INL} = 1.8V$$

With 10x range the  $V_{IN}$  thresholds are:

$$V_{IN(RISE)} = 20V, V_{IN(FALL)} = 18V$$

One possible way to configure the thresholds is by using three resistors to set the voltages on INH and INL. See Figure 2a. The solution for R1, R2 and R3 provides three equations and three unknowns. Maximum resistor size is governed by maximum input leakage current. The maximum input leakage current below 85°C is 1nA. For a maximum error of 1% due to both input currents, the resistive divider current should be at least 100 times the sum of the leakage currents, or 0.2μA.

If in this example, a leakage current error of 0.1% is desired then the total divider resistance is 1.2MΩ which results in a current of 2μA through this network. For  $R_{SUM} = 1.2M\Omega$

$$R_{SUM} = R1 + R2 + R3$$

$$R1 = \frac{(V_{INL} \cdot R_{SUM})}{V_{REF}} = \frac{(1.8V \cdot 1.2M\Omega)}{2.402V} = 899.5k\Omega$$

The closest 1% value is 909kΩ. R2 can be determined from:

$$\begin{aligned} R2 &= \frac{(V_{INH} \cdot R_{SUM})}{V_{REF}} - R1 \\ &= \frac{(2V \cdot 1.2M\Omega)}{2.402V} - 909k\Omega = 90.2k\Omega \end{aligned}$$

The closest 1% value is 90.9kΩ. R3 can be determined from  $R_{SUM}$ :

$$R3 = R_{SUM} - R1 - R2 = 1.2M\Omega - 909k\Omega - 90.9k\Omega = 200.1k\Omega$$

The closest 1% value is 200kΩ. Plugging the standard values back into the equations yields the design values for the  $V_{INH}$  and  $V_{INL}$  voltages:

$$V_{INH} = 2.001V, V_{INL} = 1.819V$$

The corresponding threshold voltages are:

$$V_{IN(RISE)} = 20.01V, V_{IN(FALL)} = 18.19V$$

Another possible way to configure the thresholds is with independent dividers using two resistors per threshold to set the voltages on INH and INL. See Figure 2b. Care must be taken such that the thresholds are not set too close to each other, otherwise the mismatch of the resistors may cause the voltage at INL to be greater than the voltage at INH which may cause the comparator to oscillate.

As in the previous example, if  $R_{SUM} = 1.2M\Omega$  is chosen and the target for  $V_{INL}$  is 1.8V:

$$R_{SUM} = R1 + R2$$

$$R1 = \frac{(V_{INL} \cdot R_{SUM})}{V_{REF}} = \frac{(1.8V \cdot 1.2M\Omega)}{2.402V} = 899.5k\Omega$$

The closest 1% value is 909kΩ. R2 can be determined by:

$$\begin{aligned} R2 &= (V_{REF} - V_{INL}) \cdot \frac{R1}{V_{INL}} \\ &= (2.402V - 1.8V) \cdot \frac{(909k\Omega)}{1.8V} = 304k\Omega \end{aligned}$$

## APPLICATIONS INFORMATION

The closest 1% value is 301k $\Omega$ . Plugging the standard values back into the equation for  $V_{INL}$  yields the design voltage for  $V_{INL}$ :

$$V_{INL} = \frac{(R1 \cdot V_{REF})}{(R1 + R2)} = \frac{(909k\Omega \cdot 2.402V)}{(301k\Omega + 909k\Omega)} = 1.804V$$

At this point in the independent divider example only the values required to set the voltage at INL have been found. Repeat the process for the INH input by substituting the above equations with  $V_{INH}$  for  $V_{INL}$ , R3 for R1, R4 for R2 and  $V_{INH} = 2.0V$ .

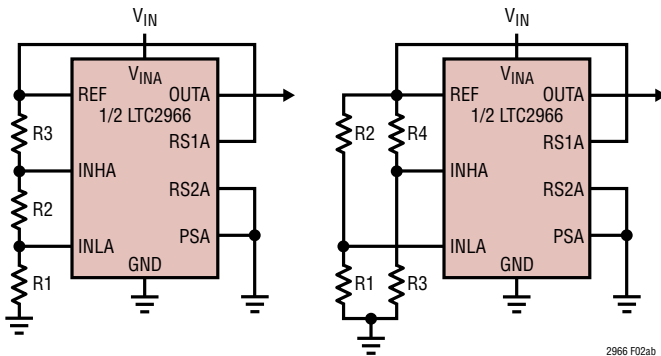


Figure 2a. Three-Resistor Threshold Configuration

Figure 2b. Two-Resistor Threshold Configuration

### Using Built-In Hysteresis

The LTC2966 has the capability of simplifying the threshold configuration such that only two resistors per channel are required. The device pins can be configured to select a built-in hysteresis voltage,  $V_{HYS}$ , which can be applied to either the rising or falling threshold depending on whether the INH or INL pin is grounded. Note that the hysteresis voltage at each range setting remains at a fixed value. Figure 3 introduces examples of each configuration. For example, if INH is biased from an external divider and the INL pin is grounded, then hysteresis is enabled on the low or falling threshold. The low threshold is then  $-V_{HYS}$  relative to the high threshold determined by INH. Figure 3a introduces built-in hysteresis on the rising edge because INH is pulled to ground. A two-resistor network, R1 and R2, is used to set the voltage on INL using:

$$\frac{R2}{R1} = \frac{V_{REF}}{V_{INL}} - 1$$

Using built-in hysteresis, the  $V_{IN}$  thresholds are:

$$V_{IN(RISE)} = RANGE \cdot (INL + V_{HYS})$$

$$V_{IN(FALL)} = RANGE \cdot INL$$

Figure 3b introduces built-in hysteresis on the falling edge because INL is pulled to ground. Similarly, a two-resistor network, R3 and R4, is used to set the voltage on INH using:

$$\frac{R4}{R3} = \frac{V_{REF}}{V_{INH}} - 1$$

Using built-in hysteresis the  $V_{IN}$  thresholds are:

$$V_{IN(RISE)} = RANGE \cdot INH$$

$$V_{IN(FALL)} = RANGE \cdot (INH - V_{HYS})$$

Consider  $V_{INH} = 2V$  with built-in hysteresis activated on the falling edge. For 10x range, 1.1% falling hysteresis is obtained. If a larger percentage of hysteresis is desired then  $V_{INH}$  is alternatively set to 1V and the range is selected to be 20x to obtain the same  $V_{IN}$  threshold but with 2.2% falling hysteresis. The amount of built-in hysteresis is scaled according to Table 2. If more hysteresis is needed then it is implemented in the external resistive divider as described in the Threshold Configuration section.

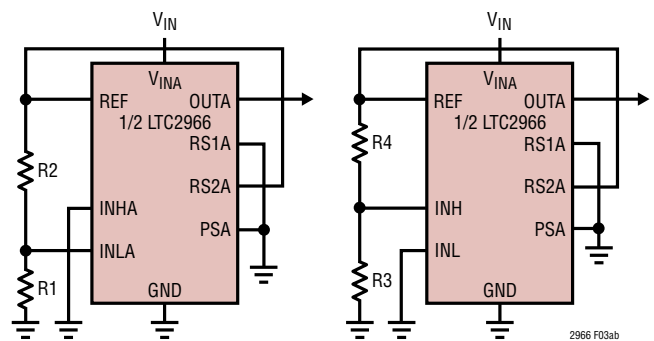


Figure 3a. Rising Edge Built-In Hysteresis by Grounding INH

Figure 3b. Falling Edge Built-In Hysteresis by Grounding INL

Table 2. Built-In Hysteresis Voltage vs Range

RANGE	$V_{IN}$ REFERRED BUILT-IN HYSTERESIS
5x	110mV
10x	220mV
20x	440mV
40x	880mV

## APPLICATIONS INFORMATION

### Error Analysis

$V_{IN}$  thresholds are subject to the following errors:

- REF Voltage Variation ( $\Delta V_{REF}$ )
- Comparator Offset ( $V_{OS}$ )
- Internal Divider Range Error ( $A_{VERR}$ )
- External Resistive Divider Error ( $A_{XERR}$ )

The effect these errors have on the  $V_{IN}$  threshold is expressed by:

$$V_{ERR} = \text{RANGE} \cdot \left[ \pm V_{OS} \pm \Delta V_{REF} \cdot \frac{V_{INH(L)}}{V_{REF}} \pm V_{INH(L)} \cdot A_{XERR} \right] \\ \pm \text{RANGE} \cdot A_{VERR} \cdot V_{INH(L)}$$

$$A_{XERR} = 2 \cdot \frac{\text{TOLERANCE}}{100} \cdot \left( 1 - \frac{V_{INH(L)}}{V_{REF}} \right)$$

External divider error is determined by the percentage tolerance values of the resistors. If 1% tolerance resistors are used in the external divider then there is a 2% worst-case voltage error associated with it. The effects of comparator offset and  $V_{REF}$  voltage are uncorrelated with each other. Therefore, a Root-Sum-Square can be applied to the error voltage referred to  $V_{IN}$ . Using the example from Threshold Configuration and assuming 1% resistors implement the external resistive divider, the falling  $V_{IN}$  threshold of approximately 18V has an error tolerance of:

$$V_{ERR(REF)} = (\text{RANGE}) \left( \pm \Delta V_{REF} \cdot \frac{V_{INL}}{V_{REF}} \right) \\ = (10) \cdot \left( \pm 24\text{mV} \cdot \frac{1.8\text{V}}{2.402\text{V}} \right) = \pm 180\text{mV}$$

$$V_{ERR(EXT)} = (\text{RANGE}) \left( \pm V_{INL} \cdot 2 \cdot 0.01 \cdot \left( 1 - \frac{V_{INL}}{V_{REF}} \right) \right) \\ = (10) \cdot (\pm 1.8\text{V} \cdot 0.005) = \pm 90\text{mV}$$

$$V_{ERR(VOS)} = (\text{RANGE}) (\pm \Delta V_{OS}) = (10) \cdot (\pm 3\text{mV}) = \pm 30\text{mV}$$

$$V_{ERR(RS)} = (\text{RANGE}) (\pm A_{VERR}) (\pm V_{INL}) \\ = (10) \cdot (\pm 0.004) \cdot (1.8\text{V}) = \pm 72\text{mV}$$

$$V_{ERR} = \sqrt{V_{ERR(REF)}^2 + V_{ERR(EXT)}^2 + V_{ERR(VOS)}^2 + V_{ERR(RS)}^2} \\ = \sqrt{(\pm 180\text{mV})^2 + (\pm 90\text{mV})^2 + (\pm 30\text{mV})^2 + (\pm 72\text{mV})^2} \\ = \pm 216\text{mV}$$

The actual  $V_{IN}$  falling threshold has an error tolerance of  $\pm 216\text{mV}$  or  $\pm 1.2\%$ .

### Improving Threshold Accuracy

The biggest threshold error terms are:

- External Resistive Divider Accuracy
- REF Voltage Variation

Even using 1% tolerance resistors, external resistive divider accuracy still accounts for as much as  $\pm 2\%$  threshold error while REF voltage variation accounts for  $\pm 1\%$  threshold error. In order to minimize these threshold error terms, an external reference can be used to set the thresholds for INH/INL as shown in Figure 4. An LT6656-2.048 has an initial accuracy of 0.05% and provides bias via the 0.1% resistive divider network for INH and INL. It is biased off of the LTC2966 REF pin. The threshold error tolerance is calculated using the method described in the Typical Applications section with  $\Delta V_{REF} = \pm 1.024\text{mV}$  given the initial accuracy of the LT6656 2.048V output and using 0.1% tolerance resistors for the external divider.

$$V_{ERR(REF)} = (\text{RANGE}) \left( \pm \Delta V_{REF} \cdot \frac{V_{INL}}{V_{REF}} \right) \\ = (10) \cdot \left( \pm 1.024\text{mV} \cdot \frac{1.8\text{V}}{2.048\text{V}} \right) = \pm 9\text{mV}$$

$$V_{ERR(EXT)} = (\text{RANGE}) \left( \pm V_{INL} \cdot 2 \cdot 0.001 \cdot \left( 1 - \frac{V_{INL}}{V_{REF}} \right) \right) \\ = (10) \cdot (\pm 1.8\text{V} \cdot 0.0005) = \pm 9\text{mV}$$

$$V_{ERR(VOS)} = (\text{RANGE}) (\pm \Delta V_{OS}) = (10) \cdot (\pm 3\text{mV}) = \pm 30\text{mV}$$

$$V_{ERR(RS)} = (\text{RANGE}) (\pm A_{VERR}) (\pm V_{INL}) \\ = (10) \cdot (\pm 0.004) \cdot (1.8\text{V}) = \pm 72\text{mV}$$

$$V_{ERR} = \sqrt{V_{ERR(REF)}^2 + V_{ERR(EXT)}^2 + V_{ERR(VOS)}^2 + V_{ERR(RS)}^2} \\ = \sqrt{(\pm 9\text{mV})^2 + (\pm 9\text{mV})^2 + (\pm 30\text{mV})^2 + (\pm 72\text{mV})^2} \\ = \pm 79\text{mV}$$

The resulting  $V_{IN}$  threshold error is reduced to  $\pm 0.44\%$  from  $\pm 1.2\%$  in the previous error analysis example.



Figure 5 shows the proper technique for disabling a channel. Table 4 summarizes the correct connections. Correctly disabling an unused channel prevents its comparator output from chattering and introducing unwanted noise in the system.

<b>PIN</b>	<b>CONNECT TO</b>
$V_{IN}$	GND
INH	REF
INL	GND
RS1	GND or REF
RS2	GND or REF
PS	GND or REF
OUT	Open



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## APPLICATIONS INFORMATION

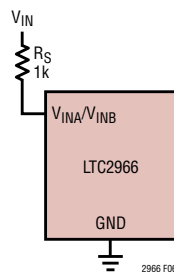


Figure 6. Hot Swap Protection

## High Voltage Pin Creepage/Clearance Options

Appropriate spacing between component lead traces is critical to avoid flashover between conductors. There are multiple industry and safety standards that have different spacing requirements depending on factors such as operating voltage, presence of conformal coat, elevation, etc. The LTC2966 is available in a 20-lead SW package which offers pin-to-pin clearance of at least 0.76mm (0.03in) to satisfy high voltage external component lead specifications for standards such as the UL60950 and IPC2221. The package incorporates unconnected pins between all adjacent high voltage and low voltage pins to maximize PC board trace clearance. For voltages >30V the SW should be used, otherwise the smaller QFN is sufficient when clearance is not an issue. For more information, refer to the printed circuit board design standards described in IPC2221 and UL60950.

## Voltage Reference

The REF pin is a buffered reference with a voltage of  $V_{REF}$  referenced to GND. A bypass capacitor up to 1000pF in value can be driven by the REF pin directly. Larger capacitances require a series resistance to dampen the transient response as shown in Figure 7A. If a resistive divider is already present then the bypass capacitor can be connected to the INH or INL pin as shown in Figure 7B. Figure 7C shows the resistor value required for different capacitor values to achieve critical damping. Bypassing the reference can help prevent false tripping of the comparators by preventing glitches on the INH/INL pins. Figure 8 shows the reference load transient response. Figure 9 shows the reference line transient response. If there is a decoupling capacitor on the INH/INL pin the time constant formed by the RC network should be considered. Use a capacitor with a compatible voltage rating.

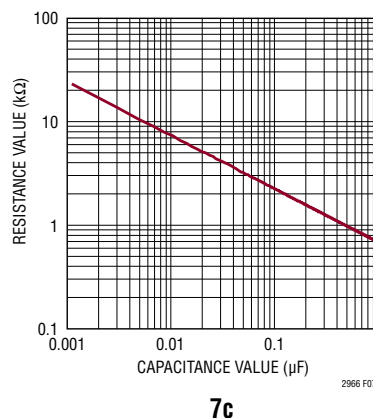
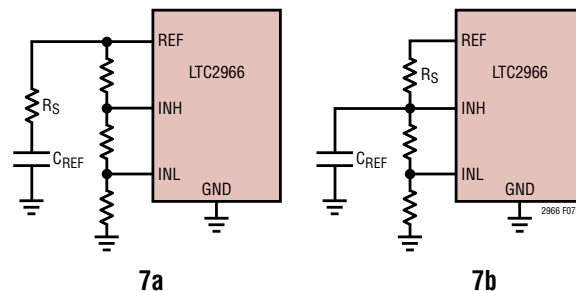
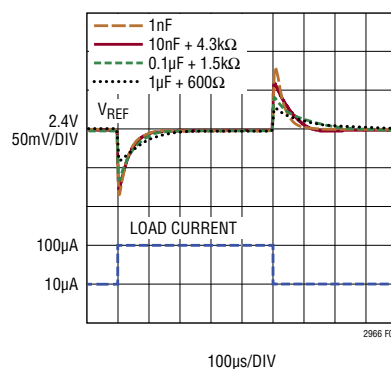
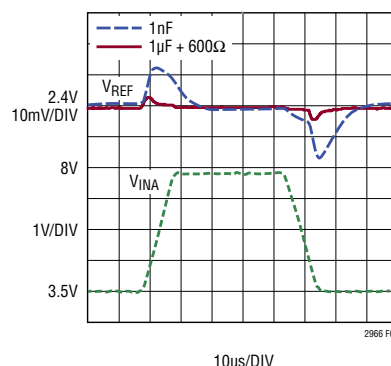


Figure 7. Using Series Resistance to Dampen REF Transient Response

Figure 8.  $V_{REF}$  Load TransientFigure 9.  $V_{REF}$  Line Transient

## TYPICAL APPLICATIONS

### 48V UV/OV Monitor

The circuit in Figure 10 monitors a single 48V supply and is configured for UV/OV window detection. Channel A is used to monitor undervoltage conditions where the 36V threshold is determined by 1.8V at INLA scaled by 20x. Channel B is used to monitor overvoltage conditions where the 72V threshold is determined by the same 1.8V at INHB with 40x range. UV is pulled high to indicate an undervoltage condition when the supply drops below the UV threshold. Therefore PSA is pulled to REF to obtain the correct polarity on OUTA. OV is pulled high when the supply rises above the OV threshold which means PSB is pulled to ground to obtain the appropriate output polarity. Connecting INHA and INLB to ground enables internal hysteresis for each channel in the appropriate direction and reduces the number of external components.

### ±15V Undervoltage Monitor

The LTC2966 can be used to monitor a positive and a negative supply simultaneously. In the circuit shown in Figure 11, Channel B is used to monitor the –15V supply by connecting  $V_{INB}$ 's internal resistor divider to REF and configuring to 5x range. The voltage at the  $V_{IN}$  sensing input of the Channel B comparator is fixed at 480mV. When the –15V supply is undervoltage  $INHB > 480mV$  and OUTB is pulled low because PSB is connected to ground. As the negative supply comes into regulation the comparator monitors the INHB pin to detect when its voltage crosses 480mV corresponding to –14.3V.  $\overline{UVB}$  is released indicating that there is no longer an undervoltage condition. As the negative supply drops out of regulation the comparator monitors the INLB pin to detect when its voltage crosses 480mV, corresponding to –13.6V due to the external divider

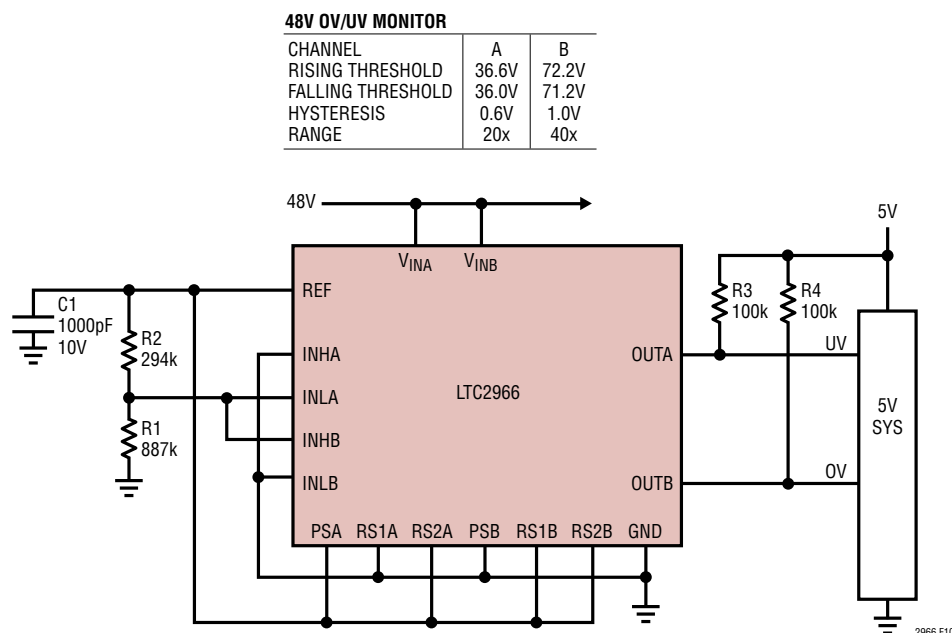


Figure 10. Use Range Selection and Built-In Hysteresis to Minimize External Components



## TYPICAL APPLICATIONS

gain.  $\overline{\text{UVB}}$  is pulled low after the comparator detects the threshold crossing to indicate an undervoltage condition. Channel A is configured to monitor for an undervoltage condition on the 15V supply by pulling  $\overline{\text{UVA}}$  low when the positive supply drops below 13.6V.

### –48V UV/OV Voltage Monitor

In the circuit shown in Figure 12, the LTC2966 is configured as a –48V UV/OV monitor by referencing the GND pin to the negative supply. R1 through R4 configure the UV and

OV thresholds, where channel A and B are configured similarly to the 48V UV/OV monitor circuit in Figure 10. Hysteresis for each comparator is implemented by the external resistor network. High voltage OUT pins allow a pair of 4N25 opto-couplers to be used in translating the status signals for the 5V system. R5, R6, R7 and R8 set the maximum current through the optos to be approximately 4.2mA. If an exposed pad is present it should be tied to the GND pin or left open.

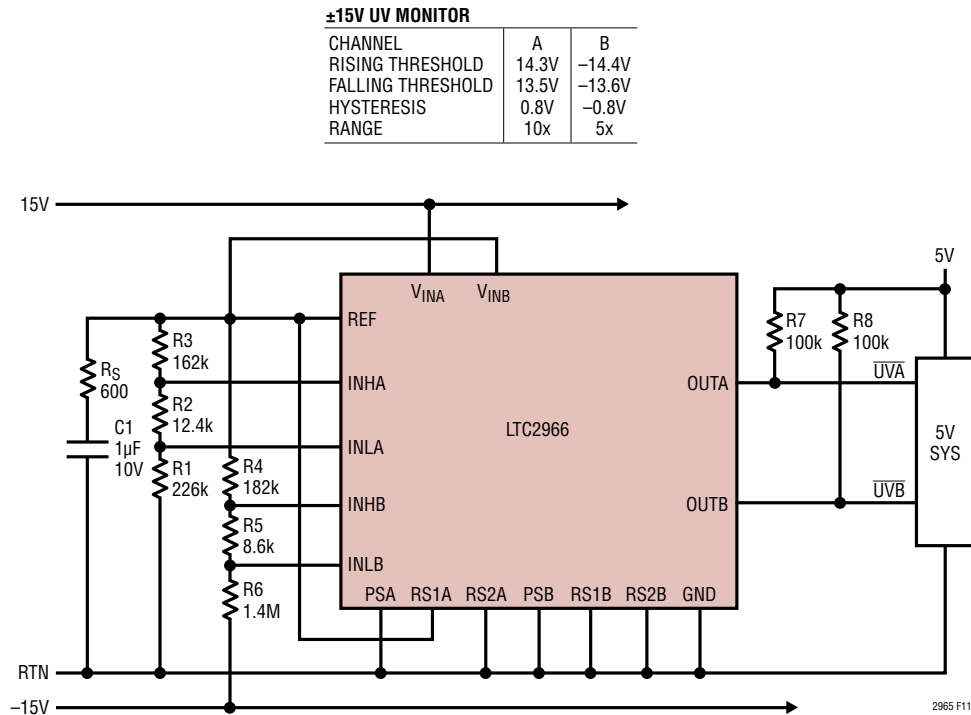


Figure 11. Dual Polarity Voltage Monitoring

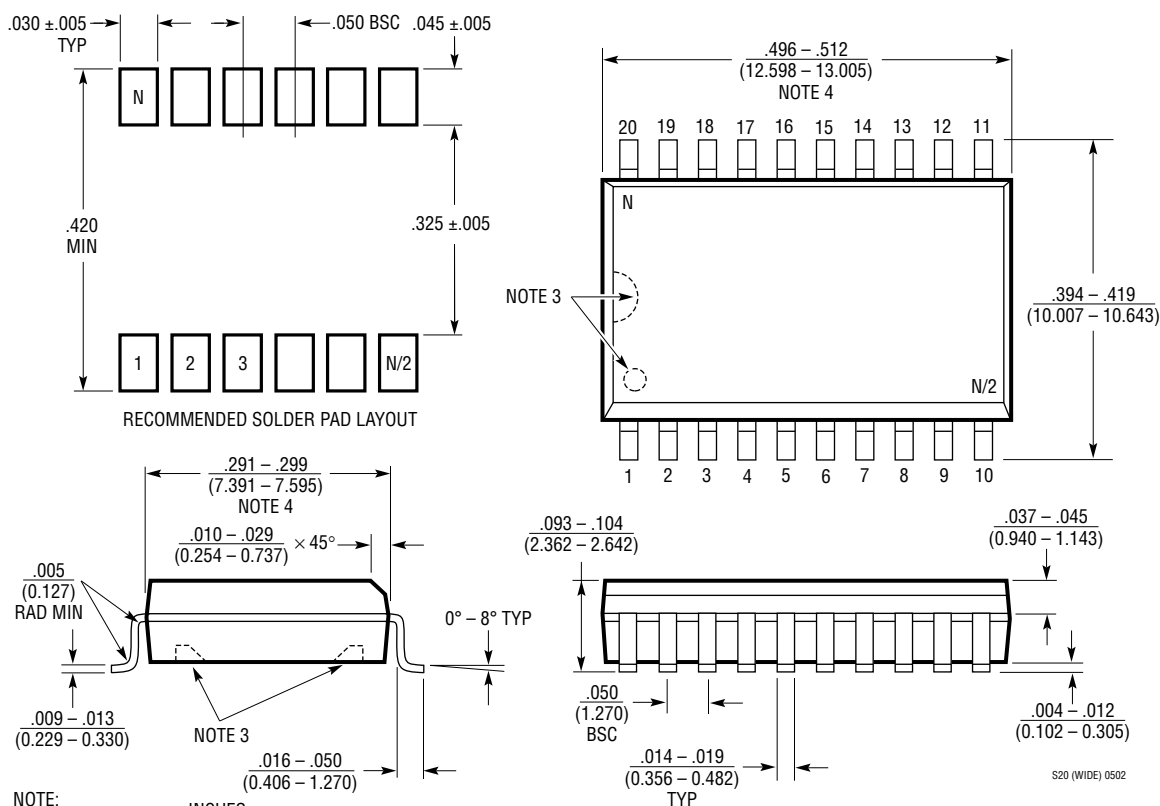




## PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/product/LTC2966#packaging> for the most recent package drawings.

### SW Package 20-Lead Plastic Small Outline (Wide .300 Inch) (Reference LTC DWG # 05-08-1620)



## REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	09/15	Fixed typos	1, 3, 10, 11, 12, 15
B	03/16	Added ABS Max Rating for INHA, INHB, INLA and INLB pins	2
C	08/17	Corrected example error threshold calculations	12

## TYPICAL APPLICATION

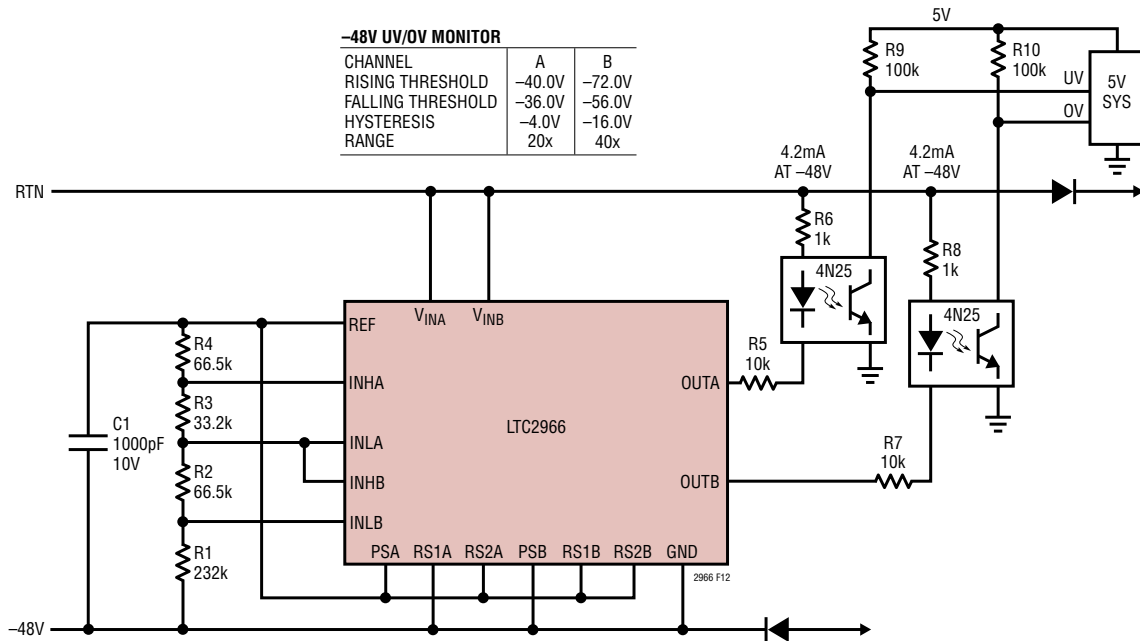


Figure 12. Monitoring Negative Voltage with Isolation

## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
<a href="#">LTC1326</a>	Micropower Triple Supply Monitor for 5V/2.5V, 3.3V and ADJ	4.725V, 3.118V, 1V Threshold ( $\pm 0.75\%$ ) and ADJ
<a href="#">LTC1440/LTC1441/LTC1442</a>	Ultralow Power Single/Dual Comparator with Reference	Adjustable Hysteresis, 3mm $\times$ 3mm $\times$ 0.75mm DFN Package
<a href="#">LTC1726/LTC1727/LTC1728</a>	Micropower Triple Supply Monitor	Adjustable Reset and Watchdog Timeouts
<a href="#">LTC1985</a>	Micropower Triple Supply Monitor with Push-Pull Reset Output	5-Lead SOT-23 Package
<a href="#">LTC2900/LTC2901/LTC2902</a>	Programmable Quad Supply Monitor	Adjustable Reset, Watchdog Timer and Tolerance, 10-Lead MSOP and DFN Packages
<a href="#">LTC2903</a>	Precision Quad Supply Monitor	6-Lead SOT-23 and DFN Packages
<a href="#">LTC2904/LTC2905/LTC2906/LTC2907</a>	Three-State Programmable Precision Dual Supply Monitor	8-Lead SOT-23 and DFN Packages
<a href="#">LTC2908</a>	Precision Six-Supply Monitor (Four Fixed and Two Adjustable)	8-Lead TSOT-23 and DFN Packages
<a href="#">LTC2909/LTC2919</a>	Precision Triple/Dual Input UV, OV and Negative Voltage Monitor	Shunt Regulated $V_{CC}$ Pin, Adjustable Threshold and Reset
<a href="#">LTC2910</a>	Octal Positive/Negative Voltage Monitor	Separate $V_{CC}$ Pin, Eight Inputs, Up to Two Negative Monitors Adjustable Reset Timer, 16-Lead SSOP and DFN Packages
<a href="#">LTC2912/LTC2913/LTC2914</a>	Single/Dual/Quad UV and OV Voltage Monitors	Separate $V_{CC}$ Pin, Adjustable Reset Timer
<a href="#">LTC2915/LTC2916/LTC2917/LTC2918</a>	Single Voltage Supervisors with 27 Pin-Selectable Thresholds	Manual Reset and Watchdog Functions, 8- and 10-Lead TSOT-23, MSOP and DFN Packages
<a href="#">LTC2965</a>	100V Micropower Single Voltage Monitor	3.5V to 98V Monitoring Range, 3.5V to 100V Operating Range, 7 $\mu$ A Quiescent Current
<a href="#">LTC2960</a>	36V Nano-Current Two Input Voltage Monitor	36V, 850nA Quiescent Current, 2mm $\times$ 2mm 8-Lead DFN and TSOT-23 Packages
<a href="#">LT6700</a>	Micropower Dual Comparator with 400mV Reference	SOT-23, 2mm $\times$ 3mm DFN Package

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