



## Features

- ## Functional Description

The eight input and output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) are placed in a high-impedance state when the device is deselected (CE<sub>1</sub> HIGH or CE<sub>2</sub> LOW), the outputs are disabled ( $\overline{\text{OE}}$  HIGH), or a write operation is in progress ( $\overline{\text{CE}}$ <sub>1</sub> LOW and CE<sub>2</sub> HIGH and  $\overline{\text{WE}}$  LOW). See the [Truth Table – CY62158H on page 11](#) for a complete description of read and write modes.

The diagram illustrates the internal architecture of a 1M x 8 RAM array. It features a central **1M x 8 RAM ARRAY** block. Address lines **A0** through **A9** are connected to a **ROW DECODER**, which provides row selection to the RAM array. Address lines **A10** through **A19** are connected to a **COLUMN DECODER**, which provides column selection to the RAM array. The RAM array's output is processed by **SENSE AMPLIFIERS** and then an **ECC DECODER**. The ECC decoder's output is connected to **DATA<sub>IN</sub> DRIVERS**, which drive the **I/O<sub>0</sub>-I/O<sub>7</sub>** bus. Error correction is handled by an **ECC ENCODER** that takes data from the **DATA<sub>IN</sub> DRIVERS** and feeds it back into the RAM array. Control signals include **WE** (Write Enable) and **OE** (Output Enable), which are combined with address lines **A10** and **A11** via AND gates to generate **CE<sub>2</sub>** and **CE<sub>1</sub>** chip enable signals.

**Cypress Semiconductor Corporation** • 198 Champion Court • San Jose, CA 95134-1709 • 408-943-2600  
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## Contents

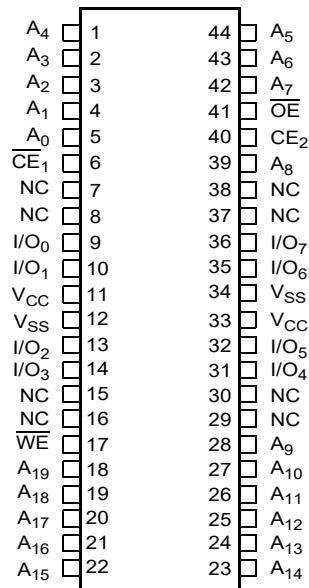
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## Product Portfolio

Product	Features and Options (see <a href="#">Pin Configurations – CY62158H</a> )	Range	V <sub>CC</sub> Range (V)	Speed (ns)	Power Dissipation			
					Operating I <sub>CC</sub> (mA)		Standby I <sub>SB2</sub> (μA)	
					f = f <sub>max</sub>			
					Typ <sup>[3]</sup>	Max	Typ <sup>[3]</sup>	Max
CY62158H	Dual Chip Enable	Industrial	4.5 V–5.5 V	45	29	36	5.5	16

## Pin Configurations – CY62158H

Figure 1. 44-pin TSOP II Pinout <sup>[4]</sup>



### Notes

- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = 5 V (for V<sub>CC</sub> range of 4.5 V–5.5 V), T<sub>A</sub> = 25 °C.
- NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... -65 °C to + 150 °C

Ambient temperature  
with power applied ..... -55 °C to + 125 °C

Supply voltage to ground potential ..... -0.5 V to  $V_{CC} + 0.5$  V

DC voltage applied to outputs  
in High Z state<sup>[5]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

DC input voltage<sup>[5]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage  
(MIL-STD-883, Method 3015) ..... >2001 V

Latch-up current ..... >140 mA

## Operating Range

Grade	Ambient Temperature	$V_{CC}$ <sup>[6]</sup>
Industrial	-40 °C to +85 °C	4.5 V to 5.5 V

## DC Electrical Characteristics

Over the Operating Range of -40 °C to 85 °C

Parameter	Description		Test Conditions	45 ns			Unit
				Min	Typ <sup>[7]</sup>	Max	
$V_{OH}$	Output HIGH voltage	4.5 V to 5.5 V	$V_{CC} = \text{Min}, I_{OH} = -1.0$ mA	2.4	—	—	V
		4.5 V to 5.5 V	$V_{CC} = \text{Min}, I_{OH} = -0.1$ mA	$V_{CC} - 0.4$ <sup>[8]</sup>	—	—	
$V_{OL}$	Output LOW voltage	4.5 V to 5.5 V	$V_{CC} = \text{Min}, I_{OL} = 2.1$ mA	—	—	0.4	V
$V_{IH}$ <sup>[5]</sup>	Input HIGH voltage	4.5 V to 5.5 V	—	2.2	—	$V_{CC} + 0.5$	V
$V_{IL}$ <sup>[5]</sup>	Input LOW voltage	4.5 V to 5.5 V	—	-0.5	—	0.8	V
$I_{IX}$	Input leakage current	$GND \leq V_{IN} \leq V_{CC}$		-1.0	—	+1.0	μA
$I_{OZ}$	Output leakage current	$GND \leq V_{OUT} \leq V_{CC}$ , Output disabled		-1.0	—	+1.0	μA
$I_{CC}$	$V_{CC}$ operating supply current	$V_{CC} = \text{Max}, I_{OUT} = 0$ mA, CMOS levels	$f = 22.22$ MHz (45 ns)	—	29.0	36.0	mA
			$f = 1$ MHz	—	7.0	9.0	
$I_{SB1}$ <sup>[9]</sup>	Automatic power down current – CMOS inputs; $V_{CC} = 4.5$ to 5.5 V	$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V, $V_{IN} \leq 0.2$ V, $f = f_{\text{max}}$ (address and data only),  $f = 0$ ( $\overline{OE}$ , and $\overline{WE}$ ), $V_{CC} = V_{CC(\text{max})}$		—	5.5	16.0	μA
$I_{SB2}$ <sup>[9]</sup>	Automatic power down current – CMOS inputs; $V_{CC} = 4.5$ to 5.5 V	$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, or $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, $f = 0$ , $V_{CC} = V_{CC(\text{max})}$	25 °C <sup>[10]</sup>	—	5.5	6.5	μA
			40 °C <sup>[10]</sup>	—	6.3	8.0	
			70 °C <sup>[10]</sup>	—	8.4	12.0	
			85 °C	—	12.0 <sup>[10]</sup>	16.0	

### Notes

5.  $V_{IL(\text{min})} = -2.0$  V and  $V_{IH(\text{max})} = V_{CC} + 2$  V for pulse durations of less than 20 ns.

6. Full Device AC operation assumes a 100 μs ramp time from 0 to  $V_{CC(\text{min})}$  and 200 μs wait time after  $V_{CC}$  stabilization.

7. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = 5$  V (for  $V_{CC}$  range of 4.5 V–5.5 V),  $T_A = 25$  °C.

8. This parameter is guaranteed by design and not tested.

9. Chip enables ( $\overline{CE}_1$  and  $CE_2$ ) must be tied to CMOS levels to meet the  $I_{SB1}$  /  $I_{SB2}$  /  $I_{CCDR}$  spec. Other inputs can be left floating.

10. The  $I_{SB2}$  limits at 25 °C, 40 °C, 70 °C and typical limit at 85 °C are guaranteed by design and not 100% tested.

## Capacitance

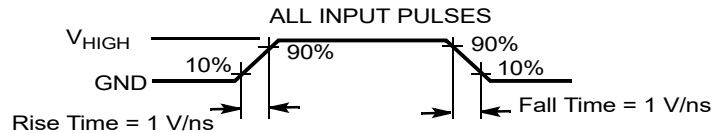
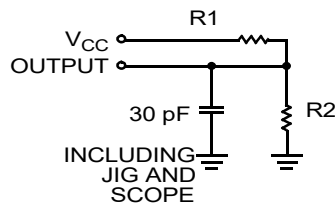
Parameter <sup>[11]</sup>	Description	Test Conditions	Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = V_{CC(\text{typ})}$	10	pF
$C_{OUT}$	Output capacitance		10	pF

## Thermal Resistance

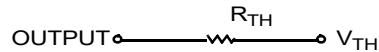
Parameter <sup>[11]</sup>	Description	Test Conditions	44-pin TSOP II	Unit
$\Theta_{JA}$	Thermal resistance (junction to ambient)	Still air, soldered on a $3 \times 4.5$ inch, four-layer printed circuit board	66.93	$^\circ\text{C/W}$
$\Theta_{JC}$	Thermal resistance (junction to case)		13.09	$^\circ\text{C/W}$

## AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Parameters	5.0 V	Unit
R1	1800	$\Omega$
R2	990	$\Omega$
$R_{TH}$	639	$\Omega$
$V_{TH}$	1.77	V
$V_{HIGH}$	5.0	V

### Note

11. Tested initially and after any design or process changes that may affect these parameters.

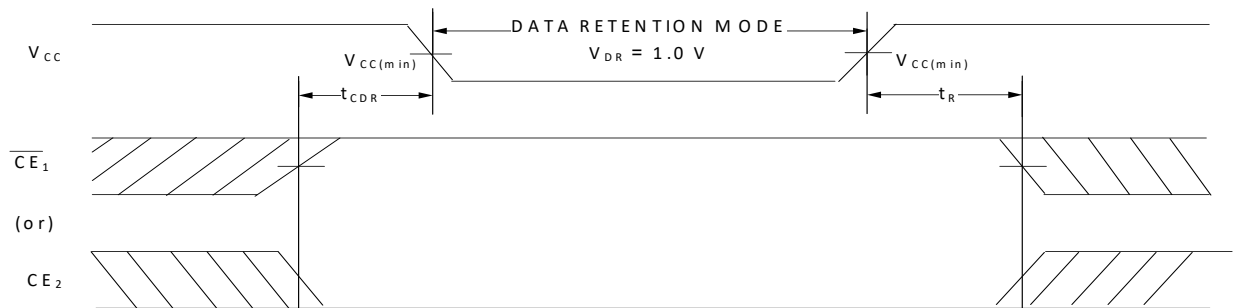
## Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ <sup>[12]</sup>	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		1.0	–	–	V
$I_{CCDR}$ <sup>[13, 14]</sup>	Data retention current	$1.2\text{ V} \leq V_{CC} \leq 2.2\text{ V}$ , $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	7.0	26.0	$\mu\text{A}$
		$2.2\text{ V} < V_{CC} \leq 3.6\text{ V}$ or $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ , $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	5.5	16.0	$\mu\text{A}$
$t_{CDR}$ <sup>[15]</sup>	Chip deselect to data retention time		0	–	–	–
$t_R$ <sup>[15, 16]</sup>	Operation recovery time		45	–	–	ns

## Data Retention Waveform

Figure 3. Data Retention Waveform



### Notes

12. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = 1.8\text{ V}$  (for  $V_{CC}$  range of 1.65 V–2.2 V),  $V_{CC} = 3\text{ V}$  (for  $V_{CC}$  range of 2.2 V–3.6 V), and  $V_{CC} = 5\text{ V}$  (for  $V_{CC}$  range of 4.5 V–5.5 V),  $T_A = 25^\circ\text{C}$ .
13. Chip enables ( $\overline{CE}_1$  and  $CE_2$ ) must be tied to CMOS levels to meet the  $I_{SB1}$  /  $I_{SB2}$  /  $I_{CCDR}$  spec. Other inputs can be left floating.
14.  $I_{CCDR}$  is guaranteed only after device is first powered up to  $V_{CC(min)}$  and brought down to  $V_{DR}$ .
15. These parameters are guaranteed by design.
16. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 100\text{ }\mu\text{s}$  or stable at  $V_{CC(min)} \geq 100\text{ }\mu\text{s}$ .

## Switching Characteristics

Parameter <sup>[17]</sup>	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t <sub>RC</sub>	Read cycle time	45.0	–	ns
t <sub>AA</sub>	Address to data valid	–	45.0	ns
t <sub>OHA</sub>	Data hold from address change	10.0	–	ns
t <sub>ACE</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to data valid / $\overline{CE}$ LOW to ERR valid	–	45.0	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to data valid / $\overline{OE}$ LOW to ERR valid	–	22.0	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[18, 19, 20]</sup>	5.0	–	ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[18, 19, 20, 21]</sup>	–	18.0	ns
t <sub>LZCE</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to Low Z <sup>[18, 19, 20]</sup>	10.0	–	ns
t <sub>HZCE</sub>	$\overline{CE}_1$ HIGH and CE <sub>2</sub> LOW to High Z <sup>[18, 19, 20, 21]</sup>	–	18.0	ns
t <sub>PU</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to power-up <sup>[20]</sup>	0	–	ns
t <sub>PD</sub>	$\overline{CE}_1$ HIGH and CE <sub>2</sub> LOW to power-down <sup>[20]</sup>	–	45.0	ns
Write Cycle <sup>[22, 23]</sup>				
t <sub>WC</sub>	Write cycle time	45.0	–	ns
t <sub>SCE</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to write end	35.0	–	ns
t <sub>AW</sub>	Address setup to write end	35.0	–	ns
t <sub>HA</sub>	Address hold from write end	0	–	ns
t <sub>SA</sub>	Address setup to write start	0	–	ns
t <sub>PWE</sub>	$\overline{WE}$ pulse width	35.0	–	ns
t <sub>SD</sub>	Data setup to write end	25.0	–	ns
t <sub>HD</sub>	Data hold from write end	0	–	ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[18, 19, 20, 21]</sup>	–	18.0	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[18, 19, 20]</sup>	10.0	–	ns

### Notes

17. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for  $V_{CC} \geq 3$  V) and  $V_{CC}/2$  (for  $V_{CC} < 3$  V), and input pulse levels of 0 to 3 V (for  $V_{CC} \geq 3$  V) and 0 to  $V_{CC}$  (for  $V_{CC} < 3$  V). Test conditions for the read cycle use output loading shown in AC Test Loads and Waveforms section, unless specified otherwise.

18. At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.

19. Tested initially and after any design or process changes that may affect these parameters.

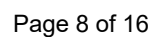
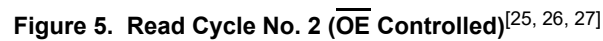
20. These parameters are guaranteed by design and are not tested.

21.  $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high impedance state.

22. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE}_1 = V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.

23. The minimum write cycle pulse width for Write cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  Low) should be equal to the sum of  $t_{HZWE}$  and  $t_{SD}$ .

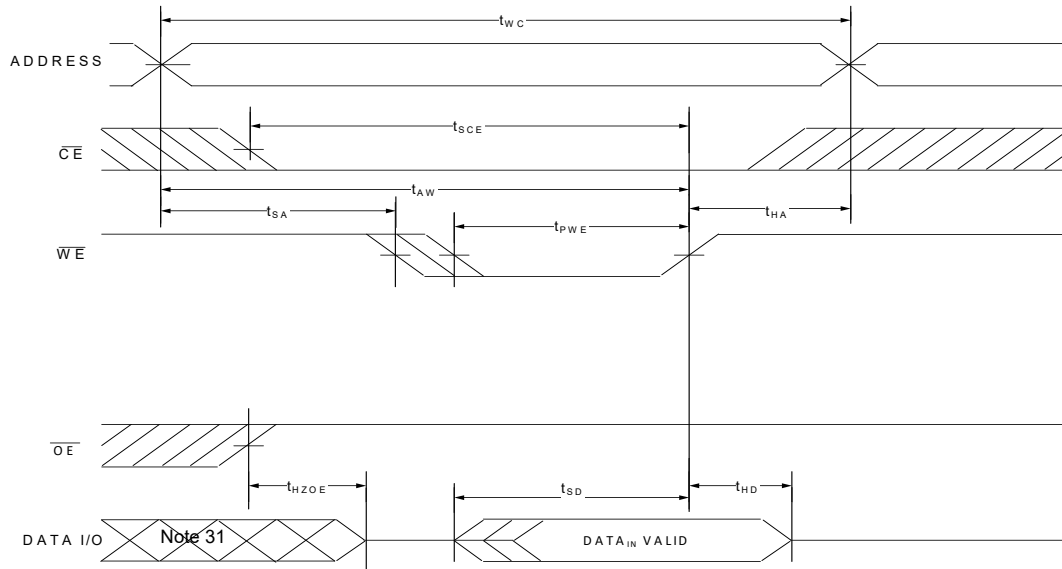
**Figure 4. Read Cycle No. 1 (Address Transition Controlled)<sup>[24, 25]</sup>**





## Switching Waveforms (continued)

**Figure 6. Write Cycle No. 1 ( $\overline{WE}$  Controlled)** [28, 29, 30]



### Notes

28. For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.

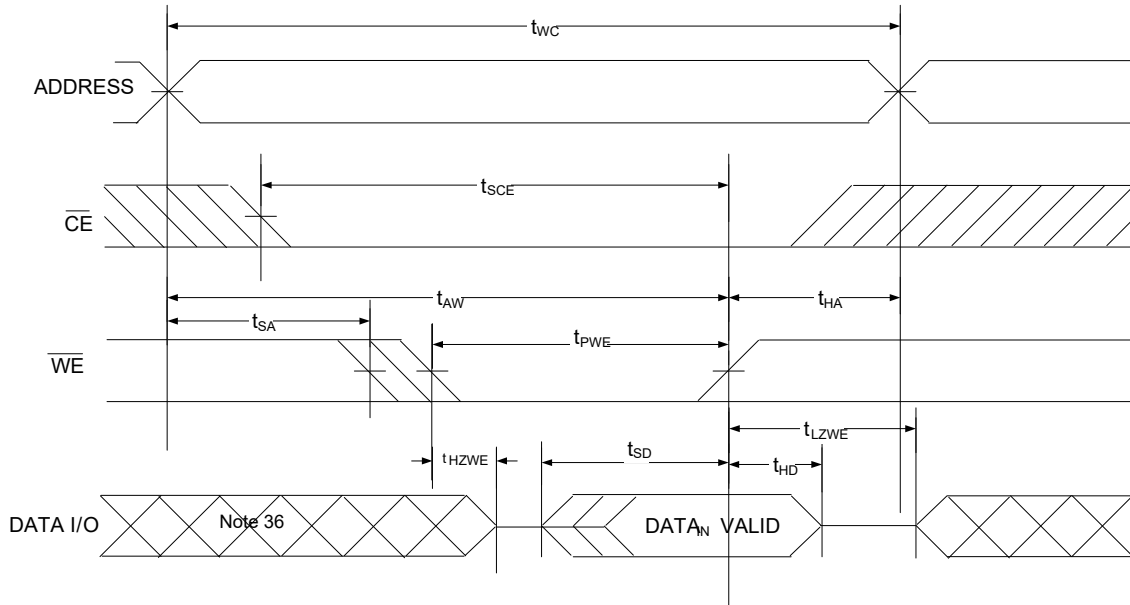
29. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE}_1 = V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.

30. Data I/O is in the high-impedance state if  $\overline{CE} = V_{IH}$ , or  $\overline{OE} = V_{IH}$ .

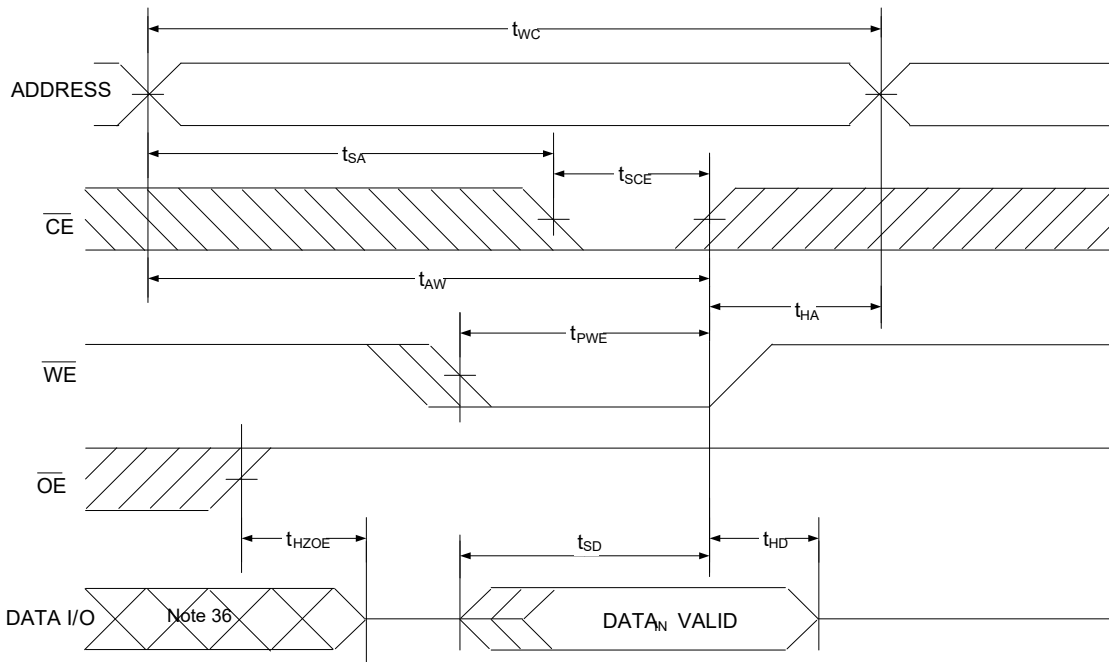
31. During this period, the I/Os are in output state. Do not apply input signals.

## Switching Waveforms (continued)

**Figure 7. Write Cycle No. 2 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  Low)**<sup>[32, 33, 34, 35]</sup>



**Figure 8. Write Cycle No. 3 ( $\overline{\text{CE}}$  Controlled)**<sup>[32, 33, 34]</sup>



### Notes

32. For all dual chip enable devices,  $\overline{\text{CE}}$  is the logical combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$ . When  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW; when  $\overline{\text{CE}}_1$  is HIGH or  $\text{CE}_2$  is LOW,  $\overline{\text{CE}}$  is HIGH.

33. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}} = V_{\text{IL}}$ ,  $\overline{\text{CE}}_1 = V_{\text{IL}}$ , and  $\text{CE}_2 = V_{\text{IH}}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.

34. Data I/O is in high impedance state if  $\overline{\text{CE}} = V_{\text{IH}}$ , or  $\overline{\text{OE}} = V_{\text{IH}}$ .

35. The minimum write cycle pulse width should be equal to the sum of the  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .

36. During this period I/O are in the output state. Do not apply input signals.

**Truth Table – CY62158H**

$\overline{CE}_1$	$CE_2$	$\overline{WE}$	$\overline{OE}$	I/Os	Mode	Power
H	$X^{[37]}$	$X^{[37]}$	$X^{[37]}$	High Z	Deselect / Power down	Standby ( $I_{SB2}$ )
$X^{[37]}$	L	$X^{[37]}$	$X^{[37]}$	High Z	Deselect / Power down	Standby ( $I_{SB2}$ )
L	H	H	L	Data Out ( $I/O_0$ – $I/O_7$ )	Read	Active ( $I_{CC}$ )
L	H	H	H	High Z	Output disabled	Active ( $I_{CC}$ )
L	H	L	X	Data In ( $I/O_0$ – $I/O_7$ )	Write	Active ( $I_{CC}$ )

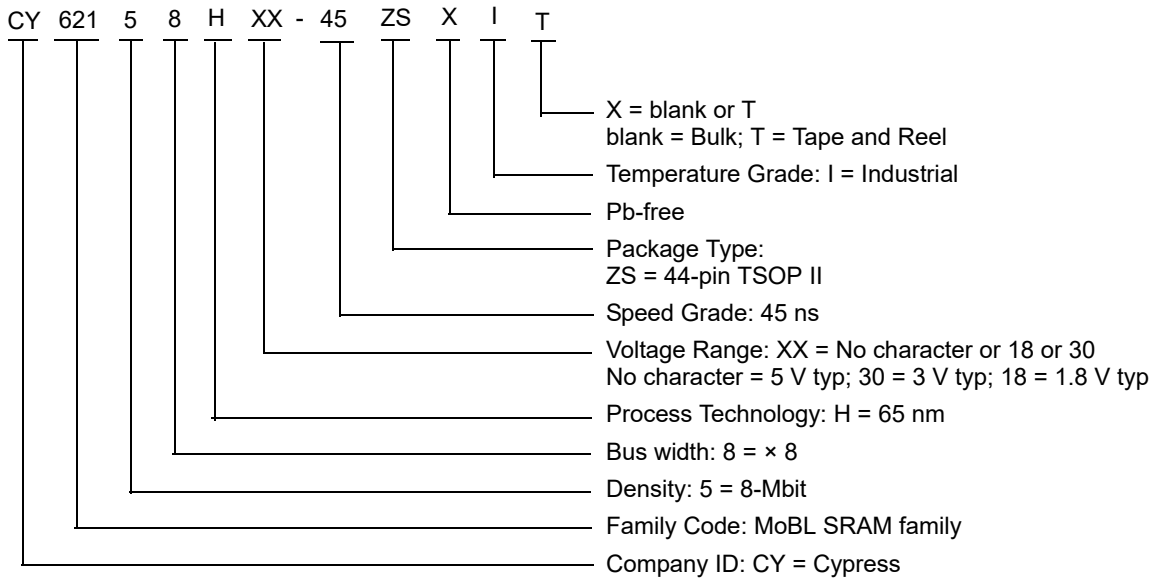
**Note**

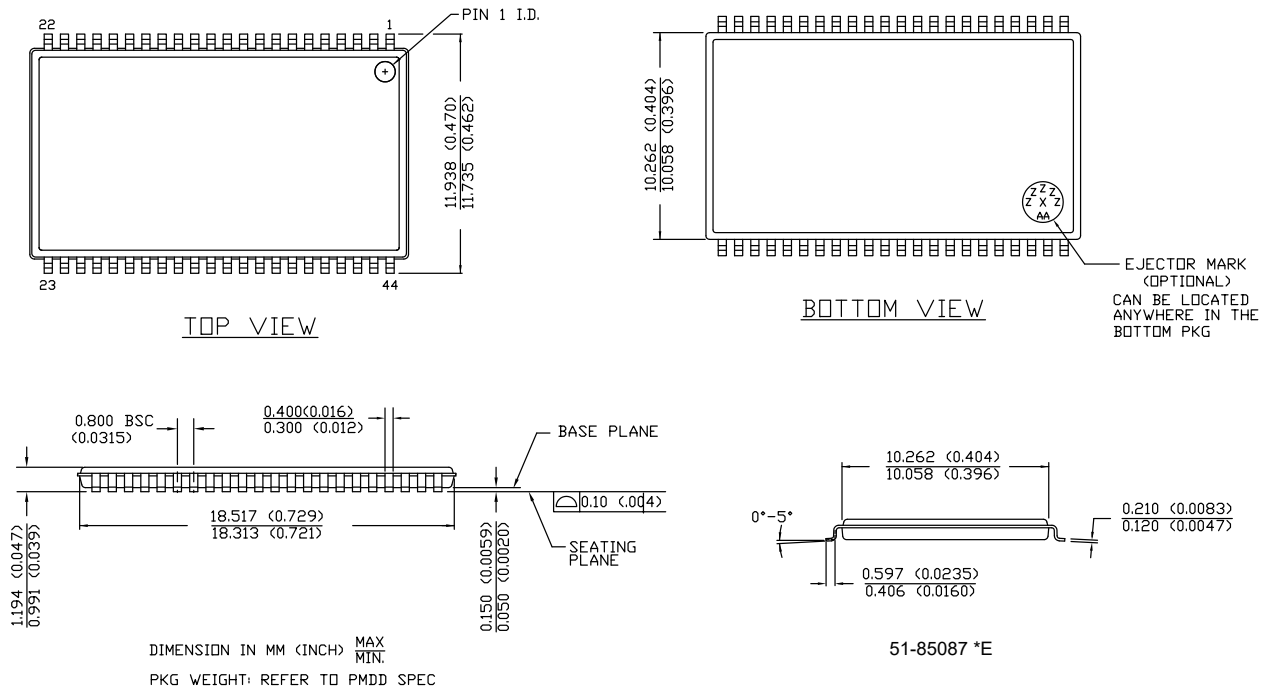
37. The 'X' (Don't care) state for the chip enables refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

## Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type (all Pb-free)	Operating Range
45	CY62158H-45ZSXI	51-85087	44-pin TSOP II (Pb-free)	Industrial
	CY62158H-45ZSXIT			

## Ordering Code Definitions





## Acronyms

**Table 1. Acronyms Used in this Document**

Acronym	Description
CE	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
OE	Output Enable
SRAM	Static Random Access Memory
VFBGA	Very Fine-Pitch Ball Grid Array
WE	Write Enable
ECC	Error Correcting Code

## Document Conventions

### Units of Measure

**Table 2. Units of Measure**

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt

## Document History Page

Document Title: CY62158H MoBL®, 8-Mbit (1M words × 8-bit) Static RAM with Error-Correcting Code (ECC) Document Number: 001-96968				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*B	5258628	NILE	05/06/2016	Changed status from Preliminary to Final.
*C	5430402	VINI	09/13/2016	Updated <a href="#">DC Electrical Characteristics</a> : Updated Note 5 (Replaced 2 ns with 20 ns). Updated <a href="#">Ordering Information</a> : Updated part numbers. Updated to new template.
*D	5980470	AESATMP8	11/30/2017	Updated logo and Copyright.
*E	6122301	NILE	04/04/2018	Updated <a href="#">Features</a> : Referred Note 1 in "Embedded error-correcting code (ECC) for single-bit error correction". Added Note 2 and referred the same note in "Embedded error-correcting code (ECC) for single-bit error correction". Updated to new template. Completing Sunset Review.

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