

LTC2449

8-/16-channel, High Speed 24-Bit Delta Sigma ADC

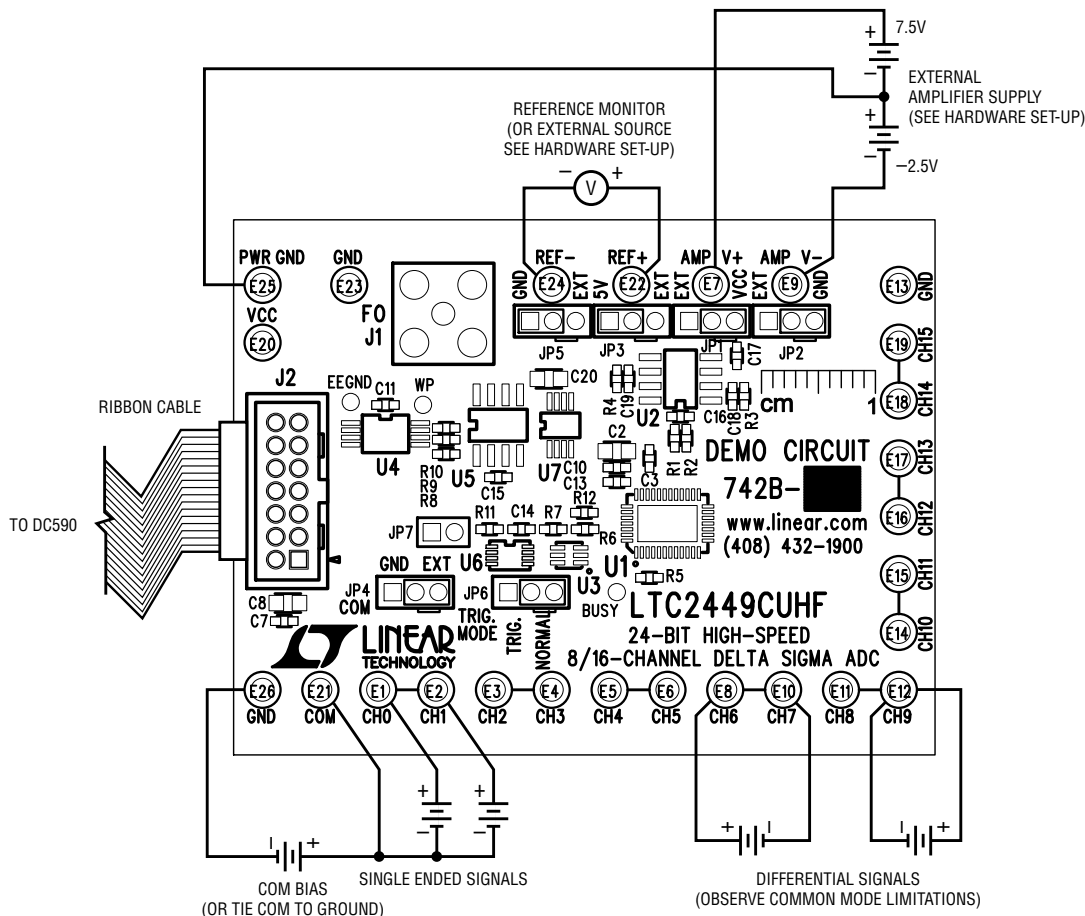
DESCRIPTION

Demonstration circuit 742B features the [LTC®2449](#), an 8-/16-channel, high speed, 24-bit $\Delta\Sigma$ ADC with ten selectable speed/resolution modes from 6.9Hz/200nV_{RMS} to 3.5kHz/23 μ V_{RMS} (4kHz with external oscillator). Key DC specifications include 5ppm INL, 5 μ V offset, 10ppm full-scale error and 20nV/°C offset drift. In the 6.9Hz/200nV_{RMS} mode, input normal mode rejection of 50Hz and 60Hz noise is better than 87dB. The accuracy (offset, full-scale, linearity, drift) and power dissipation are independent of the speed selected. The LTC2449 performs auto-zeroing of the ADC by reversing the inputs through the multiplexer output/ADC input connections. This allows an external dual buffer amplifier to isolate the signal inputs from the sampling current of the ADC.

DC742B is a member of Linear Technology's QuikEval™ family of demonstration boards. It is designed to allow easy evaluation of the LTC2449 and may be connected directly to the target application's analog signals while using the DC590 USB Serial Controller board and supplied software to measure performance. The exposed ground planes allow proper grounding to prototype circuitry. After evaluating with LTC's software, the digital signals can be connected to the application's processor/controller for development of the serial interface.

Design files for this circuit board are available at
<http://www.linear.com/demo/DC742B>

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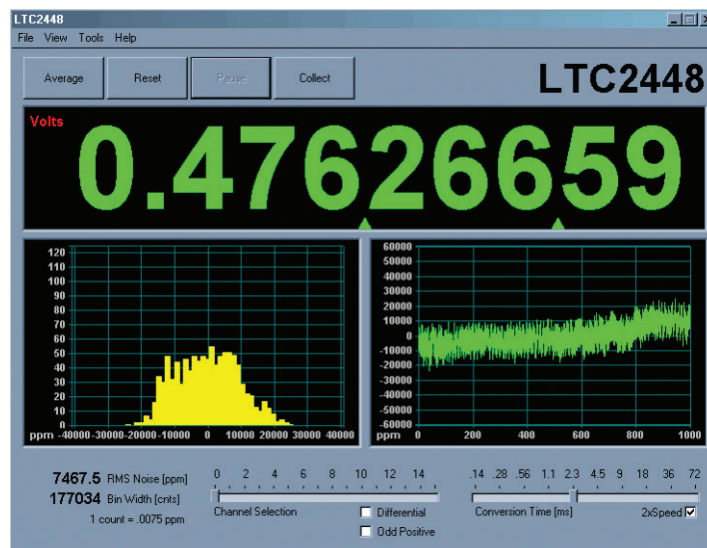
DEMO MANUAL DC742B

QUICK START PROCEDURE

Connect DC742B to a DC590 USB Serial Controller using the supplied 14-conductor ribbon cable. Connect DC590 to host PC with a standard USB A/B cable. Run the evaluation software supplied with DC590 or downloaded from www.linear.com. The correct program will be loaded automatically. Click the COLLECT button to start reading the input voltage. Click the slider at the bottom of the strip

chart display to change the oversample ratio (OSR) which will in turn change the data output rate.

Tools are available for logging data, changing reference voltage, changing the number of points in the strip chart and histogram, and changing the number of points averaged for the DVM display.



HARDWARE SETUP

JUMPERS

JP1, JP2: Select the positive and negative supply voltages for the onboard amplifier. Supplies can be ground and V_{CC} or supplied externally.

JP3, JP5: Select the source for REF+ and REF-, respectively. REF+ can be 5V from the onboard LT1236 reference (default) or supplied externally. REF- can be ground (0V, default) or supplied externally.

JP4: Select source for analog COM input, either tied to ground or supplied externally to the COM turret post.

JP6: Trigger mode, either normal (default) or externally triggered.

JP7: Trigger input signal. Pin 1 is a 5V logic input, pin 2 is ground. When triggered mode is selected on JP6, a rising edge starts a new conversion. Note that since a conversion

cannot be terminated once started, this signal can only be used to slow down the conversion rate.

CONNECTION TO DC590 SERIAL CONTROLLER

J2 is the power and digital interface connector. Connect to DC590 serial controller with supplied 14-conductor ribbon cable.

ANALOG CONNECTIONS

Analog signal connections are made via the row of turret posts along the edge of the board. Also, if you are connecting the board to an existing circuit, the exposed ground planes along the edges of the board may be used to form a solid connection between grounds.

GND: Ground turrets are connected directly to the internal analog ground plane.

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HARDWARE SETUP

PWR GND: Power ground, connected to the power return trace.

VCC: This is the supply for the ADC. Do not draw any power from this point. External power may be applied to this point after disabling the switching supply on DC590. If the DC590 serial controller is being used, the voltage must be regulated 5V only, as the isolation circuitry will also be powered from this supply. See the DC590 quick start guide for details.

REF+, REF-: These turrets are connected to the LTC2449 REF+ and REF- pins. If the onboard reference is being used, the reference voltage may be monitored from this point. An

external reference may be connected to these terminals if JP3 and JP5 are configured for external reference.

Note: The REF+ and REF- terminals are decoupled to ground with 0.1 μ F and 10 μ F capacitors in parallel. Thus any source connected to these terminals must be able to drive a capacitive load and have very low impedance at DC. Examples are series references that require an output capacitor and C-Load™ stable op amps such as the LT1219 and LT1368.

CH0: CH15: These are the differential inputs to the LTC2449. They may be configured either as single-ended inputs with respect to the COM pin, or adjacent pairs may be configured as differential inputs (CH0-1, CH2-3, etc.).

EXPERIMENTS

INPUT NOISE

Solder a short wire from CH0 to CH1. Ensure that the buffer amplifiers are in their active region of operation by either biasing the inputs to mid-supply with a 10k Ω to 10k Ω divider when the buffer amplifier is powered from V_{CC} and ground, or tie the inputs to ground and connect an external +7.5V/-2.5V supply to the AMP V+ and V- turrets (JP1 and JP2 must be set to EXT).

Set the demo software to OSR32768 (6.8 samples per second) and check the 2X box. Noise should be approximately 0.04ppm of V_{REF} (200nV). Next, select different oversample ratios. Measured noise for each oversample ratio should be close to values given in the LTC2449 data sheet.

COMMON MODE REJECTION

Tie the two inputs (still connected together from previous experiment) to ground through a short wire and note the indicated voltage. Tie the inputs to REF+; the difference should be less than 5 μ V due to the 120dB CMRR of the LTC2449.

This experiment requires an external power supply to the buffer amplifier.

If the common mode voltage is limited to GND + 0.25V to V_{CC} - 0.25V, this test may be performed with the amplifier supplies set to ground and V_{CC}.

INPUT NORMAL MODE REJECTION

The LTC2449's SINC4 digital filter is trimmed to strongly reject both 50Hz and 60Hz line noise when operated with the internal conversion clock and oversample ratio 32768 (6.8 samples per second). To measure input normal mode rejection, connect COM to a 2.5V source such as an LT1790-2.5 reference or a power supply. Connect any other input (CH0 to CH15) to the same supply through a 10k resistor. Apply a 10Hz, 2V peak-to-peak sine wave to the input through a 1 μ F capacitor.

Select OSR32768 (6.8 samples per second) and 2 $\times$ mode in the demo software and start taking data. The input noise will be quite large, and the graph of output vs time should show large variations.

Next, slowly increase the frequency to 55Hz. The noise should be almost undetectable in the graph. Note that the indicated noise in ppm may still be above that of the data sheet specification because the inputs are not connected to a DC source.

Change the OSR to 16384 (13.75 samples per second;) the noise will increase substantially, as the first notch at this OSR is at 110Hz. Increase the signal generator frequency to 110Hz, the noise will drop again.

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PARTS LIST

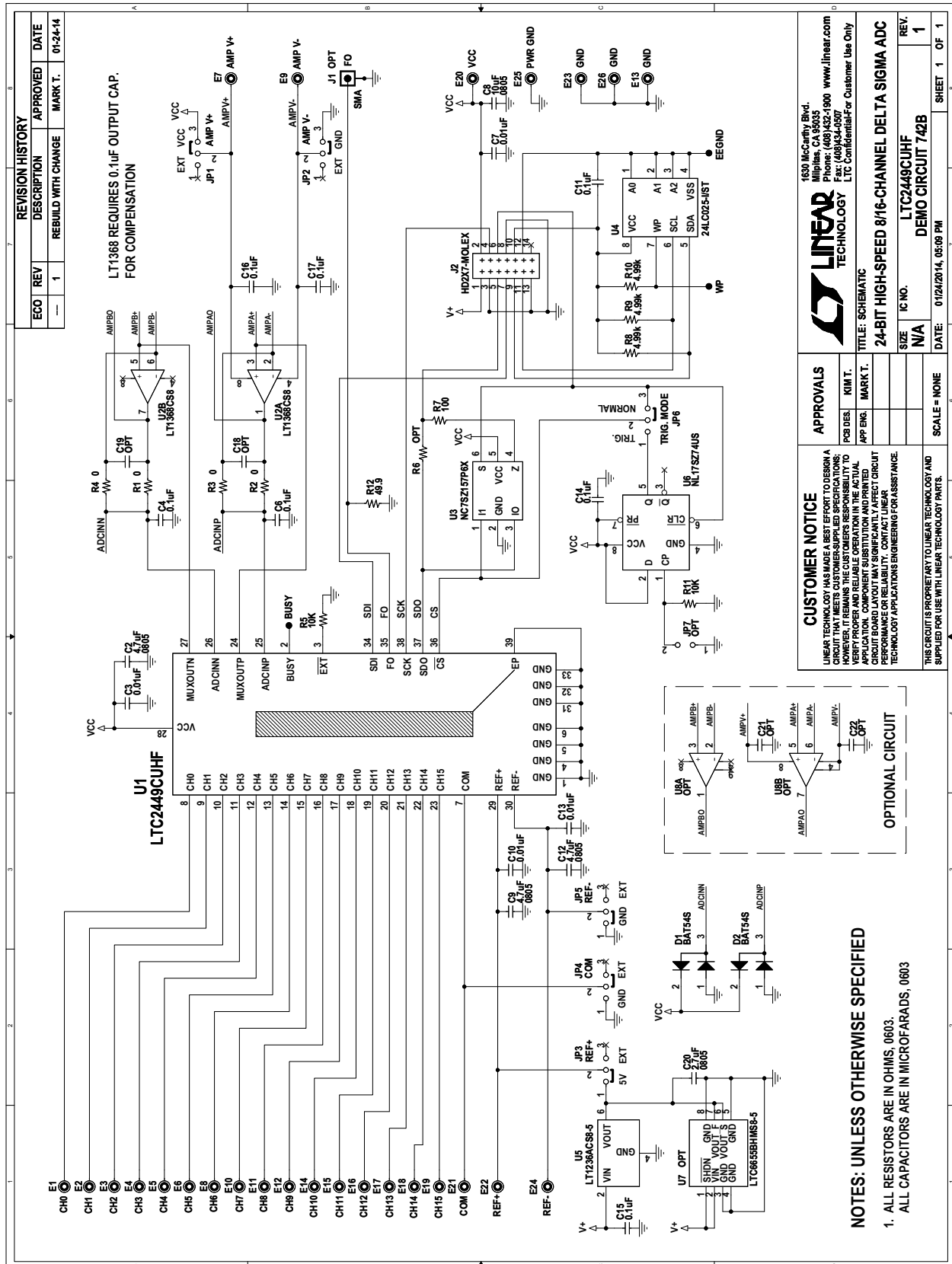
ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	3	C2, C9, C12	CAP., 4.7 μ F, X5R, 6.3V, 20%, 0805	TAIYO YUDEN, JMK212BJ475MG-T AVX, 08056D475MAT2A
2	4	C3, C7, C10, C13	CAP., 0.01 μ F, X7R, 16V, 10%, 0603	AVX, 0603YC103KAT2A MURATA, GRM188R71C103KA01D
3	9	C4, C6, C11, C14, C15, C16, C17	CAP., 0.1 μ F, X7R, 16V, 20%, 0603	AVX, 0603YC104MAT2A MURATA, GRM188R71C104MA01D
4	1	C8	CAP., 10 μ F, X5R, 6.3V, 20%, 0805	TDK, C2012X5R0J106M125AB AVX, 08056D106MAT2A SAMSUNG, CL21A106MQFNNE
5	0	C18, C19, C21, C22	CAP., OPTION, 0603	OPT
6	1	C20	CAP., 2.7 μ F, X5R, 10V, 10%, 0805	KEMET, C0805C275K8PACTU
7	2	D1, D2	DIODE, SCHOTTKY, 30V, 200mA, SOT23	DIODES INC., BAT54S-7-F
8	26	E1-E26	TEST POINT, TURRET, 0.064 THT	MILL-MAX, 2308-2-00-80-00-00-07-0
9	6	JP1-JP6	CONN., HEADER, 1 $\times$ 3, 2mm, THT	SULLINS, NRPN031PAEN-RC
10	0	JP7	CONN., HEADER, 1 $\times$ 2, 2mm, THT	SULLINS, NRPN021PAEN-RC
11	0	J1	CONN., OPTION, JACK, SMA COAXIAL STRT.	OPT
12	1	J2	CONN., HEADER, SHROUDED, 2 $\times$ 7, 2mm, THT	MOLEX, 87831-1420
13	4	R1, R2, R3, R4	RES., 0 Ω , 1/10W, 0603	VISHAY, CRCW06030000Z0EA
14	2	R5, R11	RES., 10k Ω , 5%, 1/10W, 0603	VISHAY, CRCW060310K0JNEA PANASONIC, ERJ3GEYJ103V
15	0	R6	RES., OPTION, 0603	OPT
16	1	R7	RES., 100 Ω , 1%, 1/10W, 0603	VISHAY, CRCW0603100RFKEA
17	3	R8, R9, R10	RES., 4.99k Ω , 1%, 1/10W, 0603	VISHAY, CRCW06034K99FKEA
18	1	R12	RES., 49.9 Ω , 1%, 1/10W, 0603	VISHAY, CRCW060349R9FKEA PANASONIC, ERJ3EKF49R9V ROHM, MCR03EZPFX49R9
19	1	U1	I.C., 8-/16-CHANNEL DELTA SIGMA ADCs, QFN38UHF-5 $\times$ 7	LINEAR TECH., LTC2449CUHF#PBF
20	1	U2	I.C., DUAL & QUAD PRECISION OP AMP, SO8	LINEAR TECH., LT1368CS8#PBF
21	1	U3	I.C., NON-INVERTING MULTIPLEXER, SC70-6	FAIRCHILD, NC7SZ157P6X
22	1	U4	IC, MEMORY, I ² C Serial EEPROM, 2K-bit, TSSOP8	MICROCHIP, 24LC025-I/ST
23	1	U5	I.C., PRECISION REFERENCE, SO8	LINEAR TECH., LT1236ACS8-5#PBF
24	1	U6	I.C., SINGLE D FLIP-FLOP, US8	ON SEMI., NL17SZ74USG
25	0	U7	I.C., PRECISION REFERENCE, MSOP8	LINEAR TECH., LTC6655BHMS8-5#PBF
26	0	U8	I.C., OPTION, DFN8DD-3 $\times$ 3	OPT
27	6	SHUNTS FOR JP1- JP6 (SEE ASSY DWG)	SHUNT, 2 POS, 2mm	SAMTEC, 2SN-BK-G

REVISION NOTES

BOARD REVISION	DESCRIPTION	DATE
B	Add Locations for Other Amplifier Configurations	1/2014

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SCHEMATIC DIAGRAM



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DEMONSTRATION BOARD IMPORTANT NOTICE

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Please read the DEMO BOARD manual prior to handling the product. Persons handling this product must have electronics training and observe good laboratory practice standards. **Common sense is encouraged.**

This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

Mailing Address:

Linear Technology
1630 McCarthy Blvd.
Milpitas, CA 95035

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