# LC²MOS 4-/8-Channel High Performance Analog Multiplexers

Data Sheet

# ADG408/ADG409

## FEATURES

- 44 V supply maximum ratings
- $V_{SS}$ to $V_{DD}$ analog signal range
- Low on resistance (100 Ω maximum)
- Low power ($I_{SUPPLY}$ < 75 µA)
- Fast switching
- Break-before-make switching action
- Plug-in replacement for DG408/DG409

## APPLICATIONS

- Audio and video routing
- Automatic test equipment
- Data acquisition systems
- Battery-powered systems
- Sample-and-hold systems
- Communication systems

## FUNCTIONAL BLOCK DIAGRAMS

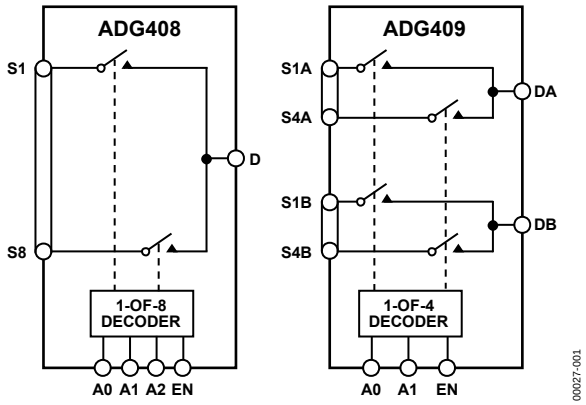


*Figure 1.*

## GENERAL DESCRIPTION

The ADG408/ADG409 are monolithic CMOS analog multiplexers comprising eight single channels and four differential channels, respectively. The ADG408 switches one of eight inputs to a common output as determined by the 3-bit binary address lines A0, A1, and A2. The ADG409 switches one of four differential inputs to a common differential output, as determined by the 2-bit binary address lines A0 and A1. An EN input on both devices is used to enable or disable the device. When the device is disabled, all channels are switched off.

The ADG408/ADG409 are designed on an enhanced LC²MOS process that provides low power dissipation yet gives high switching speed and low on resistance. Each channel conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked. All channels exhibit break-before-make switching action, preventing momentary shorting when switching channels. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

The ADG408/ADG409 are improved replacements for the DG408/DG409 analog multiplexers.

## PRODUCT HIGHLIGHTS

1. Extended Signal Range. The ADG408/ADG409 are fabricated on an enhanced LC²MOS process, giving an increased signal range that extends to the supply rails.
2. Low Power Dissipation.
3. Low $R_{ON}$.
4. Single-Supply Operation. For applications where the analog signal is unipolar, the ADG408/ADG409 can be operated from a single rail power supply. The parts are fully specified with a single 12 V power supply and remain functional with single supplies as low as 5 V.

Rev. D
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## REVISION HISTORY

**3/15—Rev. C to Rev. D**

Changes to Figure 12 and Figure 15 ..... 9
Updated Outline Dimensions ..... 16
Changes to Ordering Guide ..... 16

**10/06—Rev. B to Rev. C**

Updated Format ..... Universal
Changes to Table 3 ..... 6
Inserted Table 4 and Table 5 ..... 7
Updated Outline Dimensions ..... 14
Changes to Ordering Guide ..... 15

**3/03—Rev. A to Rev. B**

Changes to Ordering Guide ..... 4
Updated Outline Dimensions ..... 11

**2/01—Revision 0: Initial Version**

# SPECIFICATIONS

## DUAL SUPPLY

$V_{DD}$ = 15 V, $V_{SS}$ = −15 V, GND = 0 V, unless otherwise noted.

**Table 1.**

| Parameter | B Version +25°C | B Version −40°C to +85°C | T Version +25°C | T Version −55°C to +125°C | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| ANALOG SWITCH | | | | | | |
| Analog Signal Range | | $V_{SS}$ to $V_{DD}$ | | $V_{SS}$ to $V_{DD}$ | V | |
| $R_{ON}$ | 40 | | 40 | | Ω typ | $V_D$ = ±10 V, $I_S$ = −10 mA |
| | 100 | 125 | 100 | 125 | Ω max | |
| $\Delta R_{ON}$ | 15 | | 15 | | Ω max | $V_D$ = +10 V, −10 V |
| LEAKAGE CURRENTS | | | | | | |
| Source Off Leakage $I_S$ (Off) | ±0.5 | ±50 | ±0.5 | ±50 | nA max | $V_D$ = ±10 V, $V_S$ = ∓10 V; see Figure 19 |
| Drain Off Leakage $I_D$ (Off) | | | | | | $V_D$ = ±10 V, $V_S$ = ∓10 V; see Figure 20 |
| ADG408 | ±1 | ±100 | ±1 | ±100 | nA max | |
| ADG409 | ±1 | ±50 | ±1 | ±50 | nA max | |
| Channel On Leakage $I_D$, $I_S$ (On) | | | | | | $V_S$ = $V_D$ = ±10 V; see Figure 21 |
| ADG408 | ±1 | ±100 | ±1 | ±100 | nA max | |
| ADG409 | ±1 | ±50 | ±1 | ±50 | nA max | |
| DIGITAL INPUTS | | | | | | |
| Input High Voltage, $V_{INH}$ | | 2.4 | | 2.4 | V min | |
| Input Low Voltage, $V_{INL}$ | | 0.8 | | 0.8 | V max | |
| Input Current | | | | | | |
| $I_{INL}$ or $I_{INH}$ | | ±10 | | ±10 | μA max | $V_{IN}$ = 0 or $V_{DD}$ |
| $C_{IN}$, Digital Input Capacitance | 8 | | 8 | | pF typ | f = 1 MHz |
| DYNAMIC CHARACTERISTICS[1] | | | | | | |
| $t_{TRANSITION}$ | | 120 | | 120 | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF; |
| | | 250 | | 250 | ns max | $V_{S1}$ = ±10 V, $V_{S8}$ = ∓10 V; see Figure 22 |
| $t_{OPEN}$ | 10 | 10 | 10 | 10 | ns min | $R_L$ = 300 Ω, $C_L$ = 35 pF; |
| | | | | | | $V_S$ = 5 V; see Figure 23 |
| $t_{ON}$ (EN) | 85 | 125 | 85 | 125 | ns typ | $R_L$ = 300 Ω $C_L$ = 35 pF; |
| | 150 | 225 | 150 | 225 | ns max | $V_S$ = 5 V; see Figure 24 |
| $t_{OFF}$ (EN) | | 65 | | 65 | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF; |
| | | 150 | | 150 | ns max | $V_S$ = 5 V; see Figure 24 |
| Charge Injection | 20 | | 20 | | pC typ | $V_S$ = 0 V, $R_S$ = 0 Ω, $C_L$ = 10 nF; see Figure 25 |
| OFF Isolation | −75 | | −75 | | dB typ | $R_L$ = 1 kΩ, f = 100 kHz; |
| | | | | | | $V_{EN}$ = 0 V; see Figure 26 |
| Channel-to-Channel Crosstalk | 85 | | 85 | | dB typ | RL = 1 kΩ, f = 100 kHz; see Figure 27 |
| $C_S$ (OFF) | 11 | | 11 | | pF typ | f = 1 MHz |
| $C_D$ (OFF) | | | | | | f = 1 MHz |
| ADG408 | 40 | | 40 | | pF typ | |
| ADG409 | 20 | | 20 | | pF typ | |
| $C_D$, $C_S$ (ON) | | | | | | f = 1 MHz |
| ADG408 | 54 | | 54 | | pF typ | |
| ADG409 | 34 | | 34 | | pF typ | |

| Parameter | B Version +25°C | B Version −40°C to +85°C | T Version +25°C | T Version −55°C to +125°C | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| POWER REQUIREMENTS | | | | | | |
| $I_{DD}$ | | 1 | | 1 | µA typ | $V_{IN}$ = 0 V, $V_{EN}$ = 0 V |
| | | 5 | | 5 | µA max | |
| $I_{SS}$ | | 1 | | 1 | µA typ | |
| | | 5 | | 5 | µA max | |
| $I_{DD}$ | 100 | | 100 | | µA typ | $V_{IN}$ = 0 V, $V_{EN}$ = 2.4 V |
| | 200 | 500 | 200 | 500 | µA max | |

[1] Guaranteed by design, not subject to production test.

## SINGLE SUPPLY

$V_{DD}$ = 12 V, $V_{SS}$ = 0 V, GND = 0 V, unless otherwise noted.

**Table 2.**

| Parameter | B Version +25°C | B Version −40°C to +85°C | T Version +25°C | T Version −55°C to +125°C | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| ANALOG SWITCH | | | | | | |
| Analog Signal Range | | 0 to $V_{DD}$ | | 0 to $V_{DD}$ | V | |
| $R_{ON}$ | 90 | | 90 | | Ω typ | $V_D$ = 3 V, 10 V, $I_S$ = −1 mA |
| LEAKAGE CURRENTS | | | | | | |
| Source Off Leakage $I_S$ (Off) | ±0.5 | ±50 | ±0.5 | ±50 | nA max | VD = 8 V/0 V, $V_S$ = 0 V/8 V; see Figure 19 |
| Drain Off Leakage $I_D$ (Off) | | | | | | $V_D$ = 8 V/0 V, $V_S$ = 0 V/8 V; see Figure 20 |
| ADG408 | ±1 | ±100 | ±1 | ±100 | nA max | |
| ADG409 | ±1 | ±50 | ±1 | ±50 | nA max | |
| Channel On Leakage $I_D$, $I_S$ (On) | | | | | | $V_S$ = $V_D$ = 8 V/0 V; see Figure 21 |
| ADG408 | ±1 | ±100 | ±1 | ±100 | nA max | |
| ADG409 | ±1 | ±50 | ±1 | ±50 | nA max | |
| DIGITAL INPUTS | | | | | | |
| Input High Voltage, $V_{INH}$ | | 2.4 | | 2.4 | V min | |
| Input Low Voltage, $V_{INL}$ | | 0.8 | | 0.8 | V max | |
| Input Current | | | | | | |
| $I_{INL}$ or $I_{INH}$ | | ±10 | | ±10 | µA max | $V_{IN}$ = 0 or $V_{DD}$ |
| $C_{IN}$, Digital Input Capacitance | 8 | | 8 | | pF typ | f = 1 MHz |
| DYNAMIC CHARACTERISTICS[1] | | | | | | |
| $t_{TRANSITION}$ | 130 | | 130 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF; $V_{S1}$ = 8 V/0 V, $V_{S8}$ = 0 V/8 V; see Figure 22 |
| $t_{OPEN}$ | 10 | | 10 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF; $V_S$ = 5 V; see Figure 23 |
| $t_{ON}$ (EN) | 140 | | 140 | | ns typ | $R_L$ = 300 Ω $C_L$ = 35 pF; $V_S$ = 5 V; see Figure 24 |
| $t_{OFF}$ (EN) | 60 | | 60 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF; $V_S$ = 5 V; see Figure 24 |
| Charge Injection | 5 | | 5 | | pC typ | $V_S$ = 0 V, $R_S$ = 0 Ω, $C_L$ = 10 nF; see Figure 25 |
| Off Isolation | −75 | | −75 | | dB typ | $R_L$ = 1 kΩ f = 100 kHz; $V_{EN}$ = 0 V; see Figure 26 |

| Parameter | B Version | | T Version | | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| | +25°C | −40°C to +85°C | +25°C | −55°C to +125°C | | |
| Channel-to-Channel Crosstalk | 85 | | 85 | | dB typ | $R_L$ = 1 kΩ, f = 100 kHz; see Figure 27 |
| $C_S$ (Offf) | 11 | | 11 | | pF typ | f = 1 MHz |
| $C_D$ (Off) | | | | | | f = 1 MHz |
| ADG408 | 40 | | 40 | | pF typ | |
| ADG409 | 20 | | 20 | | pF typ | |
| $C_D$, $C_S$ (On) | | | | | | f = 1 MHz |
| ADG408 | 54 | | 54 | | pF typ | |
| ADG409 | 34 | | 34 | | pF typ | |
| POWER REQUIREMENTS | | | | | | |
| $I_{DD}$ | | 1 | | 1 | µA typ | $V_{IN}$ = 0 V, $V_{EN}$ = 0 V |
| | | 5 | | 5 | µA max | |
| $I_{DD}$ | 100 | | 100 | | µA typ | $V_{IN}$ = 0 V, $V_{EN}$ = 2.4 V |
| | 200 | 500 | 200 | 500 | µA max | |

[1] Guaranteed by design, not subject to production test.

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted.

**Table 3.**

| Parameter | Rating |
|---|---|
| $V_{DD}$ to $V_{SS}$ | 44 V |
| $V_{DD}$ to GND | −0.3 V to +32 V |
| $V_{SS}$ to GND | +0.3 V to −32 V |
| Analog, Digital Inputs | $V_{SS}$ − 2 V to $V_{DD}$ + 2 V or 20 mA, whichever occurs first |
| Continuous Current, S or D | 20 mA |
| Peak Current, S or D | |
| (Pulsed at 1 ms, 10% Duty Cycle Maximum) | 40 mA |
| Operating Temperature Range | |
| Industrial (B Version) | −40°C to +85°C |
| Extended (T Version) | −55°C to +125°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature | 150°C |
| CERDIP Package, Power Dissipation | 900 mW |
| $\theta_{JA}$, Thermal Impedance | 76°C/W |
| Lead Temperature, Soldering (10 sec) | 300°C |
| PDIP Package, Power Dissipation | 470 mW |
| $\theta_{JA}$, Thermal Impedance | 117°C/W |
| Lead Temperature, Soldering (10 sec) | 260°C |
| TSSOP Package, Power Dissipation | 450 mW |
| $\theta_{JA}$, Thermal Impedance | 155°C/W |
| $\theta_{JC}$, Thermal Impedance | 50°C/W |
| SOIC Package, Power Dissipation | 600 mW |
| $\theta_{JA}$, Thermal Impedance | 77°C/W |
| Lead Temperature, Soldering | |
| Vapor Phase (60 sec) | 215°C |
| Infrared (15 sec) | 220°C |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

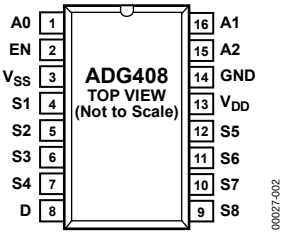



*Figure 2. ADG408 Pin Configuration*

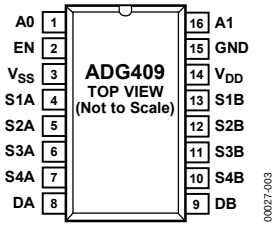



*Figure 3. ADG409 Pin Configuration*

**Table 4. ADG408 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | A0 | Logic Control Input. |
| 2 | EN | Active High Digital Input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine on switches. |
| 3 | $V_{SS}$ | Most Negative Power Supply Potential in Dual Supplies. In single-supply applications, it can be connected to ground. |
| 4 | S1 | Source Terminal 1. Can be an input or an output. |
| 5 | S2 | Source Terminal 2. Can be an input or an output. |
| 6 | S3 | Source Terminal 3. Can be an input or an output. |
| 7 | S4 | Source Terminal 4. Can be an input or an output. |
| 8 | D | Drain Terminal. Can be an input or an output. |
| 9 | S8 | Source Terminal 8. Can be an input or an output. |
| 10 | S7 | Source Terminal 7. Can be an input or an output. |
| 11 | S6 | Source Terminal 6. Can be an input or an output. |
| 12 | S5 | Source Terminal 5. Can be an input or an output. |
| 13 | $V_{DD}$ | Most Positive Power Supply Potential. |
| 14 | GND | Ground (0 V) Reference. |
| 15 | A2 | Logic Control Input. |
| 16 | A1 | Logic Control Input. |

**Table 5. ADG409 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | A0 | Logic Control Input. |
| 2 | EN | Active High Digital Input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine on switches. |
| 3 | $V_{SS}$ | Most Negative Power Supply Potential in Dual Supplies. In single-supply applications, it can be connected to ground. |
| 4 | S1A | Source Terminal 1A. Can be an input or an output. |
| 5 | S2A | Source Terminal 2A. Can be an input or an output. |
| 6 | S3A | Source Terminal 3A. Can be an input or an output. |
| 7 | S4A | Source Terminal 4A. Can be an input or an output. |
| 8 | DA | Drain Terminal A. Can be an input or an output. |
| 9 | DB | Drain Terminal B. Can be an input or an output. |
| 10 | S4B | Source Terminal 4B. Can be an input or an output. |
| 11 | S3B | Source Terminal 3B. Can be an input or an output. |
| 12 | S2B | Source Terminal 2B. Can be an input or an output. |
| 13 | S1B | Source Terminal 1B. Can be an input or an output. |
| 14 | $V_{DD}$ | Most Positive Power Supply Potential. |
| 15 | GND | Ground (0 V) Reference. |
| 16 | A1 | Logic Control Input. |

**Table 6. ADG408 Truth Table**

| A2 | A1 | A0 | EN | On Switch |
|---|---|---|---|---|
| X | X | X | 0 | None |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 2 |
| 0 | 1 | 0 | 1 | 3 |
| 0 | 1 | 1 | 1 | 4 |
| 1 | 0 | 0 | 1 | 5 |
| 1 | 0 | 1 | 1 | 6 |
| 1 | 1 | 0 | 1 | 7 |
| 1 | 1 | 1 | 1 | 8 |

**Table 7. ADG409 Truth Table**

| A1 | A0 | EN | On Switch Pair |
|---|---|---|---|
| X | X | 0 | None |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 2 |
| 1 | 0 | 1 | 3 |
| 1 | 1 | 1 | 4 |

# TYPICAL PERFORMANCE CHARACTERISTICS

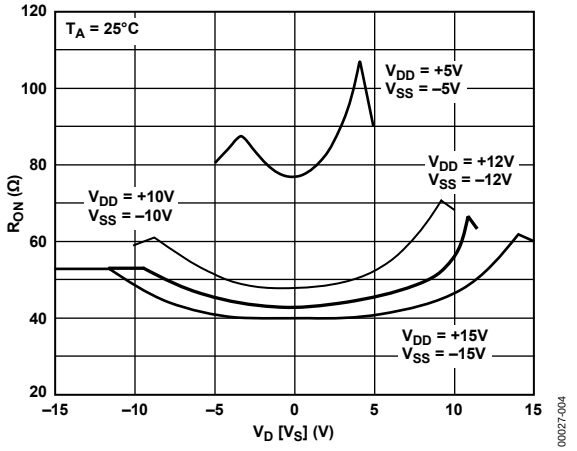



*Figure 4. $R_{ON}$ as a Function of $V_D$ ($V_S$): Dual-Supply Voltage*

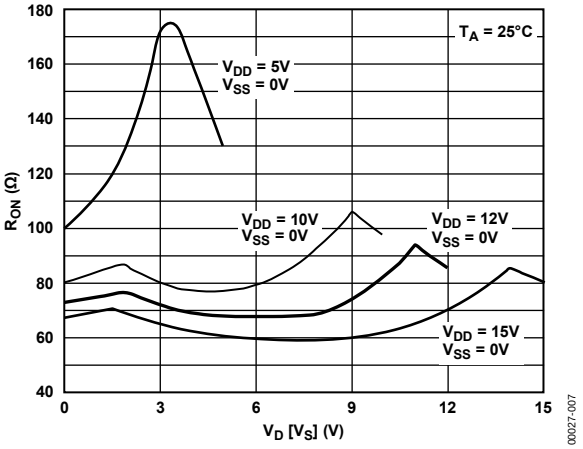



*Figure 7. $R_{ON}$ as a Function of $V_D$ ($V_S$): Single-Supply Voltage*

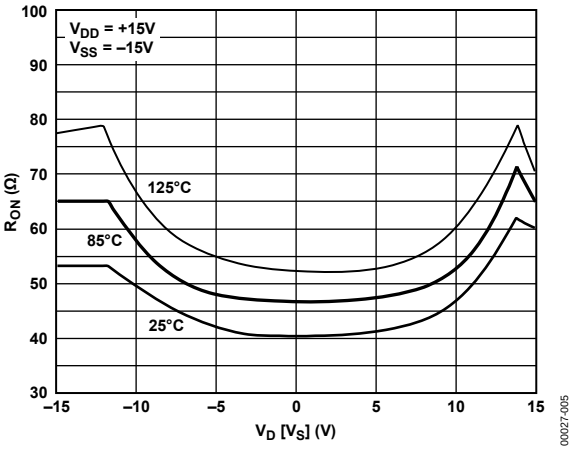



*Figure 5. $R_{ON}$ as a Function of $V_D$ ($V_S$) for Different Temperatures*

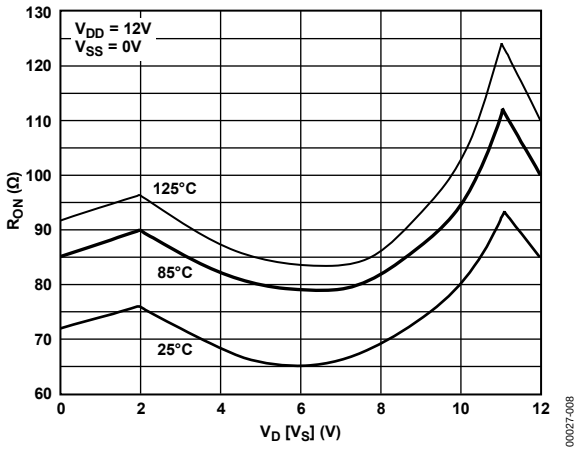



*Figure 8. $R_{ON}$ as a Function of $V_D$ ($V_S$) for Different Temperature*

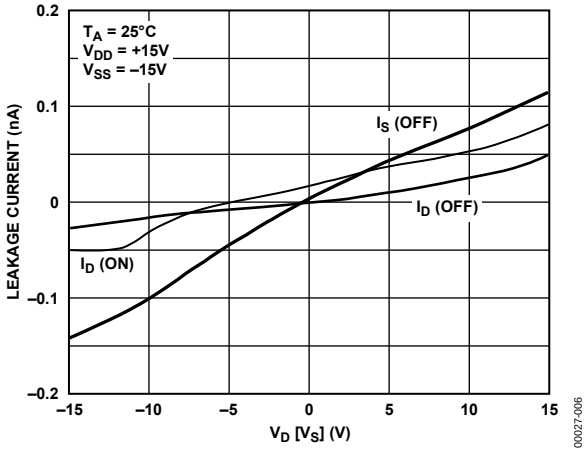



*Figure 6. Leakage Currents as a Function of $V_D$ ($V_S$)*

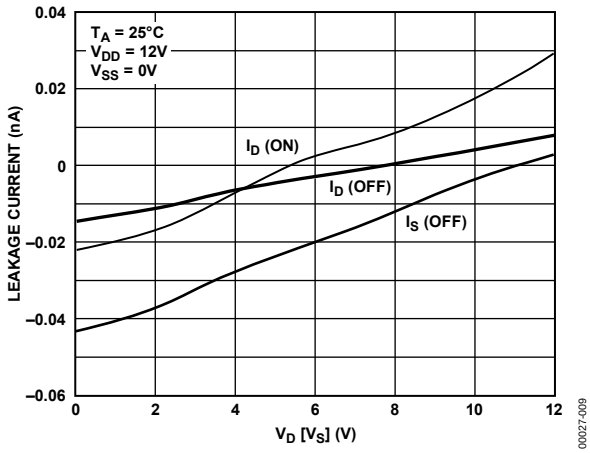



*Figure 9. Leakage Currents as a Function of $V_D$ ($V_S$)*

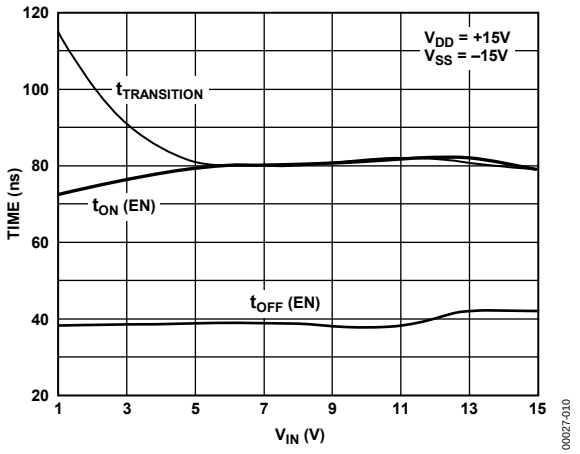



Figure 10. Switching Time vs. $V_{IN}$ (Bipolar Supply)

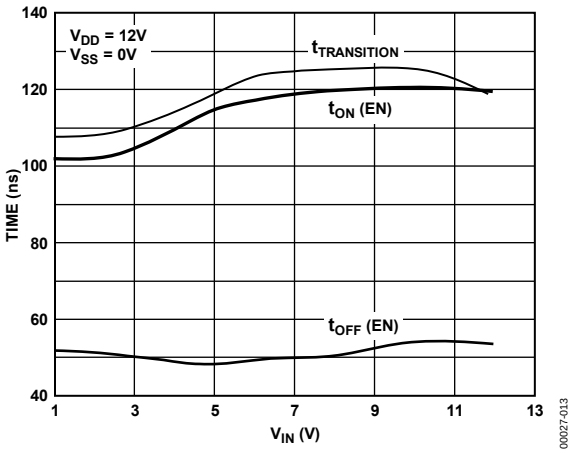



Figure 13. Switching Time vs. $V_{IN}$ (Single Supply)

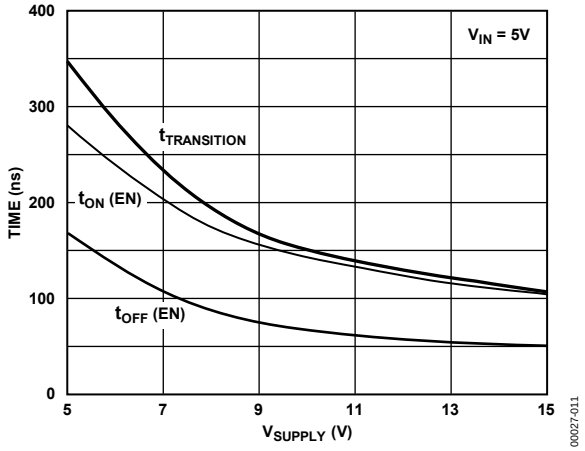



Figure 11. Switching Time vs. Single Supply

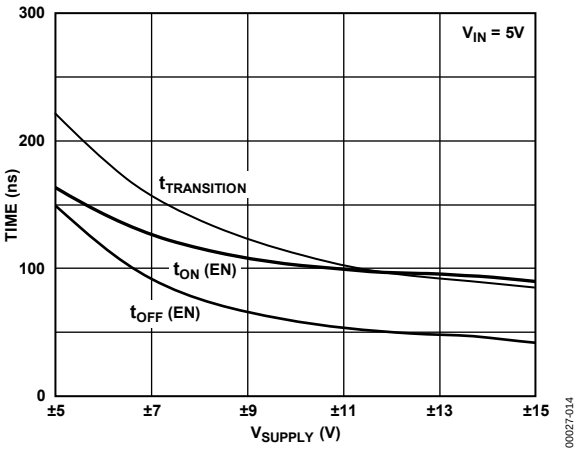



Figure 14. Switching Time vs. Bipolar Supply

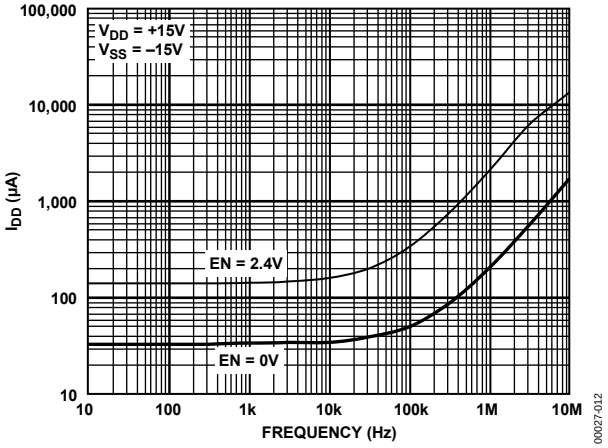



Figure 12. Positive Supply Current vs. Switching Frequency

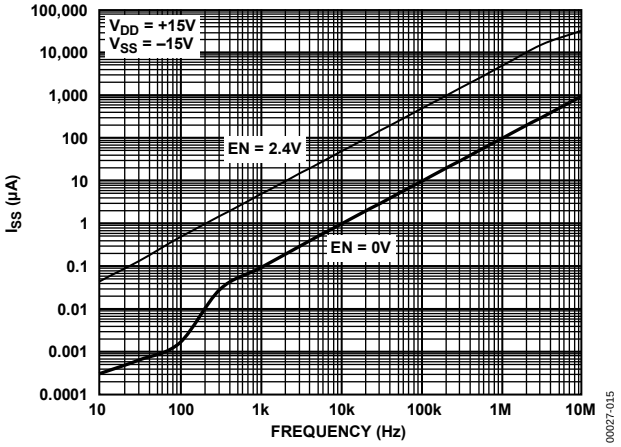



Figure 15. Negative Supply Current vs. Switching Frequency

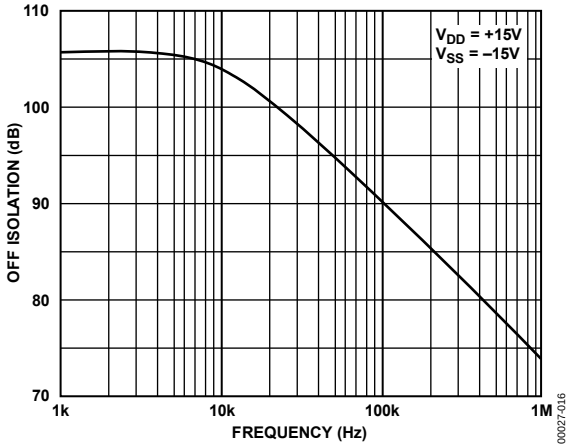



Figure 16. Off Isolation vs. Frequency

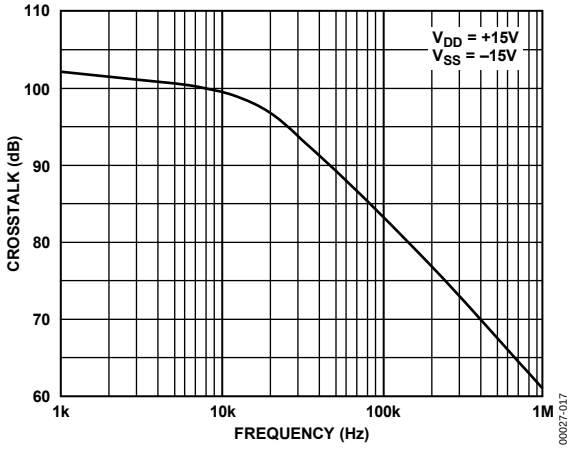



Figure 17. Crosstalk vs. Frequency

# TEST CIRCUITS

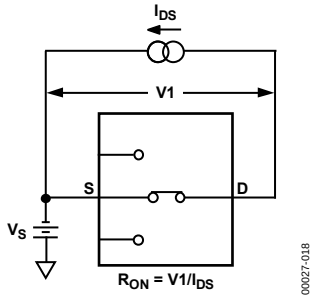



Figure 18. On Resistance

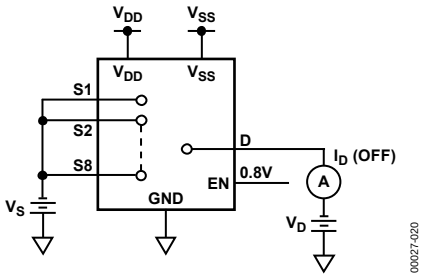



Figure 20. $I_D$ (Off)

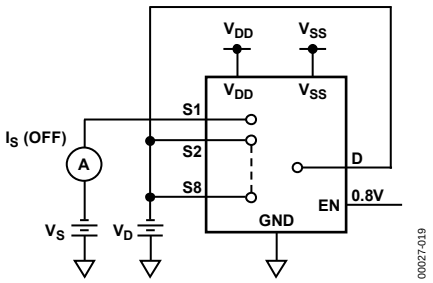



Figure 19. $I_S$ (Off)

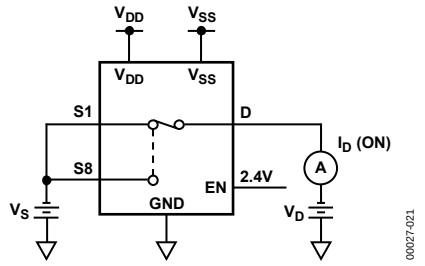



Figure 21. $I_D$ (On)

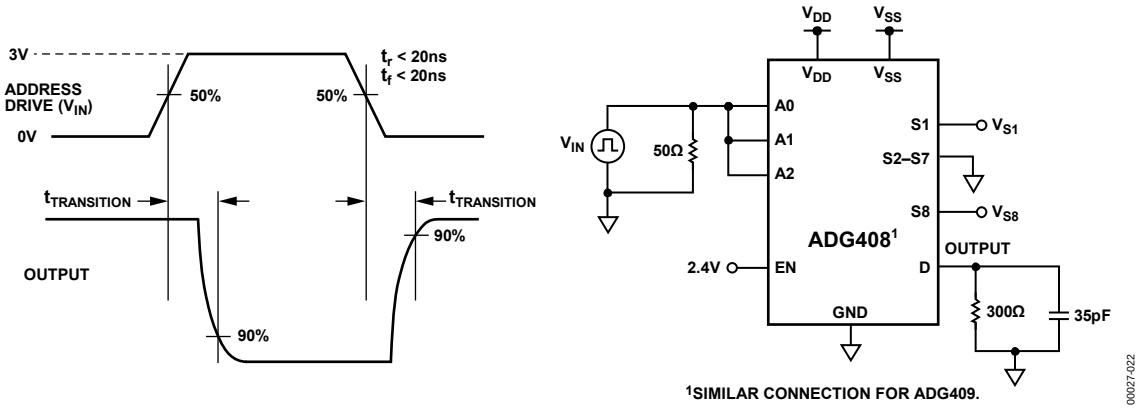



Figure 22. Switching Time of Multiplexer, $t_{TRANSITION}$

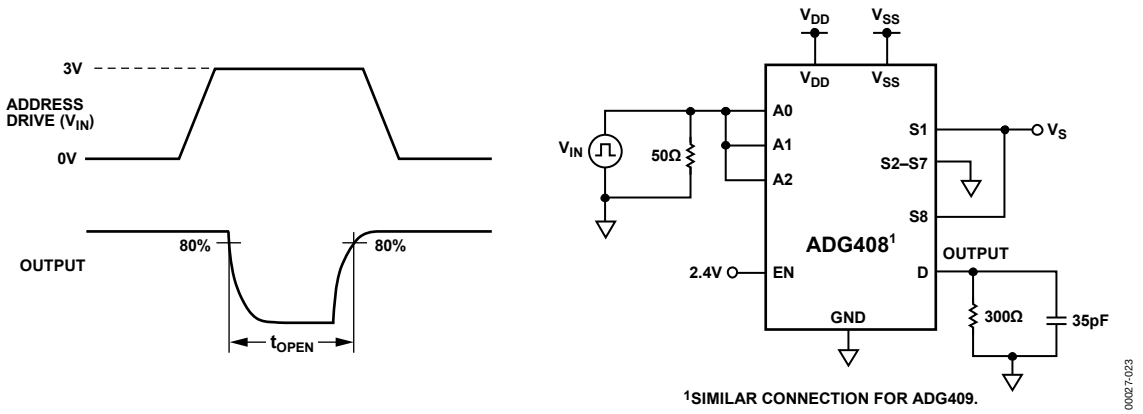



Figure 23. Break-Before-Make Delay, $t_{OPEN}$

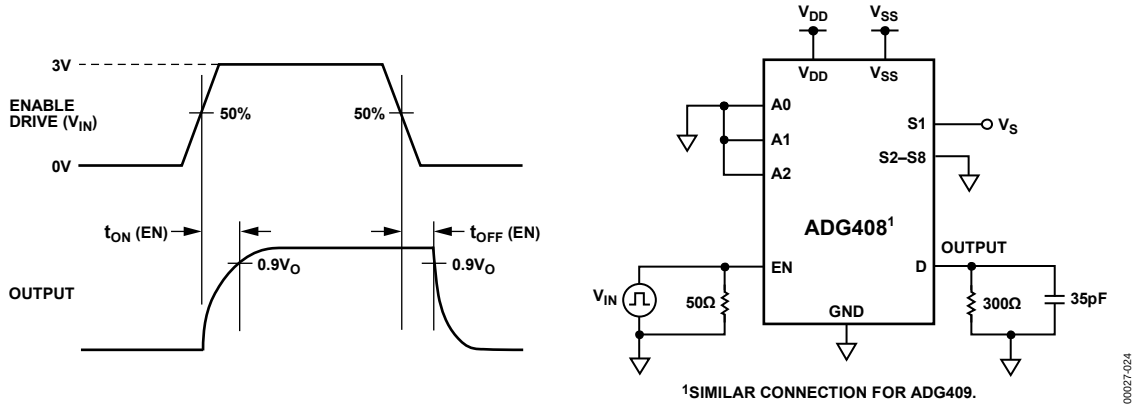



*Figure 24. Enable Delay, $t_{ON}$ (EN), $t_{OFF}$ (EN)*

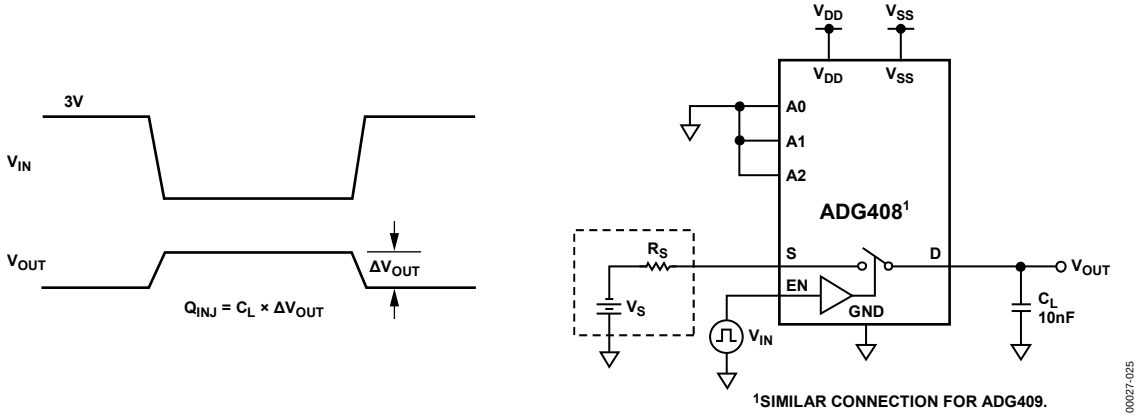



*Figure 25. Charge Injection*

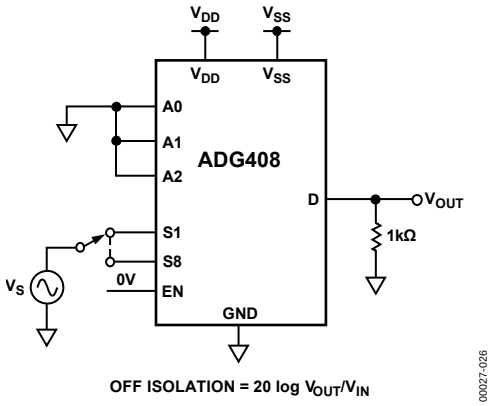



*Figure 26. Off Isolation*

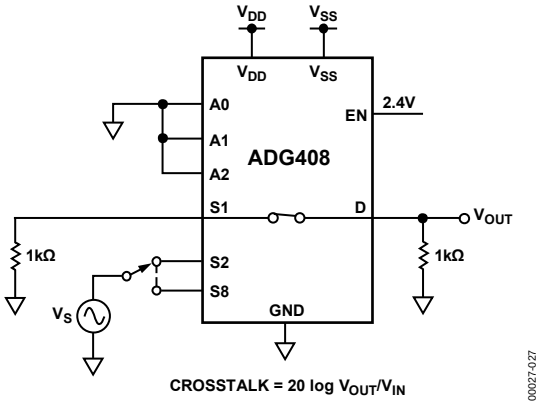



*Figure 27. Channel-to-Channel Crosstalk*

# TERMINOLOGY

**$R_{ON}$**
Ohmic resistance between D and S.

**$\Delta R_{ON}$**
Difference between the $R_{ON}$ of any two channels.

**$I_S$ (Off)**
Source leakage current when the switch is off.

**$I_D$ (Off)**
Drain leakage current when the switch is off.

**$I_D$, $I_S$ (On)**
Channel leakage current when the switch is on.

**$V_D$ ($V_S$)**
Analog voltage on Terminal D and Terminal S.

**$C_S$ (Off)**
Channel input capacitance for off condition.

**$C_D$ (Off)**
Channel output capacitance for off condition.

**$C_D$, $C_S$ (On)**
On switch capacitance.

**$C_{IN}$**
Digital input capacitance.

**$t_{ON}$ (EN)**
Delay time between the 50% and 90% points of the digital input and switch on condition.

**$t_{OFF}$ (EN)**
Delay time between the 50% and 90% points of the digital input and switch off condition.

**$t_{TRANSITION}$**
Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

**$t_{OPEN}$**
Off time measured between the 80% point of both switches when switching from one address state to another.

**$V_{INL}$**
Maximum input voltage for Logic 0.

**$V_{INH}$**
Minimum input voltage for Logic 1.

**$I_{INL}$ ($I_{INH}$)**
Input current of the digital input.

**Crosstalk**
A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

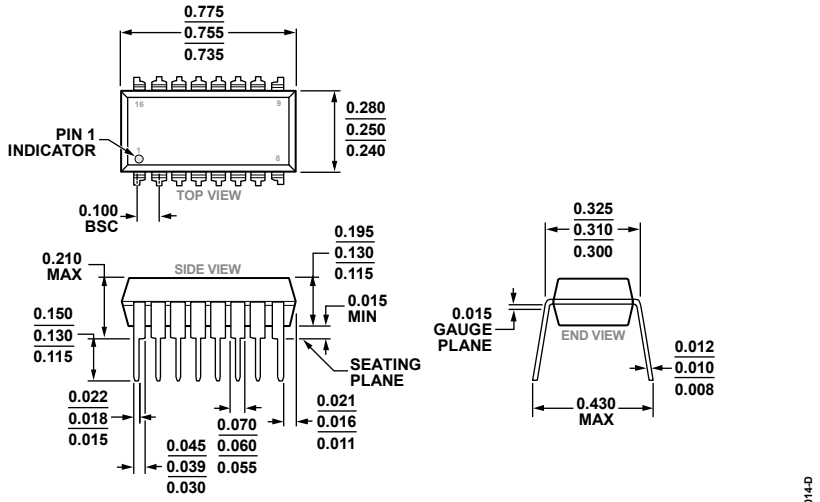
**Off Isolation**
A measure of unwanted signal coupling through an off channel.

**Charge Injection**
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

**$I_{DD}$**
Positive supply current.

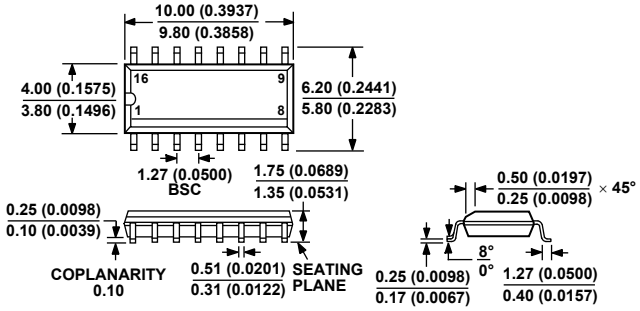
**$I_{SS}$**
Negative supply current.

# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MS-001-BB

*Figure 28. 16-Lead Plastic Dual In-Line Package [PDIP]*
*Narrow Body*
*(N-16)*
*Dimensions shown in inches and (millimeters)*




COMPLIANT TO JEDEC STANDARDS MS-012-AC

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

*Figure 29. 16-Lead Standard Small Outline Package [SOIC_N]*
*Narrow Body*
*(R-16)*
*Dimensions shown in millimeters and (inches)*

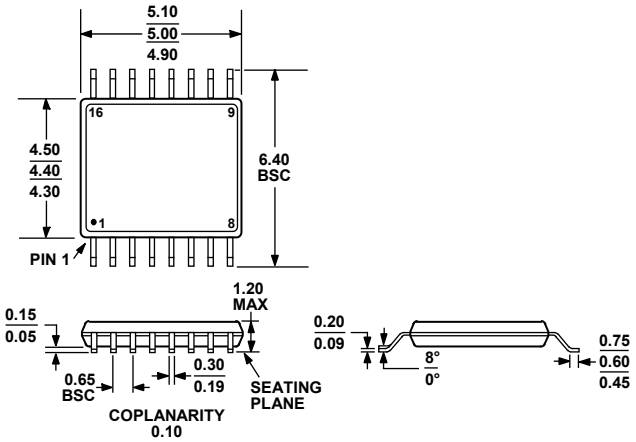



*Figure 30. 16-Lead Thin Shrink Small Outline Package [TSSOP]*
*(RU-16)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| ADG408BN | −40°C to +85°C | 16-Lead Plastic Dual In-Line Package [PDIP] | N-16 |
| ADG408BNZ | −40°C to +85°C | 16-Lead Plastic Dual In-Line Package [PDIP] | N-16 |
| ADG408BR | −40°C to +85°C | 16-Lead Narrow Body Small Outline Package [SOIC_N] | R-16 |
| ADG408BR-REEL | −40°C to +85°C | 16-Lead Narrow Body Small Outline Package [SOIC_N] | R-16 |
| ADG408BR-REEL7 | −40°C to +85°C | 16-Lead Narrow Body Small Outline Package [SOIC_N] | R-16 |
| ADG408BRU | −40°C to +85°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG408BRU-REEL | −40°C to +85°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG408BRU-REEL7 | −40°C to +85°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG408BRUZ | −40°C to +85°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG408BRUZ-REEL | −40°C to +85°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG408BRUZ-REEL7 | −40°C to +85°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG408BRZ | −40°C to +85°C | 16-Lead Narrow Body Small Outline Package [SOIC_N] | R-16 |
| ADG408BRZ-REEL | −40°C to +85°C | 16-Lead Narrow Body Small Outline Package [SOIC_N] | R-16 |
| ADG408BRZ-REEL7 | −40°C to +85°C | 16-Lead Narrow Body Small Outline Package [SOIC_N] | R-16 |
| ADG408BCHIPS | | DIE | |
| ADG409BNZ | −40°C to +85°C | 16-Lead Plastic Dual In-Line Package [PDIP] | N-16 |
| ADG409BR | −40°C to +85°C | 16-Lead Narrow Body Small Outline Package [SOIC_N] | R-16 |
| ADG409BR-REEL7 | −40°C to +85°C | 16-Lead Narrow Body Small Outline Package [SOIC_N] | R-16 |
| ADG409BRUZ | −40°C to +85°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG409BRUZ-REEL7 | −40°C to +85°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG409BRZ | −40°C to +85°C | 16-Lead Narrow Body Small Outline Package [SOIC_N] | R-16 |
| ADG409BRZ-REEL | −40°C to +85°C | 16-Lead Narrow Body Small Outline Package [SOIC_N] | R-16 |
| ADG409BRZ-REEL7 | −40°C to +85°C | 16-Lead Narrow Body Small Outline Package [SOIC_N] | R-16 |

[1] Z = RoHS Compliant Part

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