Lead-free Green

40V COMPLEMENTARY DUAL ENHANCEMENT MODE MOSFET

Product Summary

Device	$V_{(BR)DSS}$	$R_{DS(on)}$ Max	I_D T_A = 25°C
Q1	40V	28mΩ @ V_{GS}= 10V	7.2A
		49mΩ @ V_{GS}= 4.5V	5.4A
Q2	-40V	50mΩ @ V_{GS}= -10V	-5.2A
		79mΩ @ V_{GS}= -4.5V	-4.7A

Features and Benefits

- Low on-resistance
- Fast switching speed
- **"Lead Free", RoHS Compliant (Note 1)**
- **Halogen and Antimony Free "Green" Device (Note 2)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Description and Applications

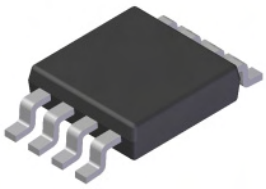
This MOSFET has been designed to minimize the on-state resistance and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- Motor control
- Backlighting
- DC-DC Converters
- Power management functions

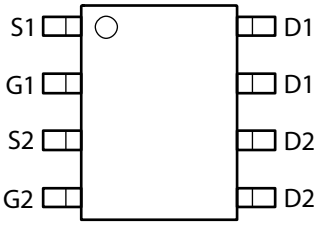
Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0 (Note 1)
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals Connections: See diagram below
- Terminals: Finish - Matte Tin annealed over Copper lead frame. Solderable per MIL-STD-202, Method 208
- Weight: 0.074 grams (approximate)

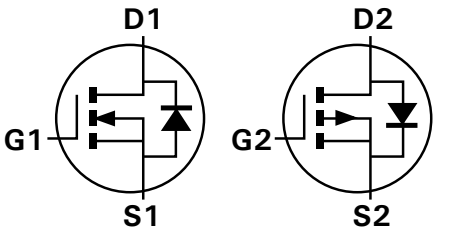
SO-8



Top View



Top View



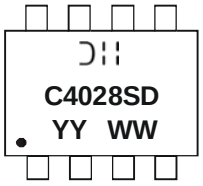
Equivalent Circuit

Ordering Information (Note 3)

Product	Marking	Reel size (inches)	Tape width (mm)	Quantity per reel
DMC4028SSD-13	C4028SD	13	12	2,500

Notes:
1. No purposefully added lead.
2. Diodes Inc.'s "Green" policy can be found on our website at http://www.diodes.com.
3. For packaging details, go to our website at http://www.diodes.com.

Marking Information



= Manufacturer's Marking
C4028SD = Product Type Marking Code
YYWW = Date Code Marking
YY = Year (ex: 09 = 2009)
WW = Week (01 - 53)

Maximum Ratings @T_A = 25°C unless otherwise specified

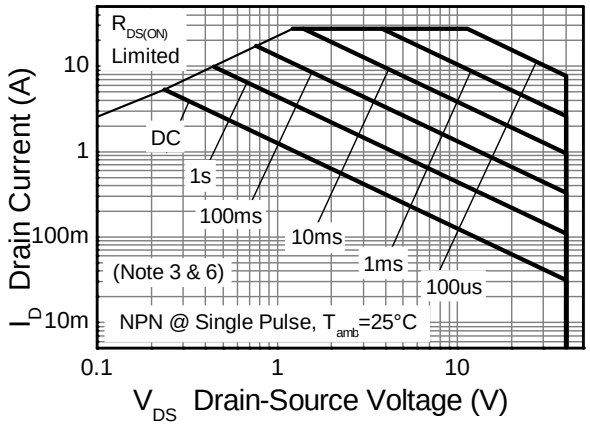
Characteristic			Symbol	N-Channel - Q1	P-Channel - Q2	Units
Drain-Source Voltage			V_{DSS}	40	-40	V
Gate-Source Voltage		(Note 4)	V_{GSS}	±20	±20	V
Continuous Drain Current	V_{GS} = 10V	(Notes 6 & 8)	I_D	7.2	5.2	A
		T_A = 70°C (Notes 6 & 8)		5.5	4.2	
		(Notes 5 & 8)		5.4	4	
		(Notes 5 & 9)		6.5	4.8	
Pulsed Drain Current	V_{GS} = 10V	(Notes 7 & 8)	I_{DM}	27.3	20.4	A
Continuous Source Current (Body diode)		(Notes 6 & 8)	I_S	3.35	3.15	A
Pulsed Source Current (Body diode)		(Notes 7 & 8)	I_{SM}	27.3	20.4	A

Thermal Characteristics @T_A = 25°C unless otherwise specified

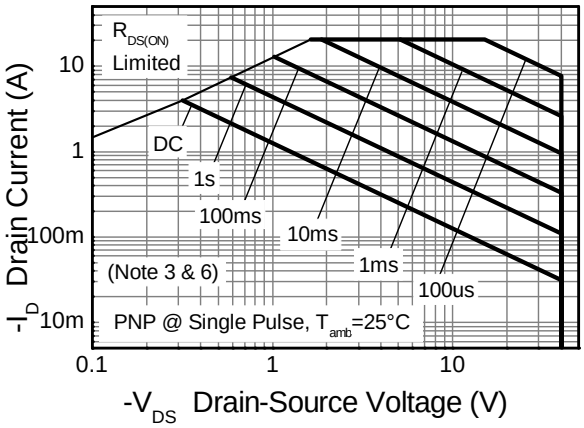
Characteristic		Symbol	N-Channel - Q1	P-Channel - Q2	Unit
Power Dissipation Linear Derating Factor	(Notes 5 & 8)	P_D	1.25 10		W mW/°C
	(Notes 5 & 9)		1.8 14.3		
	(Notes 6 & 8)		2.16 17.2		
Thermal Resistance, Junction to Ambient	(Notes 5 & 8)	$R_{\theta JA}$	100		°C/W
	(Notes 5 & 9)		70		
	(Notes 6 & 8)		58		
Thermal Resistance, Junction to Lead	(Notes 8 & 10)	$R_{\theta JL}$	53	53	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150		°C

Notes:
4. AEC-Q101 V_{GS} maximum is ±16V.
5. For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
6. Same as note (5), except the device is measured at t ≤ 10 sec.
7. Same as note (5), except the device is pulsed with D= 0.02 and pulse width 300 µs. The pulse current is limited by the maximum junction temperature.
8. For a dual device with one active die.
9. For a device with two active die running at equal power.
10. Thermal resistance from junction to solder-point (at the end of the drain lead).

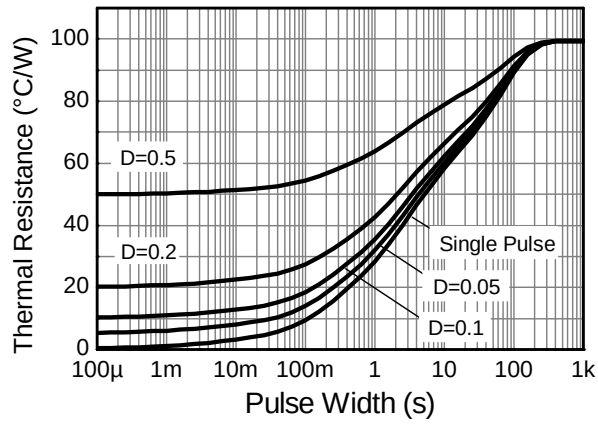
Thermal Characteristics



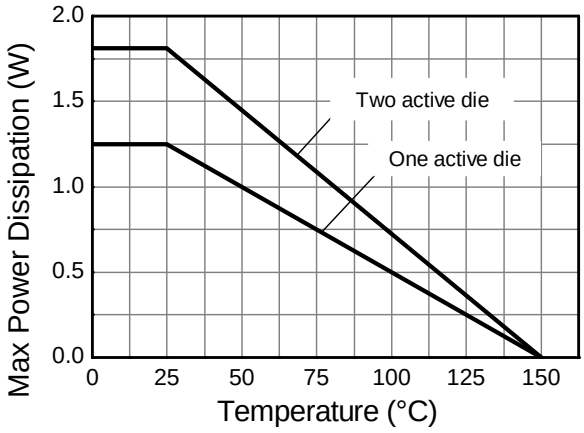
N-channel Safe Operating Area



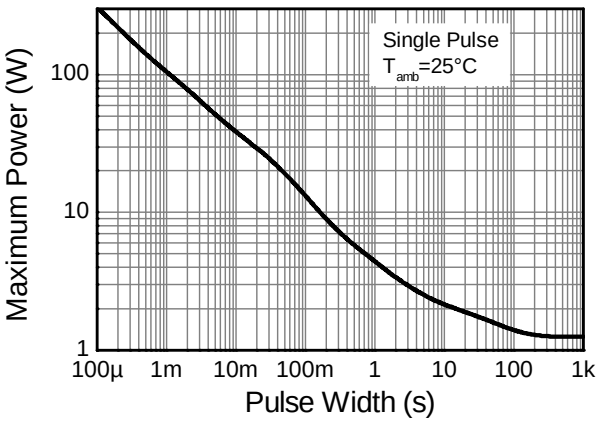
P-channel Safe Operating Area



Transient Thermal Impedance



Derating Curve



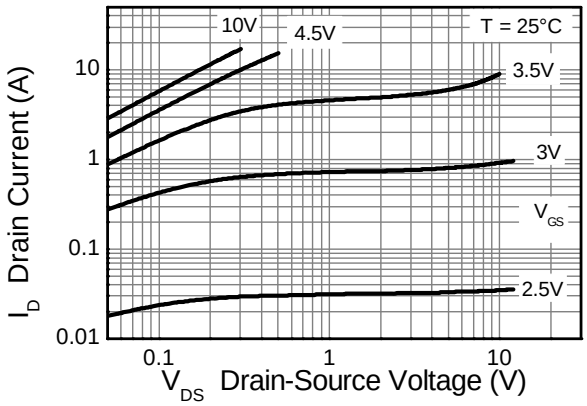
Pulse Power Dissipation

Electrical Characteristics – Q1 N-Channel T_A = 25°C unless otherwise specified

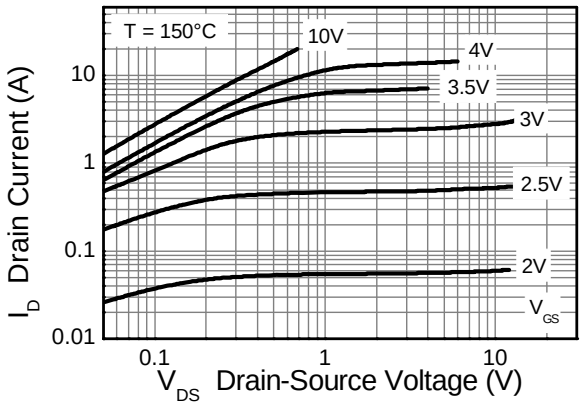
Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	40	—	—	V	I_D = 250μA, V_{GS} = 0V
Zero Gate Voltage Drain Current	I_{DSS}	—	—	0.5	μA	V_{DS} = 40V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(th)}$	1.0	—	3.0	V	I_D = 250μA, V_{DS} = V_{GS}
Static Drain-Source On-Resistance (Note 11)	$R_{DS\ (ON)}$	—	0.018	0.028	Ω	V_{GS} = 10V, I_D = 6A
			0.033	0.049		V_{GS} = 4.5V, I_D = 5A
Forward Transconductance (Notes 11 & 12)	g_{fs}	—	22.8	—	S	V_{DS} = 15V, I_D = 6A
Diode Forward Voltage (Note 11)	V_{SD}	—	0.845	1.1	V	I_S = 6A, V_{GS} = 0V
Reverse recovery time (Note 12)	t_{rr}		135	—	ns	I_S = 6A, di/dt = 100A/μs
Reverse recovery charge (Note 12)	Q_{rr}	—	799	—	nC	
DYNAMIC CHARACTERISTICS (Note 12)						
Input Capacitance	C_{iss}	—	604	—	pF	V_{DS} = 20V, V_{GS} = 0V f = 1MHz
Output Capacitance	C_{oss}	—	106	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	59.6	—	pF	
Total Gate Charge (Note 13)	Q_g	—	6.5	—	nC	V_{GS} = 4.5V; V_{DS} = 20V, I_D = 6A
Total Gate Charge (Note 13)	Q_g	—	12.9	—	nC	V_{GS} = 10V; V_{DS} = 20V, I_D = 6A
Gate-Source Charge (Note 13)	Q_{gs}	—	2.3	—	nC	
Gate-Drain Charge (Note 13)	Q_{gd}	—	3.6	—	nC	
Turn-On Delay Time (Note 13)	$t_{D(on)}$	—	4.2	—	ns	V_{DD} = 20V, V_{GS} = 10V I_D = 6A, $R_G \cong 6.0\Omega$
Turn-On Rise Time (Note 13)	t_r	—	12.4	—	ns	
Turn-Off Delay Time (Note 13)	$t_{D(off)}$	—	13.8	—	ns	
Turn-Off Fall Time (Note 13)	t_f	—	10.7	—	ns	

Notes: 11. Measured under pulsed conditions. Pulse width ≤ 300μs; duty cycle ≤ 2%
12. For design aid only, not subject to production testing.
13. Switching characteristics are independent of operating junction temperatures.

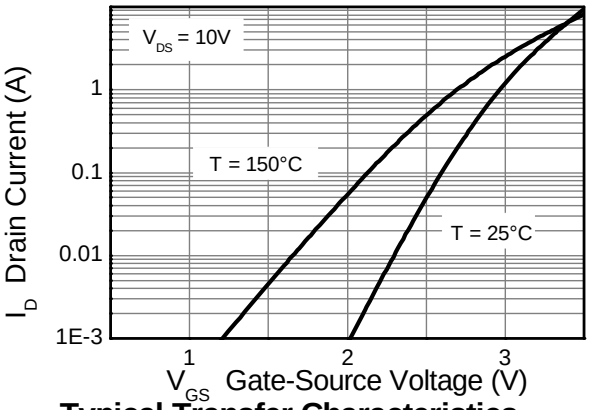
Typical Characteristics – Q1 N-Channel



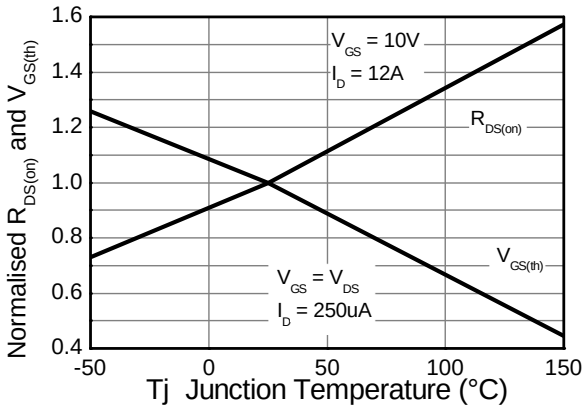
Output Characteristics



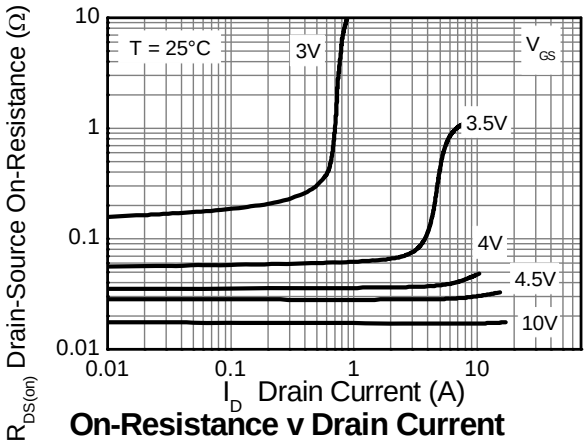
Output Characteristics



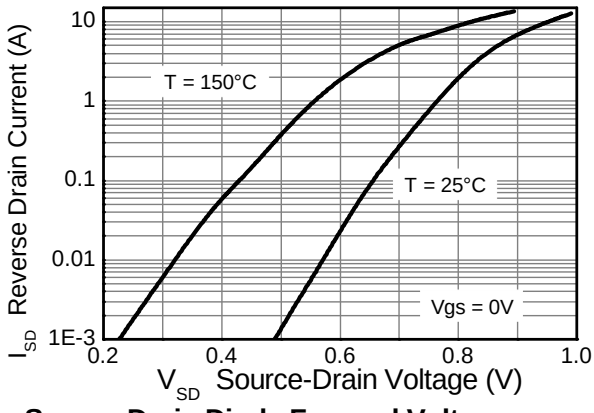
Typical Transfer Characteristics



Normalised Curves v Temperature

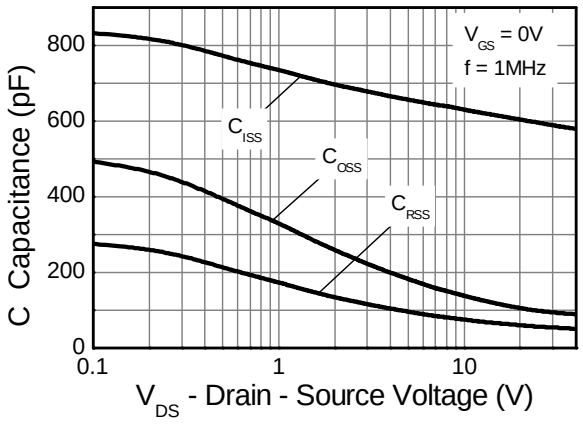


On-Resistance v Drain Current

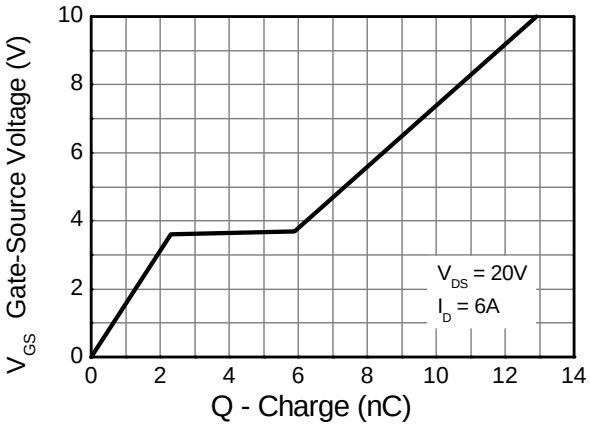


Source-Drain Diode Forward Voltage

Typical Characteristics – Q1 N-Channel - continued

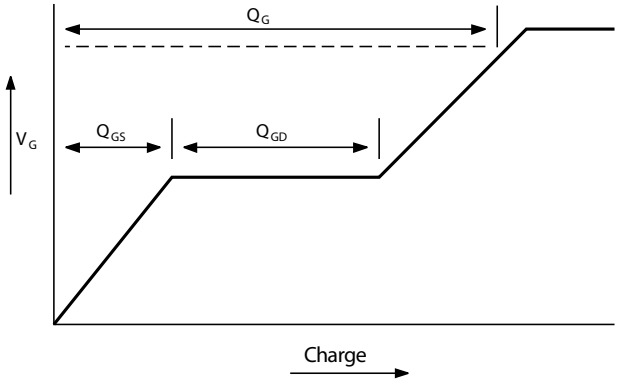


Capacitance v Drain-Source Voltage

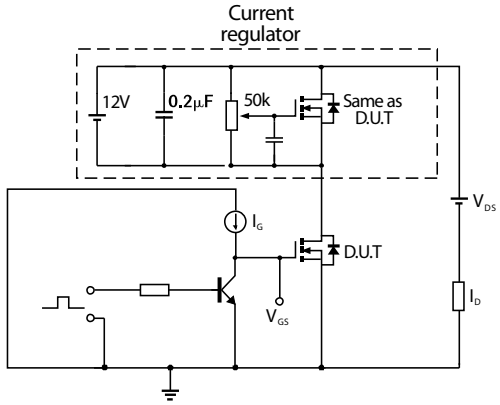


Gate-Source Voltage v Gate Charge

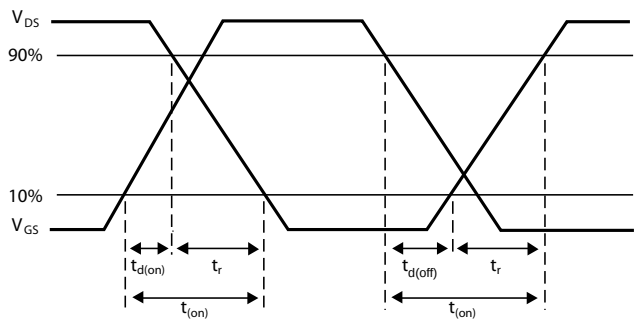
Test Circuits – Q1 N-Channel



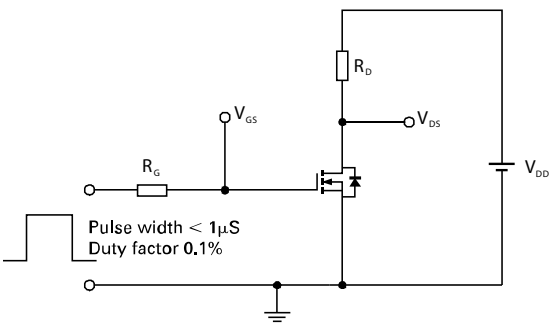
Basic gate charge waveform



Gate charge test circuit



Switching time waveforms



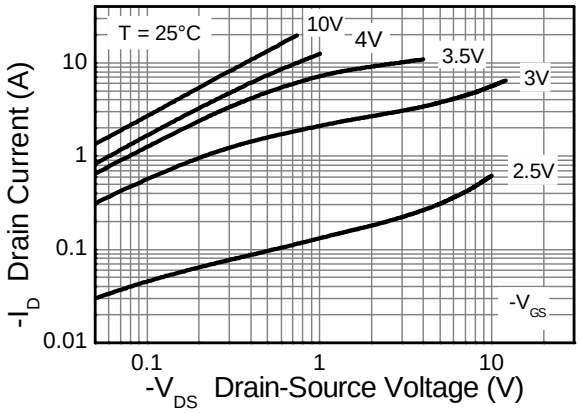
Switching time test circuit

Electrical Characteristics – Q2 P-Channel @T_A = 25°C unless otherwise specified

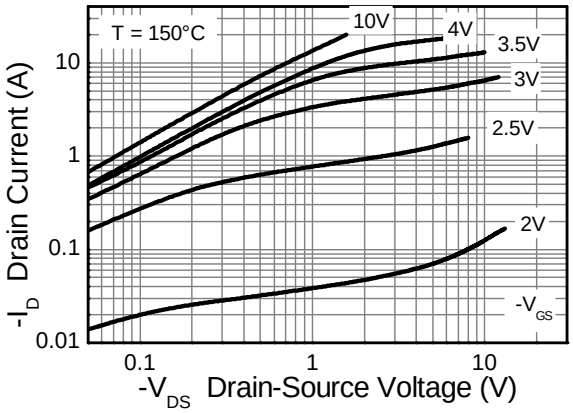
Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	-40	–	–	V	I_D = -250μA, V_{GS} = 0V
Zero Gate Voltage Drain Current	I_{DSS}	–	–	-0.5	A	V_{DS} = -40V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	–	–	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(th)}$	-1.0	–	-3.0	V	I_D = -250μA, V_{DS} = V_{GS}
Static Drain-Source On-Resistance (Note 14)	$R_{DS\ (ON)}$	–	0.039	0.050	Ω	V_{GS} = -10V, I_D = -6A
			0.060	0.079		V_{GS} = -4.5V, I_D = -5A
Forward Transconductance (Notes 14 & 15)	g_{fs}	–	16.6	–	S	V_{DS} = -15V, I_D = -6A
Diode Forward Voltage (Note 4)	V_{SD}	–	-0.865	-1.1	V	I_S = -6A, V_{GS} = 0V
Reverse recovery time (Note 15)	t_{rr}	–	138	–	ns	I_S = -6A, di/dt = 100A/μs
Reverse recovery charge (Note 15)	Q_{rr}	–	841	–	nC	
DYNAMIC CHARACTERISTICS (Note 15)						
Input Capacitance	C_{iss}	–	674	–	pF	V_{DS} = -20V, V_{GS} = 0V f = 1MHz
Output Capacitance	C_{oss}	–	115	–	pF	
Reverse Transfer Capacitance	C_{rss}	–	67.7	–	pF	
Total Gate Charge (Note 16)	Q_g	–	7.0	–	nC	V_{GS} = -4.5V V_{DS} = -20V I_D = -6A
Total Gate Charge (Note 16)	Q_g	–	14	–	nC	V_{GS} = -10V
Gate-Source Charge (Note 16)	Q_{gs}	–	2.2	–	nC	
Gate-Drain Charge (Note 16)	Q_{gd}	–	3.7	–	nC	
Turn-On Delay Time (Note 16)	$t_{D(on)}$	–	2.3	–	ns	V_{DD} = -20V, V_{GS} = -10V I_D = -6A, $R_G \cong$ 6.0Ω
Turn-On Rise Time (Note 16)	t_r	–	14.1	–	ns	
Turn-Off Delay Time (Note 16)	$t_{D(off)}$	–	25.1	–	ns	
Turn-Off Fall Time (Note 16)	t_f	–	14.3	–	ns	

Notes: 14. Measured under pulsed conditions. Pulse width ≤ 300μs; duty cycle ≤ 2%
15. For design aid only, not subject to production testing.
16. Switching characteristics are independent of operating junction temperatures.

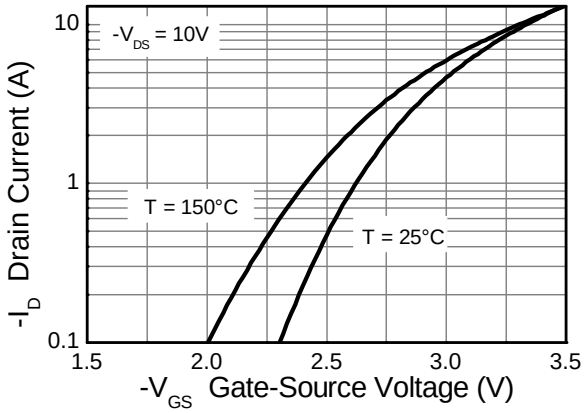
Typical Characteristics – Q2 P-Channel



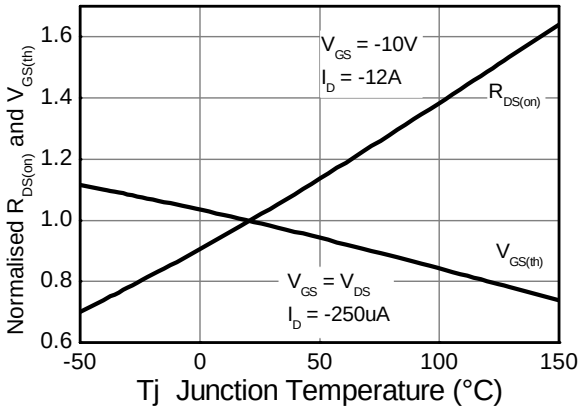
Output Characteristics



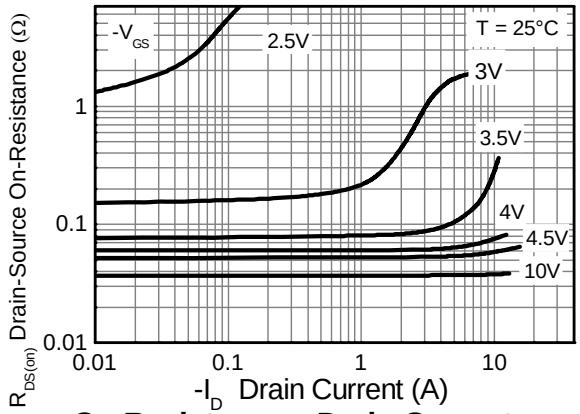
Output Characteristics



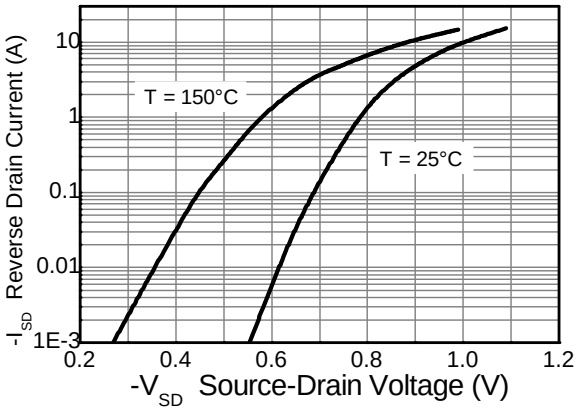
Typical Transfer Characteristics



Normalised Curves v Temperature

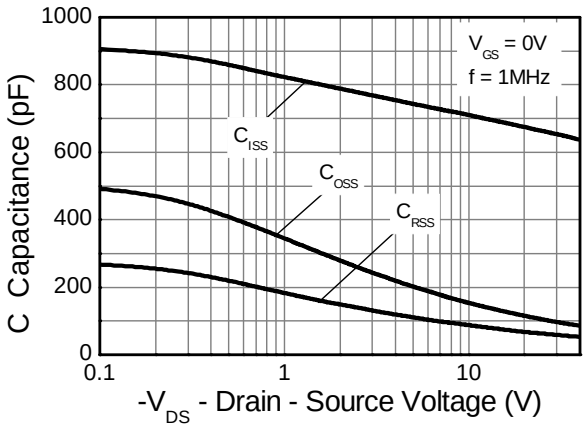


On-Resistance v Drain Current

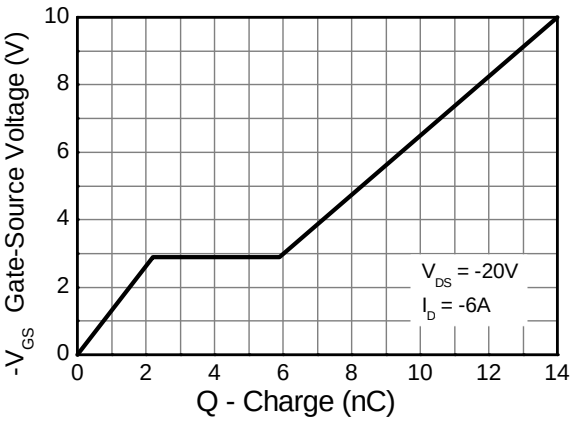


Source-Drain Diode Forward Voltage

Typical Characteristics – Q2 P-Channel - continued

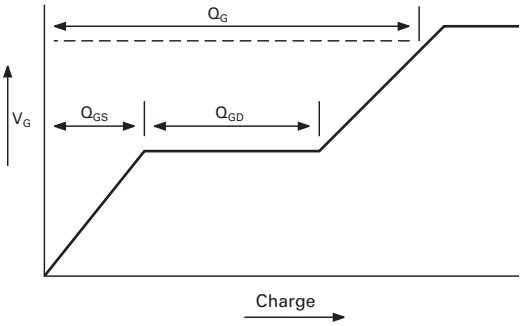


Capacitance v Drain-Source Voltage

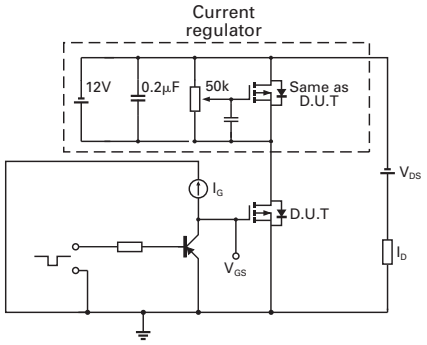


Gate-Source Voltage v Gate Charge

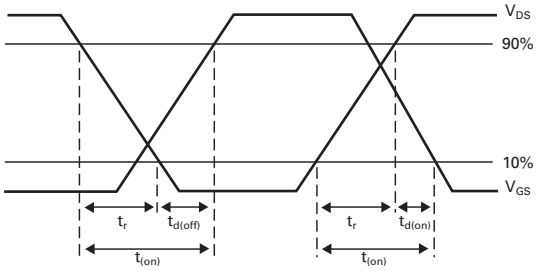
Test Circuits – Q2 P-Channel



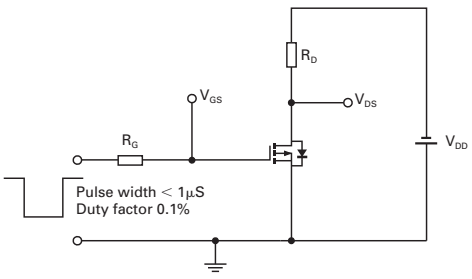
Basic gate charge waveform



Gate charge test circuit

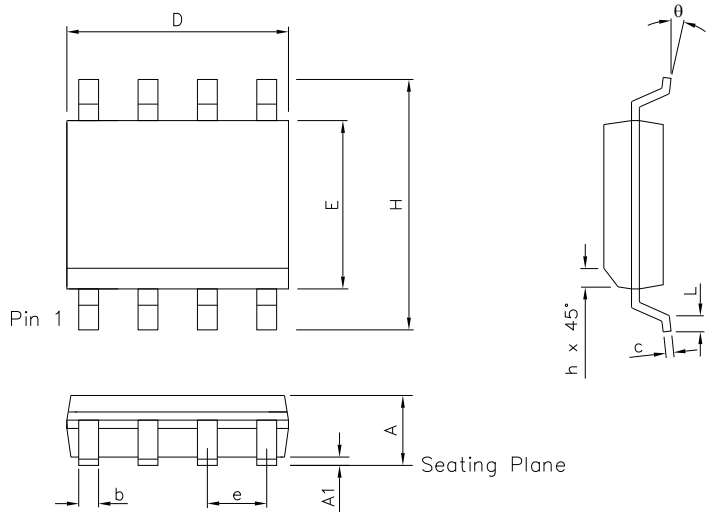


Switching time waveforms



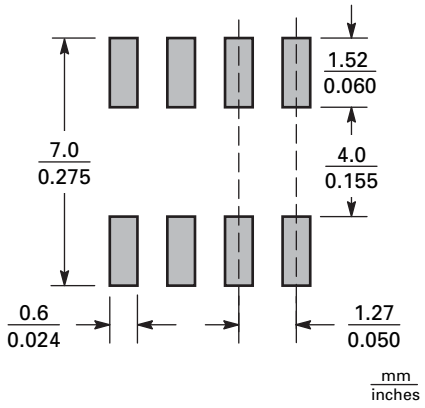
Switching time test circuit

Package Outline Dimensions



DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.053	0.069	1.35	1.75	e	0.050 BSC		1.27 BSC	
A1	0.004	0.010	0.10	0.25	b	0.013	0.020	0.33	0.51
D	0.189	0.197	4.80	5.00	c	0.008	0.010	0.19	0.25
H	0.228	0.244	5.80	6.20	θ	0°	8°	0°	8°
E	0.150	0.157	3.80	4.00	h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27	-	-	-	-	-

Suggested Pad Layout



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