TPS65132 Single Inductor - Dual Output Power Supply

1 Features

- Split-Rail Power Supply
- SIMO (Single-Inductor Multiple-Output) Technology
- >85% Efficiency at I_{OUT} > 10 mA
- >83% Efficiency at I_{OUT} > 10 mA (TPS65132Wx)
- 2.5-V to 5.5-V Input Voltage Range
- Undervoltage Lockout Rising/Falling
- Programmable Output Voltages
- Positive Output Voltage Range : 4 V to 6 V (0.1-V step)
- Negative Output Voltage Range: –6 V to –4 V (0.1-V step)
- 1% Output Voltage Accuracy
- Maximum Output Current: 150 mA (TPS65132Sx)
- Programmable Power-Up and Power-Down Sequencing (TPS65132Sx)
- Programmable Active Discharge
- Internal EEPROM Type Memory (1000× Re-programmable)
- Excellent Line Regulation
- Advanced Power-Save Mode for Light-Load Efficiency
- Thermal Shutdown
- 15-Ball CSP Package
- 20-Pins QFN Package

2 Applications

- General Dual Power Supply Applications
- Operational Amplifier Supply (Including Audio)
- DAC Supply
- TFT LCD Smartphones
- TFT LCD Tablets
- OLED Displays

3 Description

The TPS65132 is designed to support general positive/negative driven applications. The device uses a single inductor scheme in order to provide the user the smallest solution size possible as well as high efficiency. With its input voltage range of 2.5 V to 5.5 V, it is optimized for products powered by single-cell batteries (Li-Ion, Ni-Li, Li-Polymer) and output currents up to 80 mA for the A- and B-version, and up to 150 mA for the S-version. The device is delivered in a WCSP package of 15 balls.

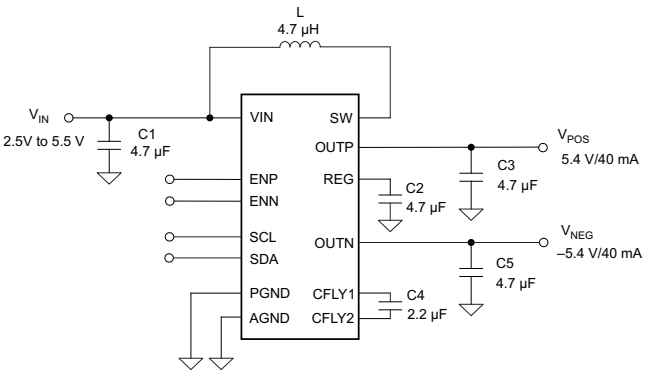
Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM.)
TPS65132	DSBGA (15)	2.11 mm × 1.51 mm
TPS65132S (2)	DSBGA (15)	2.11 mm × 1.51 mm
TPS65132W	WQFN (20)	4.00 mm × 3.00 mm

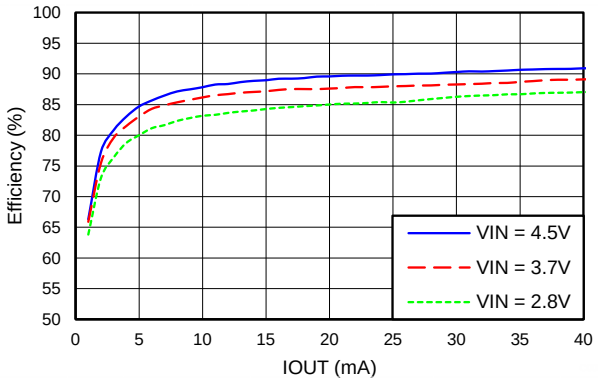
(1) For all available packages, see the orderable addendum at the end of the datasheet.

(2) Product Preview

Typical Application



Efficiency vs Output Current



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (June 2015) to Revision G — **Page**

- Changed scope figures for Boost Converter switching. ... 13

Changes from Revision E (November 2014) to Revision F — **Page**

- Added high current Feature (150mA) ... 1
- Added TPS65132L1 device to Device Comparison table ... 4
- Added TPS65132T6 device to the Device Comparison Table. ... 4
- Separated LOGIC SCL, SDA spec MIN/MAX from LOGIC EN, ENN, ENP, SYNC spec MIN/MAX ... 9
- Changed DAC Registers section for clarity ... 21
- Added High-current Applications (≤ 150 mA) section ... 43

Changes from Revision D (October 2014) to Revision E — **Page**

- Added TPS65132L0 device to Device Comparison table ... 4

Changes from Revision C (July 2014) to Revision D — **Page**

- Changed package type to industry standard identifier in the Device Information table ... 1

Changes from Revision B (May 2014) to Revision C — **Page**

- Added note to Device Comparison Table ... 4
- Added reference to Power-Down And Discharge (LDO) and Power-Down And Discharge (CPN) ... 12
- Added "Power-Down And Discharge (LDO) shows the V_{POS} active discharge behavior of each device variant". ... 14
- Added Table 1 and various references to it ... 14

- Added "Power-Down And Discharge (CPN) shows the V_{NEG} discharge behavior of each device variant" 16
- Added Table 2 and various references to it 16
- Added note to Figure 22 23

Changes from Revision A (August 2013) to Revision B **Page**

- Formatted to the new data sheet standard 1
- Added new package option (QFN) to Device Information table 1
- Added new package option (QFN) to Pin Configurations section 7
- Added the ESD Ratings table 8

Changes from Original (June 2013) to Revision A **Page**

- Added TPS65132Bx devices to the Device Comparison table 4

5 Device Comparison Table

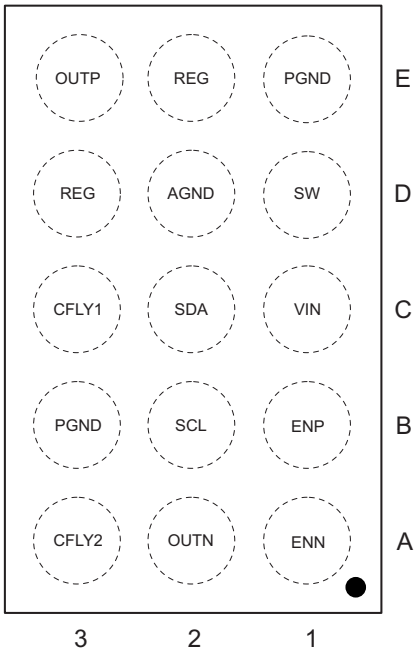
PART NUMBER (1)	DEFAULT			STARTUP TIME VPOS / VNEG (2)	I_{SD}	PACKAGE
	OUTPUT VOLTAGES	I_{OUT_MAX} (3)	ACTIVE DISCHARGE (4)			
TPS65132A	V_{POS} = 5.4 V V_{NEG} = –5.4 V	40 mA	V_{POS} / V_{NEG}	FAST	30 µA	CSP
TPS65132A0	V_{POS} = 5.0 V V_{NEG} = –5.0 V					
TPS65132B	V_{POS} = 5.4 V V_{NEG} = –5.4V	40 mA	V_{POS} / V_{NEG}	FAST	130 nA	CSP
TPS65132B0	V_{POS} = 5.0 V V_{NEG} = –5.0 V					
TPS65132B5	V_{POS} = 5.5 V V_{NEG} = –5.5 V					
TPS65132B2	V_{POS} = 5.2 V V_{NEG} = –5.2 V	40 mA	V_{POS} / V_{NEG}	SLOW	130 nA	CSP
TPS65132L	V_{POS} = 5.4 V V_{NEG} = –5.4 V					
TPS65132L0	V_{POS} = 5.0 V V_{NEG} = –5.0 V					
TPS65132L1 (5)	V_{POS} = 5.1 V V_{NEG} = –5.1 V	40 mA	V_{POS} / V_{NEG}	SLOW	130 nA	CSP
TPS65132T6	V_{POS} = 5.6 V V_{NEG} = –5.6 V	80 mA	V_{POS} / V_{NEG}	SLOW	130 nA	CSP
TPS65132S (5)	V_{POS} = 5.4 V V_{NEG} = –5.4 V	150 mA	V_{POS} / V_{NEG}	SLOW	130 nA	CSP
TPS65132W	V_{POS} = 5.4 V V_{NEG} = –5.4 V	80 mA	V_{POS} / V_{NEG}	SLOW	130 nA	QFN

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com
(2) Please refer to *Power-Up And Soft-Start (LDO)* and *Power-Up And Soft-Start (CPN)* for more details.
(3) For higher output current variant, please contact display_contact@list.ti.com.
(4) See *Power-Down And Discharge (LDO)* and *Power-Down And Discharge (CPN)* for a detailed description of how each device variant implements the active discharge function.
(5) Product preview.

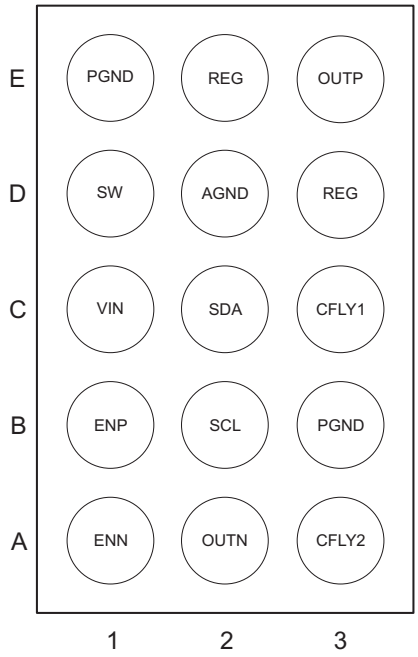
6 Pin Configuration and Functions

YFF Package
15 Bumps

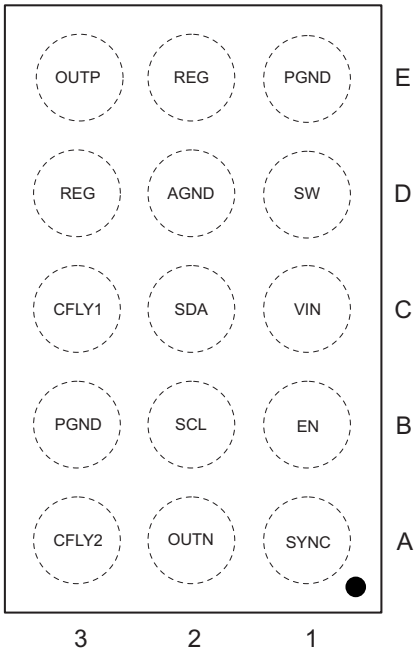
(top view)
TPS65132Ax / Bx / Lx



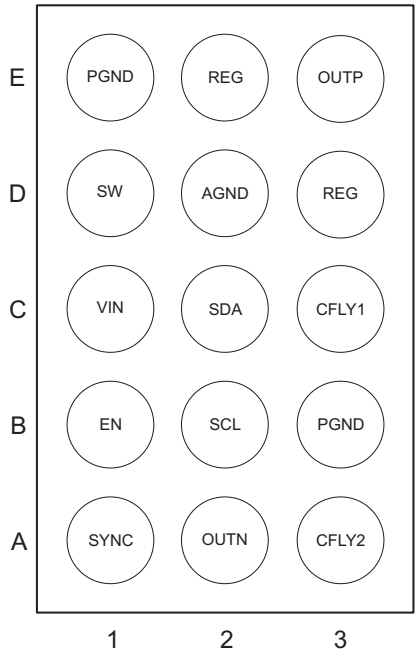
(bottom view)
TPS65132Ax / Bx / Lx



(top view)
TPS65132Sx



(bottom view)
TPS65132Sx

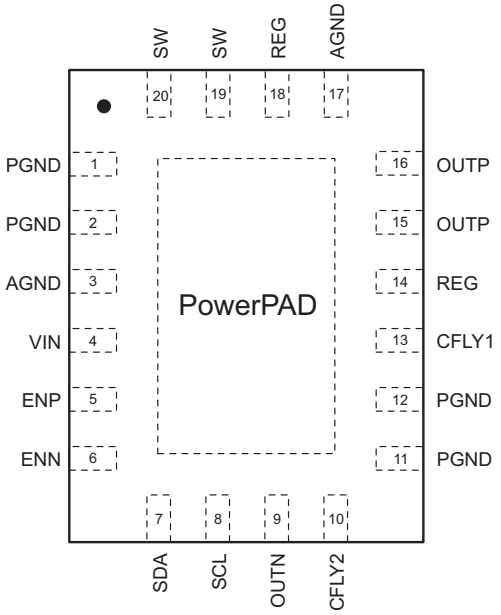


Pin Functions

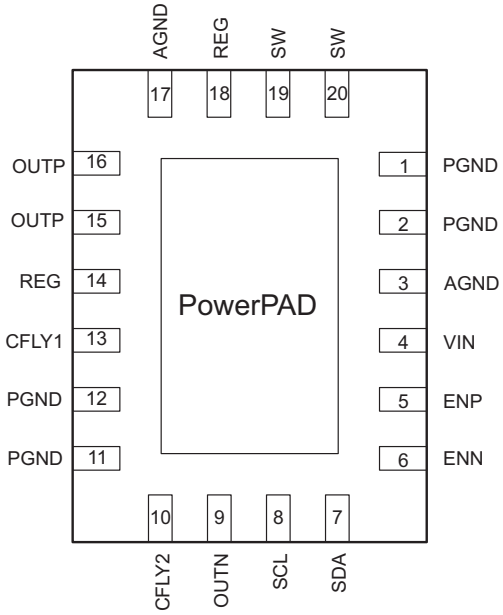
PIN			I/O	DESCRIPTION
NAME	Ax, Bx, Lx	Sx		
AGND	D2	D2	—	Analog ground
CFLY1	C3	C3	I/O	Negative charge pump flying capacitor pin
CFLY2	A3	A3	I/O	Negative charge pump flying capacitor pin
EN	—	B1		Enable pin (sequence programmed)
ENN	A1	—	I	Enable pin for V_{NEG} rail
ENP	B1	B1	I	Enable pin for V_{POS} rail
OUTP	E3	E3	O	Output pin of the LDO (V_{POS})
OUTN	A2	A2	O	Output pin of the negative charge pump (V_{NEG})
PGND	B3	B3	—	Power ground
	E1	E1		
REG	D3	D3	I/O	Boost converter output pin
	E2	E2		
SCL	B2	B2	I/O	I²C interface clock signal pin
SDA	C2	C2	I/O	I²C interface data signal pin
SW	D1	D1	I/O	Switch pin of the boost converter
SYNC	—	A1	I	Synchronization pin. 150 mA current enabled if this pin is pulled HIGH.
VIN	C1	C1	I	Input voltage supply pin

QFN Package
20 Pins

RVC package
(top view)



RVC package
(bottom view)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	Wx		
AGND	3	—	Analog ground
	17		
CFLY1	13	I/O	Negative charge pump flying capacitor pin
CFLY2	10	I/O	Negative charge pump flying capacitor pin
ENN	6	I	Enable pin for V_{NEG} rail
ENP	5	I	Enable pin for V_{POS} rail
OUTP	16	O	Output pin of the LDO (V_{POS})
	15		
OUTN	9	O	Output pin of the negative charge pump (V_{NEG})
PGND	1	—	Power ground
	2		
	11		
	12		
REG	14	I/O	Boost converter output pin
	18		
SCL	8	I/O	I²C interface clock signal pin
SDA	7	I/O	I²C interface data signal pin
SW	19	I/O	Switch pin of the boost converter
	20		
VIN	4	I	Input voltage supply pin

7 Specifications

7.1 Absolute Maximum Ratings[1][2]

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Voltage range	CFLY1, EN, ENN, ENP, OUTP, REG, SCL, SDA, SW, SYNC, VIN	–0.3	7	V
	CFLY2, OUTN	–7	0.3	V
Continuous total power dissipation		See *Thermal Information*		
Operating junction temperature, T_J		–40	150	°C
Operating ambient temperature, T_A		–40	85	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to ground.

7.2 ESD Ratings

		VALUE	UNIT
V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
	Charged device model (CDM) per JEDEC specification JESD22-C101, all pins[2]	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	2.5		5.5	V
L	Inductor[1]	2.2		4.7	µH
C_{IN}	Input capacitor[1][2]	4.7			µF
C_{FLY}	Flying capacitor[1][2]	2.2			µF
C_{OUTP}, C_{OUTN}, C_{REG}	Output capacitors[1][2]	4.7			µF
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

(1) Please see Detailed Description section for further information.
(2) X7R (or better dielectric material) is recommended.

7.4 Thermal Information

THERMAL METRIC[1]		TPS65132		UNIT
		YFF	RVC	
		(15) BALLS	(20) PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	76.5	39.0	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	0.2	42.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44	13.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.6	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	43.4	13.6	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	N/A	3.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

V_{IN} = 3.7 V, EN = ENN = ENP = V_{IN}, V_{POS} = 5.4 V, V_{NEG} = –5.4 V, T_A = –40°C to 85°C; typical values are at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{IN}	Input voltage range		2.5		5.5	V
V_{UVLO}	Undervoltage lockout threshold	V_{IN} rising	2.3		2.5	V
		V_{IN} falling	2.1		2.3	
I_Q	Quiescent current			0.54		mA
	Thermal shutdown			140		°C
	Thermal shutdown hysteresis			5		°C
LOGIC EN, ENN, ENP, SYNC						
V_{IH}	High level input voltage	V_{IN} = 2.5 V to 5.5 V	1.1			V
V_{IL}	Low level input voltage				0.4	
R_{EN}	Pulldown resistors			200		kΩ
LOGIC SCL, SDA						
V_{IH}	High level input voltage	V_{IN} = 2.5 V to 5.5 V	1.1			V
V_{IL}	Low level input voltage				0.54	
BOOST CONVERTER						
I_{LIM}	Boost converter valley current limit		0.9	1.2	1.5	A
f_{SW}	Boost converter switching frequency		1.35	1.80	2.25	MHz
LDO OUTPUT V_{POS}						
V_{POS}	Positive output voltage range		4.0		6.0	V
V_{POS_acc}	Positive output voltage accuracy		–1 %		+1 %	
I_{POS}	Positive output current capability		200			mA
V_{DO}	Dropout voltage	V_{REG} = $V_{POS(NOM)}$ = 5.4V, I_{OUT} = 150 mA		160		mV
	Line regulation	V_{IN} = 2.5 V to 5.5 V, I_{OUT} = 40 mA		2.7		mV
	Load regulation	ΔI_{OUT} = 80 mA		3.4		%/A
R_D	Discharge resistor			70		Ω
NEGATIVE CHARGE PUMP OUTPUT V_{NEG}						
V_{NEG}	Negative output voltage range		–6.0		–4.0	V
V_{NEG_acc}	Negative output voltage accuracy		–1 %		+1 %	
I_{NEG}	Negative output current capability	Smartphone MODE	40			mA
		Tablet MODE	80			
I_{NEG}	Negative output current capability	TPS65132Sx, SYNC = HIGH	150			mA
f_{OSC}	Negative charge pump switching frequency		0.8	1.0	1.2	MHz
	Line regulation	V_{IN} = 2.5 V to 5.5 V, I_{OUT} = 40 mA		3.3		mV
	Load regulation	ΔI_{OUT} = 80 mA		6.1		%/A
R_D	Discharge resistor			20		Ω

7.6 I²C Interface Timing Requirements / Characteristics (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency	Standard mode			100	kHz
		Fast mode			400	kHz
t_{LOW}	LOW period of the SCL clock	Standard mode	4.7			µs
		Fast mode	1.3			µs
t_{HIGH}	HIGH period of the SCL clock	Standard mode	4.0			µs
		Fast mode	600			ns
t_{BUF}	Bus free time between a STOP and START condition	Standard mode	4.7			µs
		Fast mode	1.3			µs
$t_{hd;STA}$	Hold time for a repeated START condition	Standard mode	4.0			µs
		Fast mode	600			ns
$t_{su;STA}$	Setup time for a repeated START condition	Standard mode	4.7			µs
		Fast mode	600			ns
$t_{su;DAT}$	Data setup time	Standard mode	250			ns
		Fast mode	100			ns
$t_{hd;DAT}$	Data hold time	Standard mode	0.05		3.45	µs
		Fast mode	0.05		0.9	µs
t_{RCL1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	Standard mode	20 + 0.1C_B		1000	ns
		Fast mode	20 + 0.1C_B		1000	ns
t_{RCL}	Rise time of SCL signal	Standard mode	20 + 0.1C_B		1000	ns
		Fast mode	20 + 0.1C_B		300	ns
t_{FCL}	Fall time of SCL signal	Standard mode	20 + 0.1C_B		300	ns
		Fast mode	20 + 0.1C_B		300	ns
t_{RDA}	Rise time of SDA signal	Standard mode	20 + 0.1C_B		1000	ns
		Fast mode	20 + 0.1C_B		300	ns
t_{FDA}	Fall time of SDA signal	Standard mode	20 + 0.1C_B		300	ns
		Fast mode	20 + 0.1C_B		300	ns
$t_{su;STO}$	Setup time for STOP condition	Standard mode	4.0			µs
		Fast mode	600			ns
C_B	Capacitive load for SDA and SCL				0.4	nF

(1) Industry standard I²C timing characteristics acoording to I²C-Bus Specification, Version 2.1, January 2000. Not tested in production.

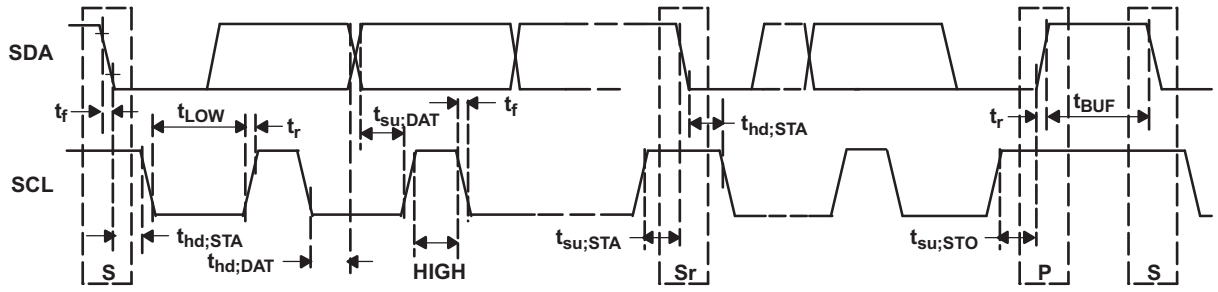


Figure 1. Serial Interface Timing For F/S-Mode

7.7 Typical Characteristics

V_{IN}= 3.7 V, V_{POS}= 5.4 V, V_{NEG}= –5.4 V, unless otherwise noted

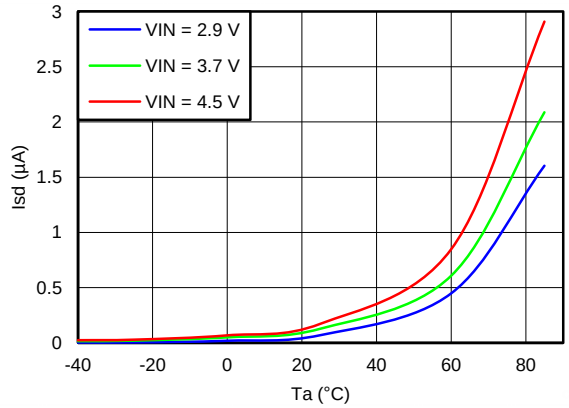


Figure 2. Shutdown Current

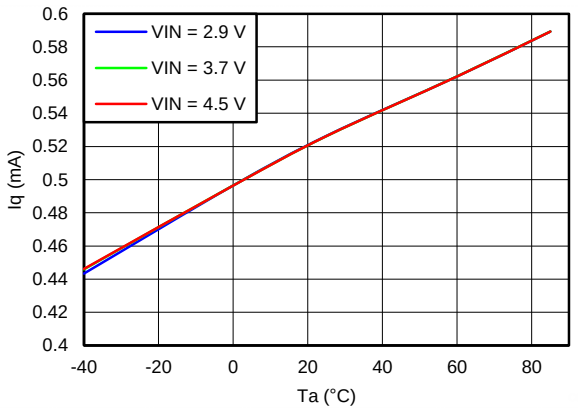


Figure 3. Quiescent Current

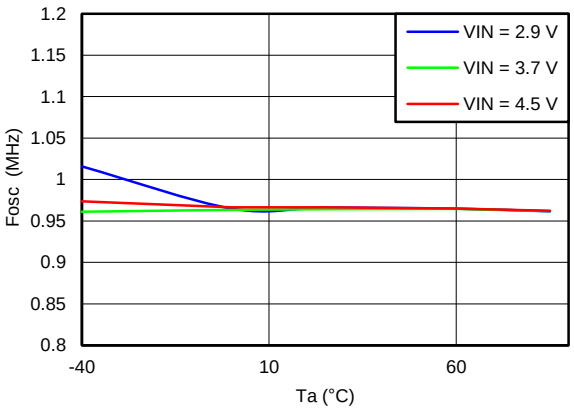


Figure 4. Main Oscillator Frequency

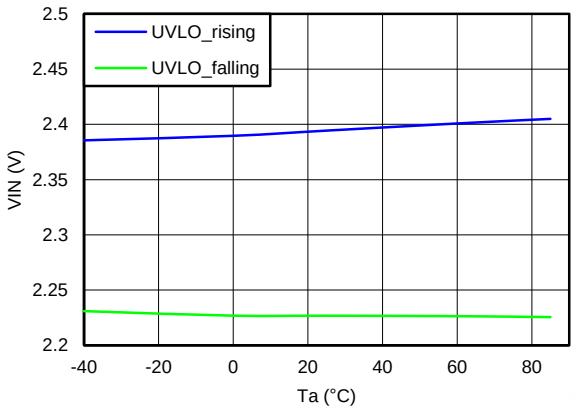


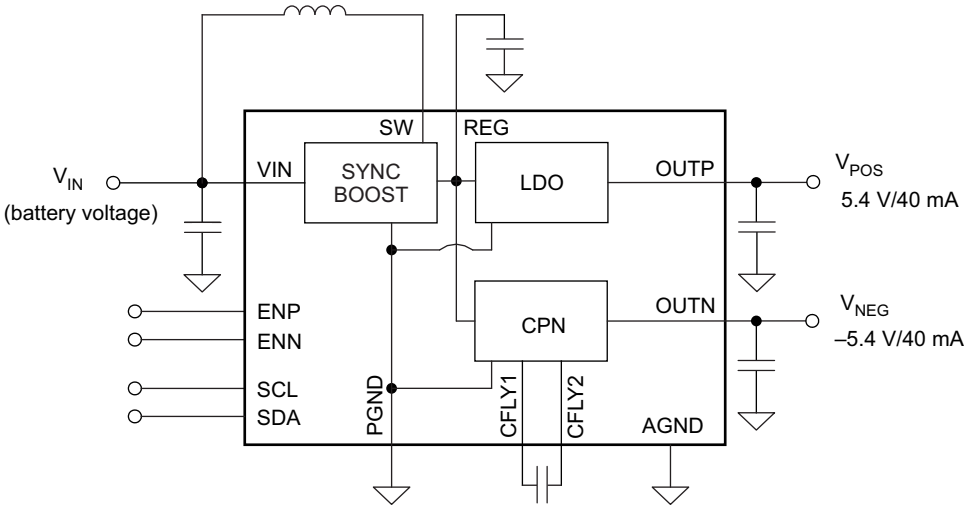
Figure 5. UVLO

8 Detailed Description

8.1 Overview

The TPS65132, supporting input voltage range from 2.5 V to 5.5 V, operates with a single inductor scheme to provide a high efficiency with a small solution size. The synchronous boost converter generates a positive voltage that is regulated down by an integrated LDO, providing the positive supply rail (V_{POS}). The negative supply rail (V_{NEG}) is generated by an integrated negative charge pump (or CPN) driven from the boost converter output pin REG. The operating mode can be selected between Smartphone and Tablet in order to select the necessary output current capability and to get the best efficiency possible based on the application. The device topology allows a 100% asymmetry of the output currents.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Undervoltage Lockout (UVLO)

The TPS65132 integrates an undervoltage lockout block (UVLO) that enables the device once the voltage on the VIN pin exceeds the UVLO threshold (2.5 V maximum). No output voltage will however be generated as long as the enable signals are not pulled HIGH. The device, as well as all converters (boost converter, LDO, CPN), will be disabled as soon as the V_{IN} voltage falls below the UVLO threshold. The UVLO threshold is designed in a way that the TPS65132 will continue operating as long as V_{IN} stays above 2.3 V. This guarantees a proper operation even in the event of extensive line transients when the battery gets suddenly heavily loaded.

For TPS65132Ax, a 40 ms delay is starting as soon as the UVLO threshold is reached. This delay prevents the device to be disabled and enabled by an unwanted VIN voltage spike. Once this delay has passed, the output rails can be enabled and disabled as desired with the enable signals without any delay.

8.3.2 Active Discharge

An active discharge of the positive rail and/or the negative rail can be programmed (DISP and DISN bits respectively - refer to *DAC Registers*). If programmed to be active, the discharge will occur at power down, when the enable signals go LOW (Figure 41 and Figure 42 for TPS65132Ax, Bx, Lx, Wx — Figure 42 and Figure 41 for TPS65132Sx). See *Power-Down And Discharge (LDO)* and *Power-Down And Discharge (CPN)* for a detailed description of how each device variant implements the active discharge function.

Feature Description (continued)

8.3.3 Boost Converter

8.3.3.1 Boost Converter Operation

The synchronous boost converter uses a current mode topology and operates at a quasi-fixed frequency of typically 1.8 MHz, allowing chip inductors such as 2.2 µH or 4.7 µH to be used. The converter is internally compensated and provides a regulated output voltage automatically adjusted depending on the programmed V_{POS} and V_{NEG} voltages. The boost converter operates either in continuous conduction mode (CCM) or Pulse Frequency Modulation mode (PFM), depending on the load current in order to provide the highest efficiency possible. The switch node waveforms for CCM and DCM operation are shown in Figure 6 and Figure 7.

8.3.3.2 Power-Up And Soft-Start (Boost Converter)

The boost converter starts switching as soon as the enable signal is pulled HIGH and the voltage on VIN pin is above the UVLO threshold. For TPS65132Ax, in the case where the enable signal is already HIGH when V_{IN} reaches the UVLO threshold, the boost converter will only start switching after a 40 ms delay has passed (see *Undervoltage Lockout (UVLO)*).

The boost converter starts up with an integrated soft-start to avoid drawing excessive inrush current from the supply. The output voltage V_{REG} is slowly ramped up to its target value. Typical startup waveforms are shown in Figure 37 and Figure 39.

8.3.3.3 Power-Down (Boost Converter)

The boost converter stops switching when V_{IN} is below the UVLO threshold or when both output rails are disabled. For example, due to a special sequencing, the LDO might still be operating while the CPN is already disabled, in which case, the boost will continue operating until the LDO has been disabled. Typical power-down waveforms are shown in Figure 38 and Figure 40.

8.3.3.4 Isolation (Boost Converter)

The boost converter output (REG) is isolated from the input supply V_{IN}, provinding a true shutdown.

8.3.3.5 Output Voltage (Boost Converter)

The output voltage of the boost converter is automatically adjusted depending on the programmed V_{POS} and V_{NEG} voltages.

8.3.3.6 Advanced Power-Save Mode For Light-Load Efficiency And PFM

The TPS65132 device integrates a power save mode to improve efficiency at light load. In power save mode the converter stops switching when the inductor current reaches 0 A. The device resumes its switching activity with one or more pulses once the V_{REG} voltage falls below its regulation level, and goes again into power save mode once the inductor current reaches 0 A. The pulse duration remains constant, but the frequency of these pulses varies according to the output load. This operating mode is also known as Pulse Frequency Modulation or PFM. Figure 6 provides plots of the inductor current and the switch node in PFM mode.

Feature Description (continued)

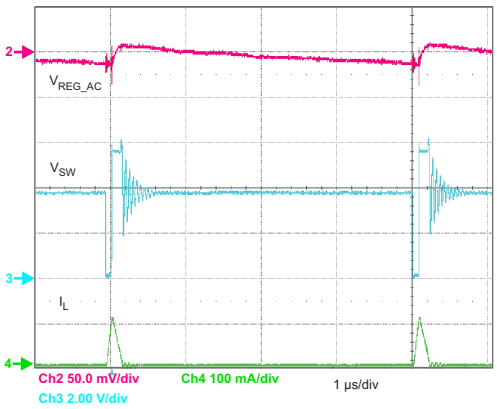


Figure 6. Boost Converter - Light Load (1 mA)

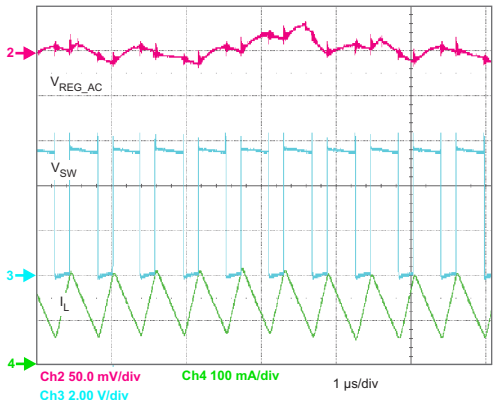


Figure 7. Boost Converter — Heavy Load (40 mA)

8.3.4 LDO Regulator

8.3.4.1 LDO Operation

The Low Dropout regulator (or LDO) generates the positive voltage rail V_{POS} by regulating down the output voltage of the boost converter (V_{REG}). Its inherent power supply rejection helps filtering the output ripple of the boost converter in order to provide on OUTP pin a clean voltage, e.g. to supply the source driver IC of the display.

8.3.4.2 Power-Up And Soft-Start (LDO)

The LDO starts operating as soon as the ENP signal is pulled HIGH, V_{IN} voltage is above the UVLO threshold and the boost converter has reached its Power Good threshold.

In the case where the enable signal is already HIGH when V_{IN} exceeds the UVLO threshold, the boost converter will start first and the LDO will only start after the boost converter has reached its target voltage. For TPS65132Ax, the boost will start after the 40 ms delay has passed (see *Undervoltage Lockout (UVLO)*).

The LDO integrates a soft-start that slowly ramps up its output voltage V_{POS} regardless of the output capacitor and the target voltage, as long as the LDO current limit is not reached. For TPS65132Ax and TPS65132Bx (except TPS65132B2), the typical startup time is 140 µs. For TPS65132B2, TPS65132Lx, TPS65132Wx, the typical ramp-up time is 500 µs and the inrush current is also reduced by a factor of 3. Typical startup waveforms are shown in Figure 37 to Figure 39.

8.3.4.3 Power-Down And Discharge (LDO)

The LDO stops operating when V_{IN} is below the UVLO threshold or when ENP is pulled LOW.

Or when EN is pulled LOW in the TPS65132Sx, and the internal sequencing has passed.

The positive rail can be actively discharged to GND during power-down if required. A discharge selection bit is available to enable or disable this function. See for more details, as well as waveforms on Figure 41 and Figure 42. Table 1 shows the V_{POS} active discharge behavior of each device variant.

Table 1. V_{POS} Active Discharge Behavior

PART NUMBER	V_{IN}	ENP	ENN	V_{POS} DISCHARGE
TPS65132Ax	< V_{UVLO}	Don't Care	Don't Care	On
	> V_{UVLO}	Low	Low	Determined by DISP bit
		Low	High	Determined by DISP bit
		High	Low	Off
		High	High	Off

Feature Description (continued)

Table 1. V_{POS} Active Discharge Behavior (continued)

PART NUMBER	V_{IN}	ENP	ENN	V_{POS} DISCHARGE
TPS65132Bx TPS65132Lx TPS65132Wx	< V_{UVLO}	Don't Care	Don't Care	On
	> V_{UVLO}	Low	Low	On
		Low	High	Determined by DISP bit
		High	Low	Off
		High	High	Off

8.3.4.4 Isolation (LDO)

The LDO is isolating the V_{POS} rail from V_{REG} (boost converter output) as long as the rail is not enabled in order to ensure flexible startup like V_{NEG} before V_{POS}.

8.3.4.5 Setting The Output Voltage (LDO)

The output voltage of the LDO is programmable via a I^2C compatible interface, from –6.0 V to –4.0 V with 100 mV steps. For more details, please refer to the section.

8.3.5 Negative Charge Pump

8.3.5.1 Operation

The negative charge pump (CPN) generates the negative voltage rail V_{NEG} by inverting and regulating the output voltage of the boost converter (V_{REG}). The charge pump uses 4 switches and an external flying capacitor to generate the negative rail. Two of the switches are turned on in the first phase to charge the flying capacitor up to V_{REG}, and in the second phase they are turned-off and the two others turn on to pump the energy negatively out of the OUTN capacitor.

8.3.5.2 Power-Up And Soft-Start (CPN)

The CPN starts operating as soon as the ENN signal is pulled HIGH, V_{IN} voltage is above the UVLO threshold and the boost converter has reached its Power Good threshold.

In the case where the enable signal is already HIGH when V_{IN} reaches the UVLO threshold, the boost converter will start first and the CPN will only start after the boost converter has reached its target voltage. For TPS65132Ax, the boost will start after the 40 ms delay has passed (see *Undervoltage Lockout (UVLO)*).

The CPN integrates a soft-start that slowly ramps up its output voltage V_{NEG} within a time defined by the selected mode (Smartphone or Tablet), the output voltage and the output capacitor value. For TPS65132Ax and TPS65132Bx (except TPS65132B2), the startup current charging the output capacitor in Smartphone mode is 50 mA, and 100 mA typically in Tablet mode. For TPS65132B2, TPS65132Lx, TPS65132Wx, the typical ramp-up times are slowed down by a factor of 4 (i.e 12.5 mA and 25 mA typical output current for Smartphone and Tablet modes respectively.) and the inrush current is also reduced by a factor of about 4. For TPS65132Sx, the negative rail starts-up in Smartphone or Tablet mode, thus the startup current is set by the mode the device is programmed to, and not related to the SYNC pin state. The full current of 150 mA minimum is only released once both rails (V_{POS} and V_{NEG}) bave reached their Power Good levels. Typical startup waveforms are shown in Figure 43 to Figure 46.

The estimated startup time can be calculated using the following formula:

$$t_{STARTUP} = \frac{C_{OUT} \times V_{NEG}}{I_{STARTUP}}$$

Where:

$t_{STARTUP}$ = startup time of the V_{NEG} rail
C_{OUT} = output capacitance of the V_{NEG} rail
V_{NEG} = target output voltage
$I_{STARTUP}$ = output current of the V_{NEG} rail charging up the output capacitor at startup (12.5 mA, 25 mA, 50 mA or 100 mA as described above)

8.3.5.3 Power-Down And Discharge (CPN)

The CPN stops operating when V_{IN} is below the UVLO threshold or when ENN is pulled LOW.

Or when EN is pulled LOW in the TPS65132Sx, and the internal sequencing has passed.

The negative rail can be actively discharged to GND during power-down if required. A discharge selection bit is available to enable or disable this function. See for more details, as well as waveforms Figure 41 and Figure 42. Table 2 shows the V_{NEG} discharge behavior of each device variant.

Table 2. V_{NEG} Active Discharge Behavior

PART NUMBER	V_{IN}	ENP	ENN	V_{NEG} DISCHARGE
TPS65132Ax	< V_{UVLO}	Don't Care	Don't Care	On
	> V_{UVLO}	Low	Low	Determined by DISN bit
		Low	High	Off
		High	Low	Determined by DISN bit
		High	High	Off
TPS65132Bx TPS65132Lx TPS65132Wx	< V_{UVLO}	Don't Care	Don't Care	On
	> V_{UVLO}	Low	Low	On
		Low	High	Off
		High	Low	Determined by DISN bit
		High	High	Off

8.3.5.4 Isolation (CPN)

The CPN isolates the V_{NEG} rail from V_{REG} (boost converter output) as long as the rail is not enabled in order to ensure flexible startup like V_{POS} before V_{NEG}.

8.3.5.5 Setting The Output Voltage (CPN)

The output voltage of the CPN is programmable via a I^2C compatible interface, from 4.0 V to 6.0 V with 100 mV steps. For more details, please refer to the section.

8.4 Device Functional Modes

8.4.1 Enabling and Disabling the Device

The TPS65132 is enabled as long as the VIN voltage is above the UVLO and one of the enable pins (ENP or ENN) is HIGH. Pulling ENP or ENN LOW disables either rail (V_{POS} or V_{NEG} respectively); and, pulling both pins LOW disables the device entirely (the internal oscillator of the TPS65132Ax continues running to allow access to the I²C interface).

8.5 Programming

8.5.1 I²C Serial Interface Description

The TPS65132 communicates through an industry standard I²C compatible interface, to receive data in slave mode. I²C is a 2-wire serial interface developed by Philips Semiconductor (see I²C-Bus Specification, Version 2.1, January 2000).

The TPS65132 integrates a non-volatile memory (EEPROM) that allows the storage of the DAC values into the registers with a capability of up to 1000 programming cycles maximum.

The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The TPS65132 works as a slave and supports the following data transfer modes, as defined in the I²C-Bus specification: standard mode (100 kbps) and fast mode (400 kbps). The data transfer protocol for standard and fast modes is exactly the same, therefore they are referred to as F/S-mode in this document. The TPS65132 supports 7-bit addressing. The device 7-bit address is 3E (see Figure 8), and the LSB enables the write or read function.

Figure 8. TPS65132 Slave Address Byte

MSB	TPS65132		Address				LSB
0	1	1	1	1	1	0	R/$\overline{W}$
R/$\overline{W}$ = R/(W)							

The device that initiates the communication is called a master, and the devices controlled by the master are slaves. The master generates the serial clock on SCL, controls the bus access, and generates START and STOP conditions (see Figure 9). A START initiates a new data transfer to a slave. Transitioning SDA from high to low while SCL remains high generates a START condition. A STOP condition ends a data transfer to slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition.

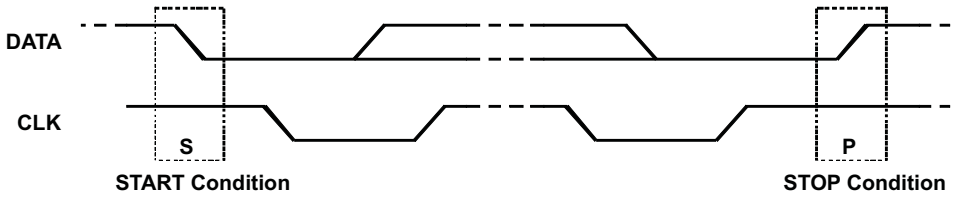


Figure 9. Start And Stop Conditions

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/(W) on the SDA line. During all transmissions, the master ensures that the data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 10). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an Acknowledgment, ACK, (see Figure 11) by pulling the SDA line low during the entire high period of the SCL cycle. Upon detecting this Acknowledgment, the master knows that communication link with a slave has been established.

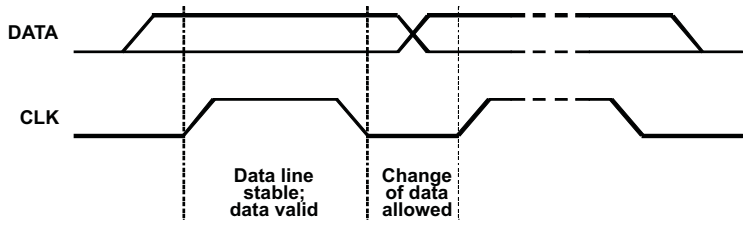


Figure 10. Bit Transfer On The Serial Interface

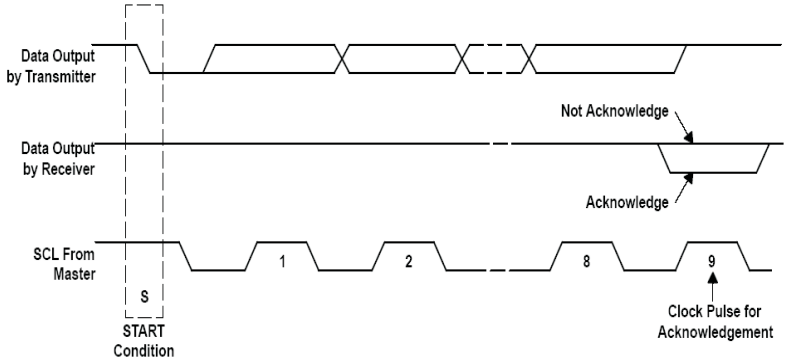


Figure 11. Acknowledge On The IC Bus[2]

The master generates further SCL cycles to either transmit data to the slave (R/(W) bit = 0) or receive data from the slave (R/(W) bit = 1). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary. To terminate the data transfer, the master generates a STOP condition by pulling the SDA line from low to high while the SCL line is high (see Figure 12). This releases the bus and stops the communication link with the addressed slave. All I^2C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

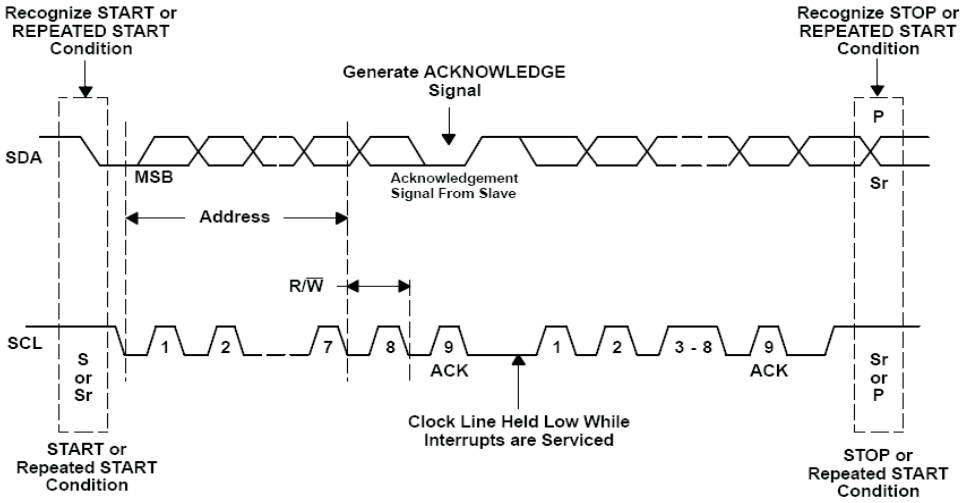


Figure 12. Bus Protocol

NOTE

With TPS65132Bx, TPS65132Lx, TPS65132Sx and TPS65132Wx, the I^2C interface is not accessible as long as EN = ENN = ENP = LOW. As soon as one of the enable pins is pulled HIGH, the I^2C interface is accessible.

8.5.2 I^2C Interface Protocol

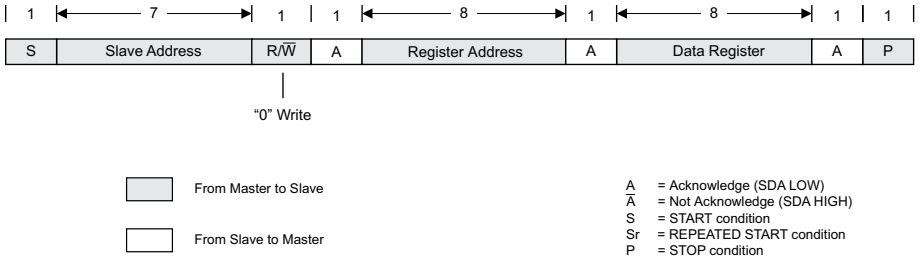


Figure 13. "Write" Data To DAC – Transfer Format In F/S-Mode

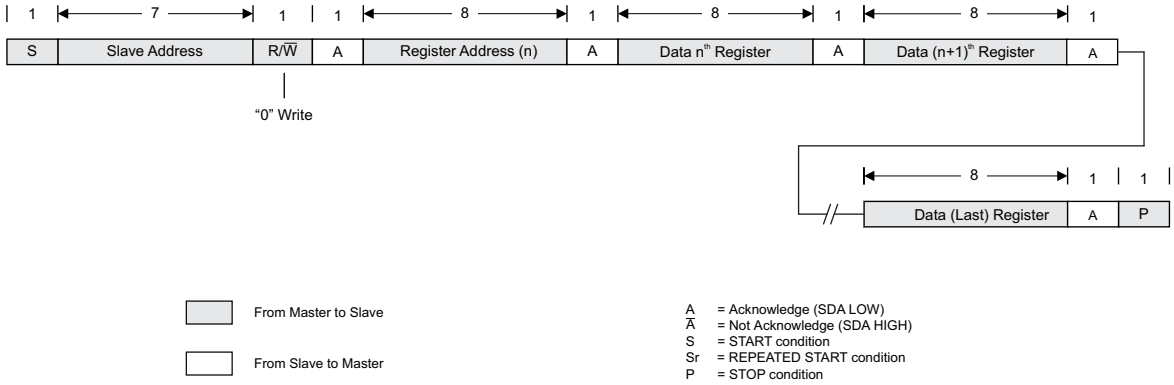


Figure 14. "Write" Data To DAC – Transfer Format In F/S-Mode Featuring Register Address Auto-Increment

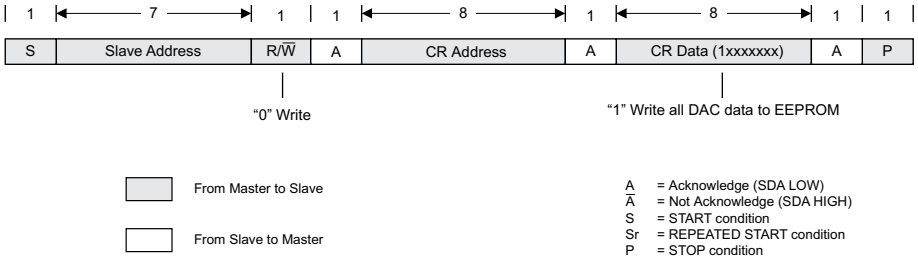


Figure 15. "Write" Data To EEPROM – Transfer Format In F/S-Mode

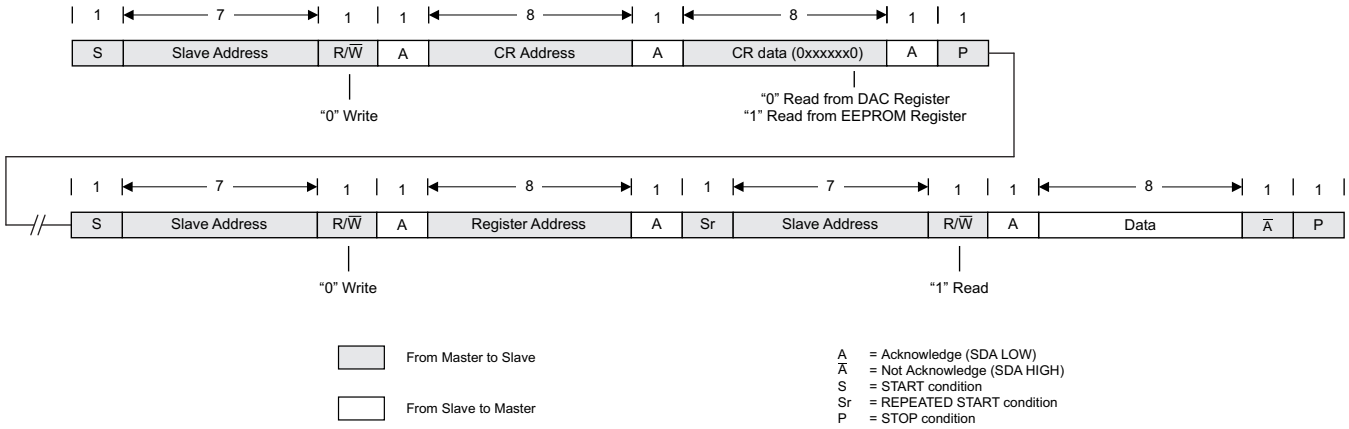


Figure 16. "Read" Data From DAC/EEPROM – Transfer Format In F/S-Mode

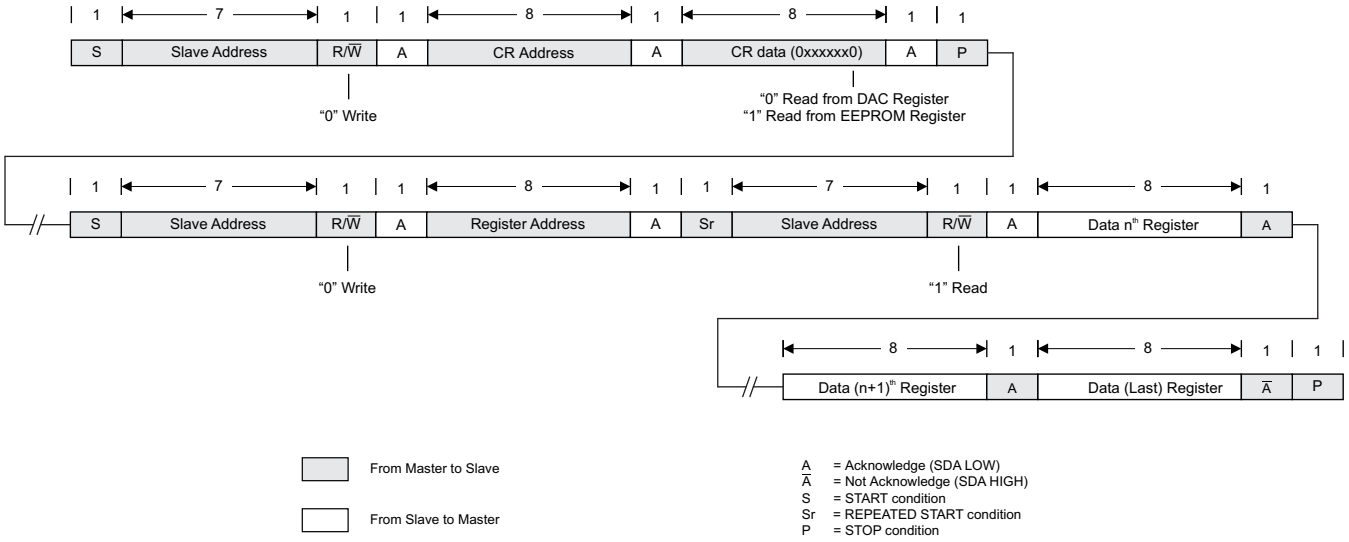


Figure 17. "Read" Data From DAC/EEPROM – Transfer Format In F/S-Mode Featuring Register Address Auto-Increment

8.6 Register Maps

The TPS65132 has one non-volatile memory which contains the initial value of the DAC and one volatile memory which contains the DAC setting. The non-volatile memory is called the Initial Value Register (IVR) and the volatile memory is called DAC Register (DR). The non-volatile IVR and the volatile DR are accessed with the same address.

Startup option: At power-up, the value contained in the IVR is loaded into the volatile DR and IVR presets the DAC to the last stored setting within less than 20 µs. The programmed factory value of the IVR of each address is described below and, at power-up, these data byte set the output voltage of each rail.

Write description: The user has to program all data registers first (0×00 ~ 0×03), then set the WED (Write EEPROM Data) bit to 1 once all desired data are addressed. A dead time of 50 ms is then initiated during which all the register data (0×00 ~ 0×03) are stored into the non volatile EEPROM cell. During that time, there should be no data flowing through the I^2C because the I^2C interface is momentarily not responding.

After the 50 ms have passed, the WED bit is automatically reset to 0, and the user is able to read the values or program again.

Register Maps (continued)

Slave address: 0x3E

X = R/W R/W = 1 → read mode

R/W = 0 → write mode

8.6.1 DAC Registers

Attempting to read data from register addresses not listed in the following section will result in 0x00 being read out.

8.6.1.1 VPOS Register – Address: 0x00

Figure 18. VPOS Register

7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	VPOS[4:0]				
0	0	0	0	1	1	1	0
R			R/W				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 3. VPOS Register Field Descriptions

Bit	Field	Description			
7:5	RSVD[2:0]	Reserved, always set to 0			
4:0	VPOS[4:0]	VPOS output voltage adjustment			
		VPOS[4:0] Value (binary)	**VPOS Output Voltage (V)**	**VPOS[4:0] Value (binary)**	**VPOS Output Voltage (V)**
		00000	4.0	01011	5.1
		00001	4.1	01100	5.2
		00010	4.2	01101	5.3
		00011	4.3	**01110**	**5.4**
		00100	4.4	01111	5.5
		00101	4.5	10000	5.6
		00110	4.6	10001	5.7
		00111	4.7	10010	5.8
		01000	4.8	10011	5.9
		01001	4.9	10100	6.0
		01010	5.0		

8.6.1.2 VNEG Register – Address 0x01

Figure 19. VNEG Register

7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	VNEG[4:0]				
0	0	0	0	1	1	1	0
R			R/W				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 4. VNEG Register Field Descriptions

Bit	Field	Description			
7:5	RSVD[2:0]	Reserved, always set to 0			
4:0	VNEG[4:0]	VNEG output voltage adjustment			
		VNEG[4:0] Value (binary)	**VNEG Output Voltage (V)**	**VNEG[4:0] Value (binary)**	**VNEG Output Voltage (V)**
		00000	–4.0	01011	–5.1
		00001	–4.1	01100	–5.2
		00010	–4.2	01101	–5.3
		00011	–4.3	**01110**	**–5.4**
		00100	–4.4	01111	–5.5
		00101	–4.5	10000	–5.6
		00110	–4.6	10001	–5.7
		00111	–4.7	10010	–5.8
		01000	–4.8	10011	–5.9
		01001	–4.9	10100	–6.0
		01010	–5.0		

8.6.1.3 DLYx Register – Address 0x02

Figure 20. DLYx Register

7	6	5	4	3	2	1	0
DLYP2	DLYP2	DLYN2	DLYN2	DLYP1	DLYP1	DLYN1	DLYN1
0	0	0	0	0	0	0	1
R/W							

Table 5. DLYx Register Field Descriptions

Bit	Field	Description	
7:6	DLYP2[1:0]	Delay, milliseconds	
5:4	DLYN2[1:0]		
3:2	DLYP1[1:0]		
1:0	DLYN1[1:0]		
	DLYx[1:0]	**DLYx Value**	**DLYx Delay (ms)**
		00	0
		01	**1**
		10	5
		11	10

8.6.1.4 APPS - SEQU - SEQD - DISP - DISN Register – Address 0x03

Figure 21. APPS - SEQU - SEQD - DISP - DISN Register

7	6	5	4	3	2	1	0
RSVD	APPS	SEQU	SEQU	SEQD	SEQD	DISP	DISN
0	0	0	0	0	0	1	0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6. APPS - SEQU - SEQD - DISP - DISN Field Descriptions

Bit	Field	Description									
7	RSVD	Reserved, always set to 0									
6:0	APPS, SEQU, SEQD, DISP, DISN	Application, Sequencing, Discharge Positive, Discharge Negative									
		APPS [6] Value		**SEQU [5:4] Value**		**SEQD [3:2] Value**		**DISP [1] Value** (1)		**DISN [0] Value** (1)	
		0	Smartphone	0	Simultaneous	0	Simultaneous	0	No discharge	0	No discharge
		1	Tablet	1	Sequential	1	Sequential	1	V_{POS} actively discharged	1	V_{NEG} actively discharged

(1) See *Power-Down And Discharge (LDO)* and *Power-Down And Discharge (CPN)* for a detailed description of how each device variant implements the active discharge function.

8.6.1.5 Control Register – Address 0xFF

Figure 22. Control Register

7	6	5	4	3	2	1	0
WED	RSVD[6:1]						EE/(DR)

The **Reserved** bits are ignored when written and return either 0 or 1 when read.

Table 7. Control Register Field Descriptions

Bit	Field	Description
7	WED	Write EEPROM Data
6:1	RSVD[6:1]	Reserved
0	EE/(DR)	EEPROM / (DAC Register)

8.6.2 Factory Default Register Value

Part number	Register address			
	0x00	0x01	0x02	0x03
TPS65132A	0x0E	0x0E	—	0x03
TPS65132A0	0x0A	0x0A	—	0x03
TPS65132B	0x0E	0x0E	—	0x03
TPS65132B0	0x0A	0x0A	—	0x03
TPS65132B2	0x0C	0x0C	—	0x03
TPS65132B5	0x0F	0x0F	—	0x03
TPS65132L	0x0E	0x0E	—	0x03
TPS65132L0	0x0A	0x0A	—	0x03
TPS65132L1 (1)	0x0B	0x0B	—	0x03
TPS65132S (1)	0x0E	0x0E	0x00	0x43
TPS65132T6	0x10h	0x10h	—	0x43
TPS65132W	0x0E	0x0E	—	0x43

(1) Product preview.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS65132xx devices, primarily intended to supplying TFT LCD displays, can be used for any application that requires positive and negative supplies, ranging from ±4 V to ±6 V and current up to 80 mA (150 mA for the TPS65132Sx version). Both output voltages can be set independently and their sequencing is also independent. The following section presents the different operating modes that the device can support as well as the different features that the user can select.

9.2 Typical Applications

9.2.1 Low-current Applications (≤ 40 mA)

The TPS65132 can be programmed to Smartphone mode with the APPS bit to support applications that require output currents up to 40 mA (refer to). The Smartphone mode limits the negative charge pump output current to 40 mA DC in order to provide the highest efficiency possible. The V_{POS} rail can deliver up to 200 mA DC regardless of the mode. Output peak currents are supported by the output capacitors.

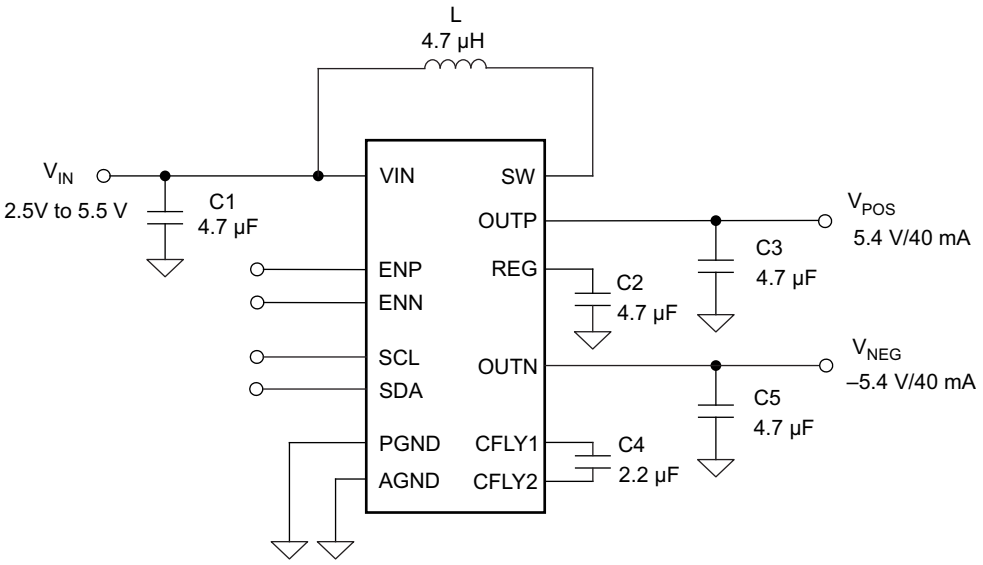


Figure 23. Typical Application Circuit For Smartphones

9.2.1.1 Design Requirements

Table 8. Design Parameters

PARAMETERS	EXAMPLE VALUES
Input Voltage Range	2.5 V to 5.5 V
Output Voltage	4.0 V to 6.0 V
Output Current Rating	40 mA
Boost Converter Switching Frequency	1.8 MHz
Negative Charge Pump Switching Frequency	1.0 MHz

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Sequencing

Each output rail (V_{POS} and V_{NEG}) is enabled and disabled using an external enable signal. If not explicitly specified, the enable signal in the rest of the document refers to ENN or ENP: ENP for the positive rail V_{POS} and ENN for the negative rail V_{NEG}. Figure 37 to Figure 40 show the typical sequencing waveforms.

NOTE

In the case where V_{IN} falls below the UVLO threshold while one of the enable signals is still high, all converters will be shut down instantaneously and both V_{POS} and V_{NEG} output rails will be actively discharged to GND.

9.2.1.2.2 Boost Converter Design Procedure

The first step in the design procedure is to verify whether the maximum possible output current of the boost converter supports the specific application requirements. A simple approach is to estimate the converter efficiency, by taking the efficiency number from the provided efficiency curves at the application's maximum load or to use a worst case assumption for the expected efficiency, e.g., 85%.

1. Duty Cycle: $D = 1 - \frac{V_{IN\_min} \times \eta}{V_{REG}}$
2. Inductor ripple current: $\Delta I_L = \frac{V_{IN\_min} \times D}{f_{SW} \times L}$
3. Maximum output current: $I_{OUT\_max} = \left(I_{LIM\_min} + \frac{\Delta I_L}{2} \right) \times (1 - D)$
4. Peak switch current of the application: $I_{SWPEAK} = \frac{I_{OUT}}{1 - D} + \frac{\Delta I_L}{2}$

η = Estimated boost converter efficiency (use the number from the efficiency plots or 85% as an estimation)
f_{SW} = Boost converter switching frequency (1.8 MHz)
L = Selected inductor value for the boost converter (see the Inductor Selection section)
I_{SWPEAK} = Boost converter switch current at the desired output current (must be < [I_{LIM_min} + ΔI_L])
ΔI_L = Inductor peak-to-peak ripple current
V_{REG} = max (V_{POS}, |V_{NEG}|) + 200 mV (in Smartphone mode — + 300 mV in Tablet mode — + 500 mV with TPS65132Sx with SYNC = HIGH)
I_{OUT} = I_{OUT_VPOS} + | I_{OUT_VNEG}| (I_{OUT_max} being the maximum current delivered on each rail)

The peak switch current is the current that the integrated switch and the inductor have to handle. The calculation must be done for the minimum input voltage where the peak switch current is highest.

9.2.1.2.2.1 Inductor Selection (Boost Converter)

Saturation current: the inductor must handle the maximum peak current (I_{L_SAT} > I_{SWPEAK}, or I_{L_SAT} > [I_{LIM_min} + ΔI_L] as conservative approach)

DC Resistance: the lower the DCR, the lower the losses

Inductor value: in order to keep the ratio $I_{OUT}/\Delta I_L$ low enough for proper sensing operation purpose, it is recommended to use a 4.7 µH inductor for Smartphone mode (a 2.2 µH might however be used, but the efficiency might be lower than with 4.7 µH at light output loads depending on the inductor characteristics).

Table 9. Inductor Selection Boost(1)

L (µH)	SUPPLIER	COMPONENT CODE	EIA SIZE	DCR TYP (mΩ)	I_{SAT} (A)
2.2	Toko	1269AS-H-2R2N=P2	1008	130	2.4
2.2	Murata	LQM2HPN2R2MG0	1008	80	1.3
2.2	Murata	LQM21PN2R2NGC	0805	250	0.8
4.7	Toko	1269AS-H-4R7N=P2	1008	250	1.6
4.7	Murata	LQM21PN4R7MGR	0805	230	0.8
4.7	FDK	MIPS2520D4R7	1008	280	0.7

(1) See *Third-Party Products Disclaimer*

9.2.1.2.2.2 Input Capacitor Selection (Boost Converter)

For best input voltage filtering low ESR ceramic capacitors are recommended. TPS65132 has an analog input pin VIN. A 4.7 µF minimum bypass capacitor is required as close as possible from VIN to GND. This capacitor is also used as the boost converter input capacitor.

For better input voltage filtering, this value can be increased or two capacitors can be used: one 4.7 µF input capacitor for the boost converter as well as a 1 µF bypass capacitor close to the VIN pin. Refer to the *Recommended Operating Conditions*, Table 10 and the Figure 23 for input capacitor recommendations.

9.2.1.2.2.3 Output Capacitor Selection (Boost Converter)

For the best output voltage filtering, low-ESR ceramic capacitors are recommended. A minimum of 4.7 µF ceramic output capacitor is required. Higher capacitor values can be used to improve the load transient response. Refer to the *Recommended Operating Conditions*, Table 10 and Figure 23 for output capacitor recommendations.

Table 10. Input And Output Capacitor Selection(1)

CAPACITOR (µF)	SUPPLIER	COMPONENT CODE	EIA SIZE (Thickness max.)	VOLTAGE RATING (V)	COMMENTS
2.2	Murata	GRM188R61C225KAAD	0603 (0.9 mm)	16	C_{FLY}
4.7	Murata	GRM188R61C475KAAJ	0603 (0.95 mm)	16	C_{IN}, C_{NEG}, C_{POS}, C_{REG}
10	Murata	GRM219R61C106KA73	0603 (0.95 mm)	16	C_{NEG}, C_{REG}

(1) See *Third-Party Products Disclaimer*

9.2.1.2.3 Input Capacitor Selection (LDO)

The LDO input capacitor is also the boost converter output capacitor. Refer to the *Recommended Operating Conditions*, Table 10 and the Figure 23.

9.2.1.2.4 Output Capacitor Selection (LDO)

The LDO is designed to operate with a 4.7 µF minimum ceramic output capacitor. Refer to the *Recommended Operating Conditions*, Table 10 and the Figure 23.

9.2.1.2.5 Input Capacitor Selection (CPN)

The CPN input capacitor is also the boost converter output capacitor. Refer to the *Recommended Operating Conditions*, Table 10 and the Figure 23.

9.2.1.2.6 Output Capacitor Selection (CPN)

The CPN is designed to operate with a 4.7 µF minimum ceramic output capacitor. Refer to the *Recommended Operating Conditions*, Table 10 and the Figure 23.

9.2.1.2.7 Flying Capacitor Selection (CPN)

The CPN needs an external flying capacitor. The minimum value is 2.2 µF. Special care must be taken while choosing the flying capacitor as it will directly impact the output voltage accuracy and load regulation performance. Therefore, a minimum capacitance of 1 µF must be achieved by the capacitor at a DC bias voltage of $|V_{NEG}|$ + 300 mV. For proper operation, the flying capacitor value must be lower than the output capacitor of the boost converter on REG pin.

9.2.1.3 Application Curves

V_{IN} = 3.7 V, V_{POS} = 5.4 V, V_{NEG} = –5.4 V, unless otherwise noted

Table 11. Component List Used For The Application Curves

REFERENCE	DESCRIPTION	MANUFACTURER AND PART NUMBER
C	2.2 µF, 16 V, 0603, X5R, ceramic	Murata - GRM188R61C225KAAD
	4.7 µF, 16 V, 0603, X5R, ceramic	Murata - GRM188R61C475KAAJ
	10 µF, 16 V, 0603, X5R, ceramic	Murata - GRM188R61E106MA73
L	2.2 µH, 2.4 A, 130 mΩ, 2.5 mm × 2.0 mm × 1.0 mm	Toko - DFE252010C (1269AS-H-2R2N=P2)
	4.7 µH, 1.6 A, 250 mΩ, 2.5 mm × 2.0 mm × 1.0 mm	Toko - DFE252010C (1269AS-H-4R7N=P2)
U1	TPS65132AYFF	Texas Instruments

Table 12. Table Of Graphs

PARAMETER	CONDITIONS	Figure
EFFICIENCY		
Efficiency vs. Output Current	± 5.0 V — Smartphone Mode — L = 4.7 µH	Figure 24
Efficiency vs. Output Current	± 5.4 V — Smartphone Mode — L = 4.7 µH	Figure 25
Efficiency vs. Output Current	± 5.0 V — Smartphone Mode — L = 2.2 µH	Figure 26
Efficiency vs. Output Current	± 5.4 V — Smartphone Mode — L = 2.2 µH	Figure 27
CONVERTERS WAVEFORMS		
V_{NEG} Output Ripple	I_{NEG} = 2 mA / 20 mA / 40 mA — Smartphone Mode — C_{OUT} = 4.7 µF	Figure 28
V_{NEG} Output Ripple	I_{NEG} = 2 mA / 20 mA / 40 mA — Smartphone Mode — C_{OUT} = 2 × 4.7 µF	Figure 29
V_{POS} Output Ripple	Any load	Figure 30
LOAD TRANSIENT		
Load Transient	V_{IN} = 2.9 V — I_{POS} = –I_{NEG} = 5 mA → 35 mA → 5 mA — Smartphone Mode — L = 4.7 µH	Figure 31
Load Transient	V_{IN} = 3.7 V — I_{POS} = –I_{NEG} = 5 mA → 35 mA → 5 mA — Smartphone Mode — L = 4.7 µH	Figure 32
Load Transient	V_{IN} = 4.5 V — I_{POS} = –I_{NEG} = 5 mA → 35 mA → 5 mA — Smartphone Mode — L = 4.7 µH	Figure 33
LINE TRANSIENT		
Line Transient	V_{IN} = 2.8 V → 4.5 V → 2.8 V — I_{POS} = –I_{NEG} = 0 mA — Smartphone Mode — L = 4.7 µH	Figure 34
Line Transient	V_{IN} = 2.8 V → 4.5 V → 2.8 V — I_{POS} = –I_{NEG} = 5 mA — Smartphone Mode — L = 4.7 µH	Figure 35
Line Transient	V_{IN} = 2.8 V → 4.5 V → 2.8 V — I_{POS} = –I_{NEG} = 35 mA — Smartphone Mode — L = 4.7 µH	Figure 36

Table 12. Table Of Graphs (continued)

PARAMETER	CONDITIONS	Figure
POWER SEQUENCING		
Power-up Sequencing	Simultaneous — no load	Figure 37
Power-down Sequencing	Simultaneous — no load with Active Discharge	Figure 38
Power-up Sequencing	Sequential — no load	Figure 39
Power-down Sequencing	Sequential — no load with Active Discharge	Figure 40
Power-up/down Sequencing	Simultaneous — no load with Active Discharge	Figure 41
Power-up/down Sequencing	Simultaneous — no load without Active Discharge	Figure 42
INRUSH CURRENT		
Inrush Current	Simultaneous — no load — Smartphone Mode	Figure 43
Inrush Current	Sequential — no load — Smartphone Mode	Figure 44
Inrush Current	Simultaneous — no load — Smartphone Mode — TPS65132B2, –Lx, –Sx, –Wx	Figure 45
Inrush Current	Sequential — no load — Smartphone Mode — TPS65132B2, –Lx, –Sx, –Wx	Figure 46
LOAD REGULATION		
V_{POS} vs Output Current	V_{POS} = 5.0 V — Smartphone Mode — I_{POS} = 0 mA to 40 mA — L = 4.7 µH and 2.2 µH	Figure 47
V_{POS} vs Output Current	V_{POS} = 5.4 V — Smartphone Mode — I_{POS} = 0 mA to 40 mA — L = 4.7 µH and 2.2 µH	Figure 48
V_{NEG} vs Output Current	V_{NEG} = –5.0 V — Smartphone Mode — I_{NEG} = 0 mA to 40 mA — L = 4.7 µH and 2.2 µH	Figure 49
V_{NEG} vs Output Current	V_{NEG} = –5.4 V — Smartphone Mode — I_{NEG} = 0 mA to 40 mA — L = 4.7 µH and 2.2 µH	Figure 50
LINE REGULATION		
V_{POS} vs Output Voltage	V_{IN} = 2.5 V to 5.5 V — V_{POS} = 5.0 V — Smartphone Mode — I_{POS} = 20 mA — L = 4.7 µH and 2.2 µH	Figure 51
V_{POS} vs Output Voltage	V_{IN} = 2.5 V to 5.5 V — V_{POS} = 5.4 V — Smartphone Mode — I_{POS} = 20 mA — L = 4.7 µH and 2.2 µH	Figure 52
V_{NEG} vs Output Voltage	V_{IN} = 2.5 V to 5.5 V — V_{NEG} = –5.0 V — Smartphone Mode — I_{NEG} = 20 mA — L = 4.7 µH and 2.2 µH	Figure 53
V_{NEG} vs Output Voltage	V_{IN} = 2.5 V to 5.5 V — V_{NEG} = –5.4 V — Smartphone Mode — I_{NEG} = 20 mA — L = 4.7 µH and 2.2 µH	Figure 54

NOTE

In this section, I_{OUT} means that the outputs are loaded with $I_{POS} = -I_{NEG}$ simultaneously.

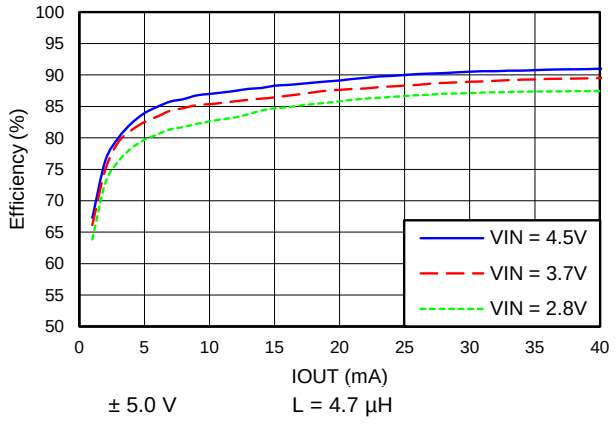


Figure 24. Combined Efficiency — Smartphone

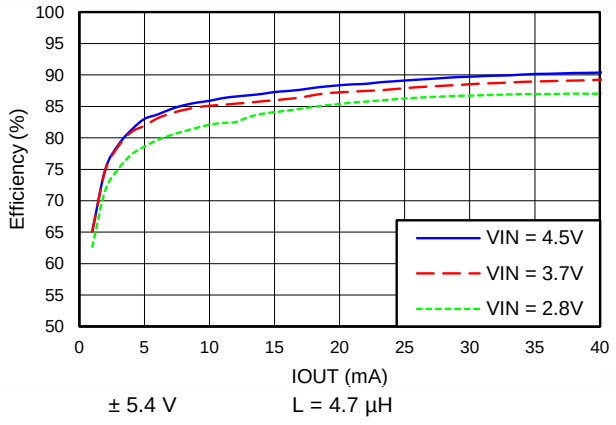
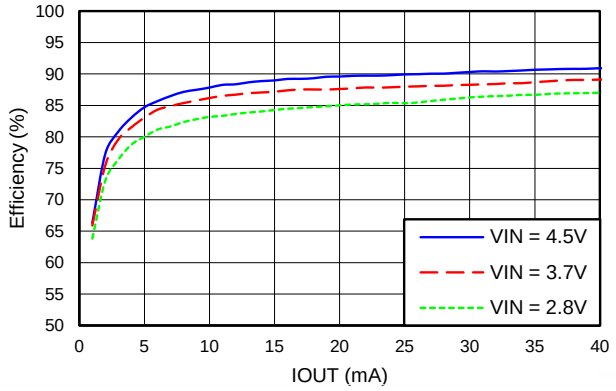
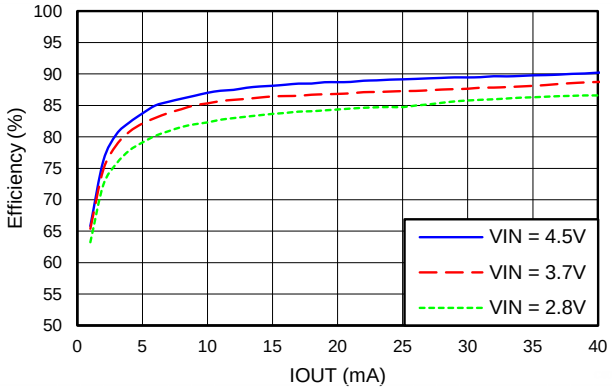


Figure 25. Combined Efficiency — Smartphone



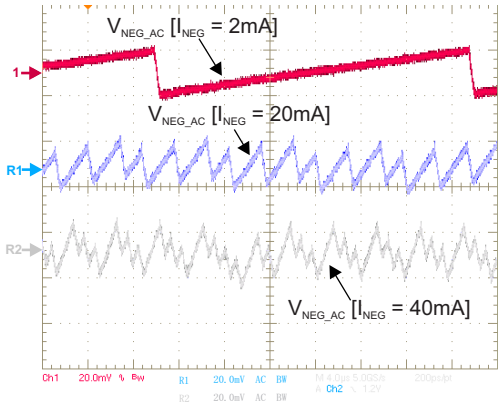
± 5.0 V L = 2.2 µH

Figure 26. Combined Efficiency — Smartphone



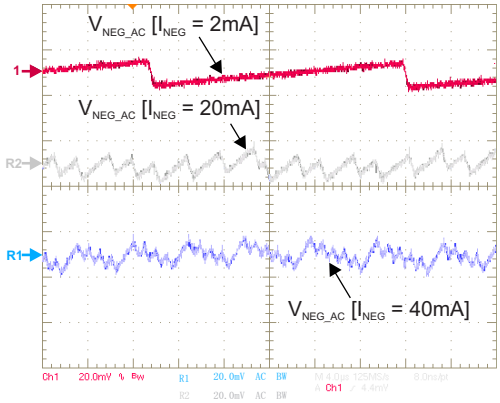
± 5.4 V L = 2.2 µH

Figure 27. Combined Efficiency — Smartphone



L = 4.7 µH C_{OUT} = 4.7 µF

Figure 28. V_{NEG} Output Voltage Ripple Smartphone



L = 4.7 µH C_{OUT} = 2 × 4.7 µF

Figure 29. V_{NEG} Output Voltage Ripple Smartphone

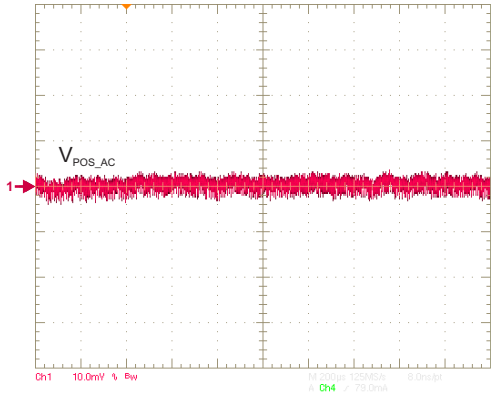
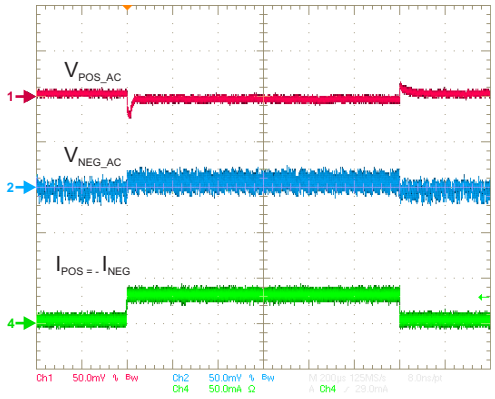
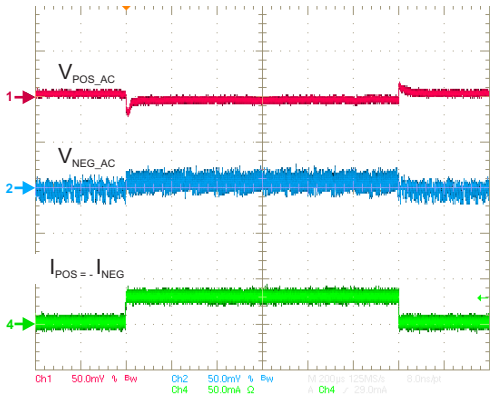


Figure 30. V_{POS} Output Voltage Ripple



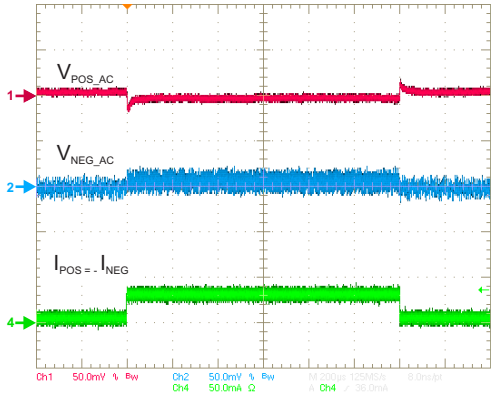
V_{IN} = 2.9 V ΔI_{OUT} = 30 mA

Figure 31. Load Transient — Smartphone



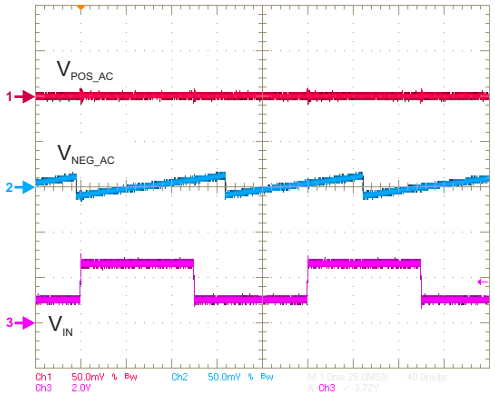
V_{IN} = 3.7 V ΔI_{OUT} = 30 mA

Figure 32. Load Transient — Smartphone



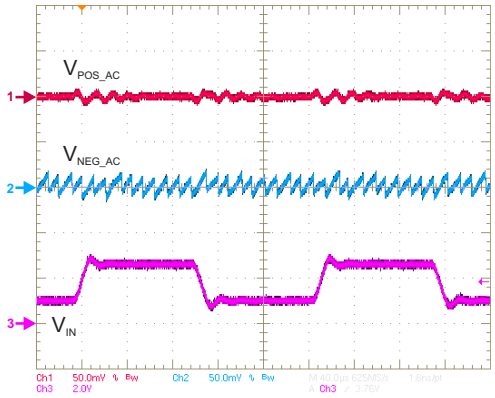
V_{IN} = 4.5 V ΔI_{OUT} = 30 mA

Figure 33. Load Transient — Smartphone



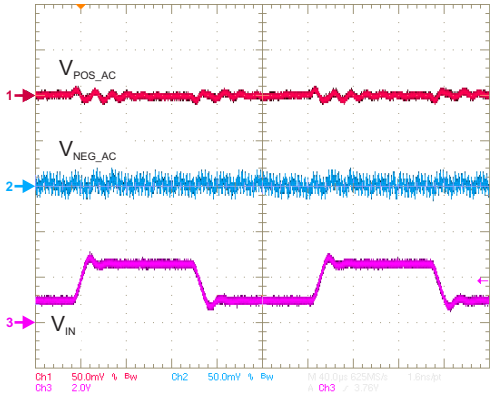
I_{OUT} = 0 mA ΔV_{IN} = 1.7 V

Figure 34. Line Transient — Smartphone



I_{OUT} = 5 mA ΔV_{IN} = 1.7 V

Figure 35. Line Transient — Smartphone



I_{OUT} = 35 mA ΔV_{IN} = 1.7 V

Figure 36. Line Transient — Smartphone

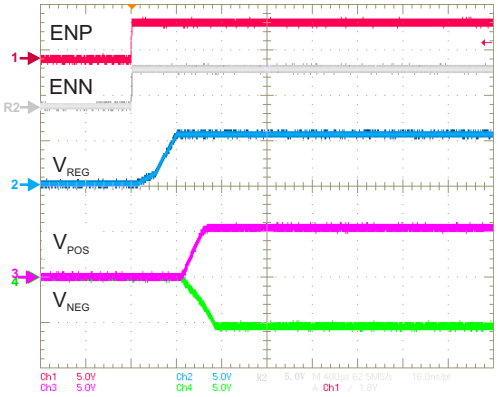


Figure 37. Power-Up Sequencing — Simultaneous

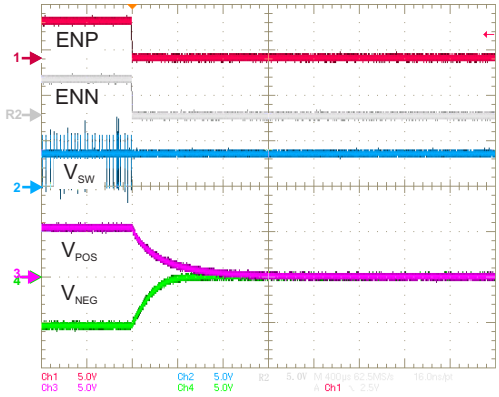


Figure 38. Power-Down Sequencing — Simultaneous (with Active Discharge)

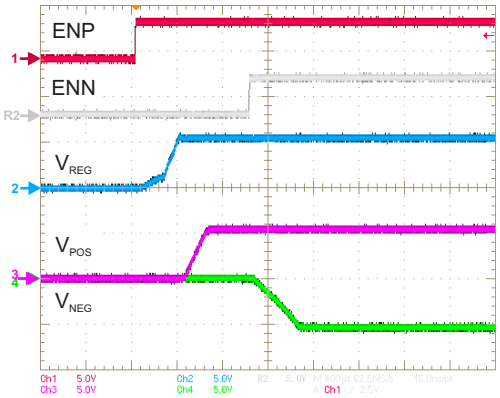


Figure 39. Power-Up Sequencing — Sequential

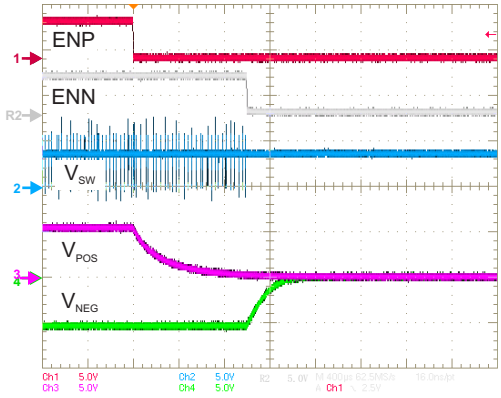


Figure 40. Power-Down Sequencing — Sequential (with Active Discharge)

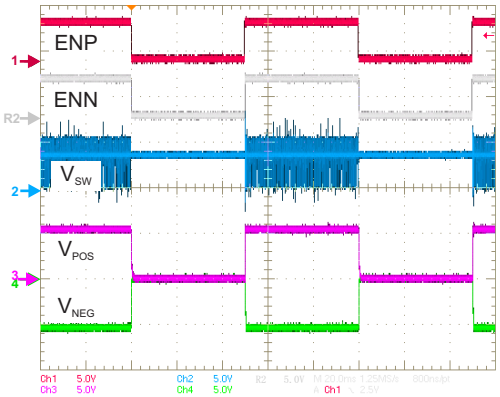


Figure 41. Power-Up/Down With Active Discharge

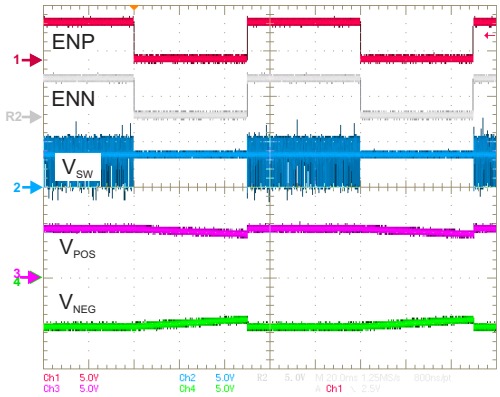


Figure 42. Power-Up/Down Without Active Discharge (TPS65132Ax only)

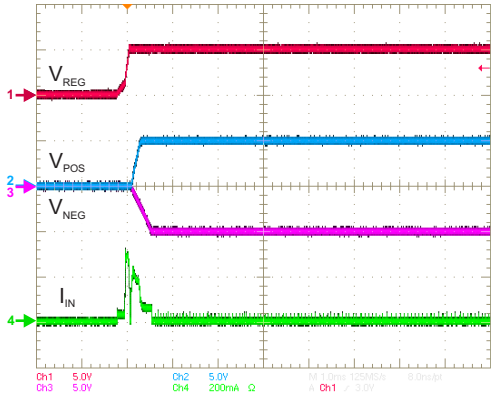


Figure 43. Inrush Current — Simultaneous

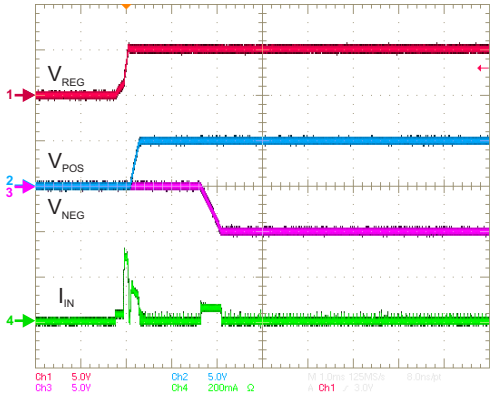


Figure 44. Inrush Current — Sequential

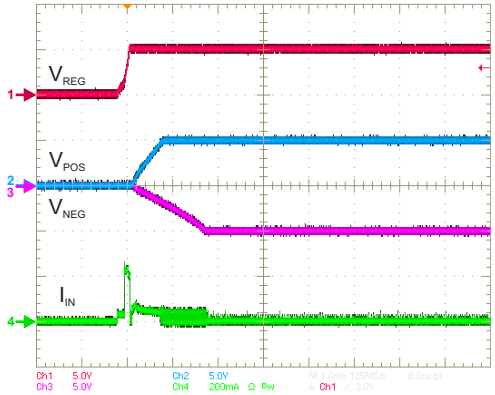


Figure 45. Inrush Current — Simultaneous (TPS65132B2, –Lx, –Sx, –Wx)

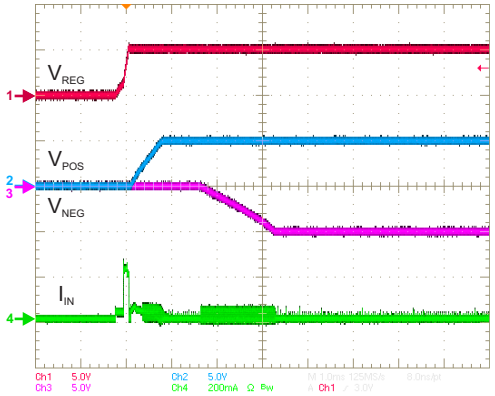
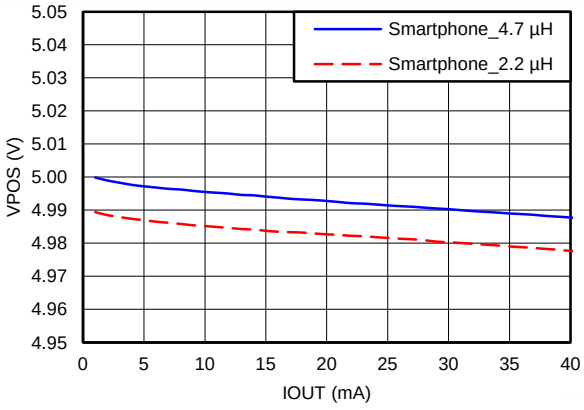
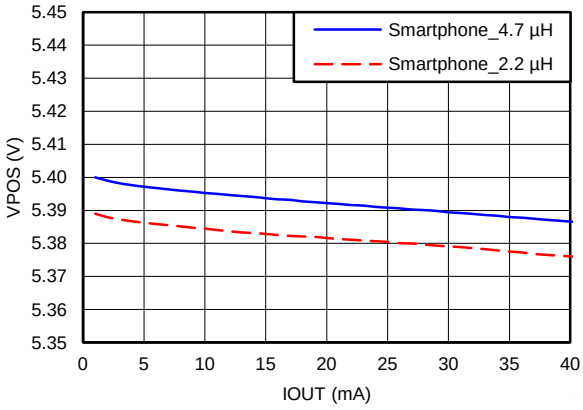


Figure 46. Inrush Current — Sequential (TPS65132B2, –Lx, –Sx, –Wx)



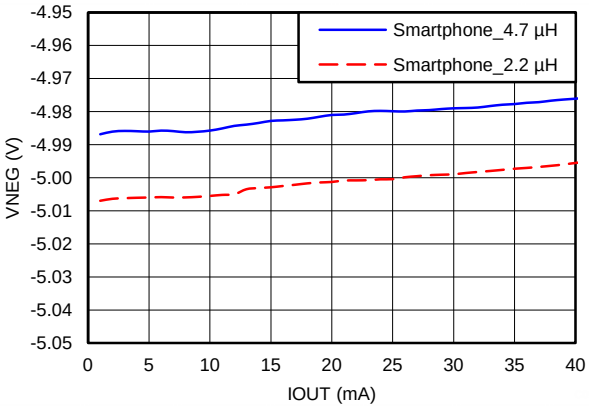
V_{POS} = 5 V

Figure 47. Load Regulation



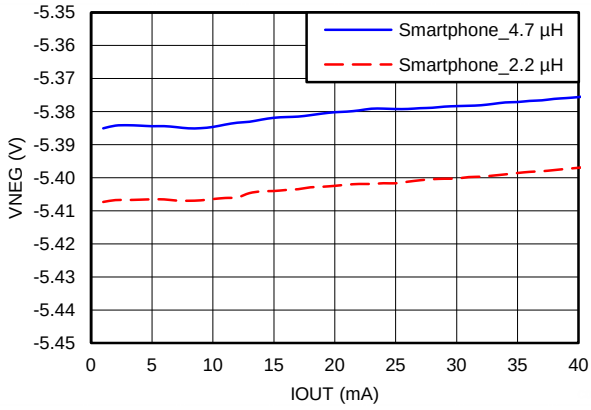
V_{POS} = 5.4 V

Figure 48. Load Regulation



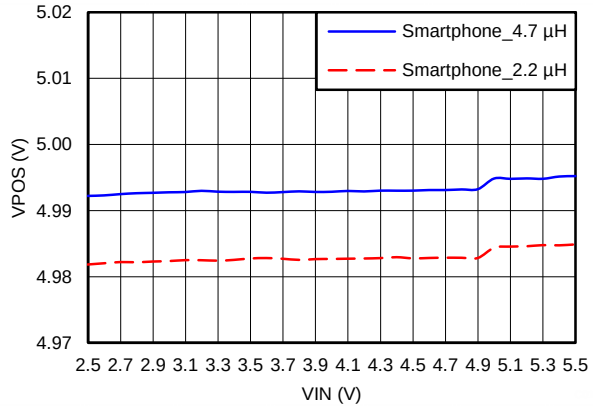
V_{NEG} = –5 V

Figure 49. Load Regulation



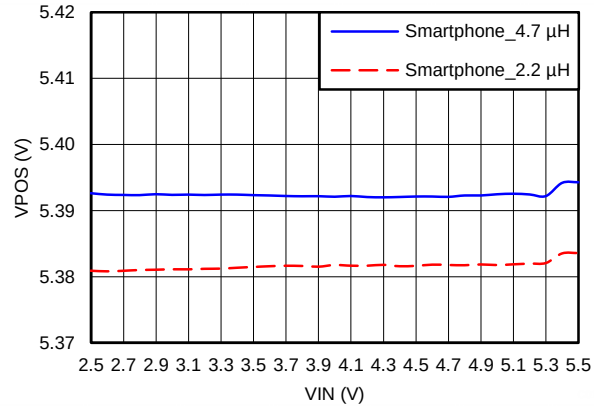
V_{NEG} = –5.4 V

Figure 50. Load Regulation



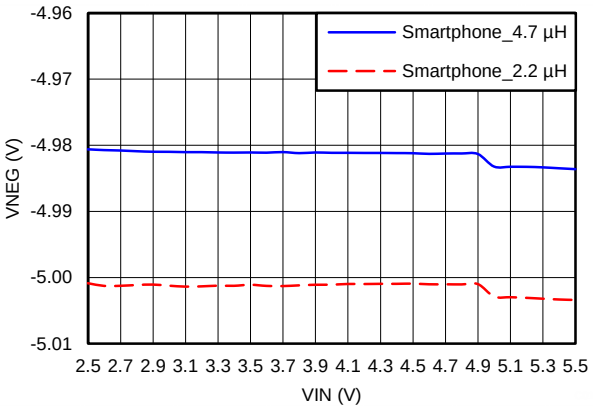
V_{POS} = 5 V

Figure 51. Line Regulation



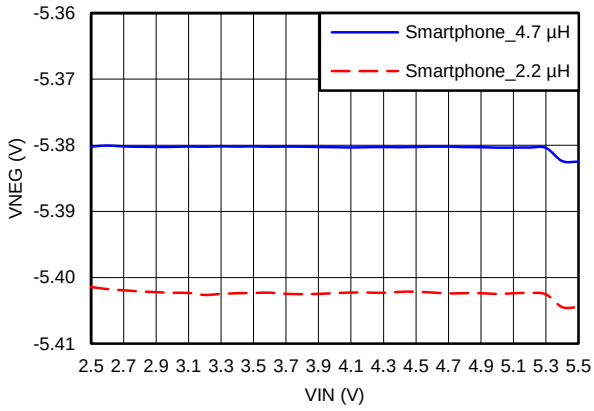
V_{POS} = 5.4 V

Figure 52. Line Regulation



V_{NEG} = –5 V

Figure 53. Line Regulation



V_{NEG} = –5.4 V

Figure 54. Line Regulation

9.2.2 Mid-current Applications (≤ 80 mA)

The TPS65132 can be programmed to Tablet mode with the APPS bit to support applications that require output currents up to 80 mA (refer to). The Tablet mode is limiting the negative charge pump (CPN) output current to 80 mA DC in order to provide the highest efficiency possible where the $V_{(POS)}$ rail can deliver up to 200 mA DC regardless of the mode. Output peak currents are supported by the output capacitors.

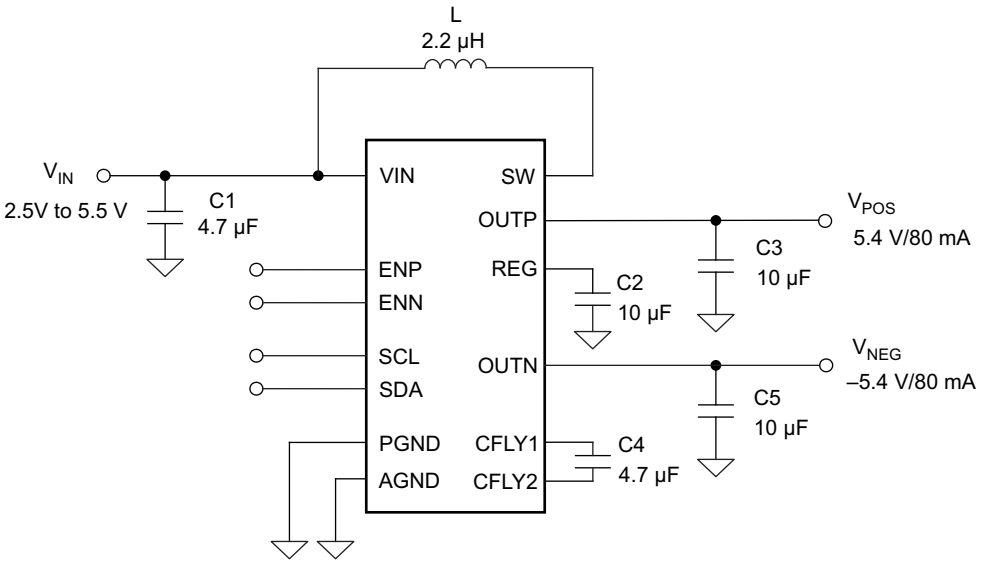


Figure 55. Typical Application Circuit For Tablets

9.2.2.1 Design Requirements

Table 13. Design Parameters

PARAMETERS	EXAMPLE VALUES
Input Voltage Range	2.5 V to 5.5 V
Output Voltage	4.0 V to 6.0 V
Output Current Rating	80 mA
Boost Converter Switching Frequency	1.8 MHz
Negative Charge Pump Switching Frequency	1.0 MHz

9.2.2.2 Detailed Design Procedure

The design procedure for the Tablet mode is identical to the Smartphone mode, except for the BOM (bill of materials). Refer to the *Sequencing* for details about the sequencing.and the general component selection.

9.2.2.2.1 Boost Converter Design Procedure

9.2.2.2.1.1 Inductor Selection (Boost Converter)

In order to keep the ratio $I_{OUT}/\Delta I_L$ low enough for proper sensing operation purpose, it is recommended to use a 2.2 µH inductor for Tablet mode. Refer to the *Inductor Selection (Boost Converter)* for details about the boost inductor selection.

9.2.2.2.1.2 Input Capacitor Selection (Boost Converter)

A 4.7 µF minimum bypass capacitor is required as close as possible from VIN to GND. This capacitor is also used as the boost converter input capacitor.

For better input voltage filtering, this value can be increased or two capacitors can be used: one 4.7 µF input capacitor for the boost converter as well as a 1 µF bypass capacitor close to the VIN pin. Refer to the *Recommended Operating Conditions*, Table 10 and Figure 55 for input capacitor recommendations.

9.2.2.2.1.3 Output Capacitor Selection (Boost Converter)

For best output voltage filtering low ESR ceramic capacitors are recommended. A minimum of 10 µF ceramic output capacitor is required. Higher capacitor values can be used to improve the load transient response. Refer to the *Recommended Operating Conditions*, Table 10 and Figure 55 for output capacitor recommendations.

9.2.2.2.2 Input Capacitor Selection (LDO)

The LDO input capacitor is also the boost converter output capacitor. Refer to the *Recommended Operating Conditions*, Table 10 and Figure 55.

9.2.2.2.3 Output Capacitor Selection (LDO)

The LDO is designed to operate with a 4.7 µF minimum ceramic output capacitor. Refer to the *Recommended Operating Conditions*, Table 10 and Figure 55.

9.2.2.2.4 Input Capacitor Selection (CPN)

The CPN input capacitor is also the boost converter output capacitor. Refer to the *Recommended Operating Conditions*, Table 10 and Figure 55.

9.2.2.2.5 Output Capacitor Selection (CPN)

The CPN is designed to operate with a 10 µF minimum ceramic output capacitor. Refer to the *Recommended Operating Conditions*, Table 10 and Figure 55.

9.2.2.2.6 Flying Capacitor Selection (CPN)

The CPN needs an external flying capacitor. The minimum value is 4.7 µF. Special care must be taken while choosing the flying capacitor as it will directly impact the output voltage accuracy and load regulation performance. Therefore, a minimum capacitance of 2.2 µF must be achieved by the capacitor at a DC bias voltage of $|V_{NEG}|$ + 300 mV. For proper operation, the flying capacitor value must be lower than the output capacitor of the boost converter on REG pin.

9.2.2.3 Application Curves

V_{IN} = 3.7 V, V_{POS} = 5.4 V, V_{NEG} = –5.4 V, unless otherwise noted

Table 14. Component List For Typical Characteristics Circuits

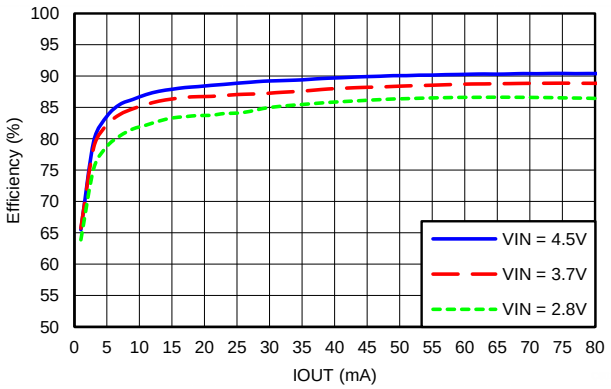
REFERENCE	DESCRIPTION	MANUFACTURER AND PART NUMBER
C	2.2 µF, 16 V, 0603, X5R, ceramic	Murata - GRM188R61C225KAAD
	4.7 µF, 16 V, 0603, X5R, ceramic	Murata - GRM188R61C475KAAJ
	10 µF, 16 V, 0603, X5R, ceramic	Murata - GRM188R61E106MA73
L	2.2 µH, 2.4 A, 130 mΩ, 2.5 mm × 2.0 mm × 1.0 mm	Toko - DFE252010C (1269AS-H-2R2N=P2)
U1	TPS65132AYFF	Texas Instruments

Table 15. Table Of Graphs

PARAMETER	CONDITIONS	Figure
EFFICIENCY		
Efficiency vs. Output Current	± 5.0 V — Tablet Mode — L = 2.2 µH	Figure 56
Efficiency vs. Output Current	± 5.4 V — Tablet Mode — L = 2.2 µH	Figure 57
CONVERTERS WAVEFORMS		
V_{NEG} Output Ripple	I_{NEG} = 4 mA / 40 mA / 80 mA — Tablet Mode — C_{OUT} = 10 µF	Figure 58
V_{NEG} Output Ripple	I_{NEG} = 4 mA / 40 mA / 80 mA — Tablet Mode — C_{OUT} = 2 × 10 µF	Figure 59
V_{POS} Output Ripple	I_{POS} = 150 mA — Tablet Mode	Figure 60
LOAD TRANSIENT		
Load Transient	V_{IN} = 2.9 V — I_{POS} = –I_{NEG} = 10 mA → 70 mA → 10 mA — Tablet Mode — L = 2.2 µH	Figure 61
Load Transient	V_{IN} = 3.7 V — I_{POS} = –I_{NEG} = 10 mA → 70 mA → 10 mA — Tablet Mode — L = 2.2 µH	Figure 62
Load Transient	V_{IN} = 4.5 V — I_{POS} = –I_{NEG} = 10 mA → 70 mA → 10 mA — Tablet Mode — L = 2.2 µH	Figure 63
LINE TRANSIENT		
Line Transient	V_{IN} = 2.8 V → 4.5 V → 2.8 V — I_{POS} = –I_{NEG} = 0 mA — Tablet Mode — L = 2.2 µH	Figure 64
Line Transient	V_{IN} = 2.8 V → 4.5 V → 2.8 V — I_{POS} = –I_{NEG} = 40 mA — Tablet Mode — L = 2.2 µH	Figure 65
Line Transient	V_{IN} = 2.8 V → 4.5 V → 2.8 V — I_{POS} = –I_{NEG} = 70 mA — Tablet Mode — L = 2.2 µH	Figure 66
POWER SEQUENCING		
Power-up Sequencing	Simultaneous — no load	Figure 67
Power-down Sequencing	Simultaneous — no load with Active Discharge	Figure 68
Power-up Sequencing	Sequential — no load	Figure 69
Power-down Sequencing	Sequential — no load with Active Discharge	Figure 70
Power-up/down Sequencing	Simultaneous — no load with Active Discharge	Figure 71
Power-up/down Sequencing	Simultaneous — no load without Active Discharge	Figure 72
INRUSH CURRENT		
Inrush Current	Simultaneous — no load — Tablet Mode	Figure 73
Inrush Current	Sequential — no load — Tablet Mode	Figure 74
Inrush Current	Simultaneous — no load — Tablet Mode — TPS65132B2, –Lx, –Sx, –Wx	Figure 75
Inrush Current	Sequential — no load — Tablet Mode — TPS65132B2, –Lx, –Sx, –Wx	Figure 76
LOAD REGULATION		
V_{POS} vs Output Current	V_{POS} = 5.0 V — Tablet Mode — I_{POS} = 0 mA to 80 mA — L = 2.2 µH	Figure 77
V_{POS} vs Output Current	V_{POS} = 5.4 V — Tablet Mode — I_{POS} = 0 mA to 80 mA — L = 2.2 µH	Figure 78
V_{NEG} vs Output Current	V_{NEG} = –5.0 V — Tablet Mode — I_{NEG} = 0 mA to 80 mA — L = 2.2 µH	Figure 79
V_{NEG} vs Output Current	V_{NEG} = –5.4 V — Tablet Mode — I_{NEG} = 0 mA to 80 mA — L = 2.2 µH	Figure 80
LINE REGULATION		
V_{POS} vs Output Voltage	V_{IN} = 2.5 V to 5.5 V — V_{POS} = 5.0 V — Tablet Mode — I_{POS} = 60 mA — L = 2.2 µH	Figure 81
V_{POS} vs Output Voltage	V_{IN} = 2.5 V to 5.5 V — V_{POS} = 5.4 V — Tablet Mode — I_{POS} = 60 mA — L = 2.2 µH	Figure 82
V_{NEG} vs Output Voltage	V_{IN} = 2.5 V to 5.5 V — V_{NEG} = –5.0 V — Tablet Mode — I_{NEG} = 60 mA — L = 2.2 µH	Figure 83
V_{NEG} vs Output Voltage	V_{IN} = 2.5 V to 5.5 V — V_{NEG} = –5.4 V — Tablet Mode — I_{NEG} = 60 mA — L = 2.2 µH	Figure 84

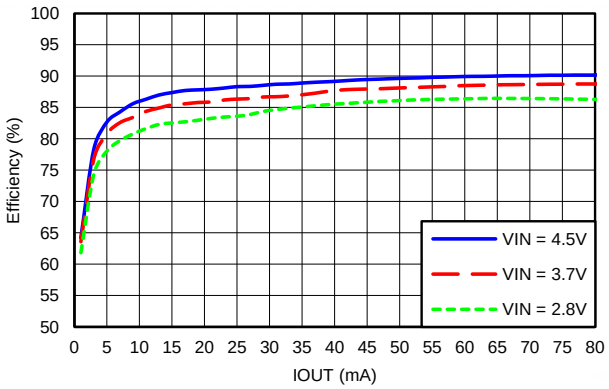
NOTE

In this section, I_{OUT} means that the outputs are loaded with I_{POS} = –I_{NEG} simultaneously.



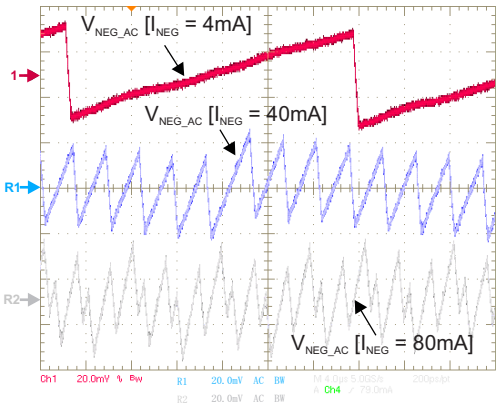
± 5 V L = 2.2 µH

Figure 56. Combined Efficiency — Tablet



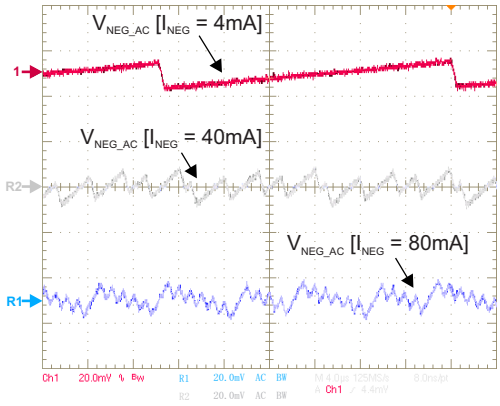
± 5.4 V L = 2.2 µH

Figure 57. Combined Efficiency — Tablet



L = 2.2 µH C_{OUT} = 10 µF

Figure 58. V_{NEG} Output Voltage Ripple Tablet



L = 2.2 µH C_{OUT} = 2 × 10 µF

Figure 59. V_{NEG} Output Voltage Ripple Tablet

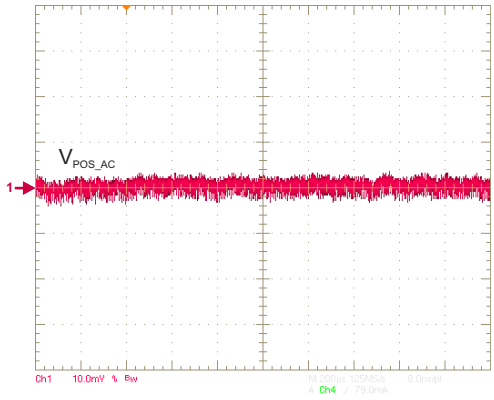
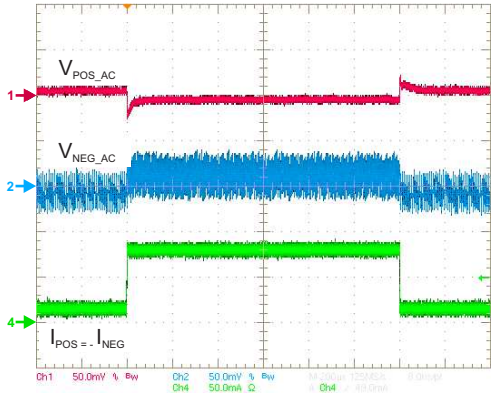
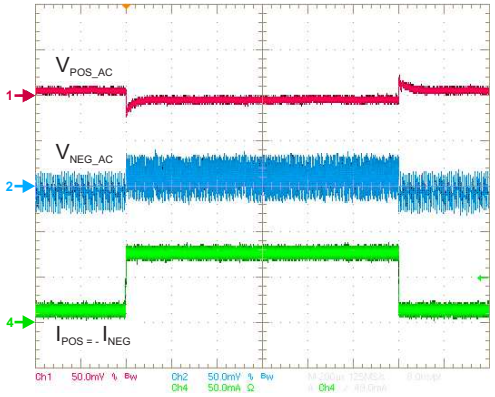


Figure 60. V_{POS} Output Voltage Ripple



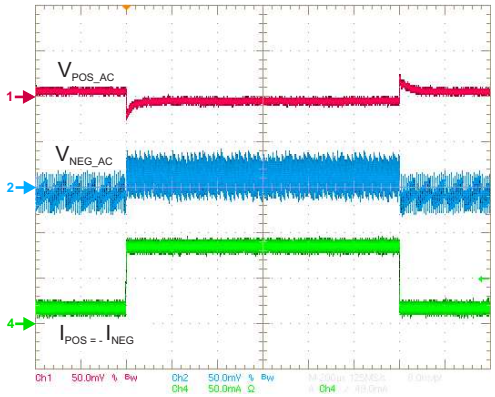
V_{IN} = 2.9 V ΔI_{OUT} = 60 mA

Figure 61. Load Transient — Tablet



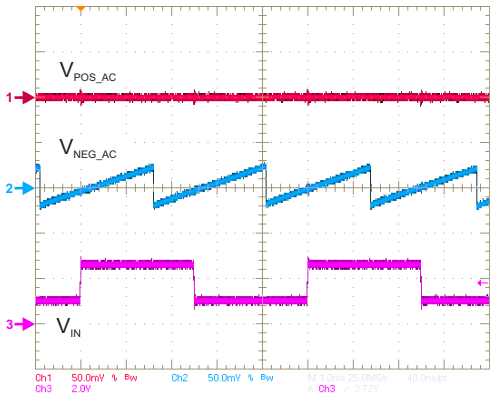
V_{IN} = 3.7 V ΔI_{OUT} = 60 mA

Figure 62. Load Transient — Tablet



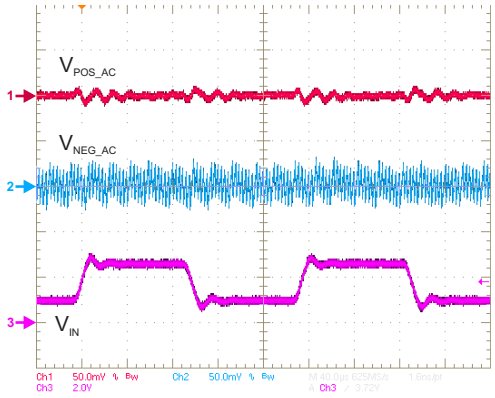
V_{IN} = 4.5 V ΔI_{OUT} = 60 mA

Figure 63. Load Transient — Tablet



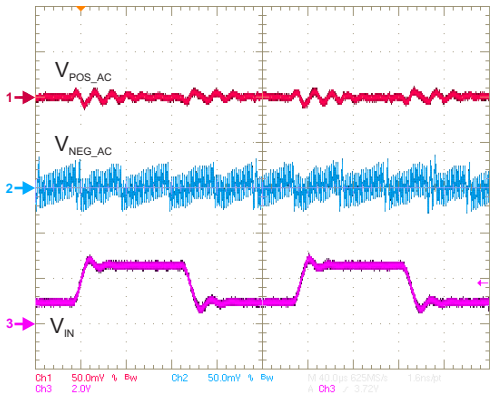
I_{OUT} = 0 mA ΔV_{IN} = 1.7 V

Figure 64. Line Transient — Tablet



I_{OUT} = 40 mA ΔV_{IN} = 1.7 V

Figure 65. Line Transient — Tablet



I_{OUT} = 70 mA ΔV_{IN} = 1.7 V

Figure 66. Line Transient — Tablet

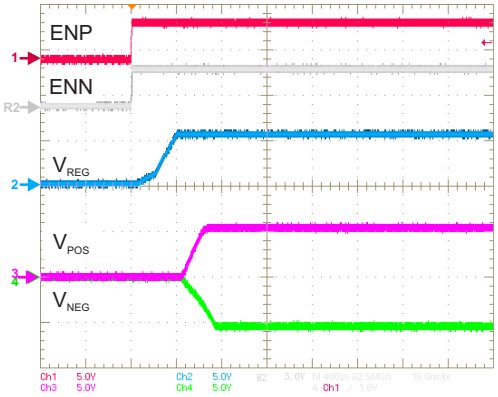


Figure 67. Power-Up Sequencing — Simultaneous

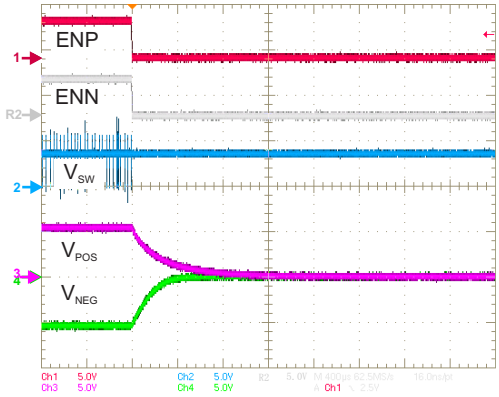


Figure 68. Power-Down Sequencing — Simultaneous (with Active Discharge)

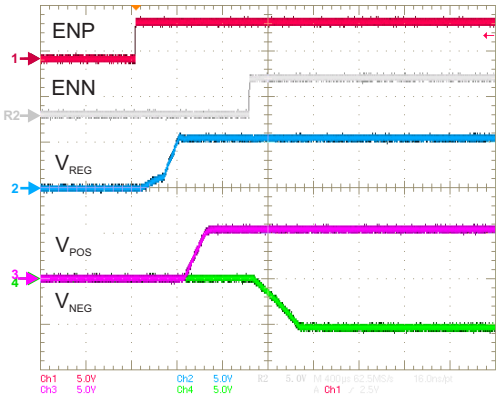


Figure 69. Power-Up Sequencing — Sequential

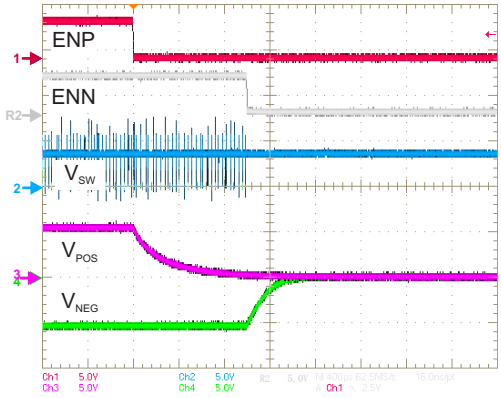


Figure 70. Power-Down Sequencing — Sequential (with Active Discharge)

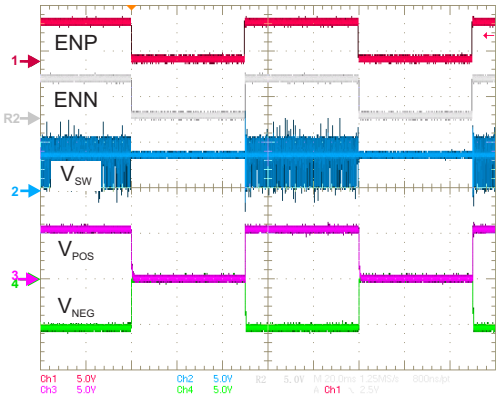


Figure 71. Power-Up/Down With Active Discharge

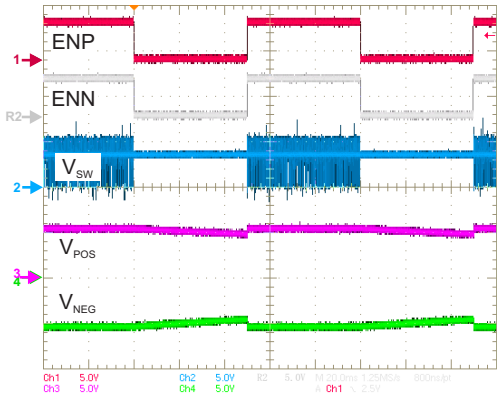


Figure 72. Power-Up/Down Without Active Discharge (TPS65132Ax only)

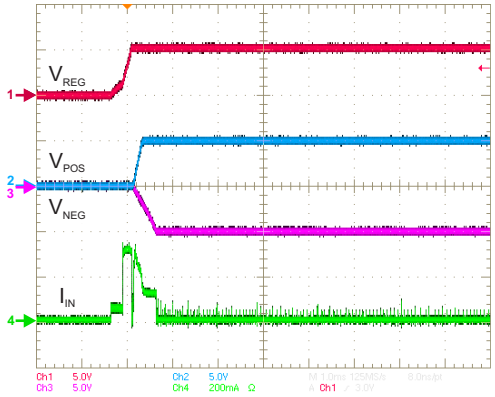


Figure 73. Inrush Current — Simultaneous

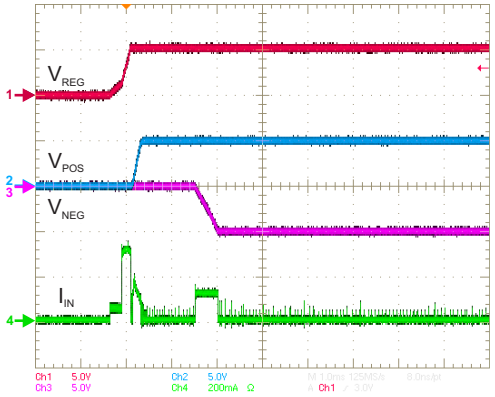


Figure 74. Inrush Current — Sequential

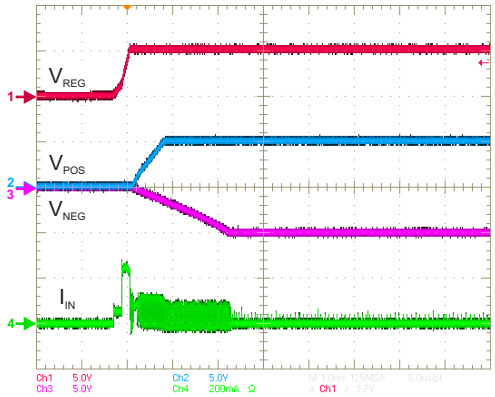


Figure 75. Inrush Current — Simultaneous (TPS65132B2, –Lx, –Sx, –Wx)

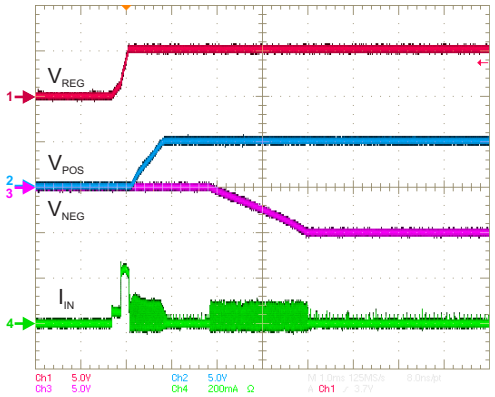
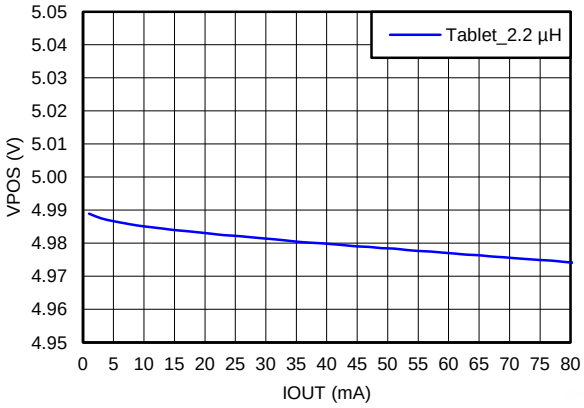
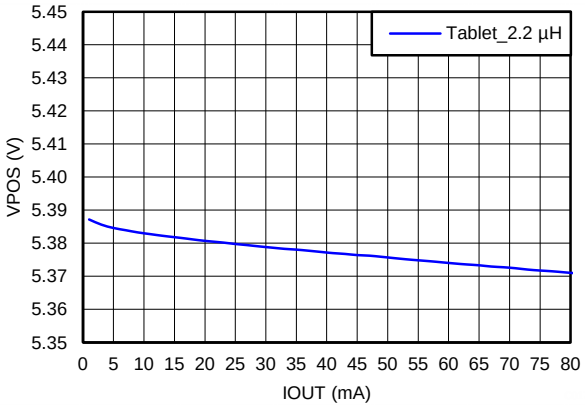


Figure 76. Inrush Current — Sequential (TPS65132B2, –Lx, –Sx, –Wx)



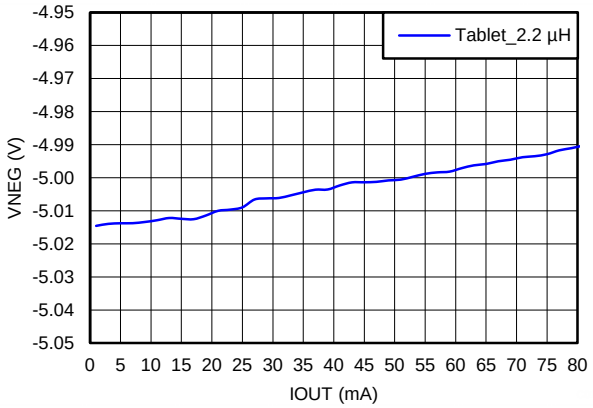
V_{POS} = 5 V

Figure 77. Load Regulation



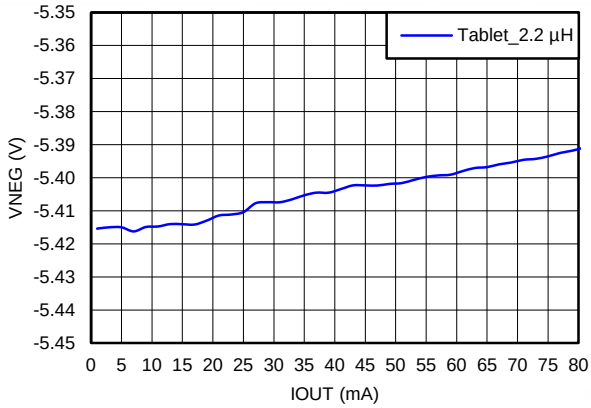
V_{POS} = 5.4 V

Figure 78. Load Regulation



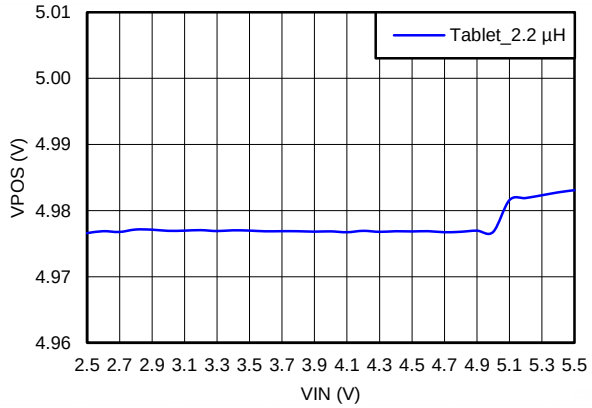
V_{NEG} = –5 V

Figure 79. Load Regulation



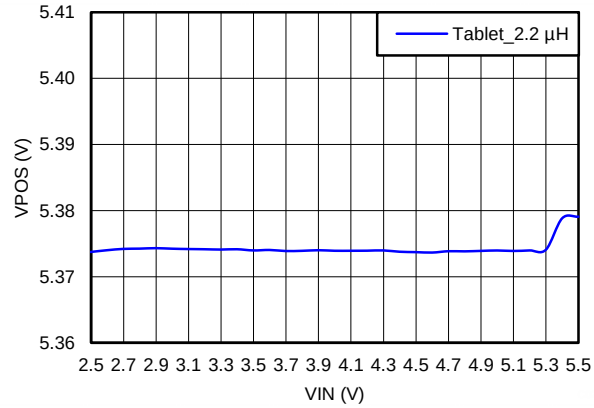
V_{NEG} = –5.4 V

Figure 80. Load Regulation



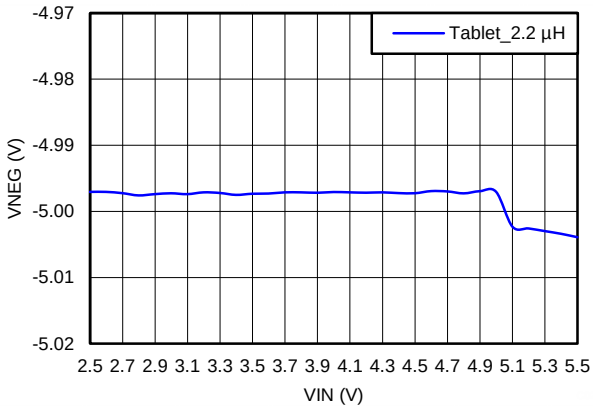
V_{POS} = 5 V

Figure 81. Line Regulation



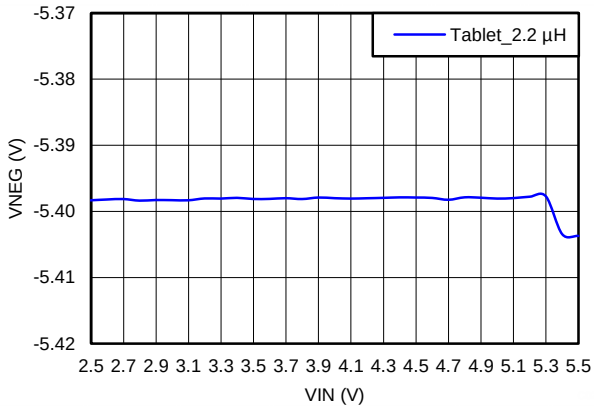
V_{POS} = 5.4 V

Figure 82. Line Regulation



V_{NEG} = –5 V

Figure 83. Line Regulation



V_{NEG} = –5.4 V

Figure 84. Line Regulation

9.2.3 High-current Applications (≤ 150 mA)

The TPS65132Sx version allows output current up to 150 mA on both V_{POS} and V_{NEG} when the SYNC pin is pulled HIGH. The TPS65132Sx can be programmed to Smartphone or Tablet mode with the APPS bit to lower the output current capability of the V_{NEG} rail if needed (in the case the efficiency is an important parameter). See *Low-current Applications (≤ 40 mA)* and *Mid-current Applications (≤ 80 mA)* for more details about the Smartphone and Tablet modes.

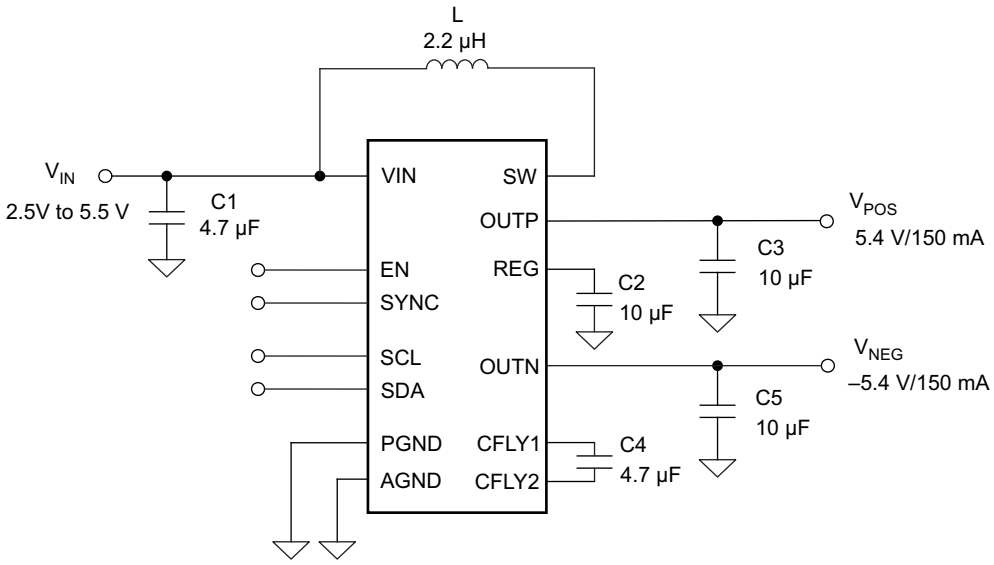


Figure 85. Typical Application Circuit For High Current

9.2.3.1 Design Requirements

Table 16. Design Parameters

PARAMETERS	EXAMPLE VALUES
Input Voltage Range	2.5 V to 5.5 V
Output Voltage	4.0 V to 6.0 V
Output Current Rating	150 mA
Boost Converter Switching Frequency	1.8 MHz
Negative Charge Pump Switching Frequency	1.0 MHz

9.2.3.2 Detailed Design Procedure

The design procedure and BOM list of the TPS65132Sx is identical to the Tablet mode. Please refer to the *Mid-current Applications (≤ 80 mA)* for more details about the general component selection.

9.2.3.2.1 Sequencing

The output rails (V_{POS} and V_{NEG}) are enabled and disabled using an external logic signal on the EN pin. The power-up and power-down sequencing events are programmable. Please refer to *Programmable Sequencing Scenarios* for the different sequencing as well as *DAC Registers* for the programming options.Figure 102 to show the typical sequencing waveforms.

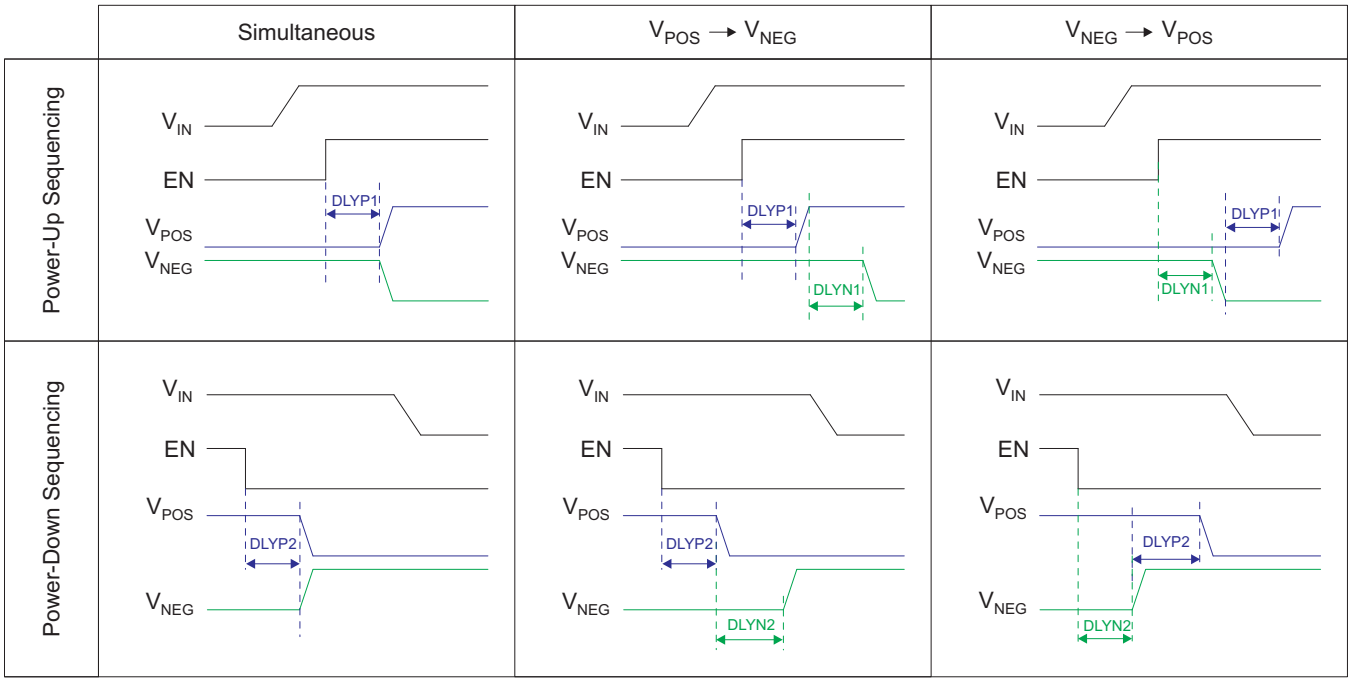


Figure 86. Programmable Sequencing Scenarios

NOTE

- In the case where the UVLO falling threshold is triggered while one of the enable signals is still high (ENN and/or ENP), all converters will be shut down instantaneously and both V_{POS} and V_{NEG} output rails will be actively discharged to GND.
- The power-up and power-down sequencings must be finalized (all delays have passed) before re-toggling the EN pin.

9.2.3.2.2 SYNC = HIGH

When the SYNC pin is pulled HIGH, the boost converter voltage increases instantaneously to allow enough headroom to deliver the 150 mA. When SYNC pin is pulled LOW, the boost converter keeps its offset for 300 µs typically, and during this time, the device is still capable if supplying 150 mA on both output rail. After these 300 µs have passed, current limit settles at 40 mA or 80 mA maximum, depending on the application mode it is programmed to (Smartphone or Tablet — see *Low-current Applications (≤ 40 mA)* and *Mid-current Applications (≤ 80 mA)* for more details) and the boost output voltage regulates down to its nominal value. See Figure 92 to Figure 95 for detailed waveforms.

9.2.3.2.3 Startup

The TPS65132Sx can startup with SYNC = HIGH, however, the boost offset as well as the 150 mA output current capability will only be available as soon as the last rail to start is in regulation.

9.2.3.3 Application Curves

V_{IN}= 3.7 V, V_{POS}= 5.4 V, V_{NEG}= –5.4 V, unless otherwise noted

Table 17. Component List For Typical Characteristics Circuits

REFERENCE	DESCRIPTION	MANUFACTURER AND PART NUMBER
C	2.2 µF, 16 V, 0603, X5R, ceramic	Murata - GRM188R61C225KAAD
	4.7 µF, 16 V, 0603, X5R, ceramic	Murata - GRM188R61C475KAAJ
	10 µF, 16 V, 0603, X5R, ceramic	Murata - GRM188R61E106MA73
L	2.2 µH, 2.4 A, 130 mΩ, 2.5 mm × 2.0 mm × 1.0 mm	Toko - DFE252010C (1269AS-H-2R2N=P2)
U1	TPS65132SYFF	Texas Instruments

Table 18. Table Of Graphs

PARAMETER	CONDITIONS	Figure
EFFICIENCY		
Efficiency vs. Output Current	± 5.0 V — SYNC = HIGH — L = 2.2 µH	Figure 87
Efficiency vs. Output Current	± 5.4 V — SYNC = HIGH — L = 2.2 µH	Figure 88
CONVERTERS WAVEFORMS		
V_{POS} Output Ripple	I_{POS} = 150 mA — SYNC = HIGH	Figure 60
V_{NEG} Output Ripple	I_{NEG} = 10mA / 80 mA / 150 mA — SYNC = HIGH — C_{OUT} = 10 µF	Figure 90
V_{NEG} Output Ripple	I_{NEG} = 4 mA / 40 mA / 80 mA — SYNC = HIGH — C_{OUT} = 2 × 10 µF	Figure 91
SYNC = HIGH Signal		
SYNC = HIGH	I_{POS} = –I_{NEG} = 10 mA	Figure 92
SYNC = HIGH	I_{POS} = –I_{NEG} = 150 mA	Figure 93
SYNC = HIGH Zoom	I_{POS} = –I_{NEG} = 10 mA	Figure 94
SYNC = LOW Zoom	I_{POS} = –I_{NEG} = 10 mA	Figure 95
LOAD TRANSIENT		
Load Transient	V_{IN} = 2.9 V — I_{POS} = –I_{NEG} = 10 mA → 150 mA → 10 mA — SYNC = HIGH — L = 2.2 µH	Figure 96
Load Transient	V_{IN} = 3.7 V — I_{POS} = –I_{NEG} = 10 mA → 150 mA → 10 mA — SYNC = HIGH — L = 2.2 µH	Figure 97
Load Transient	V_{IN} = 4.5 V — I_{POS} = –I_{NEG} = 10 mA → 150 mA → 10mA — SYNC = HIGH — L = 2.2 µH	Figure 98
LINE TRANSIENT		
Line Transient	V_{IN} = 2.8 V → 4.5 V → 2.8 V — I_{POS} = –I_{NEG} = 10 mA — SYNC = HIGH — L = 2.2 µH	Figure 99
Line Transient	V_{IN} = 2.8 V → 4.5 V → 2.8 V — I_{POS} = –I_{NEG} = 100 mA — SYNC = HIGH — L = 2.2 µH	Figure 100
Line Transient	V_{IN} = 2.8 V → 4.5 V → 2.8 V — I_{POS} = –I_{NEG} = 150 mA — SYNC = HIGH — L = 2.2 µH	Figure 101
POWER SEQUENCING		
Power-up Sequencing	Simultaneous — no load	Figure 102
Power-down Sequencing	Simultaneous — no load with Active Discharge	Figure 103
Power-up Sequencing	Sequential (V_{POS} → V_{NEG}) — no load	Figure 104
Power-down Sequencing	Sequential (V_{NEG} → V_{POS}) — no load with Active Discharge	Figure 105
Power-up Sequencing	Sequential (V_{NEG} → V_{POS}) — no load	Figure 106
Power-down Sequencing	Sequential (V_{POS} → V_{NEG}) — no load with Active Discharge	Figure 107

Table 18. Table Of Graphs (continued)

PARAMETER	CONDITIONS	Figure
Power-up/down Sequencing	Simultaneous — no load without Active Discharge	Figure 108
Power-up/down Sequencing	Simultaneous — no load with Active Discharge	Figure 109
INRUSH CURRENT		
Inrush Current	Simultaneous — no load — SYNC = HIGH — L = 2.2 µH	Figure 110
Inrush Current	Sequential — no load — SYNC = HIGH — L = 2.2 µH	Figure 111
LOAD REGULATION		
V_{POS} vs Output Current	V_{POS} = 5.0 V — SYNC = HIGH — I_{POS} = 0 mA to 150 mA — L = 2.2 µH	Figure 112
V_{POS} vs Output Current	V_{POS} = 5.4 V — SYNC = HIGH — I_{POS} = 0 mA to 150 mA — L = 2.2 µH	Figure 113
V_{NEG} vs Output Current	V_{NEG} = –5.0 V — SYNC = HIGH — I_{NEG} = 0 mA to 150 mA — L = 2.2 µH	Figure 114
V_{NEG} vs Output Current	V_{NEG} = –5.4 V — SYNC = HIGH — I_{NEG} = 0 mA to 150 mA — L = 2.2 µH	Figure 115
LINE REGULATION		
V_{POS} vs Output Voltage	V_{IN} = 2.5 V to 5.5 V — V_{POS} = 5.0 V — SYNC = HIGH — I_{POS} = 120 mA — L = 2.2 µH	Figure 116
V_{POS} vs Output Voltage	V_{IN} = 2.5 V to 5.5 V — V_{POS} = 5.4 V — SYNC = HIGH — I_{POS} = 120 mA — L = 2.2 µH	Figure 117
V_{NEG} vs Output Voltage	V_{IN} = 2.5 V to 5.5 V — V_{NEG} = –5.0 V — SYNC = HIGH — I_{NEG} = 120 mA — L = 2.2 µH	Figure 118
V_{NEG} vs Output Voltage	V_{IN} = 2.5 V to 5.5 V — V_{NEG} = –5.4 V — SYNC = HIGH — I_{NEG} = 120 mA — L = 2.2 µH	Figure 119

NOTE

In this section, I_{OUT} means that the outputs are loaded with $I_{POS} = -I_{NEG}$ simultaneously.

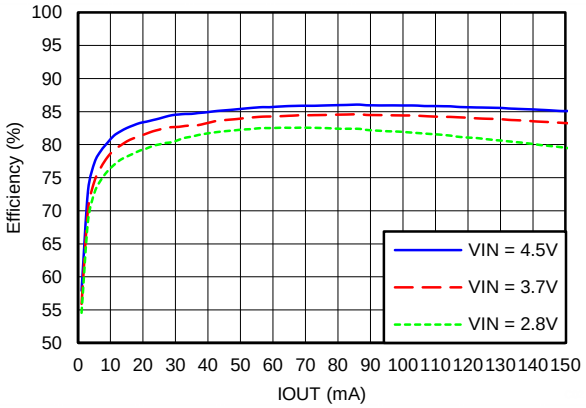


Figure 87. Combined Efficiency — ± 5.0 V — SYNC = HIGH L = 2.2 µH

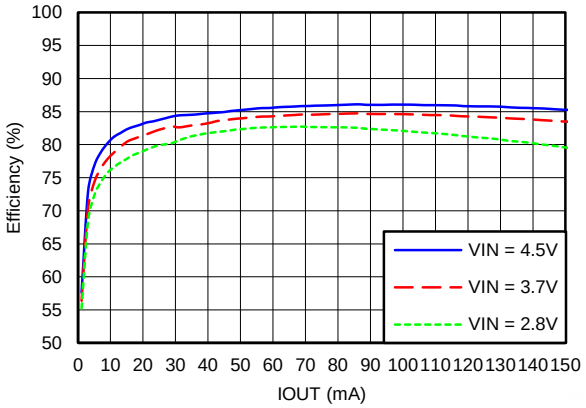


Figure 88. Combined Efficiency — ± 5.4 V — SYNC = HIGH L = 2.2 µH

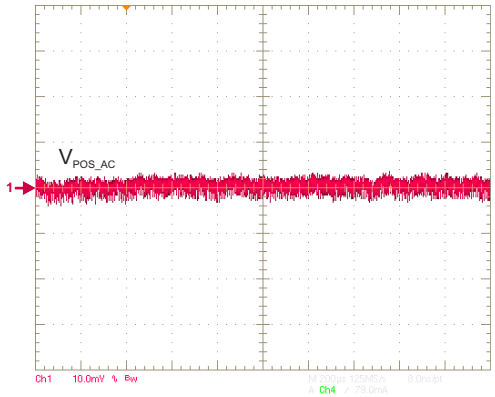


Figure 89. V_{POS} Output Voltage Ripple — SYNC = HIGH

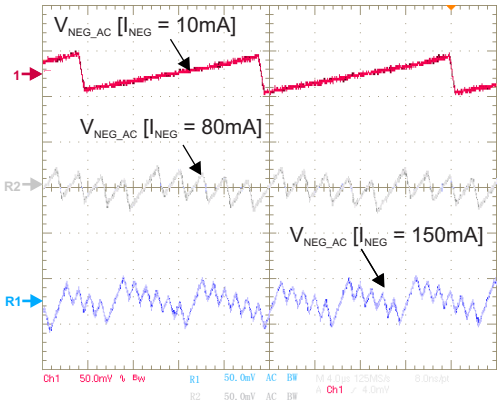


Figure 90. V_{NEG} Output Voltage Ripple — SYNC = HIGH — L = 2.2 µH — C_{OUT} = 10 µF

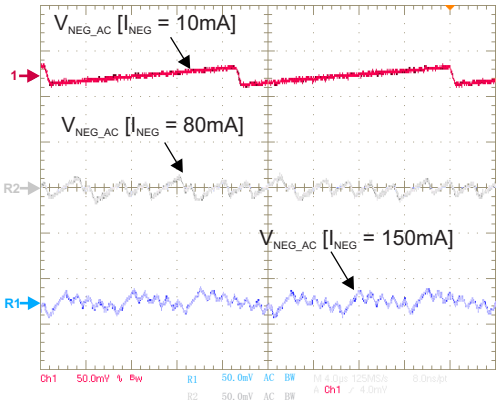


Figure 91. V_{NEG} Output Voltage Ripple — SYNC = HIGH — L = 2.2 µH — C_{OUT} = 2 × 10 µF

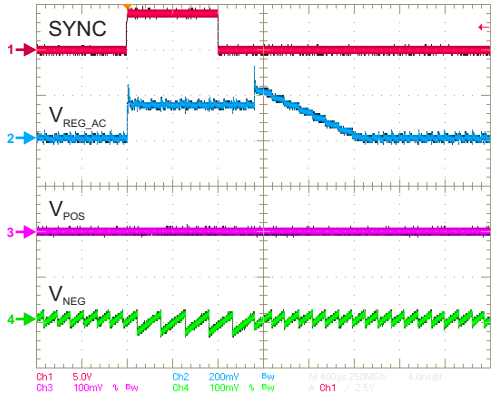


Figure 92. SYNC Signal — I_{OUT} = 10 mA

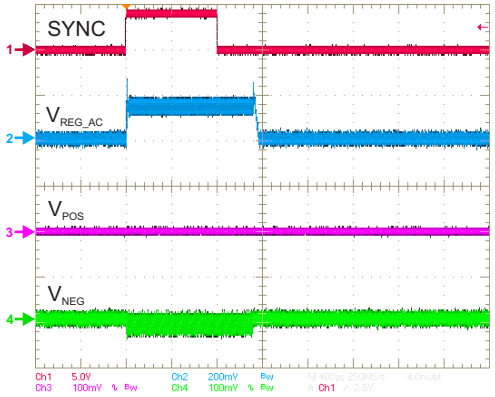


Figure 93. SYNC Signal — I_{OUT} = 150 mA

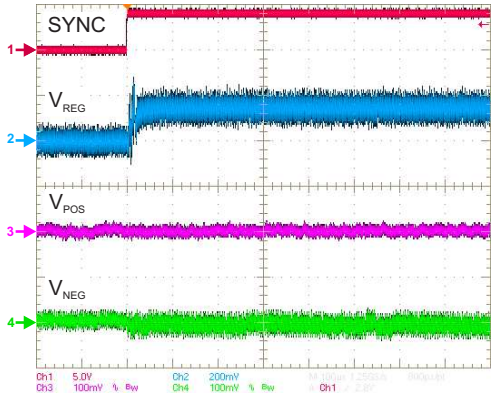


Figure 94. SYNC = HIGH (zoom)

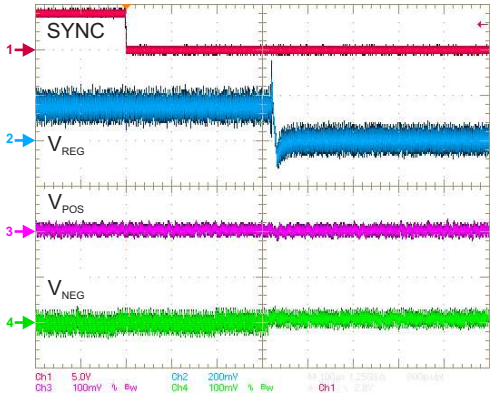


Figure 95. SYNC = LOW (zoom) with Delay

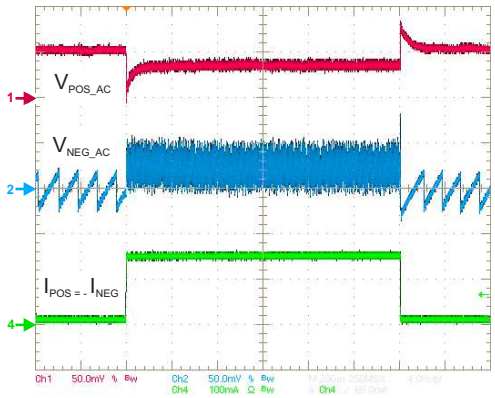


Figure 96. Load Transient — V_{IN} = 2.9 V
SYNC = HIGH — ΔI_{OUT} = 140 mA

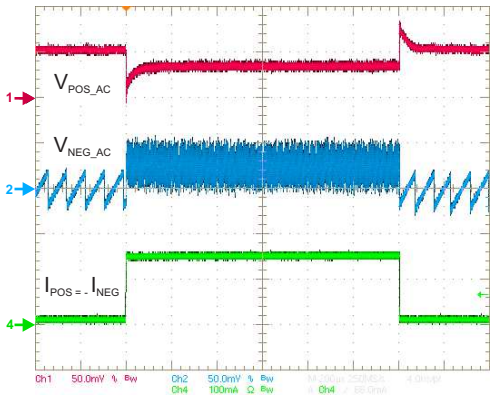


Figure 97. Load Transient — V_{IN} = 3.7 V
SYNC = HIGH — ΔI_{OUT} = 140 mA

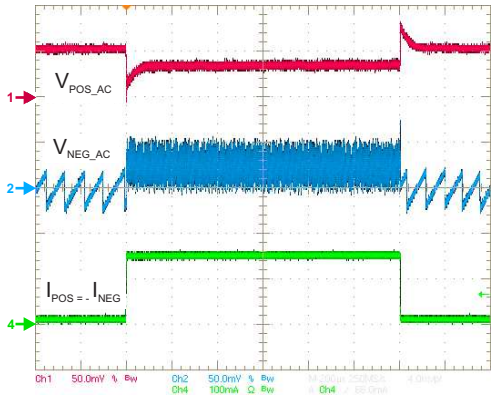


Figure 98. Load Transient — V_{IN} = 4.5 V SYNC = HIGH — ΔI_{OUT} = 140 mA

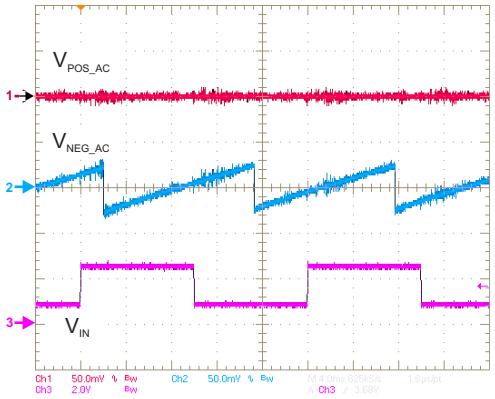


Figure 99. Line Transient — I_{OUT} = 10 mA SYNC = HIGH — ΔV_{IN} = 1.7 V

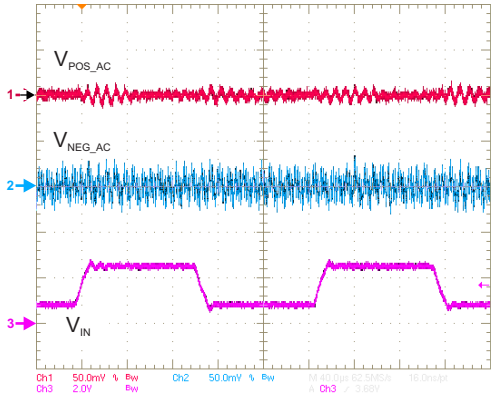


Figure 100. Line Transient — I_{OUT} = 100 mA SYNC = HIGH — ΔV_{IN} = 1.7 V

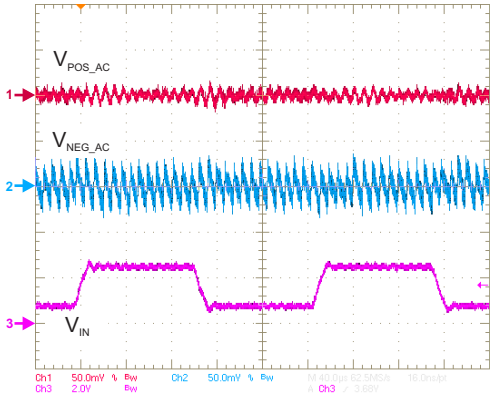


Figure 101. Line Transient — I_{OUT} = 150 mA SYNC = HIGH — ΔV_{IN} = 1.7 V

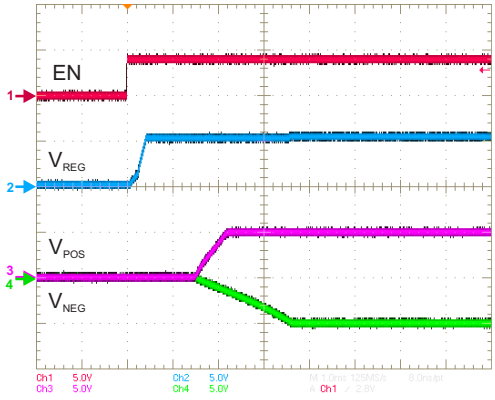


Figure 102. Power-Up Sequencing — Simultaneous SYNC = HIGH

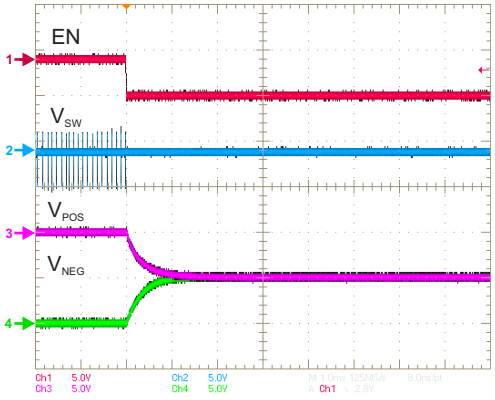


Figure 103. Power-Down Sequencing — Simultaneous SYNC = HIGH

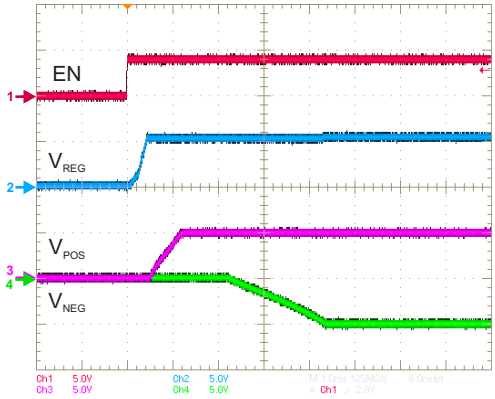


Figure 104. Power-Up Sequencing — Sequential VPOS → VNEG — SYNC = HIGH

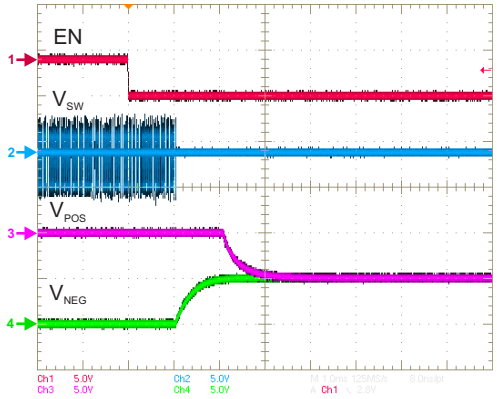


Figure 105. Power-Down Sequencing — Sequential VNEG → VPOS— SYNC = HIGH

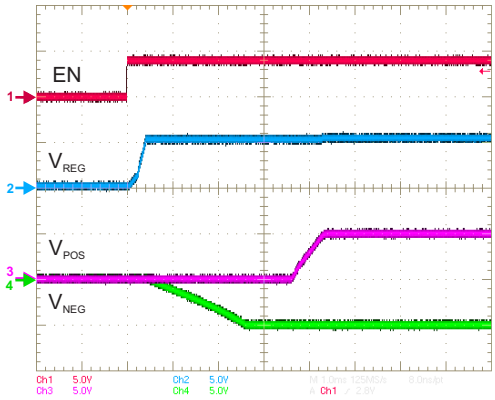


Figure 106. Power-Up Sequencing — Sequential VNEG → VPOS — SYNC = HIGH

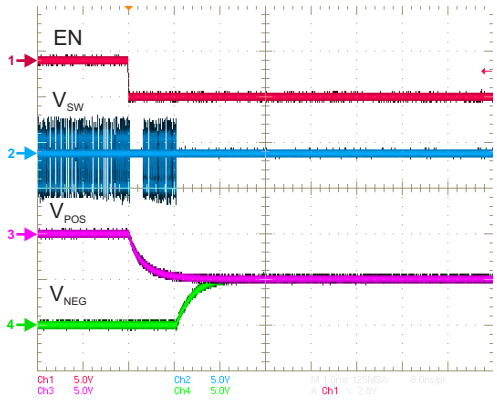


Figure 107. Power-Down Sequencing — Sequential VPOS → VNEG — SYNC = HIGH

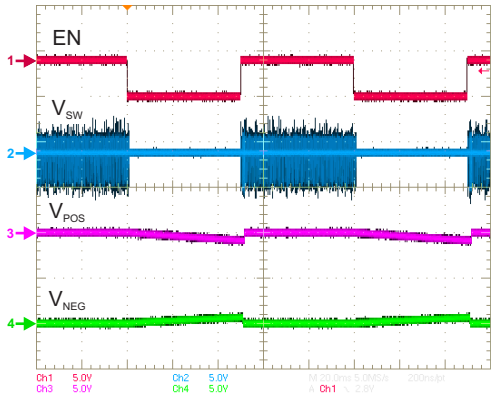


Figure 108. Power-Up/Down Without Active Discharge — SYNC = HIGH

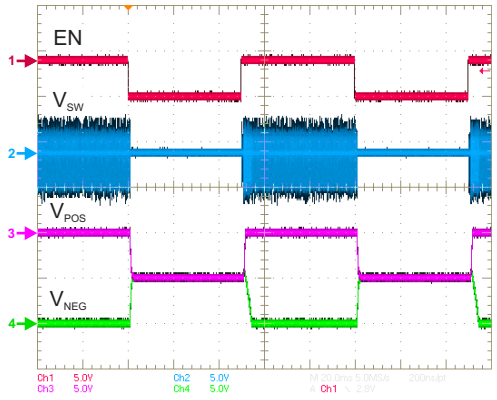


Figure 109. Power-Up/Down With Active Discharge — SYNC = HIGH

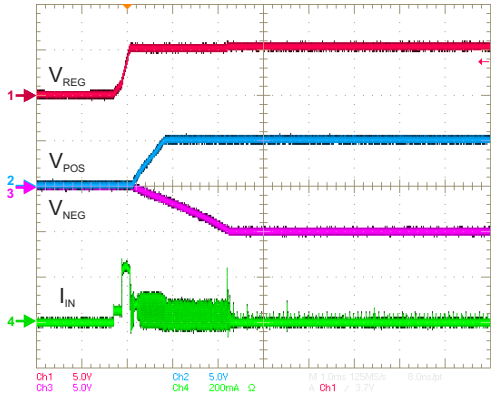


Figure 110. Inrush Current — Simultaneous — SYNC = HIGH

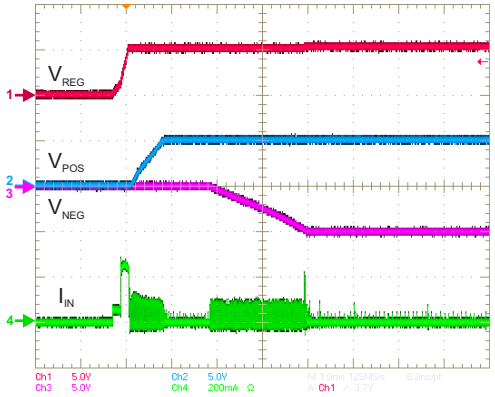


Figure 111. Inrush Current — Sequential SYNC = HIGH

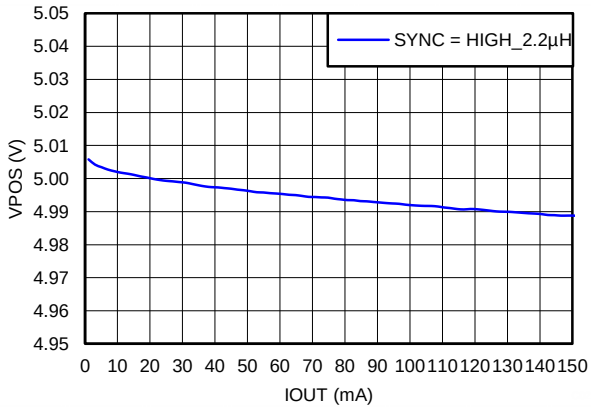


Figure 112. Load Regulation V_{POS} = 5.0 V — SYNC = HIGH

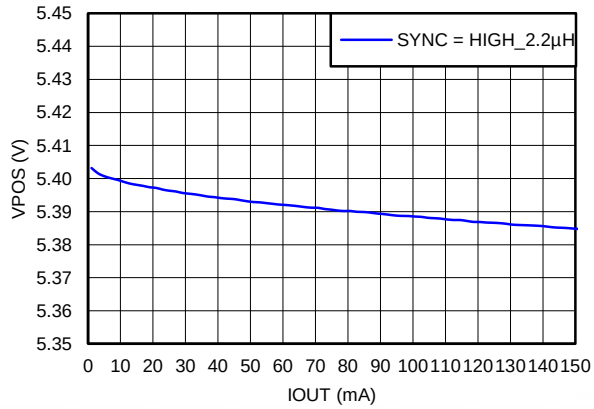


Figure 113. Load Regulation V_{POS} = 5.4 V — SYNC = HIGH

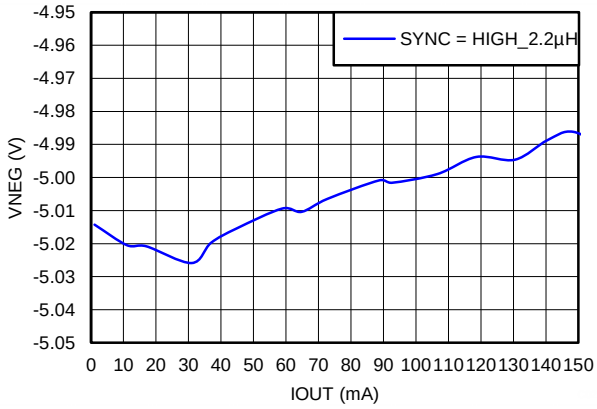


Figure 114. Load Regulation V_{NEG} = –5.0 V — SYNC = HIGH

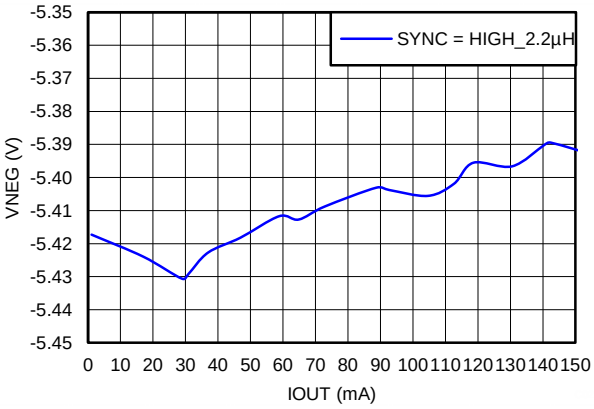


Figure 115. Load Regulation V_{NEG} = –5.4 V — SYNC = HIGH

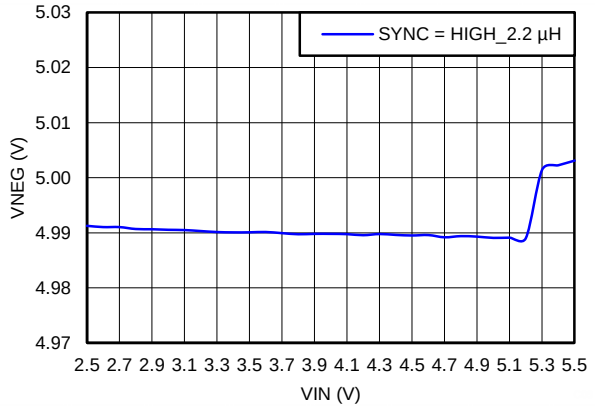


Figure 116. Line Regulation V_{POS} = 5.0 V — SYNC = HIGH

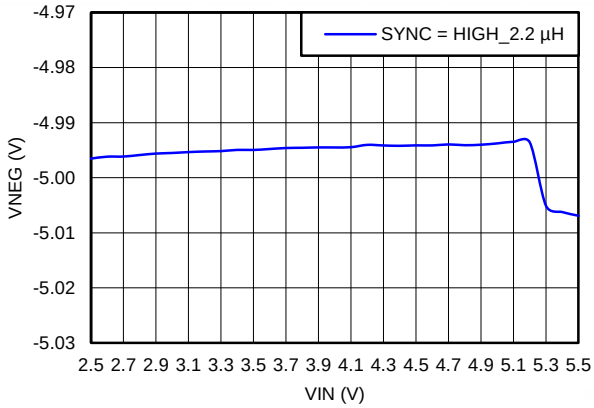


Figure 117. Line Regulation V_{POS} = 5.4 V — SYNC = HIGH

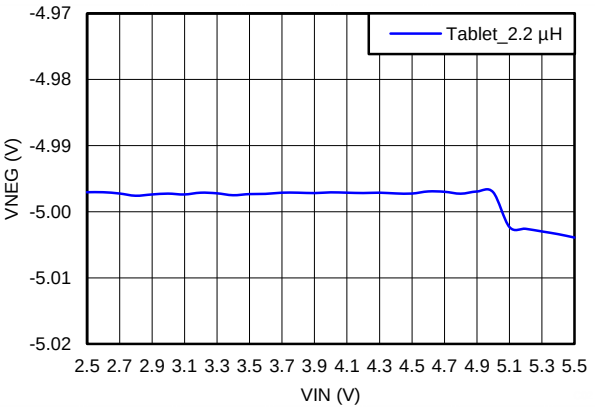


Figure 118. Line Regulation V_{NEG} = –5.0 V — SYNC = HIGH

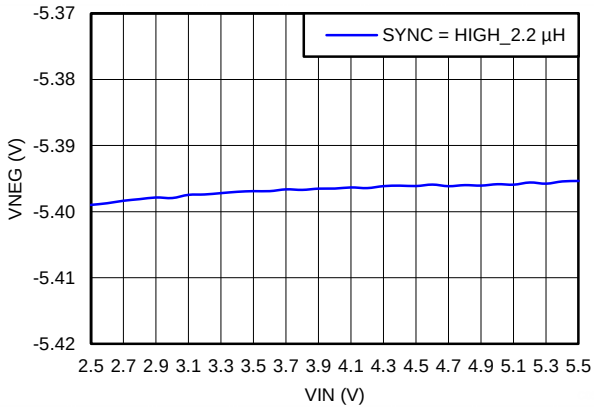


Figure 119. Line Regulation V_{NEG} = –5.4 V — SYNC = HIGH

10 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 2.5 V and 5.5 V. This input supply must be well regulated. A ceramic input capacitor with a value of 4.7 µF is a typical choice.

11 Layout

11.1 Layout Guidelines

PCB layout is an important task in the power supply design. Good PCB layout minimizes EMI and allows very good output voltage regulation. For the TPS65132 the following PCB layout guidelines are recommended.

- **Keep the power ground plane on the top layer (all capacitor grounds and PGND pins must be connected together with one uninterrupted ground plane).**
- **AGND and PGND must be connected together on the same ground plane.**
- **Place the flying capacitor as close as possible to the IC.**
- Always avoid vias when possible. They have high inductance and resistance. **If vias are necessary, always use more than one in parallel to decrease parasitics especially for power lines.**
- **Connect REG pins together.**
- For **high dv/dt** signals (switch pin traces): keep copper area to a minimum to prevent making unintentional parallel plate capacitors with other traces or to a ground plane. Best to route signal and return on same layer.
- For **high di/dt** signals: keep traces short, wide and closely spaced. This will reduce stray inductance and decrease the current loop area to help prevent EMI.
- Keep input capacitor close to the IC with low inductance traces.
- Keep trace from switching node pin to inductor short if possible: **it reduces EMI emissions and noise that may couple into other portions of the converter.**
- Isolate analog signal paths from power paths.

11.2 Layout Example

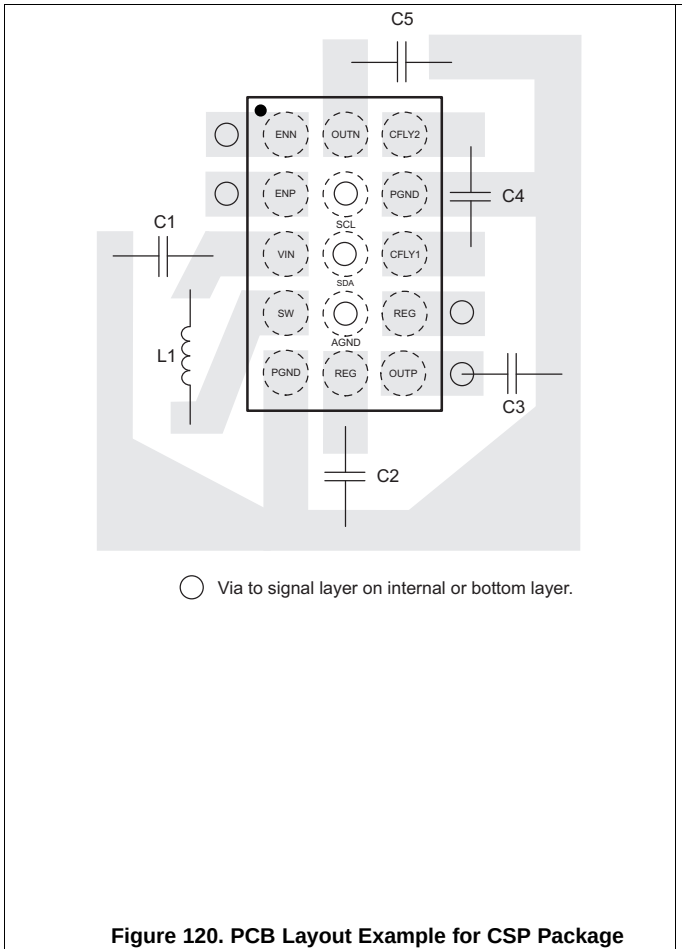


Figure 120. PCB Layout Example for CSP Package

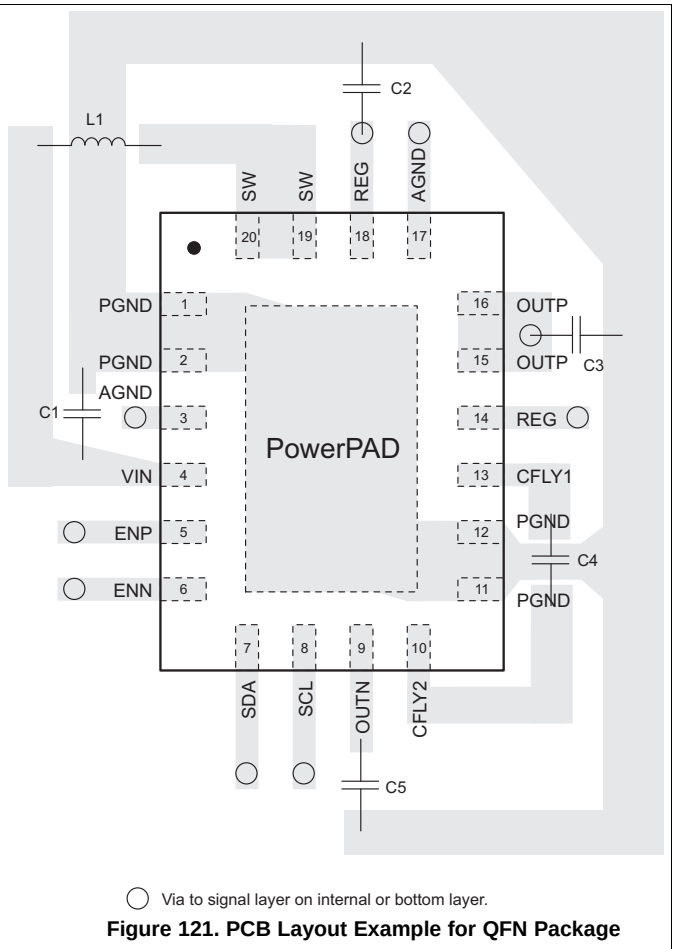


Figure 121. PCB Layout Example for QFN Package

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

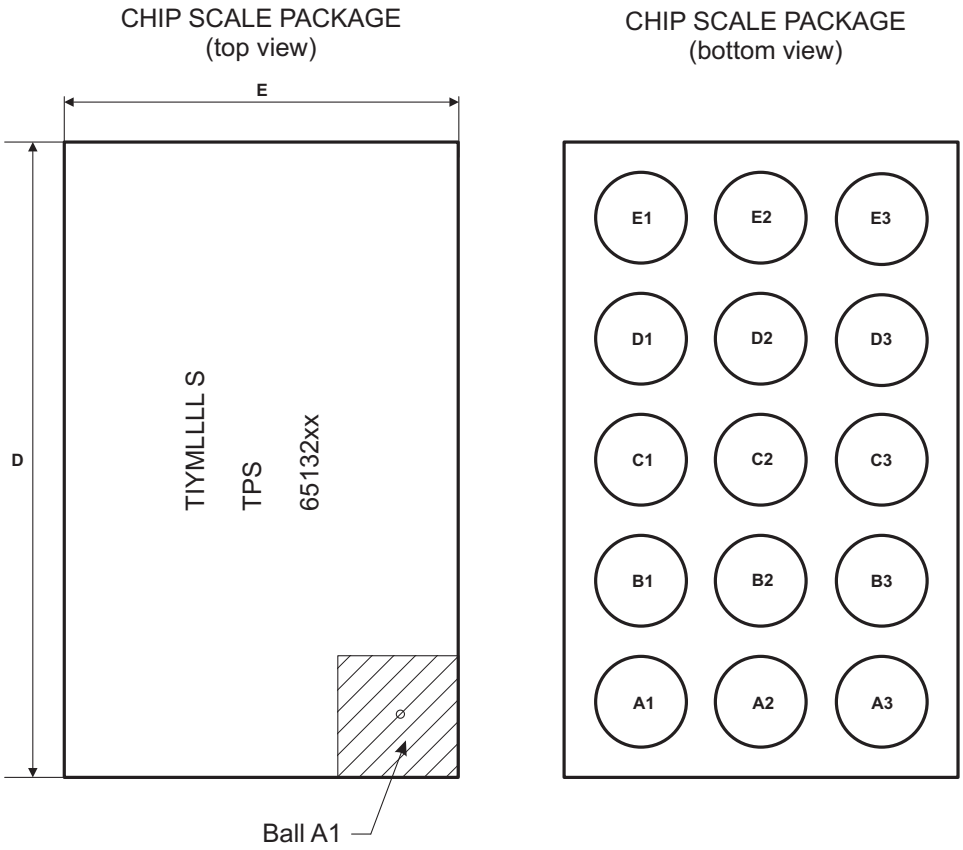
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 CSP Package Summary



Code:

- TI -- TI letters
- YM -- Year-Month date code
- LLLL -- Lot trace code
- S -- Assembly site code
- xx -- Revision code (contains alpha-numeric characters - can be left blank), refer to the Ordering Information section for detailed information)

13.1.1 Chip Scale Package Dimensions

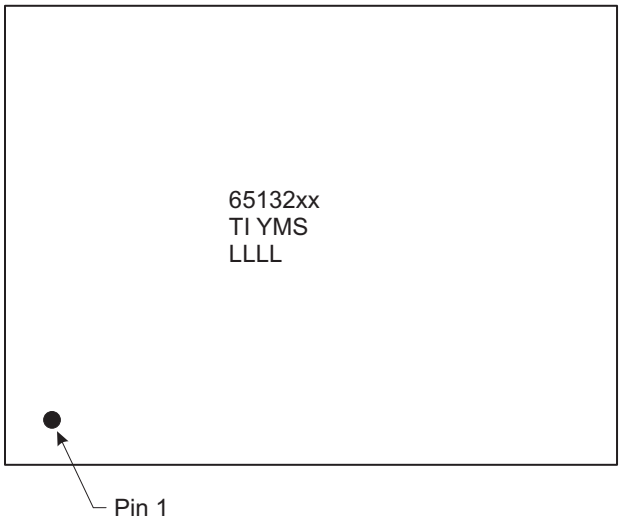
The TPS65132 device is available in a 15-bump chip scale package (YFF, NanoFree™). The package dimensions are given as:

- D = 2108 ±30 µm
- E = 1514 ±30 µm

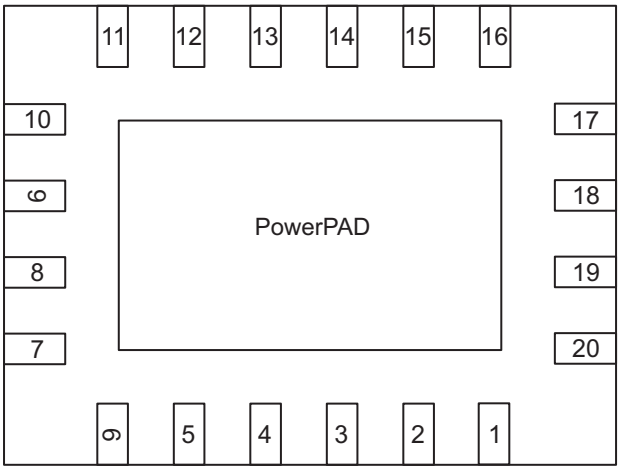
CSP Package Summary (continued)

13.1.2 RVC Package Summary

QFN PACKAGE
(top view)



QFN PACKAGE
(bottom view)



Code:

- TI -- TI letters
- YM -- Year-Month date code
- LLLL -- Lot trace code
- S -- Assembly site code
- xx -- Revision code (contains alpha-numeric characters - can be left blank), refer to the Ordering Information section for detailed information)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65132A0YFFR	ACTIVE	DSBGA	YFF	15	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS 65132A0	Samples
TPS65132AYFFR	ACTIVE	DSBGA	YFF	15	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS 65132A	Samples
TPS65132B0YFFR	ACTIVE	DSBGA	YFF	15	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS 65132B0	Samples
TPS65132B2YFFR	ACTIVE	DSBGA	YFF	15	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS 65132B2	Samples
TPS65132B5YFFR	ACTIVE	DSBGA	YFF	15	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS 65132B5	Samples
TPS65132BYFFR	ACTIVE	DSBGA	YFF	15	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS 65132B	Samples
TPS65132L0YFFR	ACTIVE	DSBGA	YFF	15	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS 65132L0	Samples
TPS65132L0YFFT	ACTIVE	DSBGA	YFF	15	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS 65132L0	Samples
TPS65132LYFFR	ACTIVE	DSBGA	YFF	15	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS 65132L	Samples
TPS65132T6YFFR	ACTIVE	DSBGA	YFF	15	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS 65132T6	Samples
TPS65132T6YFFT	ACTIVE	DSBGA	YFF	15	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS 65132T6	Samples
TPS65132WRVCR	ACTIVE	WQFN	RVC	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	65132YA	Samples
TPS65132WRVCT	ACTIVE	WQFN	RVC	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	65132YA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

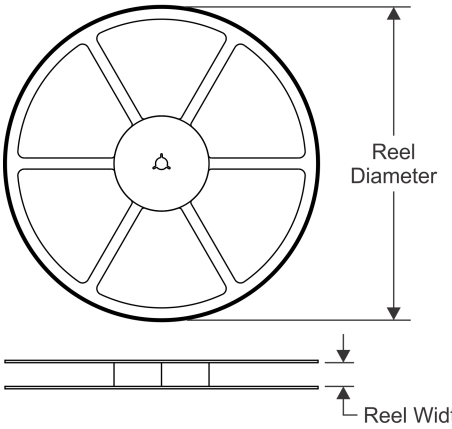
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

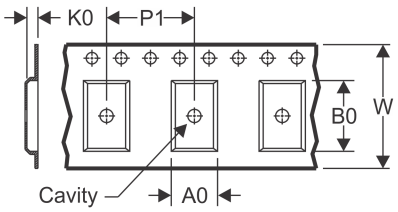
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

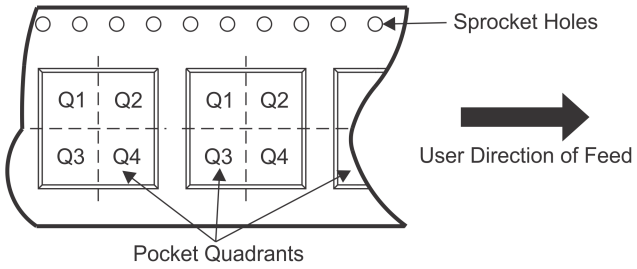


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

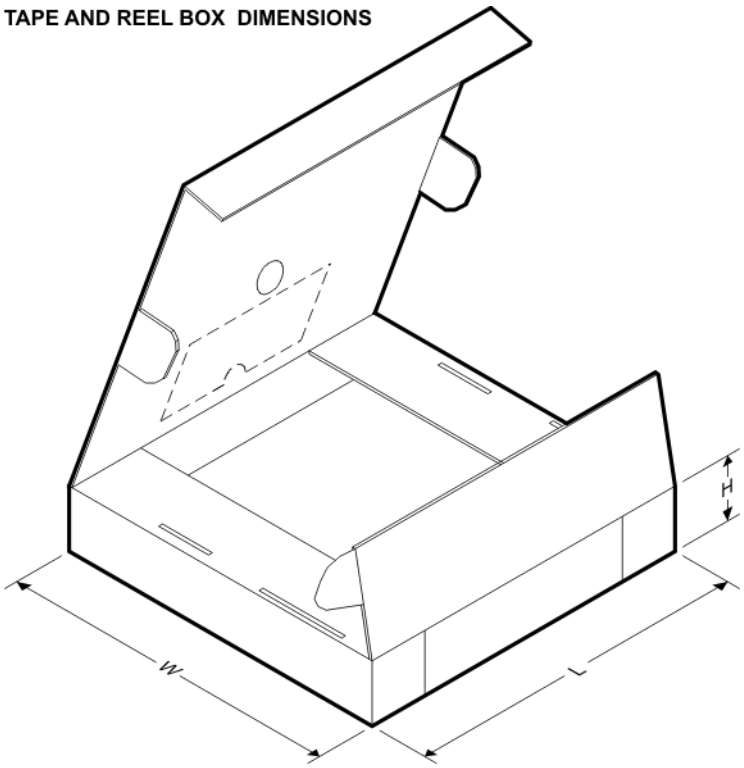
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65132B0YFFR	DSBGA	YFF	15	3000	180.0	8.4	1.61	2.21	0.7	4.0	8.0	Q1
TPS65132B5YFFR	DSBGA	YFF	15	3000	180.0	8.4	1.61	2.21	0.7	4.0	8.0	Q1
TPS65132L0YFFT	DSBGA	YFF	15	250	180.0	8.4	1.61	2.21	0.7	4.0	8.0	Q1
TPS65132LYFFR	DSBGA	YFF	15	3000	180.0	8.4	1.61	2.21	0.7	4.0	8.0	Q1
TPS65132T6YFFR	DSBGA	YFF	15	3000	180.0	8.4	1.61	2.21	0.7	4.0	8.0	Q1
TPS65132T6YFFT	DSBGA	YFF	15	250	180.0	8.4	1.61	2.21	0.7	4.0	8.0	Q1
TPS65132WRVCR	WQFN	RVC	20	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
TPS65132WRVCT	WQFN	RVC	20	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1

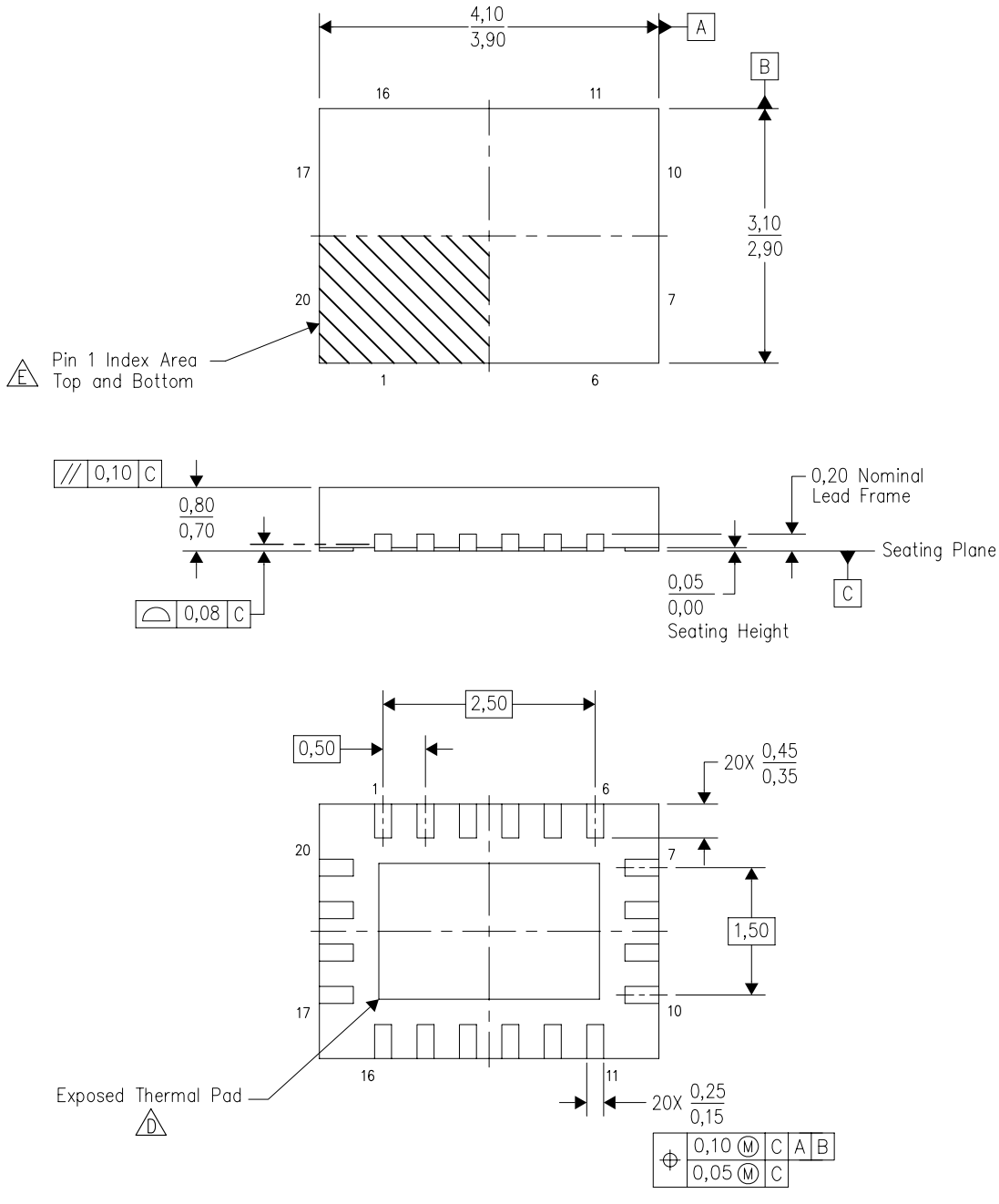
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65132B0YFFR	DSBGA	YFF	15	3000	182.0	182.0	20.0
TPS65132B5YFFR	DSBGA	YFF	15	3000	182.0	182.0	20.0
TPS65132L0YFFT	DSBGA	YFF	15	250	182.0	182.0	20.0
TPS65132LYFFR	DSBGA	YFF	15	3000	182.0	182.0	20.0
TPS65132T6YFFR	DSBGA	YFF	15	3000	182.0	182.0	20.0
TPS65132T6YFFT	DSBGA	YFF	15	250	182.0	182.0	20.0
TPS65132WRVCR	WQFN	RVC	20	3000	552.0	367.0	36.0
TPS65132WRVCT	WQFN	RVC	20	250	552.0	185.0	36.0

RVC (R–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



4209819/A 10/2008

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

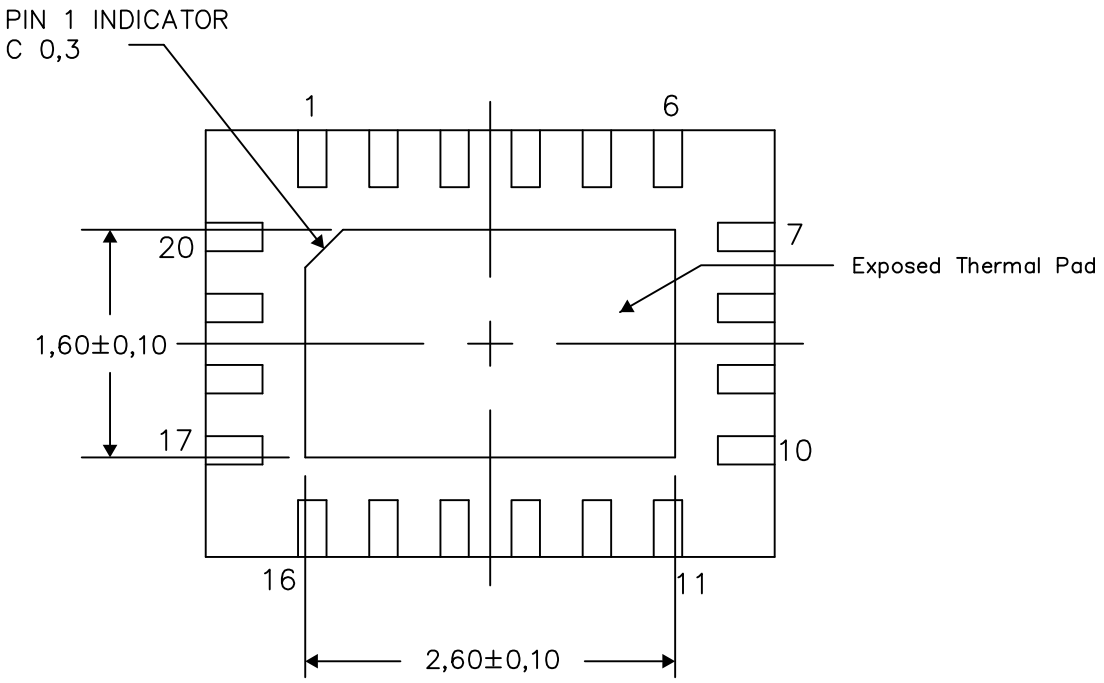
RVC (R–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



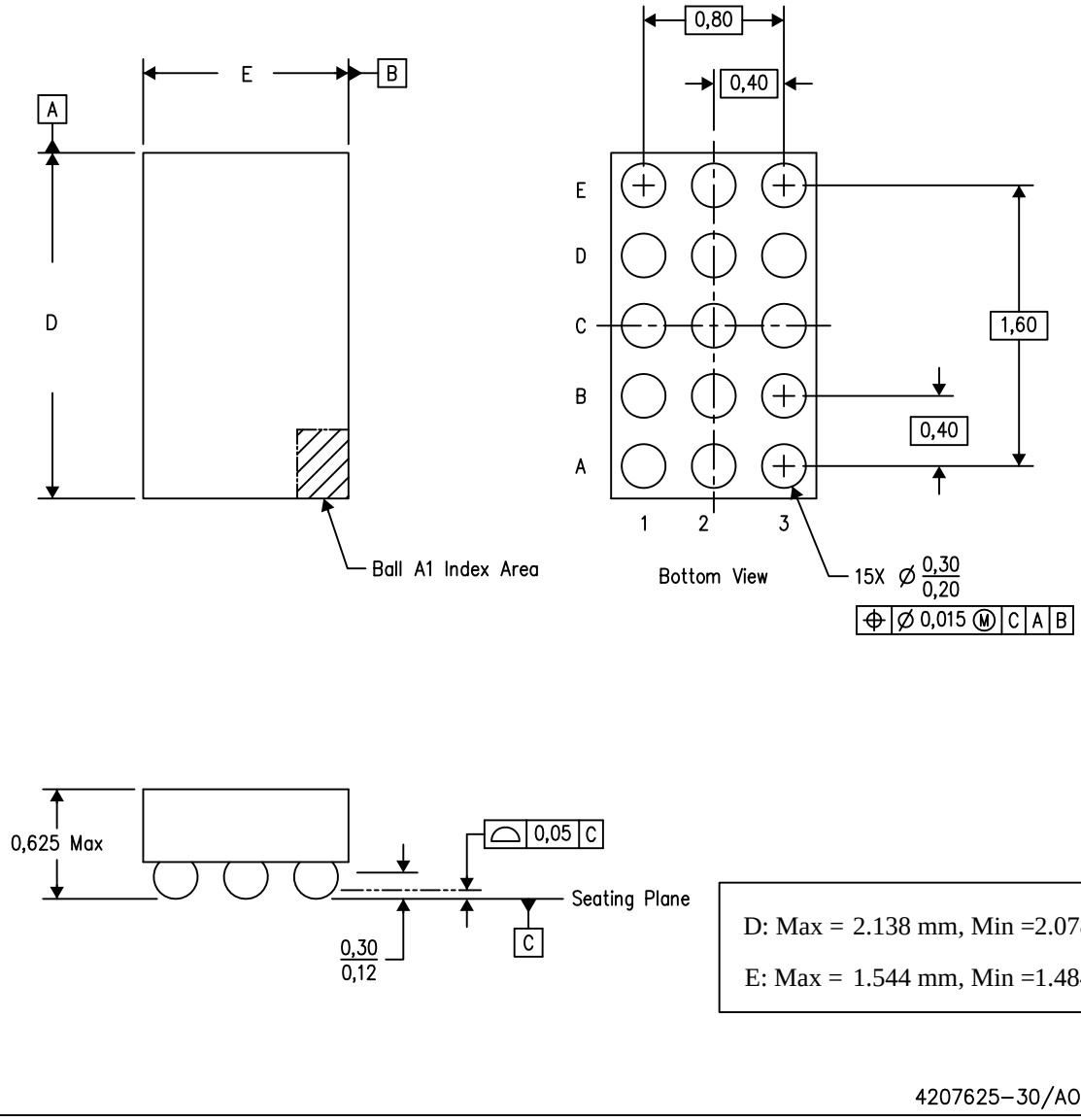
Bottom View

Exposed Thermal Pad Dimensions

4209820–2/F 03/15

NOTE: All linear dimensions are in millimeters

YFF (R–XBGA–N15) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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