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April 1st, 2010 Renesas Electronics Corporation

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MOS FIELD EFFECT TRANSISTOR NP36P04SDG

SWITCHING P-CHANNEL POWER MOSFET

DESCRIPTION

The NP36P04SDG is P-channel MOS Field Effect Transistor designed for high current switching applications.

ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE		
NP36P04SDG-E1-AY Note			TO 050 (MD 07//)		
NP36P04SDG-E2-AY Note	6P04SDG-E2-AY Note Pure Sn (Tin)	Tape 2500 p/reel	TO-252 (MP-3ZK)		

Note Pb-free (This product does not contain Pb in external electrode.)

FEATURES

Super low on-state resistance

 $R_{DS(on)1}$ = 17.0 m Ω MAX. (VGS = -10 V, ID = -18 A)

 $R_{DS(on)2}$ = 23.5 m Ω MAX. (V_{GS} = -4.5 V, I_D = -18 A)

- Low input capacitance
- Ciss = 2800 pF TYP.

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (Vgs = 0 V)	VDSS	-40	V
Gate to Source Voltage (VDS = 0 V)	Vgss	∓20	V
Drain Current (DC) (Tc = 25°C)	ID(DC)	∓36	Α
Drain Current (pulse) ^{Note1}	D(pulse)	∓108	Α
Total Power Dissipation (Tc = 25°C)	P _{T1}	56	W
Total Power Dissipation (T _A = 25°C)	P _{T2}	1.2	W
Channel Temperature	Tch	175	°C
Storage Temperature	Tstg	-55 to +175	°C
Single Avalanche Current Note2	las	26	Α
Single Avalanche Energy Note2	Eas	67	mJ

Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

2. Starting T_{ch} = 25°C, V_{DD} = -20 V, R_G = 25 Ω , V_{GS} = $-20 \rightarrow 0$ V

THERMAL RESISTANCE

<R>

Channel to Case Thermal Resistance	Rth(ch-C)	2.68	°C/W
Channel to Ambient Thermal Resistance	Rth(ch-A)	125	°C/W

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(TO-252)

The mark <R> shows major revised points.

The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

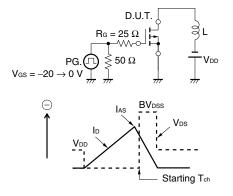
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	ldss	V _{DS} = -40 V, V _{GS} = 0 V			-10	μA
Gate Leakage Current	lgss	V _{GS} = ∓20 V, V _{DS} = 0 V			∓100	nA
Gate to Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-1.0	-1.6	-2.5	V
Forward Transfer Admittance Note	y _{fs}	V _{DS} = -10 V, I _D = -18 A	12	23		S
Drain to Source On-state Resistance Note	RDS(on)1	V _{GS} = −10 V, I _D = −18 A		12.5	17.0	mΩ
	RDS(on)2	V _{GS} = −4.5 V, I _D = −18 A		15.4	23.5	mΩ
Input Capacitance	Ciss	V _{DS} = -10 V,		2800		рF
Output Capacitance	Coss	V _{GS} = 0 V,		450		рF
Reverse Transfer Capacitance	Crss	f = 1 MHz		280		рF
Turn-on Delay Time	td(on)	$V_{DD} = -20 V$, $I_D = -18 A$,		8		ns
Rise Time	tr	V _{GS} = -10 V,		10		ns
Turn-off Delay Time	td(off)	Rg = 0 Ω		250		ns
Fall Time	tr			140		ns
Total Gate Charge	QG	$V_{DD} = -32 V,$		55		nC
Gate to Source Charge	Q _{GS}	V _{GS} = -10 V,		7		nC
Gate to Drain Charge	Qgd	I⊳ = –36 A		15		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	IF = -36 A, V _{GS} = 0 V		0.95	1.5	V
Reverse Recovery Time	trr	IF = -36 A, VGS = 0 V,		44		ns
Reverse Recovery Charge	Qrr	di/dt = −100 A/µs		51		nC

ELECTRICAL CHARACTERISTICS (TA = 25°C)

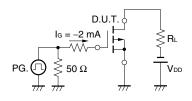
Note Pulsed test PW \leq 350 μ s, Duty Cycle \leq 2%

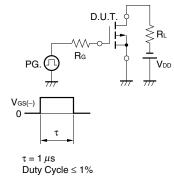
TEST CIRCUIT 1 AVALANCHE CAPABILITY

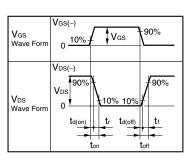
TEST CIRCUIT 2 SWITCHING TIME



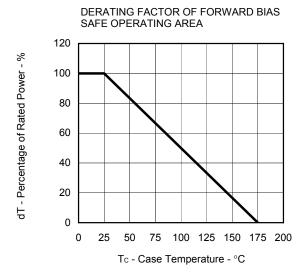
TEST CIRCUIT 3 GATE CHARGE



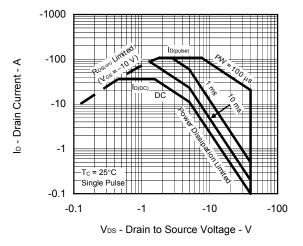


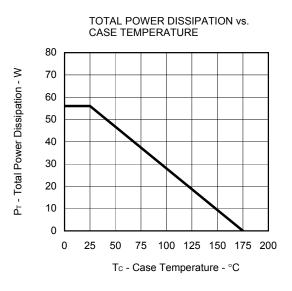


TYPICAL CHARACTERISTICS (TA = 25°C)

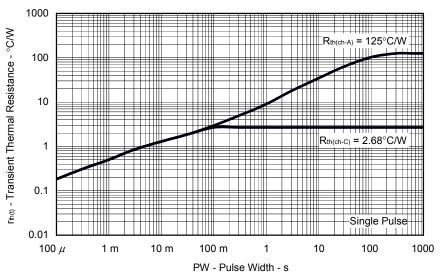




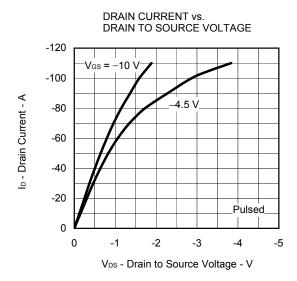




TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

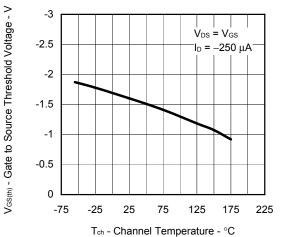


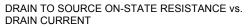
Data Sheet D19074EJ2V0DS

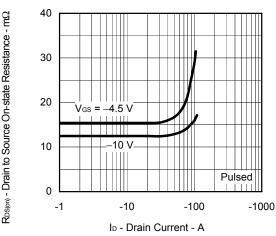


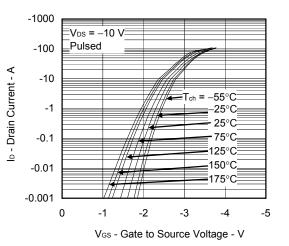
NEC

GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



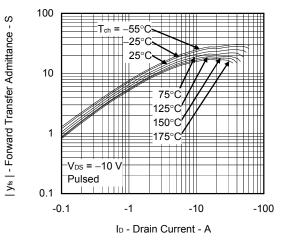


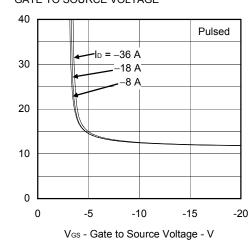




FORWARD TRANSFER CHARACTERISTICS

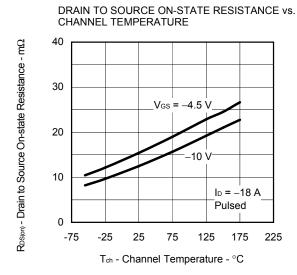
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

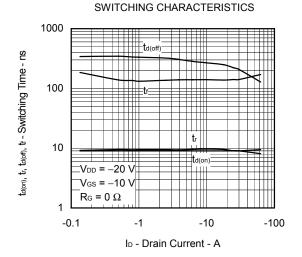


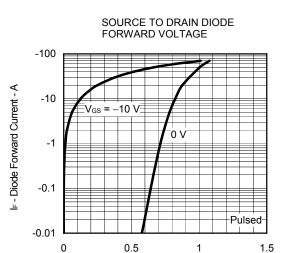


DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

RDS(on) - Drain to Source On-state Resistance - m0

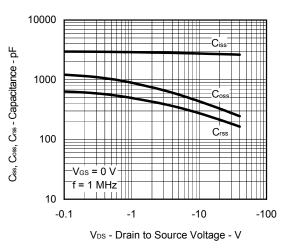




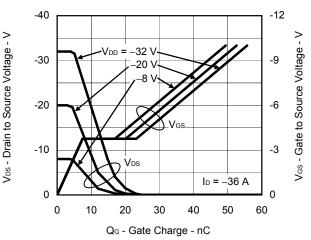


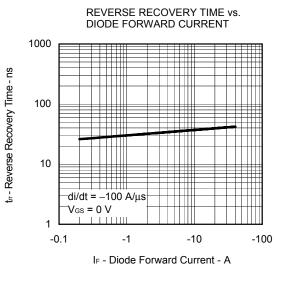
VF(S-D) - Source to Drain Voltage - V

CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

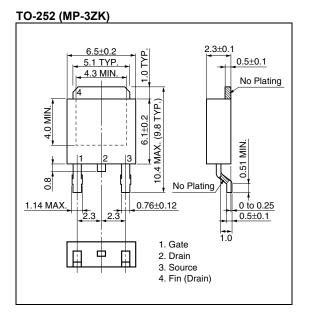


DYNAMIC INPUT/OUTPUT CHARACTERISTICS

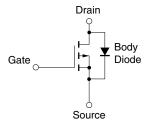




PACKAGE DRAWING (Unit: mm)



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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