

P-Channel Power MOSFET

-20V, -4.7A, 50mΩ

FEATURES

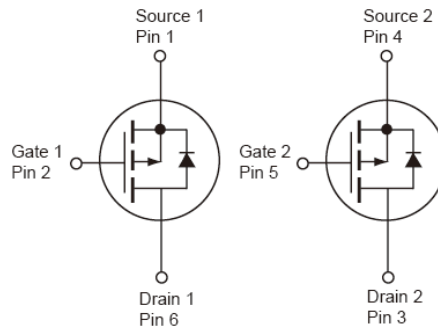
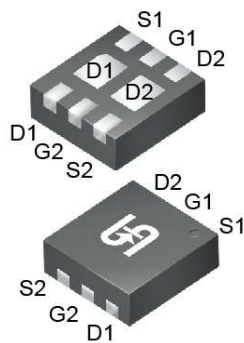
- Halogen-free
- Suited for 1.8V drive applications
- Low profile package

APPLICATION

- Battery Pack
- Load Switch

KEY PERFORMANCE PARAMETERS

PARAMETER		VALUE	UNIT
V_{DS}		-20	V
$R_{DS(on)}$ (max)	$V_{GS} = -4.5V$	50	mΩ
	$V_{GS} = -2.5V$	65	
	$V_{GS} = -1.8V$	85	
Q_g		9.6	nC


TDFN2x2

Notes: Moisture sensitivity level: level 3. Per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	± 10	V
Continuous Drain Current ^(Note 1)	$T_C = 25^\circ\text{C}$	I_D	-4.7	A
	$T_C = 100^\circ\text{C}$		-2.82	
Pulsed Drain Current ^(Note 2)		I_{DM}	-18.8	A
Total Power Dissipation @ $T_C = 25^\circ\text{C}$		P_{DTOT}	0.62	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	$^\circ\text{C}$

THERMAL PERFORMANCE

PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	200	$^\circ\text{C/W}$

Notes: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 PCB in still air.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static ^(Note 3)						
Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = -250μA	BV _{DSS}	-20	--	--	V
Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250μA	V _{GS(TH)}	-0.3	-0.6	-0.8	V
Gate Body Leakage	V _{GS} = ±10V, V _{DS} = 0V	I _{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V _{DS} = -20V, V _{GS} = 0V	I _{DSS}	--	--	-1	μA
Drain-Source On-State Resistance	V _{GS} = -4.5V, I _D = -3A	R _{DS(ON)}	--	42	50	mΩ
	V _{GS} = -2.5V, I _D = -2A		--	57	65	
	V _{GS} = -1.8V, I _D = -1A		--	75	85	
Forward Transconductance	V _{DS} = -10V, I _D = -3A	g _{fs}	--	7	--	S
Dynamic ^(Note 4)						
Total Gate Charge	V _{DS} = -10V, I _D = -3.0A, V _{GS} = -4.5V	Q _g	--	9.6	13	nC
Gate-Source Charge		Q _{gs}	--	1.6	2	
Gate-Drain Charge		Q _{gd}	--	2	4	
Input Capacitance	V _{DS} = -10V, V _{GS} = 0V, f = 1.0MHz	C _{iss}	--	850	1230	pF
Output Capacitance		C _{oss}	--	70	100	
Reverse Transfer Capacitance		C _{rss}	--	55	80	
Switching ^(Note 5)						
Turn-On Delay Time	V _{DD} = -10V, R _{GEN} = 25Ω, I _D = -1A, V _{GS} = -4.5V,	t _{d(on)}	--	6	11	ns
Turn-On Rise Time		t _r	--	21.6	41	
Turn-Off Delay Time		t _{d(off)}	--	51	97	
Turn-Off Fall Time		t _f	--	13.8	26	
Source-Drain Diode ^(Note 3)						
Continuous Source Current	V _G = V _D = 0V, Force Current	I _S	--	--	-4.7	A
Pulsed Source Current		I _{SM}	--	--	-18.8	A
Forward On Voltage	I _S = -1.0A, V _{GS} = 0V	V _{SD}	--	--	-1.0	V

Notes:

1. Current limited by package
2. Pulse width limited by the maximum junction temperature
3. Pulse test: $PW \leq 300\mu s$, duty cycle $\leq 2\%$
4. For DESIGN AID ONLY, not subject to production testing.
5. Switching time is essentially independent of operating temperature.

ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM500P02DCQ RFG	TDFN 2x2	3,000pcs / 7" Reel

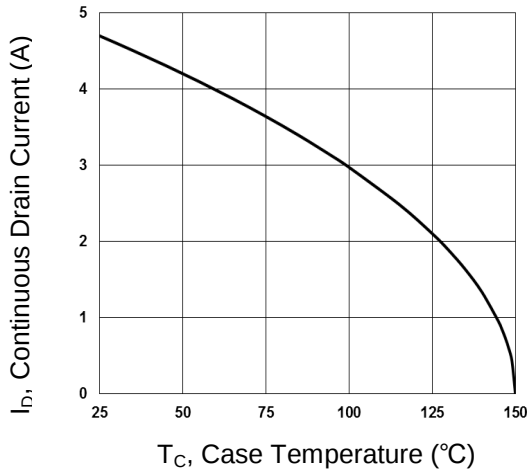
Note:

1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
2. Halogen-free according to IEC 61249-2-21 definition

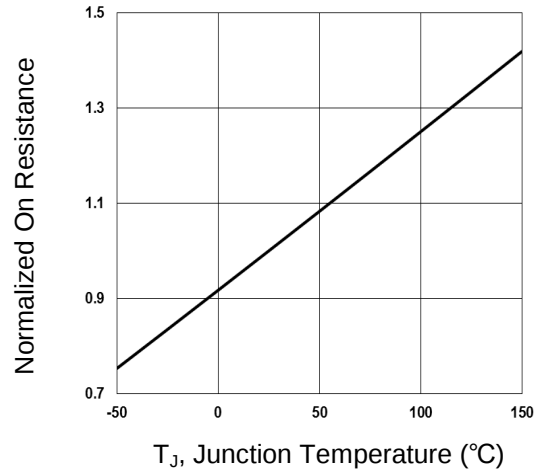
CHARACTERISTICS CURVES

($T_C = 25^\circ\text{C}$ unless otherwise noted)

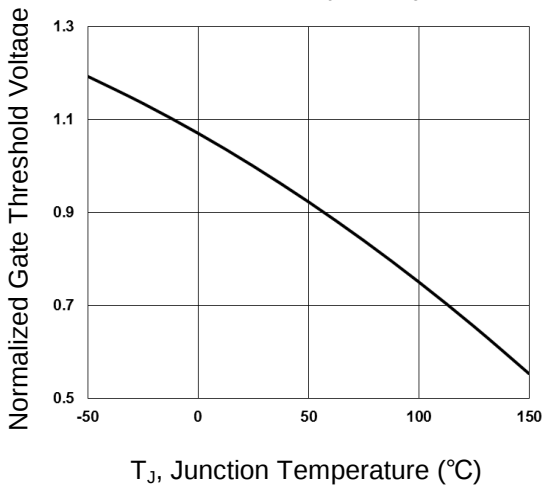
Continuous Drain Current vs. T_C



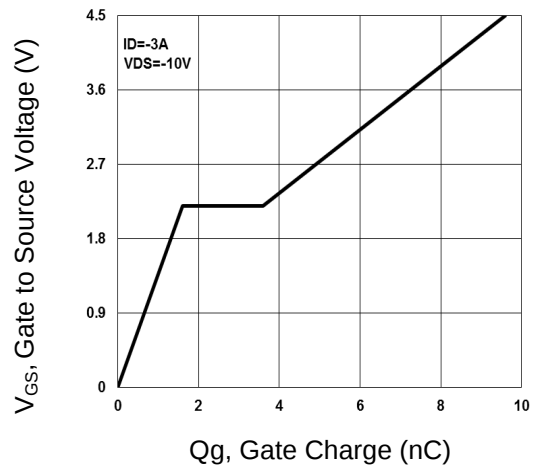
Normalized $R_{DS(on)}$ vs. T_J



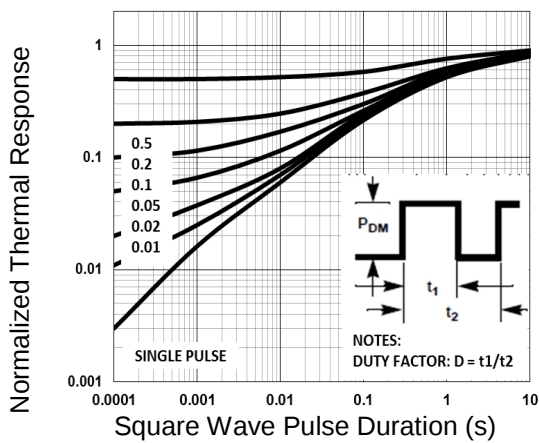
Normalized V_{th} vs. T_J



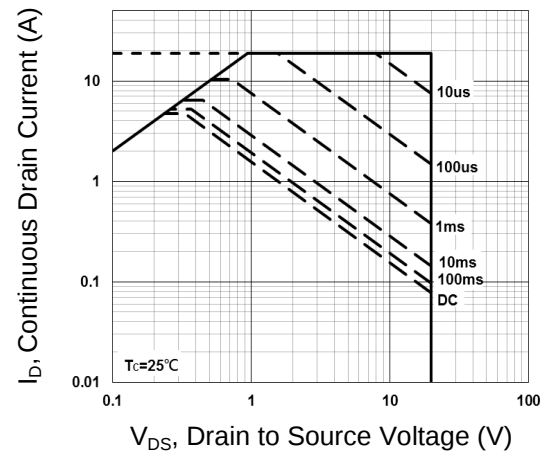
Gate Charge Waveform



Normalized Transient Impedance

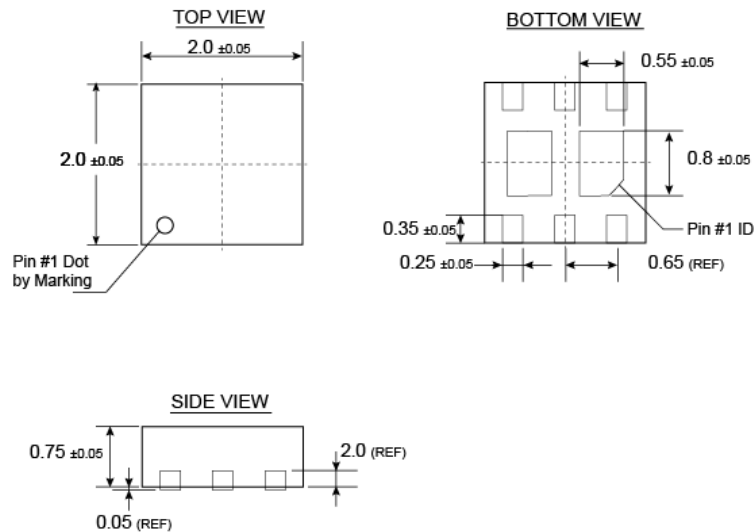


Maximum Safe Operation Area

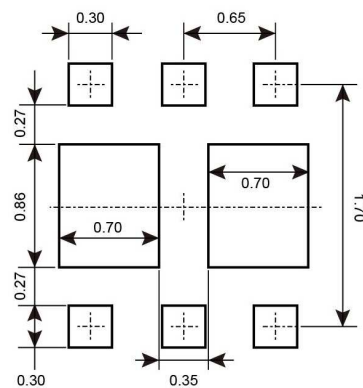


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

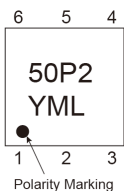
TDFN2x2



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



Y = Year Code

M = Month Code for Halogen Free Product

O =Jan **P** =Feb **Q** =Mar **R** =Apr

S =May **T** =Jun **U** =Jul **V** =Aug

W =Sep **X** =Oct **Y** =Nov **Z** =Dec

L = Lot Code (1~9, A~Z)

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