4-Channel, I²C, Ultralow Power, 12-Bit ADC in 20-Lead LFCSP/TSSOP

Data Sheet **AD7091R-5**

FEATURES

- I²C-compatible serial interface supports standard and fast modes
- Ultralow power: 90 µW typical at 3 V in fast mode
- Specified for V_{DD} of 2.7 V to 5.25 V
- On-chip accurate 2.5 V reference, 5 ppm/°C typical drift
- 4 single-ended analog input channels
- ALERT function
- BUSY function
- Autocycle mode
- Wide input bandwidth
  - 68 dB signal-to-noise ratio (SNR) typical at input frequency of 1 kHz
- Flexible power/throughput rate management
- No pipeline delays
- Power-down mode
  - 550 nA typical at V_{DD} = 5.25 V
  - 435 nA typical at V_{DD} = 3 V
- 20-lead LFCSP and TSSOP packages
- Temperature range: −40°C to +125°C

APPLICATIONS

- Battery-powered systems
  - Personal digital assistants
  - Medical instruments
  - Mobile communications
- Instrumentation and control systems
- Data acquisition systems
- Optical sensors
- Diagnostic/monitoring functions

FUNCTIONAL BLOCK DIAGRAM

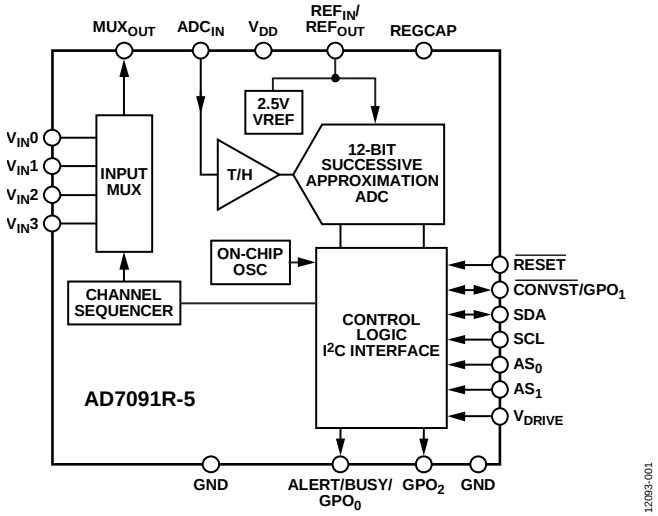

Figure 1.

GENERAL DESCRIPTION

The AD7091R-5 is a 12-bit, multichannel, ultralow power, successive approximation analog-to-digital converter (ADC). The AD7091R-5 operates from a single 2.7 V to 5.25 V power supply and typically consumes only 24 µA at a 3 V supply in fast mode.

The AD7091R-5 provides a 2-wire serial interface compatible with I²C interfaces. The conversion process can be controlled by a sample mode via the $\overline{\text{CONVST}}/\text{GPO}_1$ pin, an autocycle mode selected through software control, or a command mode in which conversions occur across I²C write operations.

The device contains a wide bandwidth track-and-hold amplifier that can handle input frequencies up to 1.5 MHz. The AD7091R-5 also features an on-chip conversion clock, an on-chip accurate 2.5 V reference, and a programmable out of bounds user alert function.

The AD7091R-5 offers four single-ended analog input channels with a channel sequencer that allows a preprogrammed selection of channels to be converted sequentially.

The AD7091R-5 uses advanced design techniques to achieve ultralow power dissipation without compromising performance. It also features flexible power management options. An on-chip configuration register allows the user to set up different operating conditions. These include power management, alert functionality, busy indication, channel sequencing, and general-purpose output pins. The MUX_{OUT} and ADC_{IN} pins allow signal conditioning of the multiplexer output before acquisition by the ADC.

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REVISION HISTORY

7/15—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.7 V to 5.25 V, V_{DRIVE} = 1.8 V to 5.25 V, f_{SCL} = 400 kHz, fast SCL mode, V_{REF} = 2.5 V internal/external, T_A = −40°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE	f_{IN} = 1 kHz sine wave				
Signal-to-Noise Ratio (SNR)			68		dB
Signal-to-Noise-and-Distortion Ratio (SINAD)			67		dB
Total Harmonic Distortion (THD)			−80		dB
Spurious-Free Dynamic Range (SFDR)			−81		dB
Channel to Channel Isolation			−105		dB
Aperture Delay			5		ns
Aperture Jitter			40		ps
Full Power Bandwidth	At −3 dB		1.5		MHz
	At −0.1 dB		1.2		MHz
DC ACCURACY					
Resolution		12			Bits
Integral Nonlinearity (INL)		−1.25	±0.8	+1.25	LSB
Differential Nonlinearity (DNL)	Guaranteed no missing codes to 12 bits	−0.9	±0.3	+0.9	LSB
Offset Error	T_A = 25°C	−1.5	±0.3	+1.5	mV
Offset Error Matching	T_A = 25°C	−1.5	±0.3	+1.5	mV
Offset Error Drift			2		ppm/°C
Gain Error	T_A = 25°C	−0.1	0.0	+0.1	% FS
Gain Error Matching	T_A = 25°C	−0.1	0.0	+0.1	% FS
Gain Error Drift			1		ppm/°C
ANALOG INPUT					
Input Voltage Range[1]	At ADC_{IN}	0		V_{REF}	V
DC Leakage Current		−1		+1	µA
Input Capacitance[2]	During acquisition phase		10		pF
	Outside acquisition phase		1.5		pF
Multiplexer On Resistance	V_{DD} = 5.0 V		50		Ω
	V_{DD} = 2.5 V		100		Ω
VOLTAGE REFERENCE INPUT/OUTPUT					
REF_{OUT}[3]	Internal reference output, T_A = 25°C	2.49	2.5	2.51	V
REF_{IN}[3]	External reference input	1.0		V_{DD}	V
Drift			5		ppm/°C
Power-On Time	C_{REF} = 2.2 µF		50		ms
LOGIC INPUTS					
Input Voltage					
High (V_{IH})		0.7 × V_{DRIVE}			V
Low (V_{IL})				0.3 × V_{DRIVE}	V
Input Current (I_{IN})	V_{IN} = 0 V or V_{DRIVE}	−1	0.01	+1	µA
LOGIC OUTPUTS					
Output Voltage					
High (V_{OH})	I_{SOURCE} = 200 µA	V_{DRIVE} − 0.2			V
Low (V_{OL})	I_{SINK} = 200 µA			0.4	V
Floating State Leakage Current		−1		+1	µA
Output Coding		Straight (natural) binary			

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CONVERSION RATE					
Conversion Time			550		ns
Update Rate					
Autocycle Setting 00		90	100	110	µs
Autocycle Setting 01		180	200	220	µs
Autocycle Setting 10		360	400	440	µs
Autocycle Setting 11		720	800	880	µs
Throughput Rate	f_{SCL} = 400 kHz, command mode			22.22	kSPS
POWER REQUIREMENTS					
V_{DD}		2.7		5.25	V
V_{DRIVE} Range		1.8		5.25	V
I_{DD}	V_{IN} = 0 V				
Normal Mode—Static	V_{DD} = 5.25 V		22	50	µA
	V_{DD} = 3 V		21.6	46	µA
Normal Mode—Operational	V_{DD} = 5.25 V, f_{SCL} = 400 kHz		26	55	µA
	V_{DD} = 3 V, f_{SCL} = 400 kHz		24	52	µA
	V_{DD} = 5.25 V, f_{SCL} = 100 kHz		25	54	µA
	V_{DD} = 3 V, f_{SCL} = 100 kHz		23	51	µA
	V_{DD} = 3 V, autocycle mode		70	105	µA
Power-Down Mode	V_{DD} = 5.25 V		0.550	17	µA
	V_{DD} = 5.25 V, T_A = −40°C to +85°C		0.550	8	µA
	V_{DD} = 3 V		0.435	15	µA
I_{DRIVE}	V_{IN} = 0 V				
Normal Mode—Static	V_{DRIVE} = 5.25 V		2	4	µA
	V_{DRIVE} = 3 V		1	3.5	µA
Normal Mode—Operational	V_{DRIVE} = 5.25 V, f_{SCL} = 400 kHz		6	15	µA
	V_{DRIVE} = 3 V, f_{SCL} = 400 kHz		5	14	µA
	V_{DRIVE} = 5.25 V, f_{SCL} = 100 kHz		5	14	µA
	V_{DRIVE} = 3 V, f_{SCL} = 100 kHz		4	13	µA
Total Power Dissipation[4]	V_{IN} = 0 V				
Normal Mode—Static	V_{DD} = V_{DRIVE} = 5.25 V		130	290	µW
	V_{DD} = V_{DRIVE} = 3 V		70	150	µW
Normal Mode—Operational	V_{DD} = V_{DRIVE} = 5.25 V, f_{SCL} = 400 kHz		170	370	µW
	V_{DD} = V_{DRIVE} = 3 V, f_{SCL} = 400 kHz		90	200	µW
	V_{DD} = V_{DRIVE} = 5.25 V, f_{SCL} = 100 kHz		160	360	µW
	V_{DD} = V_{DRIVE} = 3 V, f_{SCL} = 100 kHz		85	195	µW
	V_{DD} = V_{DRIVE} = 3 V, autocycle mode		210	315	µW
Power-Down Mode	V_{DD} = 5.25 V		3	95	µW
	V_{DD} = 5.25 V, T_A = −40°C to +85°C		3	33	µW
	V_{DD} = V_{DRIVE} = 3 V		1.4	50	µW

[1] The multiplexer input voltage must not exceed V_{DD}.
[2] Sample tested during initial release to ensure compliance.
[3] When referring to a single function of a multifunction pin in the parameters, only the portion of the pin name that is relevant to the specification is listed. For full pin names of multifunction pins, see the Pin Configurations and Function Descriptions section.
[4] Total power dissipation includes contributions from V_{DD}, V_{DRIVE}, and REF_{IN} (see Note 3).

I²C TIMING SPECIFICATIONS

All values measured with the input filtering enabled. C_B refers to the capacitive load on the bus line, with rise time and fall time measured between $0.3 \times V_{DRIVE}$ and $0.7 \times V_{DRIVE}$ (see Figure 2). V_{DD} = 2.7 V to 5.25 V, V_{DRIVE} = 1.8 V to 5.25 V, V_{REF} = 2.5 V internal/external, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

	Limit at T_{MIN}, T_{MAX}				
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Description**
f_{SCL}			100	kHz	Serial clock frequency, standard mode
			400	kHz	Fast mode
t_1	4			µs	SCL high time, standard mode
	0.6			µs	Fast mode
t_2	4.7			µs	SCL low time, standard mode
	1.3			µs	Fast mode
t_3	250			ns	Data setup time, standard mode
	100			ns	Fast mode
t_4[1]	0		3.45	µs	Data hold time, standard mode
	0		0.9	µs	Fast mode
t_5	4.7			µs	Setup time for a repeated start condition, standard mode
	0.6			µs	Fast mode
t_6	4			µs	Hold time for a repeated start condition, standard mode
	0.6			µs	Fast mode
t_7	4.7			µs	Bus-free time between a stop and a start condition, standard mode
	1.3			µs	Fast mode
t_8	4			µs	Setup time for a stop condition, standard mode
	0.6			µs	Fast mode
t_9			1000	ns	Rise time of the SDA signal, standard mode
	$20 + 0.1C_B$		300	ns	Fast mode
t_{10}			300	ns	Fall time of the SDA signal, standard mode
	$20 + 0.1C_B$		300	ns	Fast mode
t_{11}			1000	ns	Rise time of the SCL signal, standard mode
	$20 + 0.1C_B$		300	ns	Fast mode
t_{11A}			1000	ns	Rise time of the SCL signal after a repeated; not shown in Figure 2, standard mode
	$20 + 0.1C_B$		300	ns	Start condition and after an acknowledge bit, fast mode
t_{12}			300	ns	Fall time of the SCL signal, standard mode
	$20 + 0.1C_B$		300	ns	Fast mode
t_{SP}	0		50	ns	Pulse width of the suppressed spike; not shown in Figure 2, fast mode
$t_{RESETPW}$	10			ns	$\overline{\text{RESET}}$ pulse width (see Figure 35)
t_{RESET_DELAY}	50			ns	$\overline{\text{RESET}}$ pulse delay upon power-up (see Figure 35)

[1] A device must provide a data hold time for SDA to bridge the undefined region of the SCL falling edge.

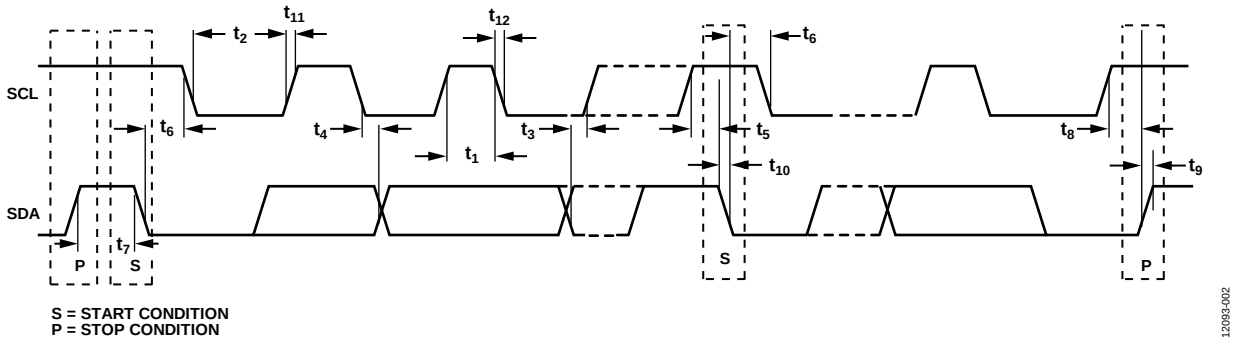


Figure 2. 2-Wire Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{DRIVE} to GND	−0.3 V to +7 V
Analog Input Voltage to GND	−0.3 V to V_{REF} + 0.3 V
Digital Input[1] Voltage to GND	−0.3 V to V_{DRIVE} + 0.3 V
Digital Output[2] Voltage to GND	−0.3 V to V_{DRIVE} + 0.3 V
Input Current to Any Pin Except Supplies[3]	±10 mA
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
ESD	
Human Body Model (HBM)	1.5 kV
Field Induced Charged Device Model (FICDM)	500 V

[1] The digital input pins include the following: AS_0, $\overline{RESET}$, AS_1, SCL, SDA, and $\overline{CONVST}/GPO_1$.
[2] The digital output pins include: ALERT/BUSY/GPO_0, GPO_2, and SDA.
[3] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
20-Lead LFCSP_WQ	52	6.5	°C/W
20-Lead TSSOP	84.3	18.4	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

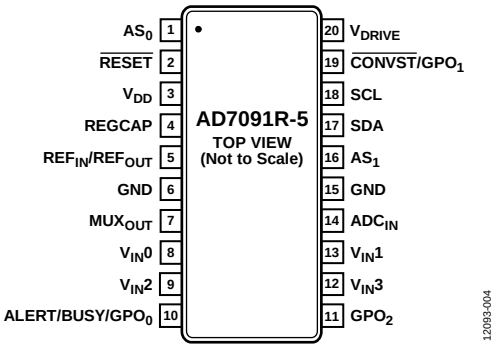


Figure 3. Pin Configuration, 20-Lead TSSOP

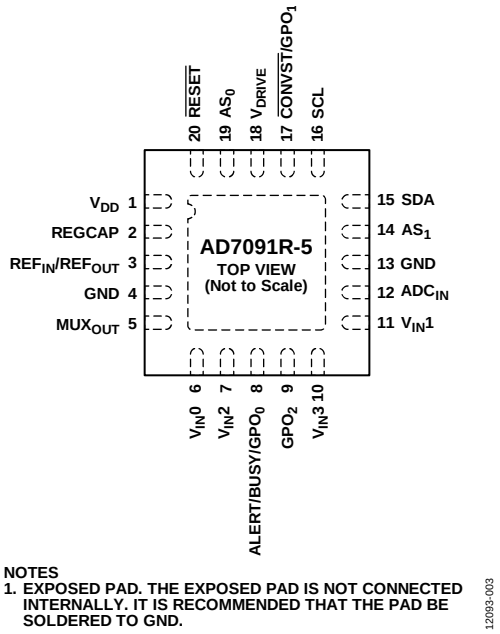


Figure 4. Pin Configuration, 20-Lead LFCSP

Table 5. Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	19	AS_0	I^2C Address Bit 0. Together with AS_1, the logic state of these two inputs selects a unique I^2C address for the AD7091R-5. The device address depends on the logic state of these pins.
2	20	$\overline{RESET}$	Reset. Logic input. This pin resets the device when pulled low.
3	1	V_{DD}	Power Supply Input. The V_{DD} range is from 2.7 V to 5.25 V. Decouple this supply pin to GND.
4	2	REGCAP	Decoupling Capacitor Pin for Voltage Output from the Internal Regulator. Decouple this output pin separately to GND using a 2.2 µF capacitor.
5	3	REF_{IN}/REF_{OUT}	Voltage Reference Output, 2.5 V. Decouple this pin to GND. The typical recommended decoupling capacitor value is 2.2 µF. The user can either access the internal 2.5 V reference or overdrive the internal reference with the voltage applied to this pin. The reference voltage range for an externally applied reference is 1.0 V to V_{DD}.
6, 15	4, 13	GND	Chip Ground Pins. These pins are the ground reference point for all circuitry on the AD7091R-5.
7	5	MUX_{OUT}	Multiplexer Output. The output of the multiplexer appears at this pin. If no external filtering or buffering is required, tie this pin directly to the ADC_{IN} pin; otherwise, tie the output of the conditioning network to the ADC_{IN} pin.
8	6	$V_{IN}0$	Analog Input for Channel 0. Single-ended analog input. The analog input range is 0 V to V_{REF}.
9	7	$V_{IN}2$	Analog Input for Channel 2. Single-ended analog input. The analog input range is 0 V to V_{REF}.
10	8	ALERT/BUSY/GPO_0	This is a multifunction pin determined by the configuration register. Alert Output Pin (ALERT). When functioning as ALERT, this pin is a logic output indicating that a conversion result has fallen outside the limit of the register settings. Busy Output (BUSY). The BUSY pin indicates when a conversion is taking place. General-Purpose Digital Output 0 (GPO_0).
11	9	GPO_2	General-Purpose Digital Output 2.
12	10	$V_{IN}3$	Analog Input for Channel 3. Single-ended analog input. The analog input range is 0 V to V_{REF}.
13	11	$V_{IN}1$	Analog Input for Channel 1. Single-ended analog input. The analog input range is 0 V to V_{REF}.
14	12	ADC_{IN}	ADC Input. This pin allows direct access to the ADC. If no external filtering or buffering is required, tie this pin directly to the MUX_{OUT} pin; otherwise, tie the input of the conditioning network to the MUX_{OUT} pin.

Pin No.		Mnemonic	Description
TSSOP	LFCSP		
16	14	AS_1	I^2C Address Bit 1. Together with AS_0, the logic state of these two inputs selects a unique I^2C address for the AD7091R-5. The device address depends on the logic state of these pins.
17	15	SDA	Serial Data Input/Output. This open-drain output requires a pull-up resistor. The output coding is straight binary for the voltage channels.
18	16	SCL	Digital Input Serial I^2C Bus Clock. This input requires a pull-up resistor. The data transfer rate in I^2C mode is compatible with both 100 kHz (standard mode) and 400 kHz (fast mode) operating modes.
19	17	$\overline{CONVST}/GPO_1$	This is a multifunction pin determined by the configuration register and mode of conversion. Convert Start Input Signal ($\overline{CONVST}$). Edge triggered logic input. The falling edge of $\overline{CONVST}$ places the ADC into hold mode and initiates a conversion. The logic level of $\overline{CONVST}$ at EOC controls the power modes of the AD7091R-5. General-Purpose Digital Output 1 (GPO_1). When in command or autocycle mode, this pin can function as a general-purpose digital output.
20	18	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the interface operates. Connect decoupling capacitors between V_{DRIVE} and GND. The typical recommended values are 10 µF and 0.1 µF. The voltage range on this pin is 1.8 V to 5.25 V and may differ from the voltage range at V_{DD}, but must never exceed it by more than 0.3 V.
N/A[1]	21	EPAD	Exposed Pad. The exposed pad is not connected internally. It is recommended that the pad be soldered to GND.

[1] N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

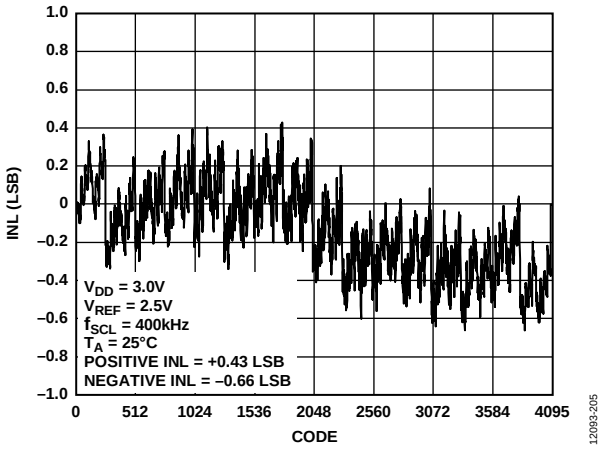


Figure 5. Integral Nonlinearity vs. Code

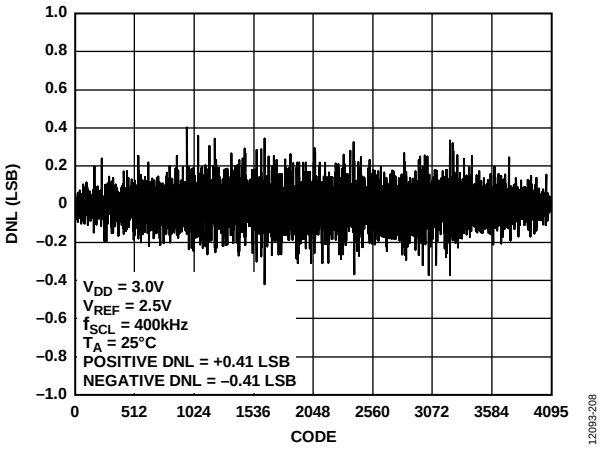


Figure 8. Differential Nonlinearity vs. Code

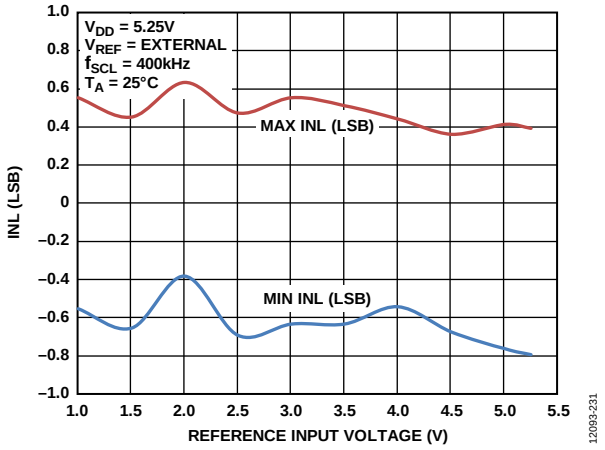


Figure 6. Minimum/Maximum INL vs. External Reference Input Voltage

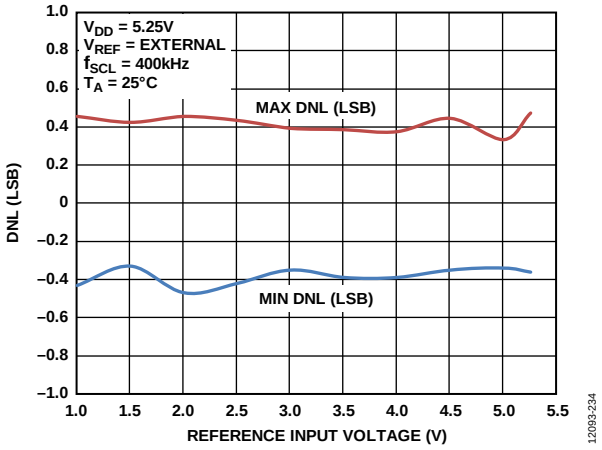


Figure 9. Minimum/Maximum DNL vs. External Reference Input Voltage

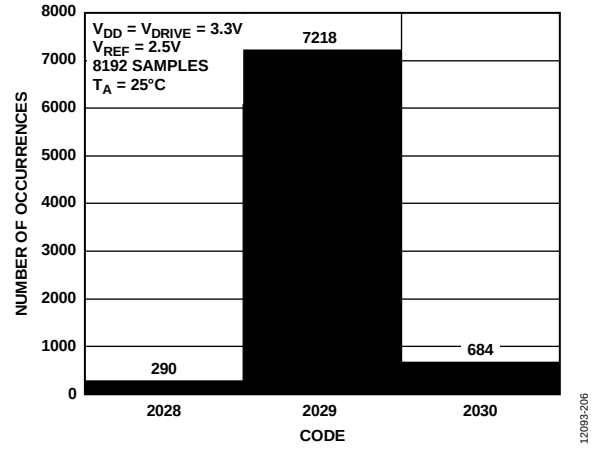


Figure 7. Histogram of a DC Input at Code Center

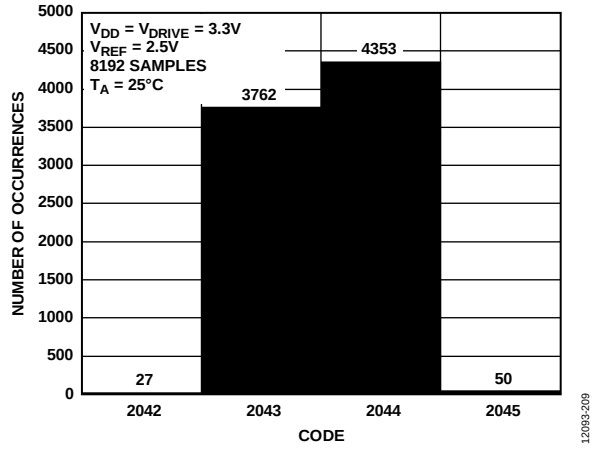


Figure 10. Histogram of a DC Input at Code Transition

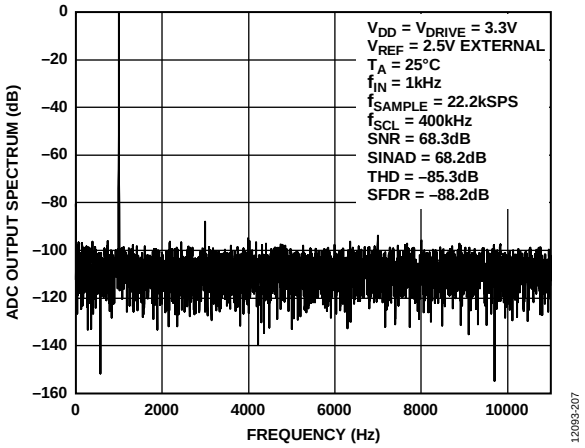


Figure 11. 10 kHz FFT, V_{DD} = 3.0 V, V_{REF} = 2.5 V External

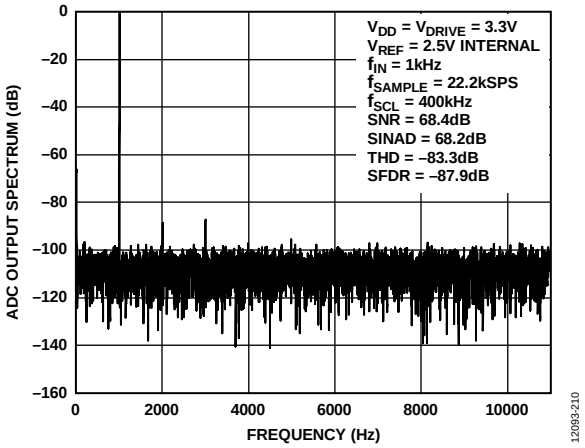


Figure 12. 10 kHz FFT, V_{DD} = 3.0 V, V_{REF} = 2.5 V Internal

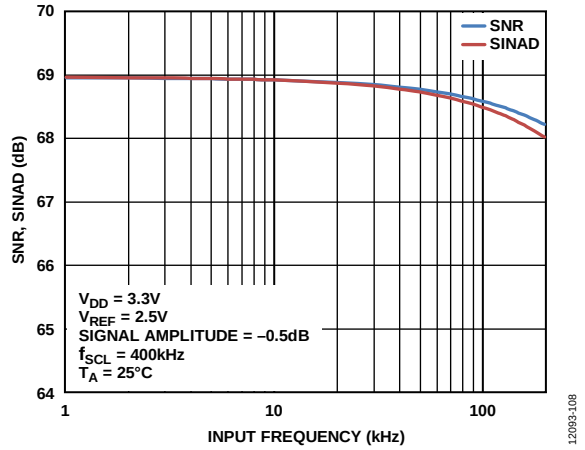


Figure 13. SNR, SINAD vs. Input Frequency

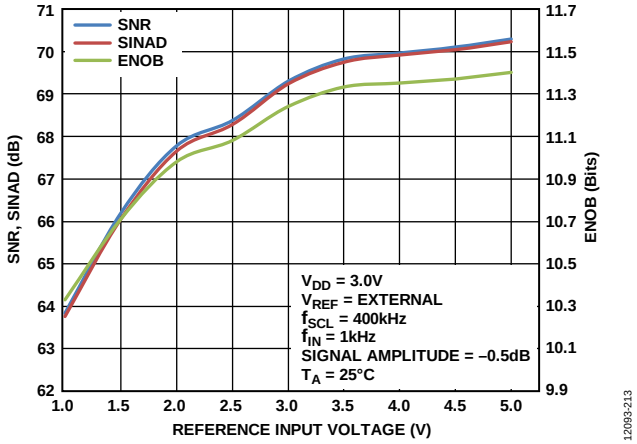


Figure 14. SNR, SINAD, and ENOB vs. Reference Input Voltage

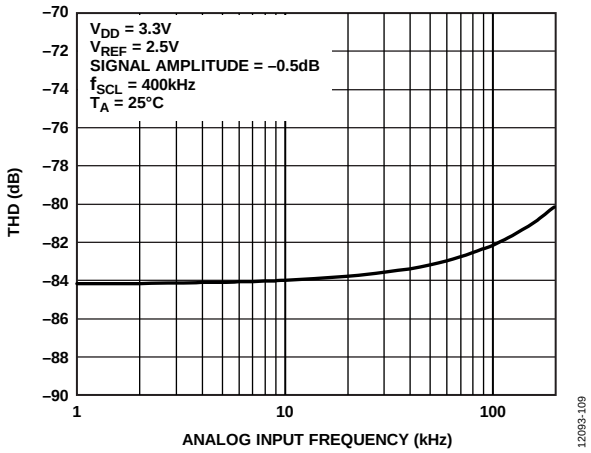


Figure 15. THD vs. Analog Input Frequency

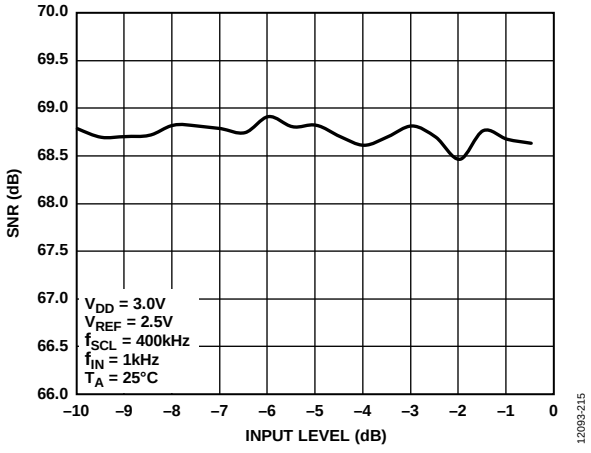


Figure 16. SNR vs. Input Level

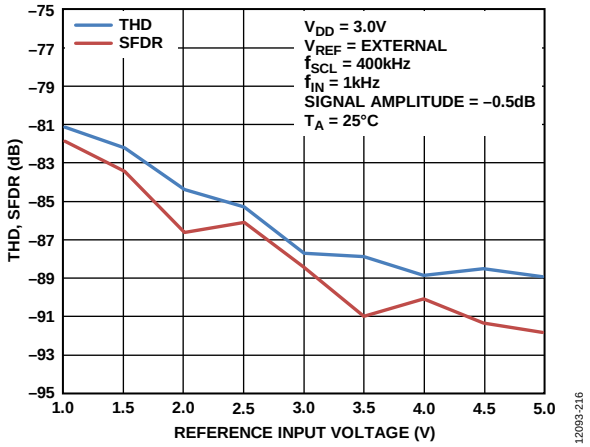


Figure 17. THD, SFDR vs. Reference Input Voltage

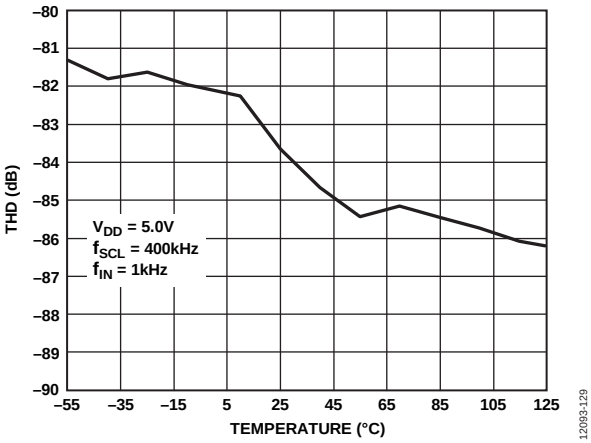


Figure 18. THD vs. Temperature

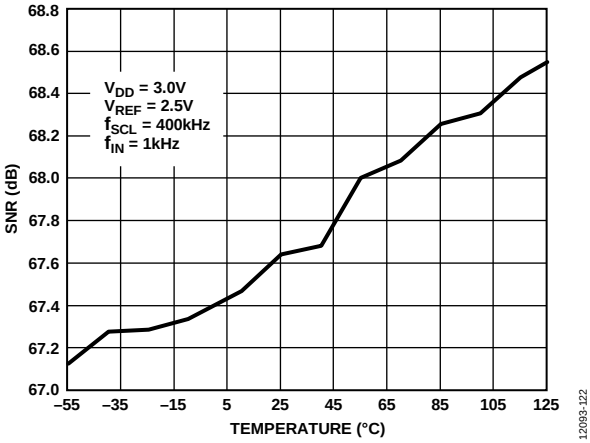


Figure 19. SNR vs. Temperature

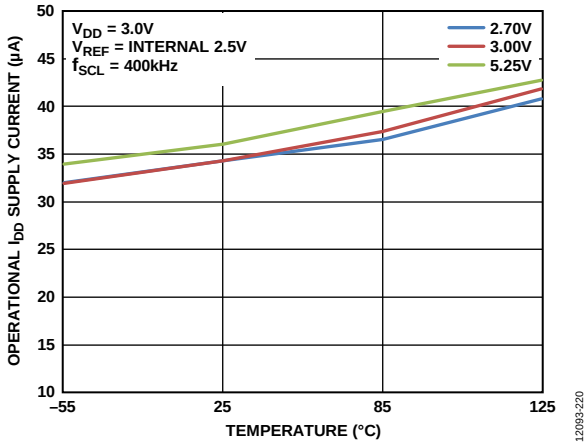


Figure 20. Operational I_{DD} Supply Current vs. Temperature for Various V_{DD} Supply Voltages

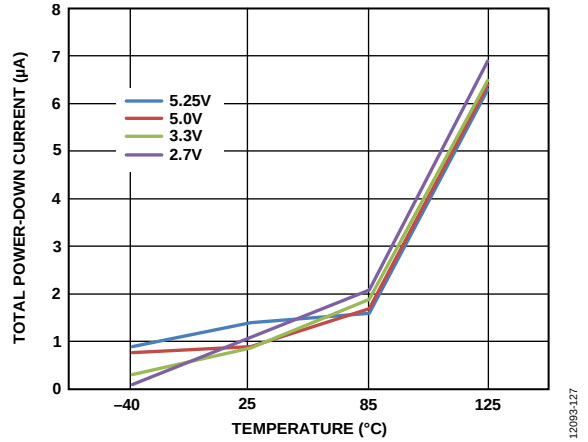


Figure 21. Total Power-Down Current vs. Temperature for Various Supply Voltages

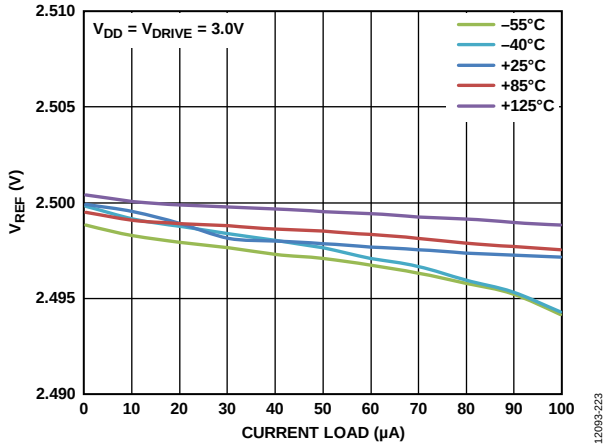


Figure 22. Reference Voltage Output (V_{REF}) vs. Current Load for Various Temperatures

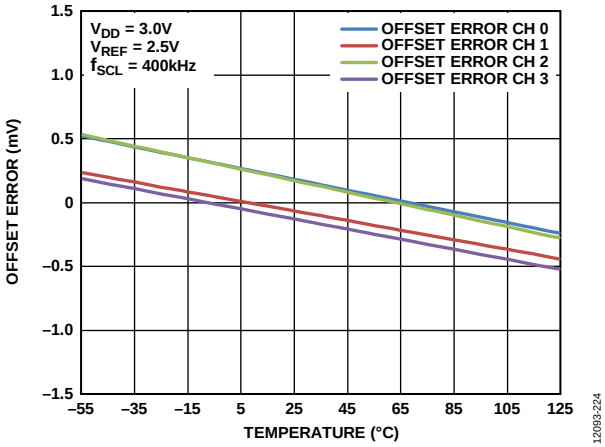


Figure 23. Offset Error vs. Temperature

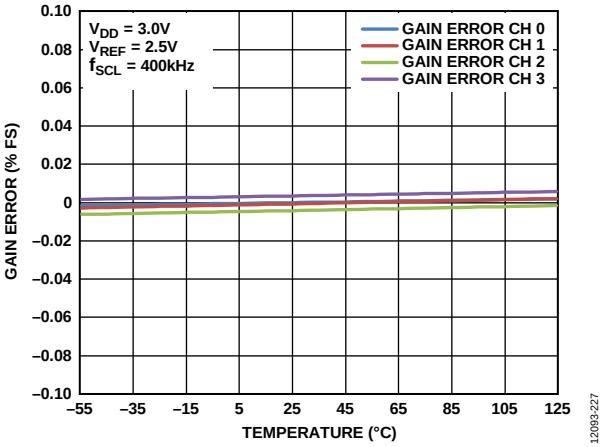


Figure 26. Gain Error vs. Temperature

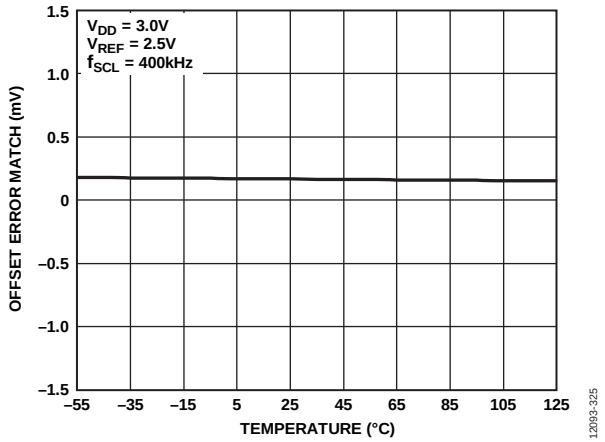


Figure 24. Offset Error Match vs. Temperature

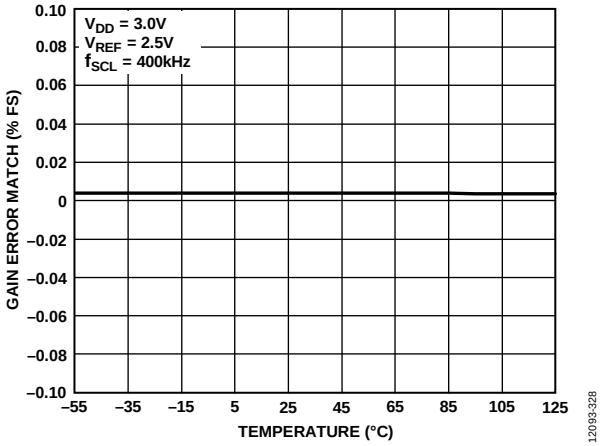


Figure 27. Gain Error Match vs. Temperature

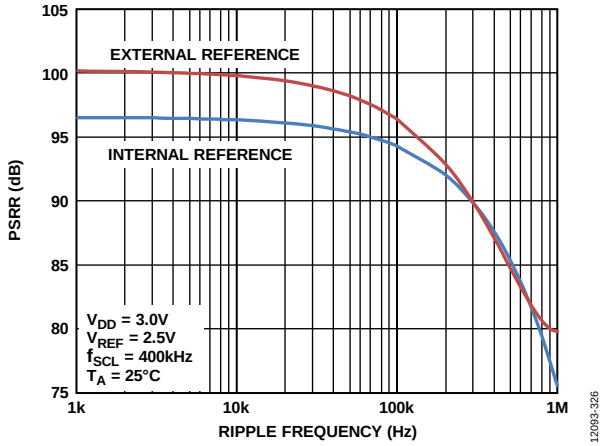


Figure 25. PSRR vs. Ripple Frequency

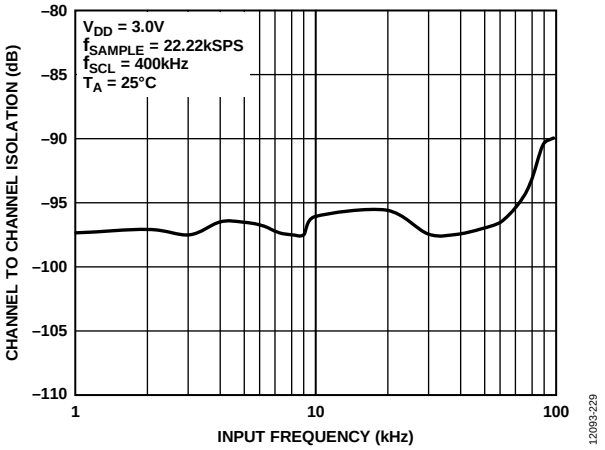


Figure 28. Channel to Channel Isolation vs. Input Frequency

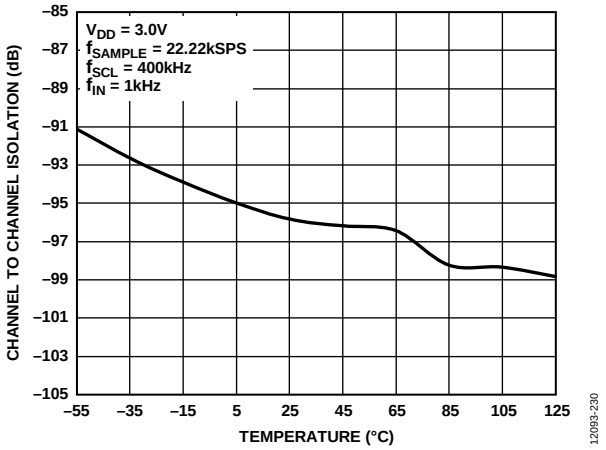


Figure 29. Channel to Channel Isolation vs. Temperature

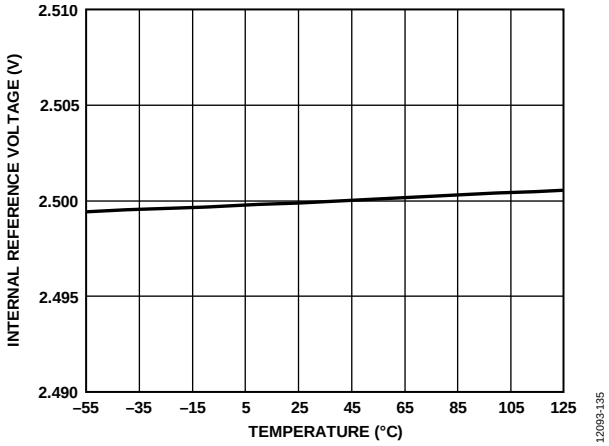


Figure 31. Internal Reference Voltage vs. Temperature

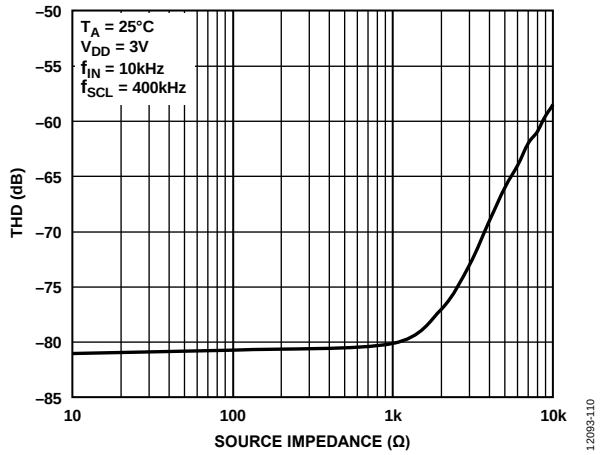


Figure 30. THD vs. Source Impedance

TERMINOLOGY

Integral Nonlinearity (INL)
INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. For the AD7091R-5, the endpoints of the transfer function are zero scale, a point ½ LSB below the first code transition, and full scale, a point ½ LSB above the last code transition.

Differential Nonlinearity (DNL)
DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
The offset error is the deviation of the first code transition (00 … 000 to 00 … 001) from the ideal (such as GND + 0.5 LSB).

Offset Error Match
Offset error match is the difference in offset error between any two input channels.

Gain Error
For the AD7091R-5, the gain error is the deviation of the last code transition (111 … 110 to 111 … 111) from the ideal (such as V_{REF} − 1.5 LSB) after the offset error has been adjusted out.

Gain Error Match
Gain error match is the difference in gain error between any two input channels.

Transient Response Time
The track-and-hold amplifier returns to track mode after the end of conversion. The track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±0.5 LSB, after the end of conversion. See the I²C Interface section for more details.

Signal-to-Noise-and-Distortion Ratio (SINAD)
SINAD is the measured ratio of the signal-to-noise-and-distortion at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc.

The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical SINAD for an ideal N-bit converter with a sine wave input is given by

$$Signal\text{-}to\text{-}(Noise + Distortion) = (6.02N + 1.76)\ (\text{dB})$$

Thus, for a 12-bit converter, the SINAD ratio is 74 dB.

Channel to Channel Isolation
Channel to channel isolation is a measure of the level of crosstalk between the selected channel and all the other channels. It is measured by applying a full-scale, 10 kHz sine wave signal to all unselected input channels and determining the degree to which the signal attenuates in the selected channel that has a dc signal applied to it. Figure 28 shows the worst case across all channels for the AD7091R-5.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of harmonics to the fundamental. For the AD7091R-5, it is defined as

$$THD(\text{dB}) = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where:
V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum; however, for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

THEORY OF OPERATION

CIRCUIT INFORMATION

The AD7091R-5 is a 12-bit, ultralow power single-supply ADC. The device operates from a 2.7 V to 5.25 V supply. The AD7091R-5 can function in both standard and fast I²C operating modes.

The AD7091R-5 provides a 4:1 multiplexer and an on-chip, track-and-hold amplifier, and is housed in either a 20-lead LFCSP or 20-lead TSSOP package. These packages offer considerable space-saving advantages over alternative solutions. The serial clock input accesses data from the device. An internally generated clock is implemented to control the successive approximation ADC. The reference voltage for the AD7091R-5 is provided externally or is generated internally by an accurate on-chip reference source. The analog input range for the AD7091R-5 is 0 V to V_{REF}.

The AD7091R-5 also features a power-down option to save power between conversions. The power-down feature is accessed through the standard serial interface as described in the Modes of Operation section.

CONVERTER OPERATION

The AD7091R-5 is a successive approximation ADC based on a charge redistribution digital-to-analog converter (DAC). Figure 32 and Figure 33 show simplified schematics of the ADC. Figure 32 shows the ADC during its acquisition phase. When Switch 2 (SW2) is closed and Switch 1 (SW1) is in Position A, the comparator is held in a balanced condition, and the sampling capacitor acquires the signal on ADC_{IN}.

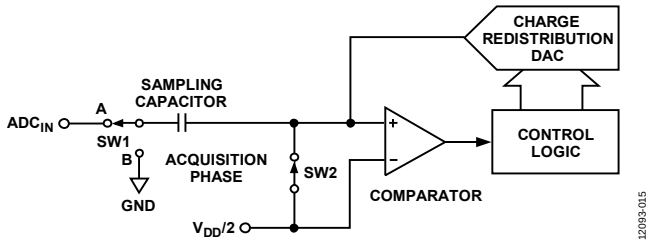


Figure 32. ADC Acquisition Phase

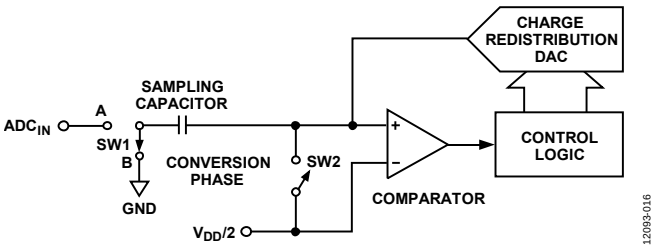


Figure 33. ADC Conversion Phase

When the ADC starts a conversion, SW2 opens and SW1 moves to Position B, causing the comparator to become unbalanced (see Figure 33). Using the control logic, the charge redistribution DAC adds and subtracts fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the SAR decisions are made, the comparator inputs are rebalanced. From these SAR decisions, the control logic generates the ADC output code.

ADC TRANSFER FUNCTION

The output coding of the AD7091R-5 is straight binary. The designed code transitions occur midway between successive integer LSB values, such as ½ LSB and 1½ LSB. The LSB size for the AD7091R-5 is $V_{REF}/4096$. The ideal transfer characteristic for the AD7091R-5 is shown in Figure 34.

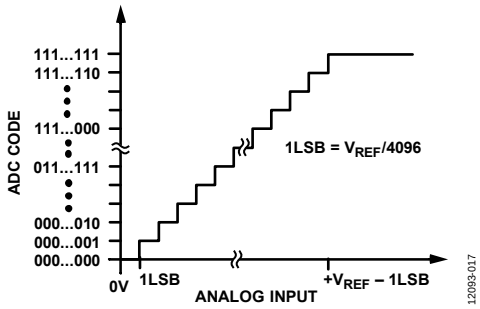


Figure 34. Transfer Characteristic

REFERENCE

The AD7091R-5 can operate with either the internal 2.5 V on-chip reference or an externally applied reference. The logic state of the P_DOWN LSB bit in the configuration register determines whether the internal reference is used. The internal reference is selected for the ADCs when the P_DOWN LSB bit is set to 1.

When the P_DOWN LSB bit is set to 0, supply an external reference in the range of 2.5 V to V_{DD} through the REF_{IN}/REF_{OUT} pin. At power-up, the internal reference disables by default.

The internal reference circuitry consists of a 2.5 V band gap reference and a reference buffer. When operating the AD7091R-5 in internal reference mode, the 2.5 V internal reference is available at the REF_{IN}/REF_{OUT} pin, which is typically decoupled to GND using a 2.2 µF capacitor. It is recommended to buffer the internal reference before applying it elsewhere in the system.

The reference buffer requires 50 ms to power up and charge the 2.2 µF decoupling capacitor.

POWER SUPPLY

The AD7091R-5 uses two power supply pins: a core supply (V_{DD}) and a digital input/output interface supply (V_{DRIVE}). V_{DRIVE} allows direct interfacing with any logic between 1.8 V and 5.25 V. To reduce the number of supplies needed, V_{DRIVE} and V_{DD} can be tied together depending upon the logic levels of the system. The AD7091R-5 is independent of power supply sequencing between V_{DRIVE} and V_{DD}. Additionally, the AD7091R-5 is insensitive to power supply variations over a wide frequency range, as shown in Figure 25.

The AD7091R-5 powers down automatically at the end of each conversion phase; therefore, the power scales linearly with the sampling rate. The automatic power-down feature makes the AD7091R-5 device ideal for low sampling rates (of even a few hertz) and battery-powered applications.

Table 6. Recommended Power Management Devices[1]

Product	Description
ADP7102	20 V, 300 mA, low noise, CMOS LDO
ADM7160	Ultralow noise, 200 mA linear regulator
ADP162	Ultralow quiescent current, CMOS linear regulator

[1] For the latest recommended power management devices, see the AD7091R-5 product page.

DEVICE RESET

Upon power-up, a reset pulse of at least 10 ns in width must be provided on the $\overline{\text{RESET}}$ pin to ensure proper initialization of the device. Failure to apply the reset pulse may result in a device malfunction. See Figure 35 for reset pulse timing relative to power supply establishment.

At any time, the $\overline{\text{RESET}}$ pin can reset the device and the contents of all internal registers, including the command register, to their default state. To activate the reset operation, bring the $\overline{\text{RESET}}$ pin low for a minimum of 10 ns while it is asynchronous to the SCL signal. It is imperative that the $\overline{\text{RESET}}$ pin be held at a stable logic level at all times to ensure normal operation.

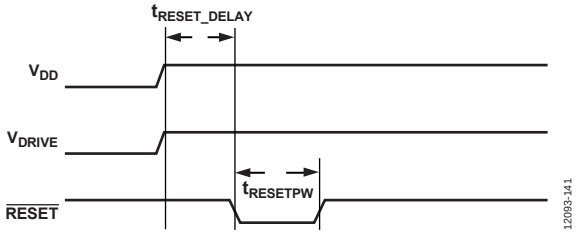


Figure 35. $\overline{\text{RESET}}$ Pin Power Up Timing

ANALOG INPUT

Figure 36 shows an equivalent circuit of the analog input structure of the AD7091R-5. The two diodes, D1 and D2, provide ESD protection for the analog input. Ensure that the analog input signal never exceeds the supply rails by more than 300 mV because this causes these diodes to become forward-biased and start conducting current into the substrate. These diodes can conduct a maximum of 10 mA without causing irreversible damage to the device.

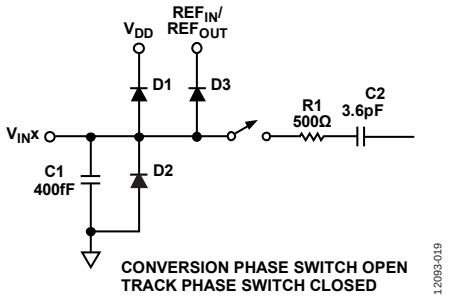


Figure 36. Equivalent Analog Input Circuit

The C1 capacitor in Figure 36 is typically approximately 400 fF and can primarily be attributed to pin capacitance. The R1 resistor is a lumped component made up of the on resistance of a switch. This resistor is typically approximately 500 Ω. The C2 capacitor is the ADC sampling capacitor and typically has a capacitance of 3.6 pF.

In applications where harmonic distortion and SNR are critical, drive the analog inputs from low impedance sources. Large source impedances significantly affect the ac performance of the ADC, which can necessitate using input buffer amplifiers, as shown in Figure 37. The choice of the op amp is a function of the particular application.

When no amplifiers are driving the analog input, limit the source impedance to low values. The maximum source impedance depends on the amount of THD that can be tolerated. The THD increases as the source impedance increases and performance degrades.

Use an external filter on the analog input signal paths to the AD7091R-5 $V_{IN}x$ pins to achieve the specified performance. This filter can be a one-pole, low-pass RC filter or similar.

Connect the MUX_{OUT} pin directly to the ADC_{IN} pin. Insert a buffer amplifier in the path, if desired. When sequencing channels, do not place a filter between MUX_{OUT} and the input to any buffer because doing so leads to crosstalk. If a buffer is not implemented, do not place a filter between MUX_{OUT} and ADC_{IN} when sequencing channels because doing so leads to crosstalk.

DRIVER AMPLIFIER CHOICE

Although the AD7091R-5 is easy to drive, a driver amplifier must meet the following requirements:

- Keep the noise generated by the driver amplifier as low as possible to preserve the SNR and transition noise performance of the AD7091R-5. The noise from the driver is filtered by the one-pole, low-pass filter of the AD7091R-5 analog input circuit, made by R1 and C2, or by the external filter, if one is used. Because the typical noise of the AD7091R-5 is 350 μV rms, the SNR degradation due to the amplifier is

$$SNR_{LOSS} = 20 \log\left(\frac{350}{\sqrt{350^2 + \frac{\pi}{2} f_{-3dB} (Ne_N)^2}}\right)$$

  where:
  f_{-3dB} is the input bandwidth, in megahertz, of the AD7091R-5 (1.5 MHz), or the cutoff frequency of the input filter, if one is used.
  N is the noise gain of the amplifier (for example, gain = 1 in a buffered configuration; see Figure 37).
  e_N is the equivalent input noise voltage of the op amp, in nV/√Hz.
- For ac applications, the driver must have a THD performance that is commensurate with the AD7091R-5.
- If a buffer is placed between MUX_{OUT} and ADC_{IN}, the driver amplifier and the AD7091R-5 analog input circuit must settle for a full-scale step onto the capacitor array at a 12-bit level (0.0244%, 244 ppm). In an amplifier data sheet, settling at 0.1% to 0.01% is more commonly specified and may differ significantly from the settling time at a 12-bit level. Be sure to verify the amplifier settling time before driver selection.

Table 7. Recommended Driver Amplifiers

Product	Description[1]
ADA4805-1	Low noise, low power, wide bandwidth amplifier
AD8031	Low voltage, low power, single channel amplifier
AD8032	Low voltage, low power, dual channel amplifier
AD8615	Low frequency, low voltage amplifier

[1] For the latest recommended ADC driver products, see the AD7091R-5 product page.

TYPICAL CONNECTION DIAGRAM

Figure 37 and Figure 38 show typical connection diagrams for the AD7091R-5.

Connect a positive power supply in the 2.7 V to 5.25 V range to the V_{DD} pin. The typical values for the V_{DD} decoupling capacitors are 100 nF and 10 μF. Place these capacitors as close as possible to the device pins. Take care to decouple the REF_{IN}/REF_{OUT} pin to achieve specified performance. The typical value for the REF_{IN}/REF_{OUT} capacitor is 2.2 μF, which provides an analog input range of 0 V to V_{REF}. The typical value for the regulator bypass (REGCAP) decoupling capacitor is 1 μF. The voltage applied to the V_{DRIVE} input controls the voltage of the serial interface; therefore, connect this pin to the supply voltage of the microprocessor. Set V_{DRIVE} in the 1.8 V to 5.25 V range. The typical values for the V_{DRIVE} decoupling capacitors are 100 nF and 10 μF. The 16-bit conversion result (3 address bits, 1 alert bit, and 12 data bits) is output in 2 bytes with the most significant byte (MSBs) presented first.

When an externally applied reference is required, disable the internal reference using the configuration register. Choose an externally applied reference voltage in the range of 1.0 V to V_{DD} and connect it to the REF_{IN}/REF_{OUT} pin.

For applications where power consumption is a concern, use the power-down mode of the ADC to improve power performance. See the Modes of Operation section for additional details.

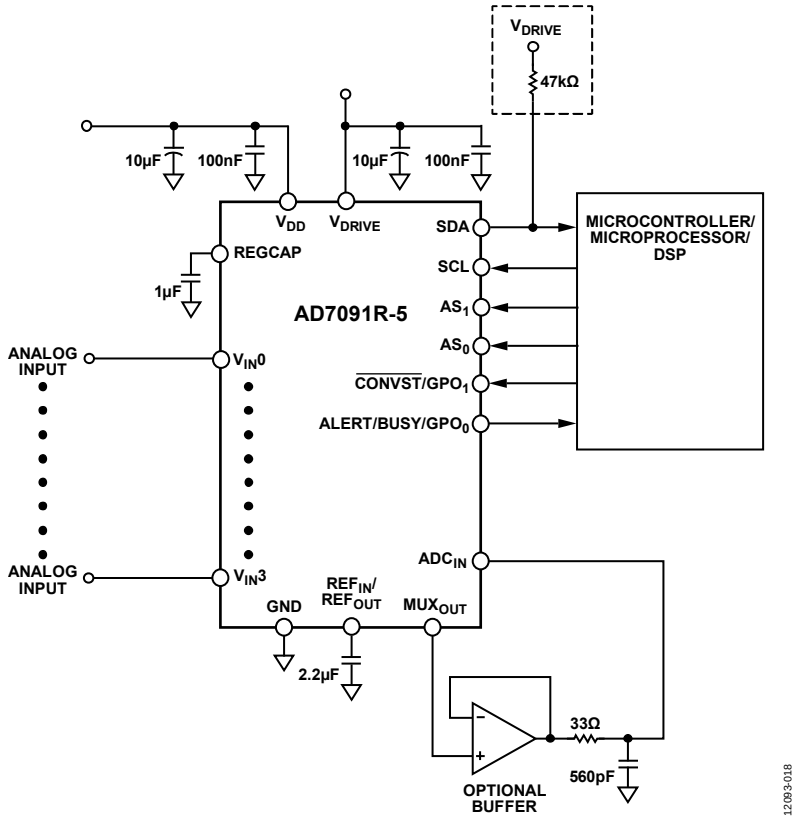


Figure 37. Typical Connection Diagram with Optional Buffer

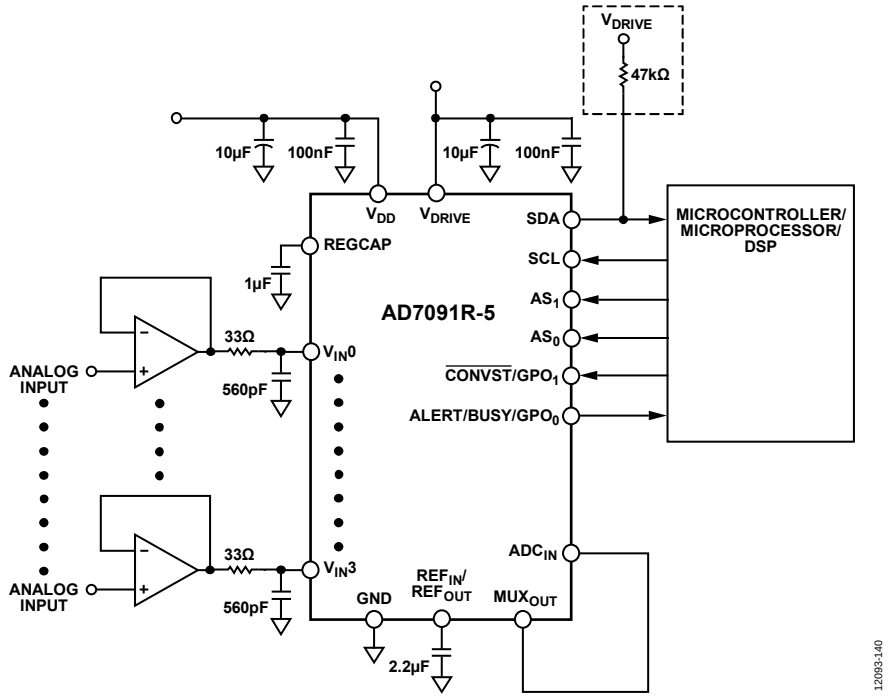


Figure 38. Typical Connection Diagram Without Optional Buffer

I²C REGISTERS

The AD7091R-5 has several user-programmable registers. Table 9 contains the complete list of registers.

The registers are either read/write (R/W) or read only (R). Data can be written to or read back from the read/write registers. Read only registers can only be read. Any write to a read only register or unimplemented register address is considered no operation (NOP) command, which is an I²C command that the AD7091R-5 ignores. After a write to a read only register, the output on the subsequent I²C frame is all zeros provided that there was no conversion before the next I²C frame. Similarly, any read of an unimplemented register outputs zeros.

ADDRESSING REGISTERS

A serial transfer on the AD7091R-5 consists of nine SCL cycles. Data is sent over the serial bus in groups of nine bits—eight bits of data from the transmitter followed by an acknowledge bit from the receiver. Data transitions on the SDA line must occur during the low period of the clock signal and remain stable during the high period. The receiver pulls the SDA line low during the acknowledge bit to signal that the preceding byte has been received correctly. If this is not the case, cancel the transaction. The first byte that the master sends must consist of a 7-bit slave address, followed by a data direction bit. Each device on the bus has a unique slave address; therefore, the first byte sets up communication with a single slave device for the duration of the transaction.

The transaction can be used either to write to a slave device (data direction bit = 0) or to read data from it (data direction bit = 1). In the case of a read transaction, it is often necessary to first write to the slave device (in a separate write transaction) to tell it from which register to read. Reading and writing cannot be combined in one transaction.

I²C REGISTER ACCESS

When the transaction is complete, the master can maintain control of the bus, initiating a new transaction by generating another start bit (high to low transition on SDA while SCL is high). This is known as a repeated start. Alternatively, the bus can be relinquished by releasing the SCL line followed by the SDA line. This low to high transition on SDA while SCL is high is known as a stop bit (P), and it leaves the I²C bus in its idle state (no current is consumed by the bus).

SLAVE ADDRESS

The first byte that the user writes to the device is the slave address byte. The AD7091R-5 has a 7-bit slave address. On the AD7091R-5, the three MSBs of the 7-bit slave address are fixed to 3'b010. The four LSBs are set by the user via external pins. Two address select pins are on each device, and high, low, or no connect can be detected on each pin, giving nine combinations.

Table 8 shows the four LSBs of the slave address for the AD7091R-5 for different configurations of the address select pins.

Table 8. Slave Addresses

AS_1[1]	AS_0[1]	A3	A2	A1	A0
V_{DD}	V_{DD}	0	0	0	0
V_{DD}	NC	0	0	1	0
V_{DD}	GND	0	0	1	1
NC	V_{DD}	1	0	0	0
NC	NC	1	0	1	0
NC	GND	1	0	1	1
GND	V_{DD}	1	1	0	0
GND	NC	1	1	1	0
GND	GND	1	1	1	1

[1] NC means leave the AS_x pins floating, V_{DD} means pulled high, and GND means pulled low.

Table 9. Register Descriptions

Address	Register Name	Default	Access
0x00	Conversion result	0x0000	R
0x01	Channel	0x0000	R/W
0x02	Configuration	0x00C0	R/W
0x03	Alert indication	0x0000	R
0x04	Channel 0 low limit	0x0000	R/W
0x05	Channel 0 high limit	0x01FF	R/W
0x06	Channel 0 hysteresis	0x01FF	R/W
0x07	Channel 1 low limit	0x0000	R/W
0x08	Channel 1 high limit	0x01FF	R/W
0x09	Channel 1 hysteresis	0x01FF	R/W
0x0A	Channel 2 low limit	0x0000	R/W
0x0B	Channel 2 high limit	0x01FF	R/W
0x0C	Channel 2 hysteresis	0x01FF	R/W
0x0D	Channel 3 low limit	0x0000	R/W
0x0E	Channel 3 high limit	0x01FF	R/W
0x0F	Channel 3 hysteresis	0x01FF	R/W

CONVERSION RESULT REGISTER

The conversion result register is a 16-bit, read only register that stores the results from the most recent ADC conversion in straight binary format. The channel ID of the converted channel and the alert status are also included in this register.

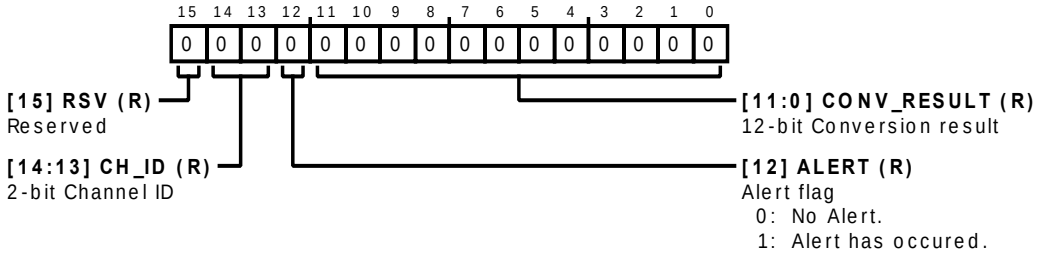


Table 10. Conversion Result Bit Map

MSB															LSB
B15	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
RSV	CH_ID		ALERT	CONV_RESULT											

Table 11. Bit Descriptions for the Conversion Result Register

Bit(s)	Name	Description			Reset	Access
15	RSV	Reserved			0x0	R
[14:13]	CH_ID	2-bit channel ID of the channel converted			0x0	R
		B14	**B13**	**Analog Input Channel**		
		0	0	Channel 0		
		0	1	Channel 1		
		1	0	Channel 2		
		1	1	Channel 3		
12	ALERT	Alert flag 0: no alert occurred 1: alert has occurred			0x0	R
[11:0]	CONV_RESULT	12-bit conversion result			0x000	R

CHANNEL REGISTER

The channel register on the AD7091R-5 is an 8-bit, read/write register. Each of the four analog input channels has one corresponding bit in the channel register. To select a channel for inclusion in the channel conversion sequence, set the corresponding channel bit to 1 in the channel register. There is a latency of one conversion before the channel conversion sequence is updated. If the channel register is programmed with a new value, the conversion sequence is reset to the lowest numbered channel in the new value.

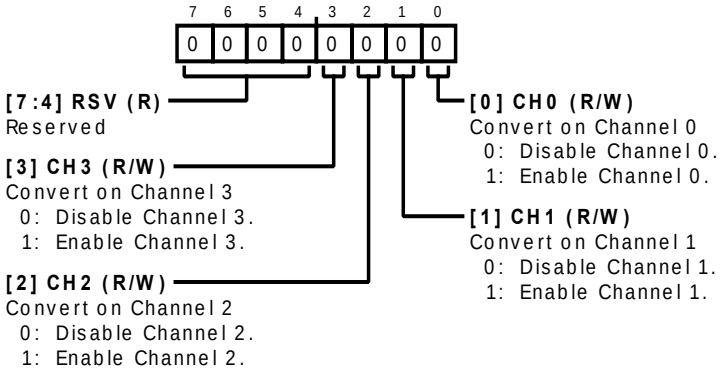


Table 12. Channel Bit Map

MSB							LSB
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
RSV				CH3	CH2	CH1	CH0

Table 13. Bit Descriptions for the Channel Register

Bit(s)	Name	Description	Reset	Access
[7:4]	RSV	Reserved	0x00	R
3	CH3	Convert on Channel 3 0: disable Channel 3 1: enable Channel 3	0x0	R/W
2	CH2	Convert on Channel 2 0: disable Channel 2 1: enable Channel 2	0x0	R/W
1	CH1	Convert on Channel 1 0: disable Channel 1 1: enable Channel 1	0x0	R/W
0	CH0	Convert on Channel 0 0: disable Channel 0 1: enable Channel 0	0x0	R/W

CONFIGURATION REGISTER

The configuration register is a 16-bit, read/write register that sets the operating modes of the AD7091R-5.

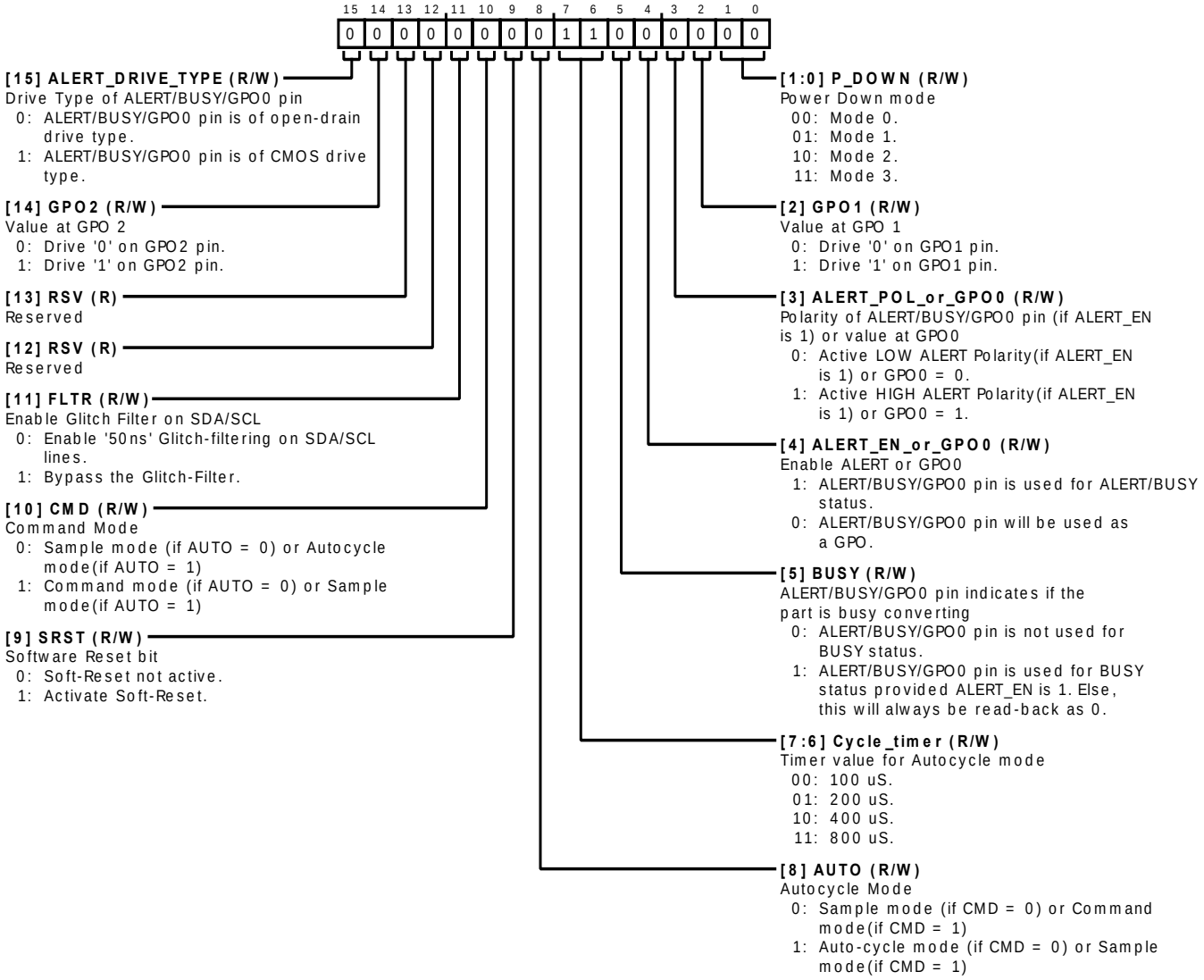


Table 14. Configuration Bit Map

MSB **LSB**

B15	B14	B13	B12	B11	B10	B9	B8	B7 B6	B5	B4	B3	B2	B1 B0
ALERT_ DRIVE_ TYPE	GPO2	RSV	RSV	FLTR	CMD	SRST	AUTO	CYCLE_ TIMER	BUSY	ALERT_ EN_OR_ GPO0	ALERT_ POL_OR_ GPO0	GPO1	P_DOWN

Table 15. Bit Descriptions for the Configuration Register[1]

Bit(s)	Name	Description	Reset	Access
15	ALERT_DRIVE_TYPE	Drive the type of the ALERT/BUSY/GPO_0 pin. 0: the ALERT/BUSY/GPO_0 pin is open-drain drive type. 1: the ALERT/BUSY/GPO_0 pin is CMOS drive type.	0x0	RW
14	GPO2	Value at GPO_2. 0: drive 0 on GPO_2 pin. 1: drive 1 on GPO_2 pin.	0x0	RW
13	RSV	Reserved.	0x00	R
12	RSV	Reserved.	0x00	R

Bit(s)	Name	Description	Reset	Access
11	FLTR	Enable the glitch filter on SDA/SCL. 0: enable 50 ns glitch filtering on the SDA/SCL lines. 1: bypass the glitch filter.	0x0	RW
10	CMD	Command mode. 0: sample mode (if AUTO = 0) or autocycle mode (if AUTO = 1). 1: command mode (if AUTO = 0) or sample mode (if AUTO = 1).	0x0	RW
9	SRST	Software reset bit. Setting this bit resets the internal digital control logic, the conversion result and alert indication registers, but not the other memory-mapped registers. This bit is automatically cleared in the next clock cycle. 0: soft reset not active. 1: activate soft reset.	0x0	RWAC
8	AUTO	Autocycle mode. 0: sample mode (if CMD = 0) or command mode (if CMD = 1). 1: autocycle mode (if CMD = 0) or sample mode (if CMD = 1).	0x0	RW
[7:6]	CYCLE_TIMER	Timer value for autocycle mode. 00: 100 µs. 01: 200 µs. 10: 400 µs. 11: 800 µs.	0x3	RW
5	BUSY	ALERT/BUSY/GPO_0 pin indicates if the device is busy converting. 0: the ALERT/BUSY/GPO_0 pin is not used for the busy status. 1: the ALERT/BUSY/GPO_0 pin is used for the busy status provided ALERT_EN_OR_GPO0 is 1. Otherwise, this bit is always read back as 0.	0x0	RW
4	ALERT_EN_OR_GPO0	Enable the ALERT/BUSY/GPO_0 pin or GPO0. 1: the ALERT/BUSY/GPO_0 pin is used for the ALERT/BUSY status. 0: the ALERT/BUSY/GPO_0 pin is used as a GPO.	0x0	RW
3	ALERT_POL_OR_GPO0	Polarity of the ALERT/BUSY/GPO_0 pin (if ALERT_EN_OR_GPO0 is 1) or value at GPO0. 0: active low ALERT/BUSY/GPO_0 polarity (if ALERT_EN_OR_GPO0 is 1) or GPO0 = 0. 1: active high ALERT/BUSY/GPO_0 polarity (if ALERT_EN_OR_GPO0 is 1) or GPO0 = 1.	0x0	RW
2	GPO1	Value at GPO_1. 0: drive 0 on the $\overline{CONVST}$/GPO_1 pin. 1: drive 1 on the $\overline{CONVST}$/GPO_1 pin.	0x0	RW
[1:0]	P_DOWN	Power-down modes.	0x0	R/W

Setting	Mode	Sleep Mode/Bias Generator	Internal Reference
00	Mode 0	Off	Off
01	Mode 1	Off	On
10	Mode 2	On	Off
11	Mode 3	On	On

[1] The AD7091R-5 supports the I²C standard glitch filter, but does not support clock stretching or general call addressing.

ALERT INDICATION REGISTER

The 8-bit alert indication register is a read only register that provides information on an alert event. If a conversion result activates the ALERT/BUSY/GPO_0 pin, as described in the Channel x Low Limit Register section and the Channel x High Limit Register section, read the alert register to determine the source of the alert. The register contains two status bits per channel, one corresponding to the high limit, and the other to the low limit. The bit with a status equal to 1 shows where the violation occurred, that is, on which channel, and whether the violation occurred on the upper or lower limit. If a second alert event occurs on another channel between receiving the first alert and interrogating the alert register, the corresponding bit for that alert event is also set.

The contents of the alert indication register are reset by reading it. When the AD7091R-5 uses the I^2C interface to read the alert indication register, the register is reset at the fourth SCL clock of the byte. By this time, the data from the register has moved to the I^2C shift register.

The alert bits for any unimplemented channels always return zeros.

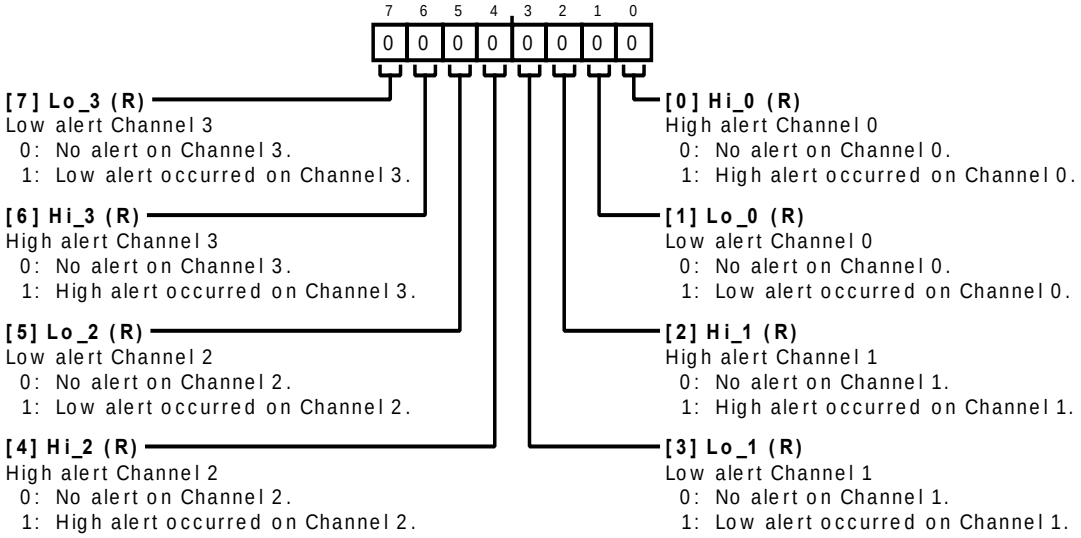


Table 16. Alert Indication Bit Map

MSB							LSB
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
LO_3	HI_3	LO_2	HI_2	LO_1	HI_1	LO_0	HI_0

Table 17. Bit Descriptions for the Alert Indication Register

Bit(s)	Bit Name	Description	Reset	Access
7	LO_3	Channel 3 low alert status 0: no alert on Channel 3 1: low alert occurred on Channel 3	0x0	R
6	HI_3	Channel 3 high alert status 0: no alert on Channel 3 1: high alert occurred on Channel 3	0x0	R
5	LO_2	Channel 2 low alert status 0: no alert on Channel 2 1: low alert occurred on Channel 2	0x0	R
4	HI_2	Channel 2 high alert status 0: no alert on Channel 2 1: high alert occurred on Channel 2	0x0	R
3	LO_1	Channel 1 low alert status 0: no alert on Channel 1 1: low alert occurred on Channel 1	0x0	R

Bit(s)	Bit Name	Description	Reset	Access
2	HI_1	Channel 1 high alert status 0: no alert on Channel 1 1: high alert occurred on Channel 1	0x0	R
1	LO_0	Channel 0 low alert status 0: no alert on Channel 0 1: low alert occurred on Channel 0	0x0	R
0	HI_0	Channel 0 high alert status 0: no alert on Channel 0 1: high alert occurred on Channel 0	0x0	R

CHANNEL x LOW LIMIT REGISTER

Each analog input channel of the AD7091R-5 has its own low limit register. The low limit registers are 16-bit read/write registers. See Table 9 for the register addresses. The low limit registers store the lower limit of the conversion value that activates the ALERT output.

Of the 16 bits, only the twelve least significant bits (LSBs) are used, Bit B11 to Bit B0. Bit B15 to Bit B12 are not used.

CHANNEL x HIGH LIMIT REGISTER

Each analog input channel of the AD7091R-5 has its own high limit register. The high limit registers are 16-bit read/write registers. See Table 9 for the register addresses. The high limit registers store the upper limit of the conversion value that activates the ALERT output.

Of the 16 bits, only the twelve least significant bits (LSBs) are used, Bit B11 to Bit B0. Bit B15 to Bit B12 are not used.

CHANNEL x HYSTERESIS REGISTER

Each analog input channel of the AD7091R-5 has its own hysteresis register, which are 16-bit read/write registers. See Table 9 for the register addresses. The hysteresis register stores the hysteresis value (N) when using the limit registers. The hysteresis value determines the reset point for the ALERT/BUSY/GPO_0 pin if a violation of the limits has occurred.

Of the 16 bits, only the twelve least significant bits (LSBs) are used, Bit B11 to Bit B0. Bit B15 to Bit B12 are not used.

Table 18. Channel x Low Limit Bit Map

MSB															LSB
B15	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
RSV				CHx LOW LIMIT											

Table 19. Bit Descriptions for Channel x Low Limit Register

Bits	Bit Name	Description	Reset	Access
[15:12]	RSV	Reserved	0x00	R
[11:0]	CHx LOW LIMIT	Low limit value for Channel x	0x000	R/W

Table 20. Channel x High Limit Bit Map

MSB															LSB
B15	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
RSV				CHx HIGH LIMIT											

Table 21. Bit Descriptions for Channel x High Limit Register

Bits	Bit Name	Description	Reset	Access
[15:12]	RSV		0x00	R
[11:0]	CHx HIGH LIMIT	High limit value for Channel x	0xFFF	R/W

Table 22. Channel x Hysteresis Bit Map

MSB															LSB
B15	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
RSV				CHx HYSTERISIS											

Table 23. Bit Descriptions for the Channel x Hysteresis Register

Bits	Bit Name	Description	Reset	Access
[15:12]	RSV		0x00	R
[11:0]	CHx HYSTERISIS	Hysteresis value for Channel x	0xFFF	R/W

I²C INTERFACE

Control of the AD7091R-5 is carried out via the I²C-compatible serial bus. The AD7091R-5 is connected to this bus as a slave device under the control of a master device such as the processor.

SERIAL BUS ADDRESS BYTE

The first byte that the user writes to the device is the slave address byte. Similar to all I²C-compatible devices, the AD7091R-5 has a 7-bit serial address. The three MSBs of this address are set to 010. The four LSBs are user programmable by the three-state input pins, AS_0 and AS_1, as shown in Table 24.

In Table 24, high means tie the pin to V_{DRIVE}, low means tie the pin to GND, and NC refers to a pin left floating. Note that in NC cases, the stray capacitance on the pin must be less than 30 pF to allow correct detection of the floating state; therefore, any printed circuit board trace must be kept as short as possible.

Table 24. Slave Address Control Using Three-State Input Pins

		Slave Address (A6 to A0)	
AS_1	AS_0	Binary	Hex
High	High	010 0000	0x20
High	NC	010 0010	0x22
High	Low	010 0011	0x23
NC	H	010 1000	0x28
NC	NC	010 1010	0x2A
NC	Low	010 1011	0x2B
Low	High	010 1100	0x2C
Low	NC	010 1110	0x2E
Low	Low	010 1111	0x2F

GENERAL I²C TIMING

Figure 39 shows the timing diagram for general read and write operations using an I²C compliant interface.

When no device is driving the bus, both SCL and SDA are high. This is known as the idle state. When the bus is idle, the master initiates a data transfer by establishing a start condition, defined as a high to low transition on the serial data line (SDA) while the serial clock line (SCL) remains high. This indicates that a data stream follows. The master device must generate the clock.

Data is sent over the serial bus in groups of nine bits—eight bits of data from the transmitter are followed by an acknowledge bit (ACK) from the receiver. Data transitions on the SDA line must occur during the low period of the clock signal and remain stable during the high period. The receiver must pull the SDA line low during the acknowledge bit to signal that the preceding byte has been received correctly. If this is not the case, cancel the transaction.

The first byte that the master sends must consist of a 7-bit slave address, followed by a data direction bit. Each device on the bus has a unique slave address; therefore, the first byte sets up communication with a single slave device for the duration of the transaction.

The transaction can be used either to write to a slave device (data direction bit = 0) or to read data from it (data direction bit = 1). In the case of a read transaction, it is often necessary first to write to the slave device (in a separate write transaction) to tell it from which register to read. Reading and writing cannot be combined in one transaction.

When the transaction is complete, the master can maintain control of the bus, initiating a new transaction by generating another start bit (high to low transition on SDA while SCL is high). This is known as a repeated start (SR). Alternatively, the bus can be relinquished by releasing the SCL line followed by the SDA line. This low to high transition on SDA while SCL is high is known as a stop bit (P), and it leaves the I²C bus in its idle state (no current is consumed by the bus).

The example in Figure 39 shows a simple write transaction with an AD7091R-5 as the slave device. In this example, the AD7091R-5 register pointer is being set up for a future read transaction.

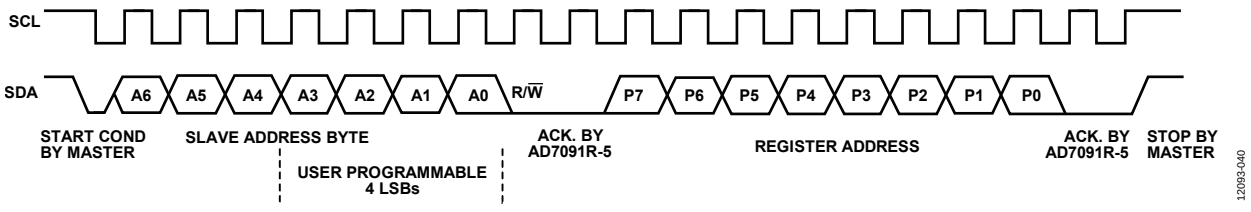


Figure 39. General I²C Timing

WRITING TO THE AD7091R-5

WRITING TWO BYTES OF DATA TO A 16-BIT REGISTER

With the exception of the channel register, all registers on the AD7091R-5 are 16-bit registers; therefore, two bytes of data are required to write a value to any one of these registers. Writing two bytes of data to a register consists of the following sequence (see Figure 40):

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master sends a register address. The slave asserts an acknowledge on SDA.
5. The master sends the first data byte (most significant).
6. The slave asserts an acknowledge on SDA.
7. The master sends the second data byte (least significant).
8. The slave asserts an acknowledge on SDA.
9. The master asserts a stop condition on SDA to end the transaction.

WRITING TO MULTIPLE REGISTERS

Writing to multiple address registers consists of the following steps (see Figure 41):

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device (AD7091R-5) asserts an acknowledge on SDA.
4. The master sends a register address, for example, the configuration register address.
5. The slave asserts an acknowledge on SDA.
6. The master sends the first data byte.
7. The slave asserts an acknowledge on SDA.
8. The master sends the second data byte.
9. The slave asserts an acknowledge on SDA.
10. The master sends a second register address, for example, the Channel 0 high limit register.
11. The slave asserts an acknowledge on SDA.
12. The master sends the first data byte.
13. The slave asserts an acknowledge on SDA.
14. The master sends the second data byte.
15. The slave asserts an acknowledge on SDA.
16. The master asserts a stop condition on SDA to end the transaction.

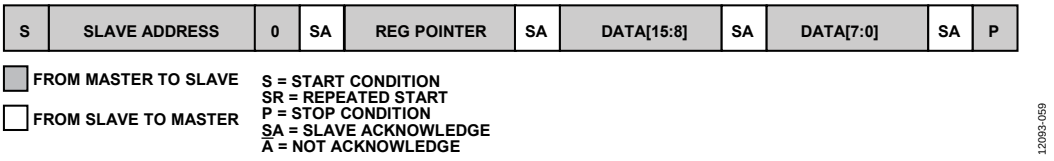


Figure 40. Writing Two Bytes of Data to a 16-Bit Register

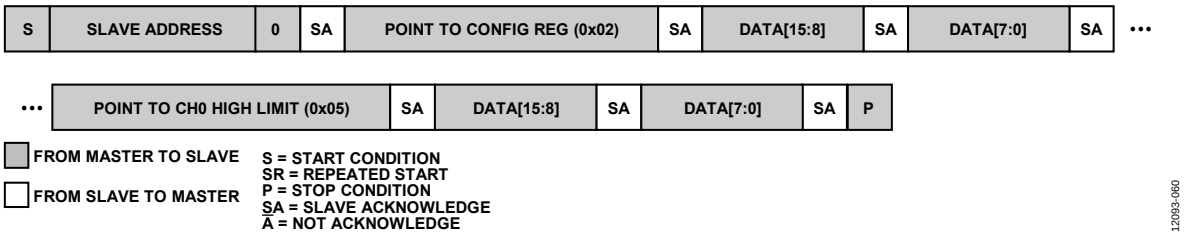


Figure 41. Writing to Multiple Registers

READING DATA FROM THE AD7091R-5

READING TWO BYTES OF DATA FROM A 16-BIT REGISTER

Reading the contents from any of the 16-bit registers is a 2-byte read operation. In this protocol, the first part of the transaction writes to the register pointer. When the register address has been set up, any number of reads can be performed from that particular register without writing to the address pointer register again. When the required number of reads is complete, the master must not acknowledge the final byte. This tells the slave to stop transmitting, allowing a stop condition to be asserted by the master. Further reads from this register can be performed in a future transaction without rewriting to the register pointer.

If a read from a different address is required, the relevant register address must be written to the address pointer register and, again, any number of reads from this register can then be performed. In the following example, the master device reads three lots of 2-byte data from a slave device, but as many lots consisting of two bytes can be read as required. This protocol assumes that the particular register address has been set up by a single-byte write operation to the address pointer register.

Reading two bytes of data from a 16-bit register consists of the following sequence (see Figure 42):

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master receives the data byte.
5. The master asserts an acknowledge on SDA.
6. The master receives the second data byte.
7. The master asserts an acknowledge on SDA.
8. The master receives the data byte.
9. The master asserts an acknowledge on SDA.
10. The master receives the second data byte.
11. The master asserts an acknowledge on SDA.
12. The master receives the data byte.
13. The master asserts an acknowledge on SDA.
14. The master receives the second data byte.
15. The master asserts a not acknowledge on SDA to notify the slave that the data transfer is complete.
16. The master asserts a stop condition on SDA to end the transaction.

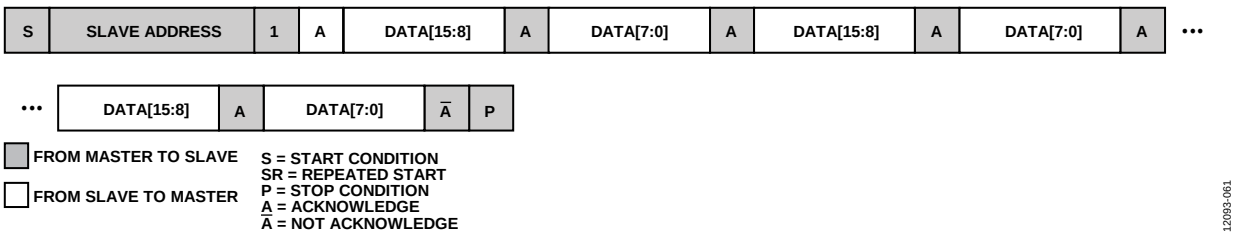


Figure 42. Reading Three Lots of Two Bytes of Data from the Conversion Result Register (Conversion Register Pointer Already Set)

MODES OF OPERATION

There are three methods of initiating a conversion on the AD7091R-5 with the I²C interface: sample mode using the $\overline{\text{CONVST}}$/GPO$_1$ pin, command mode, and autocycle mode. In the $\overline{\text{CONVST}}$/GPO$_1$ pin mode, conversions are done on demand. Whenever the $\overline{\text{CONVST}}$/GPO$_1$ pin is toggled, an ADC conversion happens. In command mode, the read of the conversion result register starts the conversion. In autocycle mode, conversions occur on the selected channels in the background periodically. This mode monitors whether signals cross certain threshold levels, the absolute value being relatively unimportant.

SAMPLE MODE

At power-up, the device wakes up in sample mode and selects Channel 0 for conversion. Sample mode can be selected subsequently by writing a value of 0 to both the CMD and auto bits of the configuration register or by writing a value of 1 to both the CMD and auto bits. In sample mode, conversions are controlled by toggling the active low $\overline{\text{CONVST}}$/GPO$_1$ pin.

To perform conversion on a channel other than Channel 0 or on a sequence of channels, before initiating any conversion, write to the channel register to select the channels for conversion. On each $\overline{\text{CONVST}}$ pulse, the next channel in the selected sequence is converted starting from the lowest numbered channel selected (0, 1 … 7).

A high to low transition on the $\overline{\text{CONVST}}$/GPO$_1$ pin puts the track-and-hold circuit into hold mode and samples the analog input. The conversion is initiated and requires approximately 550 ns to complete. When the conversion process is finished, the track-and-hold circuit goes back into track.

To read back data stored in the conversion result register, first wait until the conversion is finished. If the address pointer is pointing to the conversion result register, the conversion data can be read using the protocol described in Figure 42. Otherwise, the address pointer must be set to point at the conversion result register before conversion data can be read. When the conversion result read is completed, the user may pull the $\overline{\text{CONVST}}$ pin low again to start another conversion.

Do not toggle the $\overline{\text{CONVST}}$ pin when activity is occurring on the I²C bus.

COMMAND MODE

In command mode, the AD7091R-5 converts on demand on either a single channel or a sequence of channels. This mode of operation allows a conversion to be selected automatically any time a write operation occurs to the command register. In command mode, the AD7091R-5 converts the next programmed channel when the conversion result register is read. To enter this mode, the required combination of channels is written into the channel register. Select command mode operation by writing CMD = 1 and auto = 0 in the configuration register. Following the write operation, the AD7091R-5 must be addressed again to indicate that a read operation is required from the conversion result register.

The conversion starts on the first positive edge of SCL after the ACK for the previous byte is sent to avoid starting a conversion during the ACK cycle. This does not create an issue with the exact time that the conversion data must be sent on the I²C bus because the first three bits sent on the I²C bus correspond to the channel for which the conversion data belongs. After the conversion is completed, the ADC powers down. The next conversion in the sequence starts after a subsequent read from the conversion result register is initiated. The device cycles through the selected channels from the lowest selected channel number in the sequence to the next until all channels in the sequence are converted. After all channels in the sequence are converted, the sequence rolls back to the lowest numbered channel enabled so that the sequence can be repeated indefinitely.

To stop converting in the command mode, the master does not acknowledge the final byte of data. This NACK stops the AD7091R-5 transmission, allowing the master to assert a stop condition on the bus. On the receipt of an I²C NACK condition, the AD7091R-5 stops converting, but the content of the configuration register is preserved. After the device is readdressed and a read initiated from the conversion result register, the AD7091R-5 begins converting on the previously selected sequence of channels.

The conversion sequence starts at the first selected channel in the sequence. That is, if Channel 1, Channel 2, and Channel 3 are selected and a stop condition occurs after the result for Channel 1 is read, on the resumption of conversions, Channel 2 is converted and the conversion sequence continues. This happens provided the channel register is not written in between conversions. However, if the channel register is written, this results in the conversion starting from Channel 1.

The example in Figure 43 shows command mode converting on a sequence of channels including Channel 0, Channel 1, and Channel 2.

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device (AD7091R-5) asserts an acknowledge on SDA.
4. The master sends the configuration register address (0x02).
5. The slave asserts an acknowledge on SDA.
6. The master sends the first data byte (0x03) to the configuration register, which selects the command mode.
7. The slave asserts an acknowledge on SDA.
8. The master sends the second data byte (0x00) to the configuration register.
9. The slave asserts an acknowledge on SDA.
10. The master sends the channel register address (0x01).
11. The slave asserts an acknowledge on SDA.
12. The master sends the data byte (0x07) to the channel register, which selects Channel 0, Channel 1, and Channel 2, followed by a write bit.
13. The slave asserts an acknowledge on SDA.
14. The master sends the conversion result register address (0x00).
15. The slave asserts an acknowledge on SDA.
16. The master sends a repeated start and the 7-bit slave address followed by the read bit (high).
17. The slave (AD7091R-5) asserts an acknowledge on SDA.
18. The master receives a data byte, which contains the channel address bits, the alert bit, and the four MSBs of the converted result for Channel 0.
19. The master then asserts an acknowledge on SDA.
20. The master receives the second data byte, which contains the eight LSBs of the converted result for Channel 0. The master then asserts on acknowledge on SDA.
21. Step 18 to Step 20 repeat for Channel 1 and Channel 2.
22. After the master has received the results from all the selected channels, the slave again converts and outputs the result for the first channel in the selected sequence. Step 18 to Step 21 are repeated.
23. The master asserts a not acknowledge on SDA and a stop condition on SDA to end the conversion and exit command mode.

To change the conversion sequence, rewrite a new sequence to the command mode. If a new write to the channel register is performed while an existing conversion sequence is underway, the existing conversion sequence is terminated and the next conversion performed is the first selected channel from the new sequence. The maximum throughput that can be achieved using this mode with a 400 kHz I²C clock is (400 kHz/18) = 22.22 kSPS.

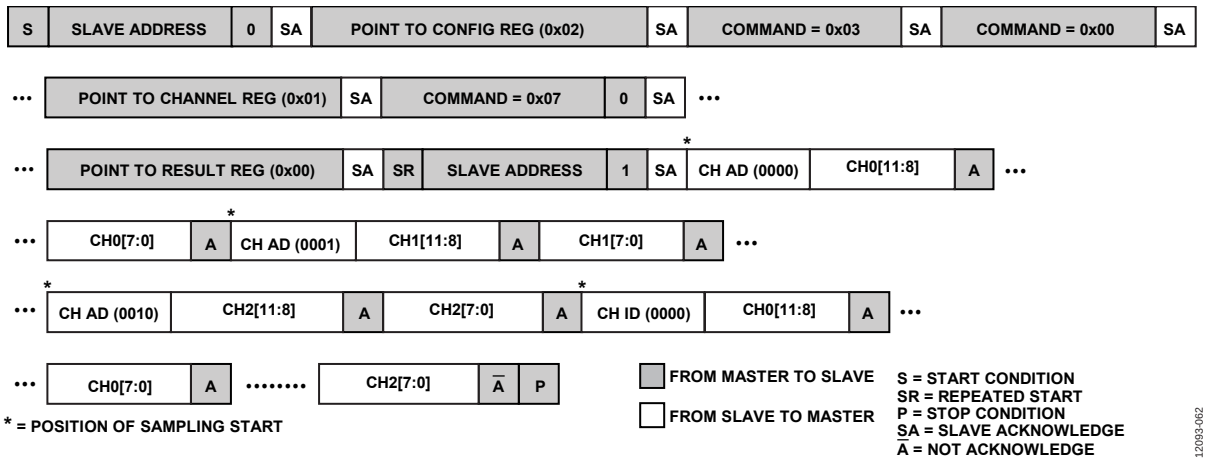


Figure 43. Command Mode Operation

AUTOCYCLE MODE

The AD7091R-5 can be configured to convert continuously on a programmable sequence of channels, making it the ideal mode of operation for system monitoring. These conversions occur automatically at intervals chosen by the CYCLE_TIMER bits in the configuration register. Typically, this mode is used to monitor a selection of channels automatically with the limit registers programmed to signal an out of bounds condition via the alert function. Reads and writes can be performed at any time (the conversion result register contains the most recent conversion result).

To enter this mode, the required combination of channels that must be monitored is written into the channel register. The required interval between conversions is selected by writing into the CYCLE_TIMER bits in the configuration register. Autocycle mode operation can then be selected by writing CMD = 0 and auto = 1 in the configuration register. If more than one channel bit is set in the channel register, the ADC automatically cycles through the channel sequence, starting with the lowest channel and working its way up through the sequence. After the sequence is complete, the ADC starts converting on the lowest channel again, continuing to loop through the sequence until this mode is exited.

As soon as a conversion is complete, the conversion result is compared with the content of the limit registers. The alert register is updated automatically with the result of the comparison. If a violation of the limit registers is found, the alert bit in the conversion result register is set and, if the ALERT/BUSY/GPO_0 pin functionality is selected in the configuration register, the ALERT/BUSY/GPO_0 pin is asserted with the polarity determined by ALERT_POL_OR_GPO0 bit in the configuration register.

If an out-of-cycle conversion is required while autocycle mode is active, it is necessary to disable autocycle mode before proceeding to the command or sample mode. When the conversion is complete, the user can reenable autocycle mode. In autocycle mode, the AD7091R-5 does not enter power-down on receipt of a stop condition; therefore, conversions and alert monitoring continues to function.

The CYCLE_TIMER value in the configuration register controls the time of conversion in autocycle mode. Four separate time intervals are available, and each is a multiple of the BASE_TIME. The reset value used is 8 × BASE_TIME. The base time for the AD7091R-5 is approximately 100 µs.

Writing to the channel register or the configuration register when in autocycle mode results in a reset of the cycle timer. This process ensures that the latest information is used for cycle timer calculation.

Table 25. Autocycle Interval Time

Command	Interval Time	Approximate Interval
00	1 × BASE_TIME	100 µs (10 kSPS)
01	2 × BASE_TIME	200 µs (5 kSPS)
10	4 × BASE_TIME	400 µs (2.5 kSPS)
11	8 × BASE_TIME	800 µs (1.25 kSPS)

Do not write to the limit and hysteresis registers when the AD7091R-5 is in autocycle mode. If these registers are written by chance, the design stalls the internal cycle timer counters for one SCL period when the registers are being updated. A write to the channel register and the configuration register in autocycle mode restarts the cycle timer counters.

Because the alert indication register is read to clear, read the register only when an alert is indicated. Otherwise, there is a risk of inadvertently clearing the alert register and the alert bit in the conversion result register.

POWER-DOWN MODE

Power-down mode is intended for use in applications where slower throughput rates and lower power consumption are required; either the ADC is powered down between each conversion, or a burst of conversions can be performed at a higher throughput rate, and the ADC is then powered down for a relatively long duration between these bursts of several conversions. When the AD7091R-5 is in power-down mode, all analog circuitry is powered down; however, the serial interface is active.

The serial interface of the AD7091R-5 is functional in power-down; therefore, the user may read back the last conversion result even after the device enters power-down mode.

To enter power-down, write to the power-down configuration bits in the configuration register, as seen in Table 15. To enter full power-down mode, set the sleep mode/bias generator bit to 1, and set the internal reference bit to 0, which ensures that all analog circuitry and the internal reference powers down. When the internal reference is enabled, it consumes power any time Bit 0 of the configuration register is set to 1.

To exit this mode of operation and power up the AD7091R-5, set the MSB of the P_DOWN word to 1. If a power-up of the internal reference is desired, the P_DOWN LSB must also be set to 1. When using the internal reference, and the device is in full power-down mode, wait to perform conversions until the internal reference has had time to power up and settle. The reference buffer requires 50 ms to power up and charge the 2.2 µF decoupling capacitor during the power-up time. After power-up is complete, the ADC is fully powered up, and the input signal is properly acquired. To start the next conversion, operate the interface as described in the Modes of Operation section.

ALERT

The alert functionality is used as an out of bounds indicator. An alert event is triggered when the value in the conversion result register exceeds the CHx high limit value in the Channel x high limit register or falls below the CHx low limit value in the Channel x low limit register for a selected channel.

Detailed alert information is accessible in the alert register. The register contains two status bits per channel, one corresponding to the high limit, and the other to the low limit. A logical OR of alert signals for all channels creates a common alert value. This value can be accessed by the alert bit in the conversion result register and configured to drive out on the ALERT/BUSY/GPO_0 pin. The ALERT/BUSY/GPO_0 pin is configured as an ALERT output by configuring the following bits in the configuration register:

- Set the ALERT_EN_OR_GPO0 bit (Bit 4) to 1.
- Set the busy bit (Bit 5) to 0.
- Set the ALERT_POL_OR_GPO0 bit (Bit 3) to 0 for the ALERT/BUSY/GPO_0 pin to be active low and set it to 1 for the ALERT/BUSY/GPO_0 pin to be active high.

The alert register, alert bit, and ALERT/BUSY/GPO_0 pin are cleared by reading the alert register contents. Additionally, if the conversion result goes beyond the hysteresis value for a selected channel, the alert bit corresponding to that channel is reset automatically. Issuing a software reset also clears the alert status.

The ALERT/BUSY/GPO_0 pin has an open-drain configuration that allows the alert outputs of several AD7091R-5 devices to be wired together when the ALERT/BUSY/GPO_0 pin is active low. The ALERT/BUSY/GPO_0 pin configuration can be controlled by the ALERT_DRIVE_TYPE bit, Bit 15 of the configuration register.

The ALERT_POL_OR_GPO0 bit (Bit 3 of the configuration register) sets the active polarity of the alert output. The power-up default is active low.

When using the ALERT/BUSY/GPO_0 output pin, an external pull-up resistor is required because the output is an open-drain configuration. Connect the external pull-up resistor to V_{DRIVE}. The resistor value is application dependent; however, it must be large enough to avoid excessive sink currents at the ALERT/BUSY/GPO_0 output pin.

BUSY

When the ALERT/BUSY/GPO_0 pin is configured as a BUSY output, the pin indicates when a conversion is taking place. The ALERT/BUSY/GPO_0 pin is configured as BUSY by configuring the following bits in the configuration register:

- Set the ALERT_EN_OR_GPO0 bit, Bit 4, to 1.
- Set the busy bit, Bit 5, to 1.
- Set the ALERT_POL_OR_GPO0 bit, Bit 3, to 0 for the ALERT/BUSY/GPO_0 pin to be active low, and set it to 1 for the ALERT/BUSY/GPO_0 pin to be active high.

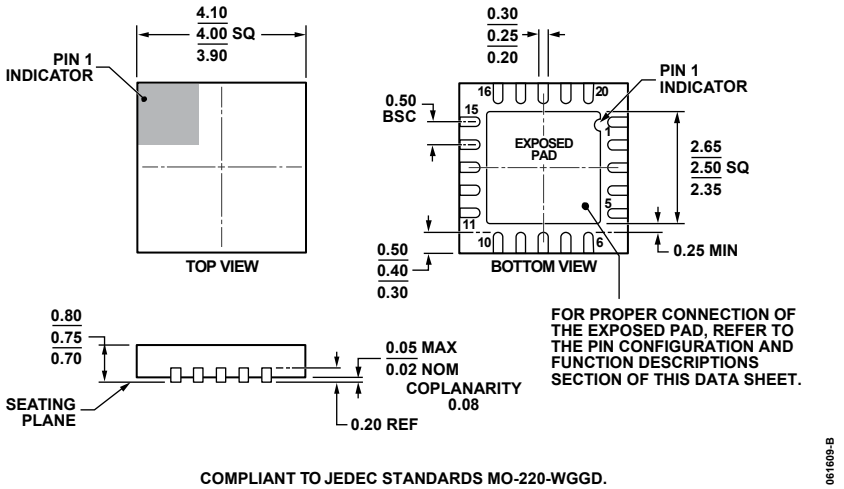
When using the ALERT/BUSY/GPO_0 output pin, an external pull-up resistor is required because the output is an open-drain configuration. Connect the external pull-up resistor to V_{DRIVE}. The resistor value is application dependent; however, it must be large enough to avoid excessive sink currents at the ALERT/BUSY/GPO_0 output pin.

CHANNEL SEQUENCER

The AD7091R-5 includes a channel sequencer useful for scanning channels in a repeated fashion. Channels included in the sequence are configured in the channel register. If all the bits in the channel register are 0, Channel 0 is selected by default, and all conversions occur on this channel. If the channel register is nonzero, the conversion sequence starts from the lowest numbered channel enabled in the channel register. The sequence cycles through all the enabled channels in ascending order. After all the channels in the sequence are converted, the sequence starts again.

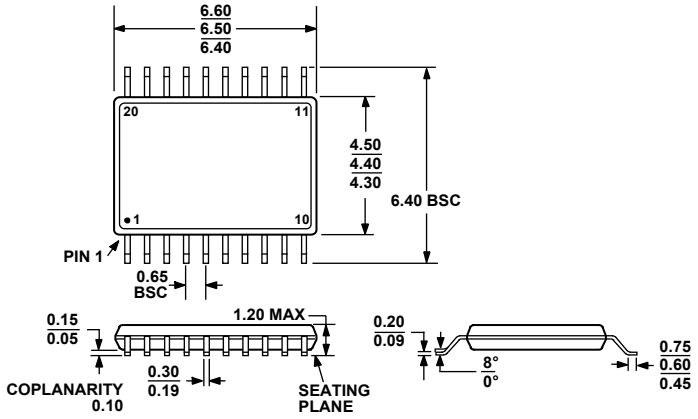
There is a latency of one conversion before the channel conversion sequence is updated. If the channel register is programmed with a new value, the conversion sequence is reset to the lowest numbered channel in the new value.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD.

Figure 44. 20-Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-20-10)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153-AC

Figure 45. 20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Channels	Temperature Range	Package Description	Package Option
AD7091R-5BCPZ	4	−40°C to +125°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-10
AD7091R-5BCPZ-RL7	4	−40°C to +125°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-10
AD7091R-5BRUZ	4	−40°C to +125°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
AD7091R-5BRUZ-RL7	4	−40°C to +125°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
EVAL-AD7091R-5SDZ			Evaluation Board	
EVAL-SDP-CB1Z			Evaluation Controller Board	

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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