ISL23328

Dual, 128-Tap, Low Voltage Digitally Controlled Potentiometer (XDCP™)

FN7902
Rev 1.00
September 29, 2015

The ISL23328 is a volatile, low voltage, low noise, low power, 128-Tap, dual digitally controlled potentiometer (DCP) with an I^2C Bus™ interface. It integrates two DCP cores, wiper switches and control logic on a monolithic CMOS integrated circuit.

Each digitally controlled potentiometer is implemented with a combination of resistor elements and CMOS switches. The position of the wipers are controlled by the user through the I^2C bus interface. Each potentiometer has an associated volatile Wiper Register (WRi, i = 0, 1) that can be directly written to and read by the user. The contents of the WRi controls the position of the wiper. When powered on, the wiper of each DCP will always commence at mid-scale (64 tap position).

The low voltage, low power consumption, and small package of the ISL23328 make it an ideal choice for use in battery operated equipment. In addition, the ISL23328 has a V_{LOGIC} pin allowing down to 1.2V bus operation, independent from the V_{CC} value. This allows for low logic levels to be connected directly to the ISL23328 without passing through a voltage level shifter.

The DCP can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

Applications

- Power supply margining
- Trimming sensor circuits
- Gain adjustment in battery powered instruments
- RF power amplifier bias compensation

Features

- Two potentiometers per package
- 128 resistor taps
- 10kΩ, 50kΩ or 100kΩ total resistance
- I^2C serial interface
  - No additional level translator for low bus supply
  - Three address pins allow up to eight devices per bus
- Power supply
  - V_{CC} = 1.7V to 5.5V analog power supply
  - V_{LOGIC} = 1.2V to 5.5V I^2C bus/logic power supply
- Maximum supply current without serial bus activity (standby)
  - 3µA @ V_{CC} and V_{LOGIC} = 5V
  - 1.7µA @ V_{CC} and V_{LOGIC} = 1.7V
- Shutdown Mode
  - Forces the DCP into an end-to-end open circuit and RWi is connected to RLi internally
  - Reduces power consumption by disconnecting the DCP resistor from the circuit
- Wiper resistance: 70Ω typical @ V_{CC} = 3.3V
- Power-on preset to mid-scale (64 tap position)
- Extended industrial temperature range: -40°C to +125°C
- 14 Ld TSSOP or 16 Ld UTQFN packages
- Pb-free (RoHS Compliant)

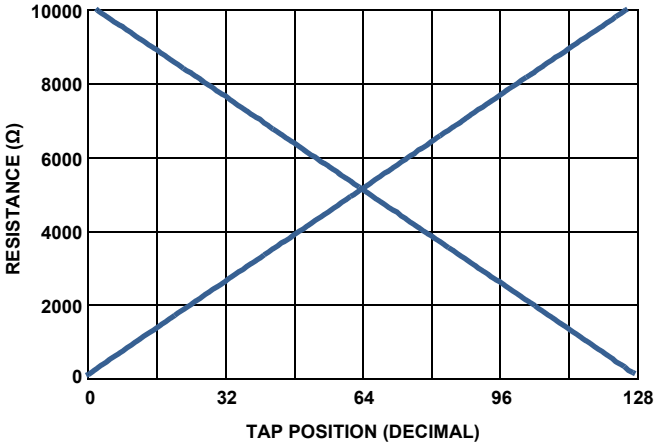


FIGURE 1. FORWARD AND BACKWARD RESISTANCE vs TAP POSITION, 10kΩ DCP

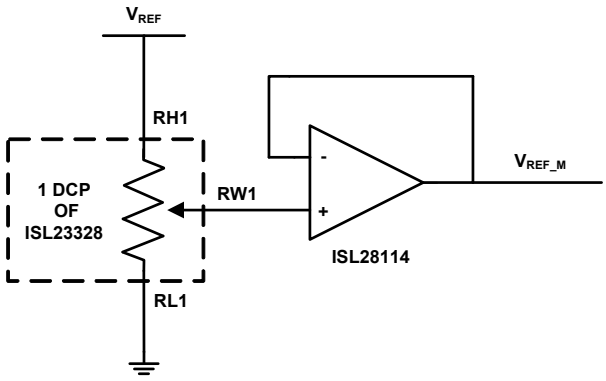
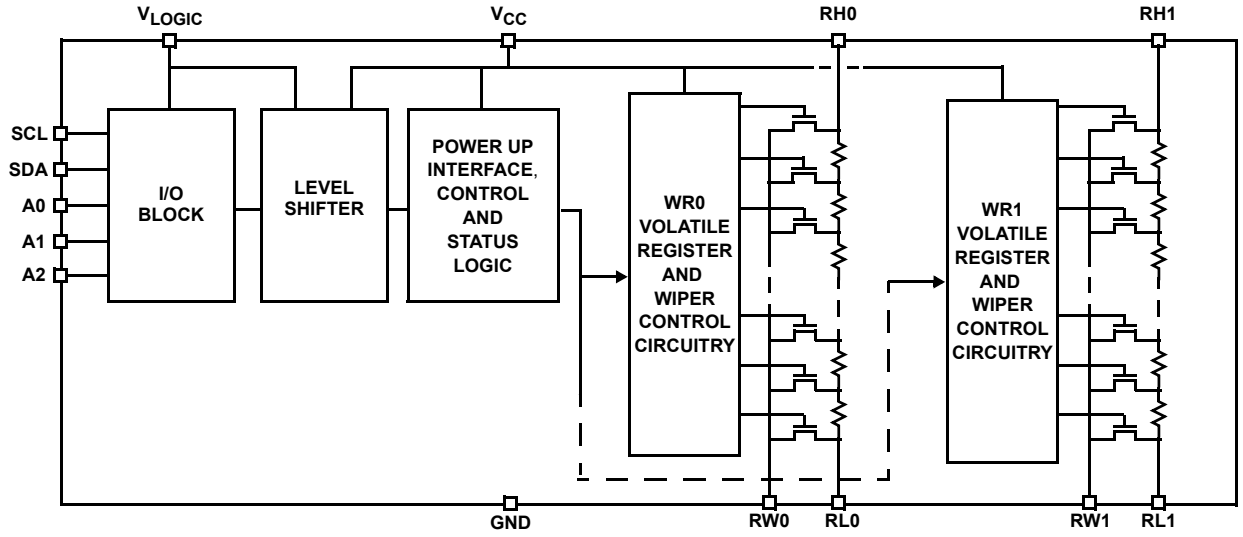


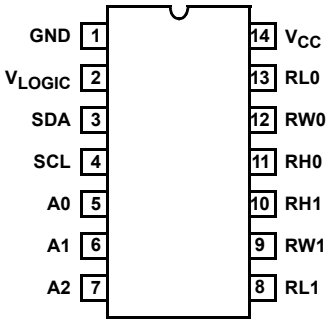
FIGURE 2. V_{REF} ADJUSTMENT

Block Diagram

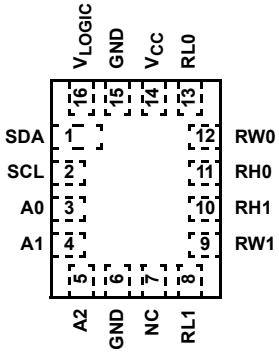


Pin Configurations

ISL23328
(14 LD TSSOP)
TOP VIEW



ISL23328
(16 LD UTQFN)
TOP VIEW



Pin Descriptions

TSSOP	UTQFN	SYMBOL	DESCRIPTION
1	6, 15	GND	Ground pin
2	16	V_{LOGIC}	I^2C bus/logic supply. Range 1.2V to 5.5V
3	1	SDA	Logic Pin - Serial bus data input/open drain output
4	2	SCL	Logic Pin - Serial bus clock input
5	3	A0	Logic Pin - Hardwire slave address pin for I^2C serial bus. Range: V_{LOGIC} or GND
6	4	A1	Logic Pin - Hardwire slave address pin for I^2C serial bus. Range: V_{LOGIC} or GND
7	5	A2	Logic Pin - Hardwire slave address pin for I^2C serial bus. Range: V_{LOGIC} or GND
8	8	RL1	DCP1 “low” terminal
9	9	RW1	DCP1 wiper terminal
10	10	RH1	DCP1 “high” terminal
11	11	RH0	DCP0 “high” terminal
12	12	RW0	DCP0 wiper terminal
13	13	RL0	DCP0 “low” terminal
14	14	V_{CC}	Analog power supply. Range 1.7V to 5.5V
	7	NC	Not Connected

Ordering Information

PART NUMBER (Note 4)	PART MARKING	RESISTANCE OPTION (kΩ)	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL23328TFVZ (Note 2)	23328 TFVZ	100	-40 to +125	14 Ld TSSOP	M14.173
ISL23328TFVZ-T7A (Notes 1, 2)	23328 TFVZ	100	-40 to +125	14 Ld TSSOP	M14.173
ISL23328TFVZ-TK (Notes 1, 2)	23328 TFVZ	100	-40 to +125	14 Ld TSSOP	M14.173
ISL23328UFVZ (Note 2) **(No longer available, recommended replacement: ISL23328TFRUZ-TK)**	23328 UFVZ	50	-40 to +125	14 Ld TSSOP	M14.173
ISL23328UFVZ-T7A (Notes 1, 2) **(No longer available, recommended replacement: ISL23328TFRUZ-TK)**	23328 UFVZ	50	-40 to +125	14 Ld TSSOP	M14.173
ISL23328UFVZ-TK (Notes 1, 2)	23328 UFVZ	50	-40 to +125	14 Ld TSSOP	M14.173
ISL23328WFVZ (Note 2)	23328 WFVZ	10	-40 to +125	14 Ld TSSOP	M14.173
ISL23328WFVZ-T7A (Notes 1, 2)	23328 WFVZ	10	-40 to +125	14 Ld TSSOP	M14.173
ISL23328WFVZ-TK (Notes 1, 2)	23328 WFVZ	10	-40 to +125	14 Ld TSSOP	M14.173
ISL23328TFRUZ-T7A (Notes 1, 3)	GBM	100	-40 to +125	16 Ld 2.6x1.8 UTQFN	L16.2.6x1.8A
ISL23328TFRUZ-TK (Notes 1, 3)	GBM	100	-40 to +125	16 Ld 2.6x1.8 UTQFN	L16.2.6x1.8A
ISL23328UFRUZ-T7A (Notes 1, 3) **(No longer available, recommended replacement: ISL23328TFRUZ-TK)**	GBL	50	-40 to +125	16 Ld 2.6x1.8 UTQFN	L16.2.6x1.8A
ISL23328UFRUZ-TK (Notes 1, 3) **(No longer available, recommended replacement: ISL23328TFRUZ-TK)**	GBL	50	-40 to +125	16 Ld 2.6x1.8 UTQFN	L16.2.6x1.8A
ISL23328WFRUZ-T7A (Notes 1, 3)	GBK	10	-40 to +125	16 Ld 2.6x1.8 UTQFN	L16.2.6x1.8A
ISL23328WFRUZ-TK (Notes 1, 3)	GBK	10	-40 to +125	16 Ld 2.6x1.8 UTQFN	L16.2.6x1.8A

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), please see device information page for ISL23328. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings

Supply Voltage Range
V_{CC} ..... -0.3V to 6.0V
V_{LOGIC} ..... -0.3V to 6.0V
Voltage on Any DCP Terminal Pin ..... -0.3V to 6.0V
Voltage on Any Digital Pins ..... -0.3V to 6.0V
Wiper Current I_W (10s) ..... ±6mA
ESD Rating
Human Body Model (Tested per JESD22-A114E) 4.5kV
Charged Device Model (Tested per JESD22-A114E) 1kV
Machine Model (Tested per JESD22-A115-A) 300V
Latch Up (Tested per JESD-78B; Class 2, Level A) .... 100mA @ +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
14 Ld TSSOP Package (Notes 5, 6)	112	40
16 Ld UTQFN Package (Notes 5, 6)	110	64

Maximum Junction Temperature (Plastic Package) ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Pb-Free Reflow Profile ..... see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Temperature ..... -40°C to +125°C
V_{CC} Supply Voltage ..... 1.7V to 5.5V
V_{LOGIC} Supply Voltage ..... 1.2V to 5.5V
DCP Terminal Voltage ..... 0 to V_{CC}
Max Wiper Current ..... ±3mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
6. For θ_{JC}, the "case temp" location is the center top of the package.

Analog Specifications

V_{CC} = 2.7V to 5.5V, V_{LOGIC} = 1.2V to 5.5V over recommended operating conditions unless otherwise stated.
Boldface limits apply over the operating temperature range, -40°C to +125°C.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 19)	TYP (Note 7)	MAX (Note 19)	UNITS
R_{TOTAL}	RH to RL Resistance	W option		10		kΩ
		U option		50		kΩ
		T option		100		kΩ
	RH to RL Resistance Tolerance		-20	±2	+20	%
	End-to-End Temperature Coefficient	W option		125		ppm/°C
		U option		65		ppm/°C
		T option		45		ppm/°C
V_{RH}, V_{RL}	DCP Terminal Voltage	V_{RH} or V_{RL} to GND	0		V_{CC}	V
RW	Wiper Resistance	RH - floating, V_{RL} = 0V, force I_W current to the wiper, $I_W = (V_{CC} - V_{RL})/R_{TOTAL}$, V_{CC} = 2.7V to 5.5V		70	200	Ω
		V_{CC} = 1.7V		580		Ω
$C_H/C_L/C_W$	Terminal Capacitance	See "DCP Macro Model" on page 9		32/32/32		pF
I_{LkgDCP}	Leakage on DCP Pins	Voltage at pin from GND to V_{CC}	-0.4	<0.1	0.4	µA
Noise	Resistor Noise Density	Wiper at middle point, W option		16		nV/√Hz
		Wiper at middle point, U option		49		nV/√Hz
		Wiper at middle point, T option		61		nV/√Hz
Feed Thru	Digital Feed-through from Bus to Wiper	Wiper at middle point		-65		dB
PSRR	Power Supply Reject Ratio	Wiper output change if V_{CC} change ±10%; wiper at middle point		-75		dB

Analog Specifications

V_{CC} = 2.7V to 5.5V, V_{LOGIC} = 1.2V to 5.5V over recommended operating conditions unless otherwise stated. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 19)	TYP (Note 7)	MAX (Note 19)	UNITS
VOLTAGE DIVIDER MODE (0V @ RL; V_{CC} @ RH; measured at RW, unloaded)						
INL (Note 12)	Integral Non-linearity, Guaranteed Monotonic	W option	**-0.5**	±0.15	**+0.5**	LSB (Note 8)
		U, T option	**-0.5**	±0.15	**+0.5**	LSB (Note 8)
DNL (Note 11)	Differential Non-linearity, Guaranteed Monotonic	W option	**-0.5**	±0.15	**+0.5**	LSB (Note 8)
		U, T option	**-0.5**	±0.15	**+0.5**	LSB (Note 8)
FSerror	Full-scale Error	W option	**-3**	-1.5	**0**	LSB (Note 8)
		U, T option	**-1.5**	-0.9	**0**	LSB (Note 8)
ZSerror (Note 9)	Zero-scale Error	W option	**0**	1.5	**3**	LSB (Note 8)
		U, T option	**0**	0.9	**1.5**	LSB (Note 8)
Vmatch (Note 21)	DCP to DCP Matching	DCPs at same tap position, same voltage at all RH terminals, and same voltage at all RL terminals	**-2**	±0.5	**2**	LSB (Note 8)
TC_V (Notes 13)	Ratiometric Temperature Coefficient	W option, Wiper Register set to 40 hex		8		ppm/°C
		U option, Wiper Register set to 40 hex		4		ppm/°C
		T option, Wiper Register set to 40 hex		2.3		ppm/°C
$t_{LS_Settling}$	Large Signal Wiper Settling Time	From code 0 to 7F hex, measured from 0 to 1 LSB settling of the wiper		300		ns
f_{cutoff}	-3dB Cutoff Frequency	Wiper at middle point W option		1200		kHz
		Wiper at middle point U option		250		kHz
		Wiper at middle point T option		120		kHz
RHEOSTAT MODE (Measurements between RW and RL pins with RH not connected, or between RW and RH with RL not connected)						
R_{INL} (Note 17)	Integral Non-linearity, Guaranteed Monotonic	W option; V_{CC} = 2.7V to 5.5V	**-1.0**	±0.5	**+1.0**	MI (Note 14)
		W option; V_{CC} = 1.7V		4		MI (Note 14)
		U, T option; V_{CC} = 2.7V to 5.5V	**-0.5**	±0.15	**+0.5**	MI (Note 14)
		U, T option; V_{CC} = 1.7V		1		MI (Note 14)
R_{DNL} (Note 16)	Differential Non-linearity, Guaranteed Monotonic	W option; V_{CC} = 2.7V to 5.5V	**-0.5**	±0.15	**+0.5**	MI (Note 14)
		W option; V_{CC} = 1.7V		±0.4		MI (Note 14)
		U, T option; V_{CC} = 2.7V to 5.5V	**-0.5**	±0.15	**+0.5**	MI (Note 14)
		U, T option; V_{CC} = 1.7V		±0.4		MI (Note 14)

Analog Specifications

V_{CC} = 2.7V to 5.5V, V_{LOGIC} = 1.2V to 5.5V over recommended operating conditions unless otherwise stated.
Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 19)	TYP (Note 7)	MAX (Note 19)	UNITS
R_{offset} (Note 15)	Offset, Wiper at 0 Position	W option; V_{CC} = 2.7V to 5.5V	**0**	1.8	**3**	MI (Note 14)
		W option; V_{CC} = 1.7V		3		MI (Note 14)
		U, T option; V_{CC} = 2.7V to 5.5V	**0**	0.3	**1**	MI (Note 14)
		U, T option; V_{CC} = 1.7V		0.5		MI (Note 14)
Rmatch (Note 22)	DCP to DCP Matching	Any two DCPs at the same tap position with the same terminal voltages	**-2**		**2**	LSB (Note 8)
TCR (Note 18)	Resistance Temperature Coefficient	W option; Wiper register set between 19 hex and 7F hex		170		ppm/°C
		U option; Wiper register set between 19 hex and 7F hex		80		ppm/°C
		T option; Wiper register set between 19 hex and 7F hex		50		ppm/°C

Operating Specifications

V_{CC} = 2.7V to 5.5V, V_{LOGIC} = 1.2V to 5.5V over recommended operating conditions unless otherwise stated.
Boldface limits apply over the operating temperature range, -40°C to +125°C.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 19)	TYP (Note 7)	MAX (Note 19)	UNITS
I_{LOGIC}	V_{LOGIC} Supply Current (Write/Read)	V_{LOGIC} = 5.5V, V_{CC} = 5.5V, f_{SCL} = 400kHz (for I^2C active read and write)			**200**	µA
		V_{LOGIC} = 1.2V, V_{CC} = 1.7V, f_{SCL} = 400kHz (for I^2C active read and write)			**5**	µA
I_{CC}	V_{CC} Supply Current (Write/Read)	V_{LOGIC} = 5.5V, V_{CC} = 5.5V			**18**	µA
		V_{LOGIC} = 1.2V, V_{CC} = 1.7V			**10**	µA
$I_{LOGIC\ SB}$	V_{LOGIC} Standby Current	V_{LOGIC} = V_{CC} = 5.5V, I^2C interface in standby			**1**	µA
		V_{LOGIC} = 1.2V, V_{CC} = 1.7V, I^2C interface in standby			**0.5**	µA
$I_{CC\ SB}$	V_{CC} Standby Current	V_{LOGIC} = V_{CC} = 5.5V, I^2C interface in standby			**2**	µA
		V_{LOGIC} = 1.2V, V_{CC} = 1.7V, I^2C interface in standby			**1.2**	µA
$I_{LOGIC\ SHDN}$	V_{LOGIC} Shutdown Current	V_{LOGIC} = V_{CC} = 5.5V, I^2C interface in standby			**1**	µA
		V_{LOGIC} = 1.2V, V_{CC} = 1.7V, I^2C interface in standby			**0.5**	µA
$I_{CC\ SHDN}$	V_{CC} Shutdown Current	V_{LOGIC} = V_{CC} = 5.5V, I^2C interface in standby			**2**	µA
		V_{LOGIC} = 1.2V, V_{CC} = 1.7V, I^2C interface in standby			**1.2**	µA
I_{LkgDig}	Leakage Current, at Pins A0, A1, A2, SDA, SCL	Voltage at pin from GND to V_{LOGIC}	**-0.4**	<0.1	**0.4**	µA

Operating Specifications

V_{CC} = 2.7V to 5.5V, V_{LOGIC} = 1.2V to 5.5V over recommended operating conditions unless otherwise stated. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 19)	TYP (Note 7)	MAX (Note 19)	UNITS
t_{DCP}	Wiper Response Time	W option; SCL rising edge of the acknowledge bit after data byte to wiper new position from 10% to 90% of the final value.		0.4		µs
		U option; SCL rising edge of the acknowledge bit after data byte to wiper new position from 10% to 90% of the final value.		1.5		µs
		T option; SCL rising edge of the acknowledge bit after data byte to wiper new position from 10% to 90% of the final value.		3.5		µs
tShdnRec	DCP Recall Time from Shutdown Mode	SCL rising edge of the acknowledge bit after ACR data byte to wiper recalled position and RH connection		1.5		µs
V_{CC}, V_{LOGIC} Ramp (Note 20)	V_{CC} , V_{LOGIC} Ramp Rate	Ramp monotonic at any level	**0.01**		**50**	V/ms

Serial Interface Specification

For SCL, SDA, A0, A1, A2 unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 19)	TYP (Note 7)	MAX (Note 19)	UNITS
V_{IL}	Input LOW Voltage		-0.3		0.3 x V_{LOGIC}	V
V_{IH}	Input HIGH Voltage		0.7 x V_{LOGIC}		V_{LOGIC} + 0.3	V
Hysteresis	SDA and SCL Input Buffer Hysteresis	V_{LOGIC} > 2V	0.05 x V_{LOGIC}			V
		V_{LOGIC} < 2V	0.1 x V_{LOGIC}			V
V_{OL}	SDA Output Buffer LOW Voltage	I_{OL} = 3mA, V_{LOGIC} > 2V	0		0.4	V
		I_{OL} = 1.5mA, V_{LOGIC} < 2V			0.2 x V_{LOGIC}	V
C_{pin}	SDA, SCL Pin Capacitance			10		pF
f_{SCL}	SCL Frequency				400	kHz
t_{sp}	Pulse Width Suppression Time at SDA and SCL Inputs	Any pulse narrower than the max spec is suppressed			50	ns
t_{AA}	SCL Falling Edge to SDA Output Data Valid	SCL falling edge crossing 30% of V_{LOGIC}, until SDA exits the 30% to 70% of V_{LOGIC} window			900	ns
t_{BUF}	Time the Bus Must be Free Before the Start of a New Transmission	SDA crossing 70% of V_{LOGIC} during a STOP condition, to SDA crossing 70% of V_{LOGIC} during the following START condition	1300			ns
t_{LOW}	Clock LOW Time	Measured at the 30% of V_{LOGIC} crossing	1300			ns
t_{HIGH}	Clock HIGH Time	Measured at the 70% of V_{LOGIC} crossing	600			ns
$t_{SU:STA}$	START Condition Set-up Time	SCL rising edge to SDA falling edge; both crossing 70% of V_{LOGIC}	600			ns

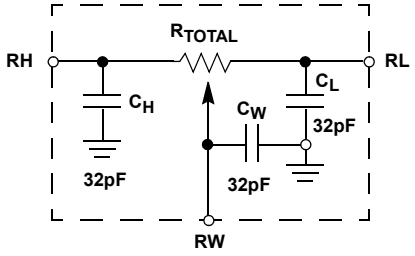
Serial Interface Specification For SCL, SDA, A0, A1, A2 unless otherwise noted. (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 19)	TYP (Note 7)	MAX (Note 19)	UNITS
$t_{HD:STA}$	START Condition Hold Time	From SDA falling edge crossing 30% of V_{LOGIC} to SCL falling edge crossing 70% of V_{LOGIC}	600			ns
$t_{SU:DAT}$	Input Data Set-up Time	From SDA exiting the 30% to 70% of V_{LOGIC} window, to SCL rising edge crossing 30% of V_{LOGIC}	100			ns
$t_{HD:DAT}$	Input Data Hold Time	From SCL falling edge crossing 70% of V_{LOGIC} to SDA entering the 30% to 70% of V_{LOGIC} window	0			ns
$t_{SU:STO}$	STOP Condition Set-up Time	From SCL rising edge crossing 70% of V_{LOGIC}, to SDA rising edge crossing 30% of V_{LOGIC}	600			ns
$t_{HD:STO}$	STOP Condition Hold Time for Read or Write	From SDA rising edge to SCL falling edge; both crossing 70% of V_{LOGIC}	1300			ns
t_{DH}	Output Data Hold Time	From SCL falling edge crossing 30% of V_{LOGIC}, until SDA enters the 30% to 70% of V_{LOGIC} window. I_{OL} = 3mA, V_{LOGIC} > 2V. I_{OL} = 0.5mA, V_{LOGIC} < 2V	0			ns
t_R	SDA and SCL Rise Time	From 30% to 70% of V_{LOGIC}	20 + 0.1 x Cb		250	ns
t_F	SDA and SCL Fall Time	From 70% to 30% of V_{LOGIC}	20 + 0.1 x Cb		250	ns
Cb	Capacitive Loading of SDA or SCL	Total on-chip and off-chip	10		400	pF
$t_{SU:A}$	A2, A1, A0 Setup Time	Before START condition	600			ns
$t_{HD:A}$	A2, A1, A0 Hold Time	After STOP condition	600			ns

NOTES:

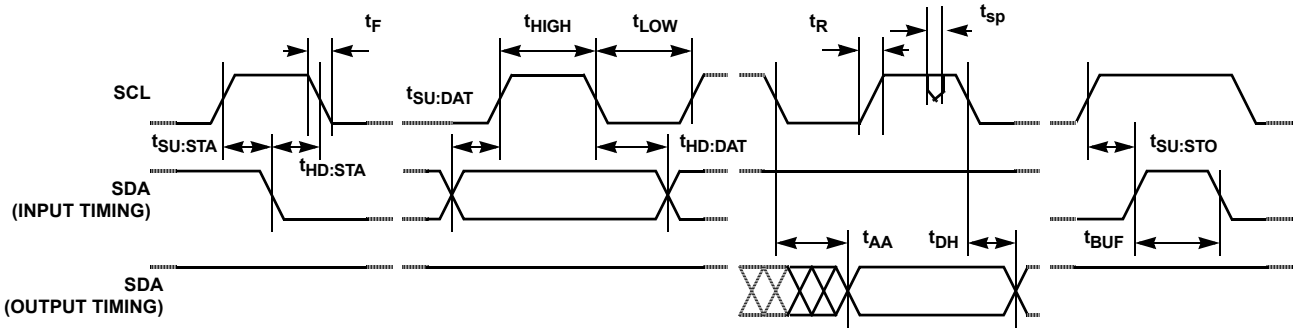
7. Typical values are for T_A = +25°C and 3.3V supply voltages.
8. LSB = $[V(RW)_{127} - V(RW)_0]/127$. $V(RW)_{127}$ and $V(RW)_0$ are V(RW) for the DCP register set to 7F hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
9. ZS error = $V(RW)_0$/LSB.
10. FS error = $[V(RW)_{127} - V_{CC}]$/LSB.
11. DNL = $[V(RW)_i - V(RW)_{i-1}]$/LSB-1, for i = 1 to 127. i is the DCP register setting.
12. INL = $[V(RW)_i - i \bullet LSB - V(RW)_0]$/LSB for i = 1 to 127
13. $TC_V = \frac{Max(V(RW)_i) - Min(V(RW)_i)}{V(RW_i(+25°C))} \times \frac{10^6}{+165°C}$ For i = 8 to 127decimal, T = -40°C to +125°C. Max( ) is the maximum value of the wiper voltage and Min( ) is the minimum value of the wiper voltage over the temperature range.
14. MI = $|RW_{127} - RW_0|/127$. MI is a minimum increment. RW_{127} and RW_0 are the measured resistances for the DCP register set to 7F hex and 00 hex respectively.
15. Roffset = RW_0/MI, when measuring between RW and RL.
    Roffset = RW_{127}/MI, when measuring between RW and RH.
16. RDNL = $(RW_i - RW_{i-1})$/MI -1, for i = 8 to 127.
17. RINL = $[RW_i - (MI \bullet i) - RW_0]$/MI, for i = 8 to 127.
18. $TC_R = \frac{[Max(Ri) - Min(Ri)]}{Ri(+25°C)} \times \frac{10^6}{+165°C}$ for i = 8 to 127, T = -40°C to +125°C. Max( ) is the maximum value of the resistance and Min( ) is the minimum value of the resistance over the temperature range.
19. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
20. It is preferable to ramp up both the V_{LOGIC} and the V_{CC} supplies at the same time. If this is not possible, it is recommended to ramp-up the V_{LOGIC} first followed by the V_{CC}.
21. VMATCH = [V(RWx)i - V(RWy)i]/LSB, for i = 1 to 127, x = 0 to 1 and y = 0 to 1.
22. RMATCH = (RWi,x - RWi,y)/MI, for i = 1 to 127, x = 0 to 1 and y = 0 to 1.

DCP Macro Model

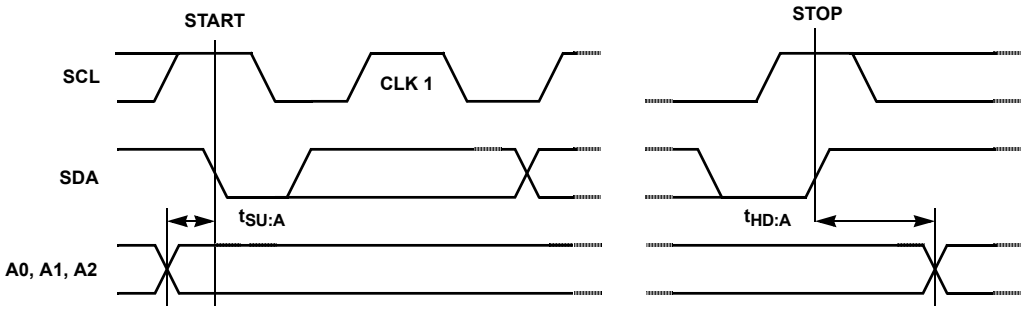


Timing Diagrams

SDA vs SCL Timing



A0, A1, and A2 Pin Timing



Typical Performance Curves

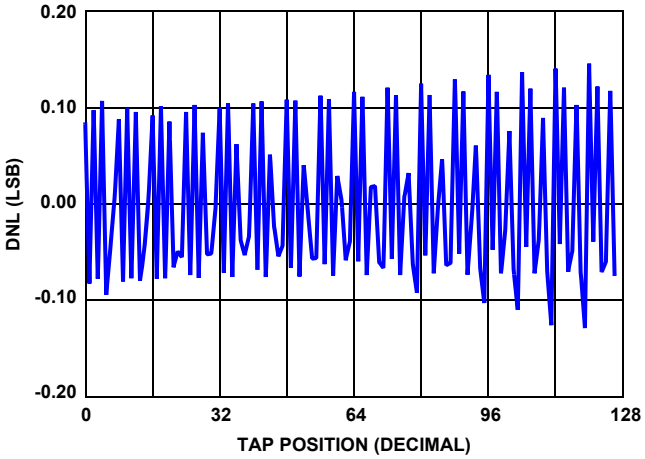


FIGURE 3. 10kΩ DNL vs TAP POSITION, V_{CC} = 3.3V, +25°C

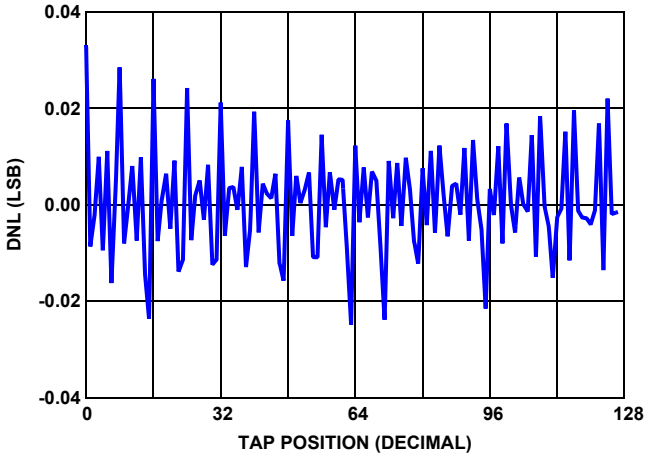


FIGURE 4. 50kΩ DNL vs TAP POSITION, V_{CC} = 3.3V, +25°C

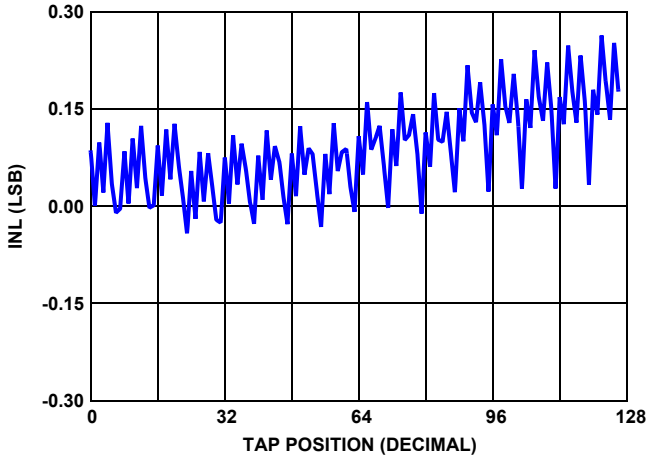


FIGURE 5. 10kΩ INL vs TAP POSITION, V_{CC} = 3.3V, +25°C

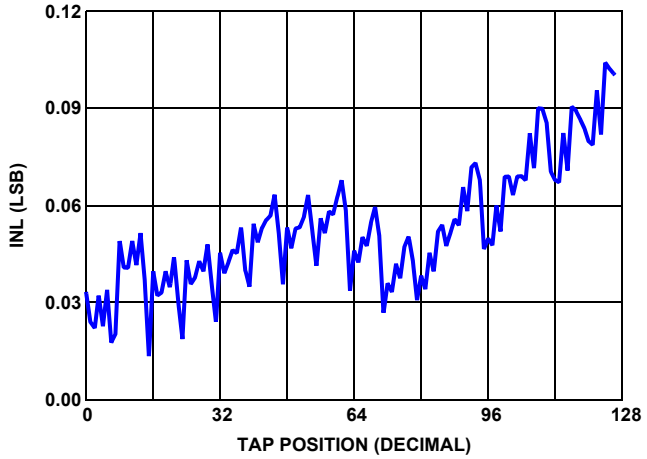


FIGURE 6. 50kΩ INL vs TAP POSITION, V_{CC} = 3.3V, +25°C

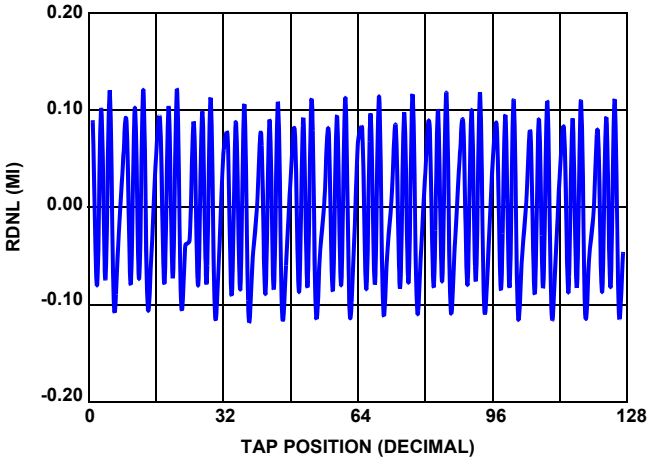


FIGURE 7. 10kΩ RDNL vs TAP POSITION, V_{CC} = 3.3V, +25°C

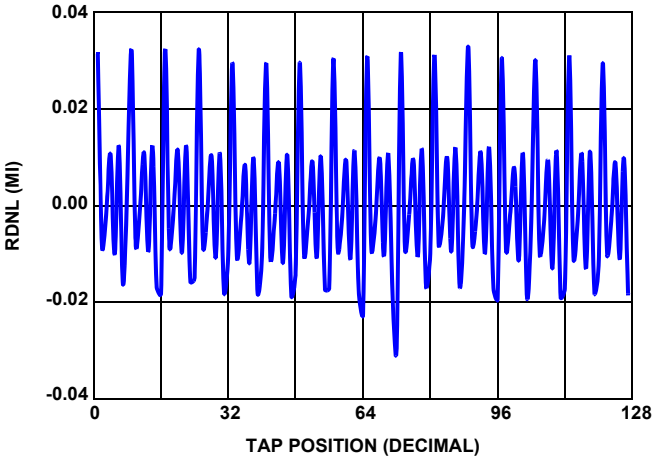


FIGURE 8. 50kΩ RDNL vs TAP POSITION, V_{CC} = 3.3V, +25°C

Typical Performance Curves (Continued)

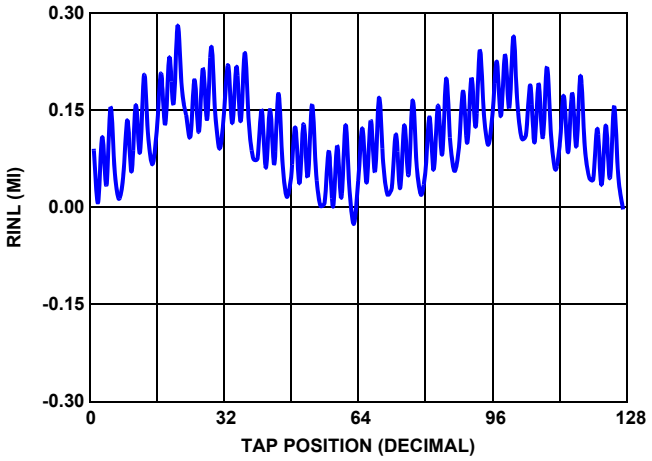


FIGURE 9. 10kΩ RINL vs TAP POSITION, V_{CC} = 3.3V, +25°C

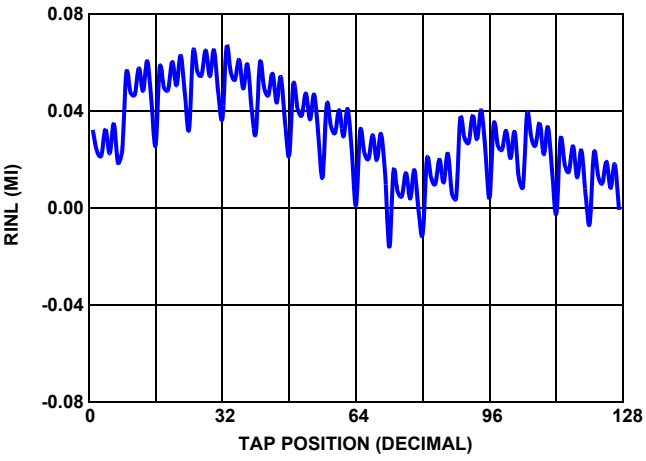


FIGURE 10. 50kΩ RINL vs TAP POSITION, V_{CC} = 3.3V, +25°C

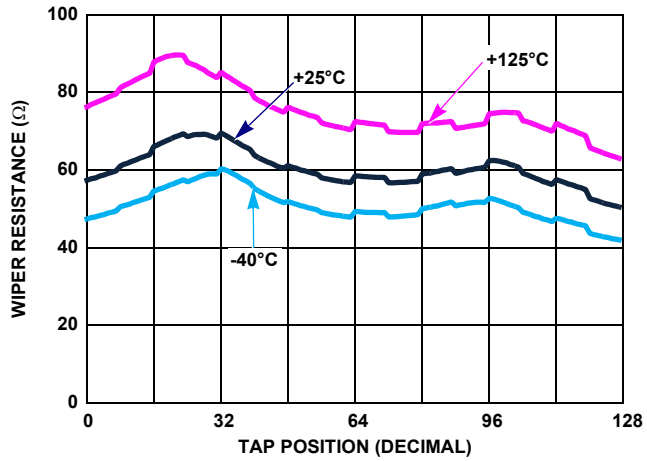


FIGURE 11. 10kΩ WIPER RESISTANCE vs TAP POSITION, V_{CC} = 3.3V

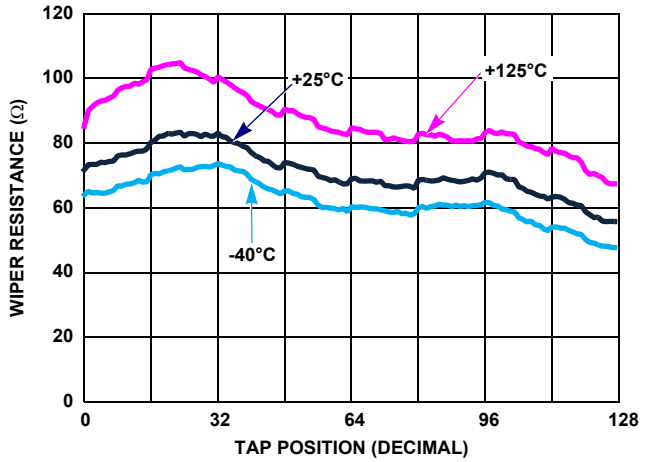


FIGURE 12. 50kΩ WIPER RESISTANCE vs TAP POSITION, V_{CC} = 3.3V

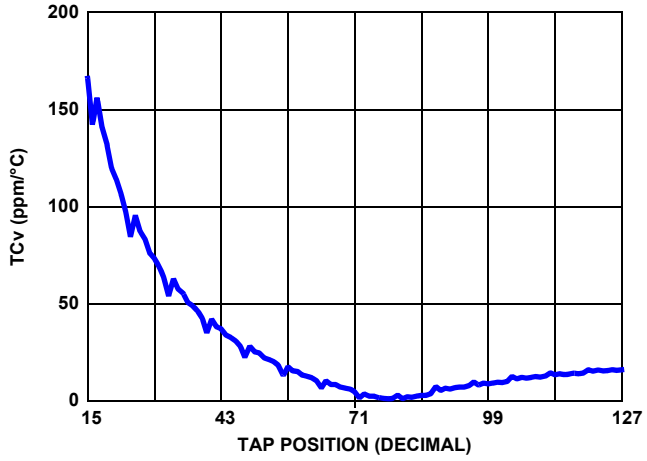


FIGURE 13. 10kΩ TCv vs TAP POSITION, V_{CC} = 3.3V

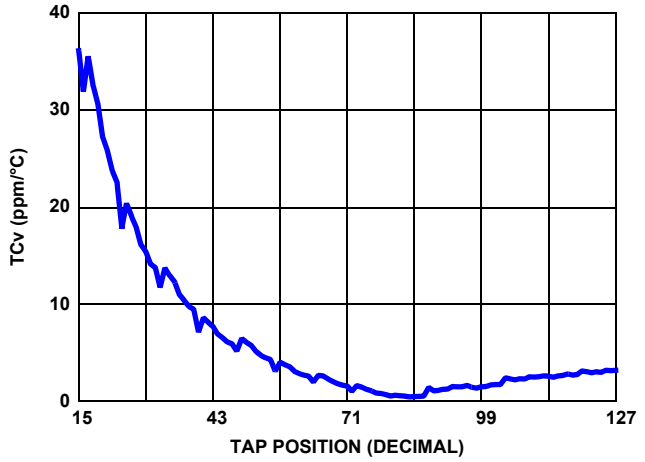


FIGURE 14. 50kΩ TCv vs TAP POSITION, V_{CC} = 3.3V

Typical Performance Curves (Continued)

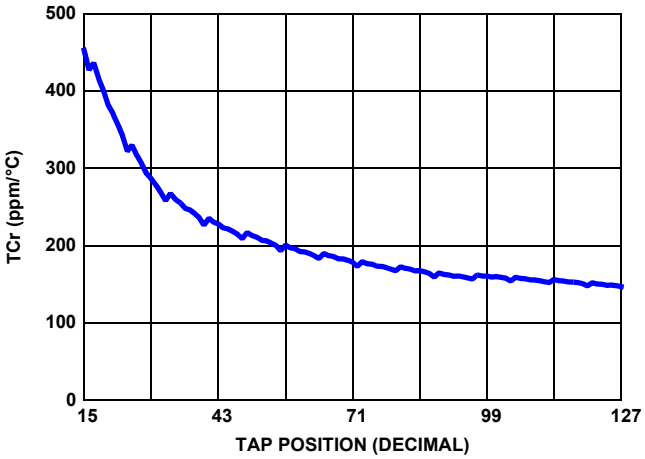


FIGURE 15. 10kΩ TCr vs TAP POSITION

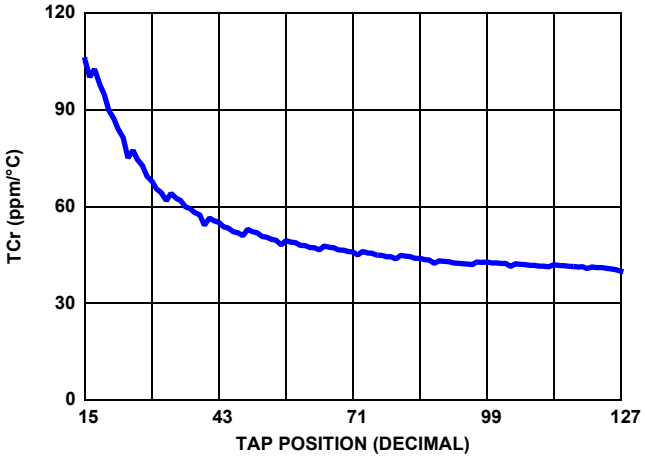


FIGURE 16. 50kΩ TCr vs TAP POSITION, V_{CC} = 3.3V

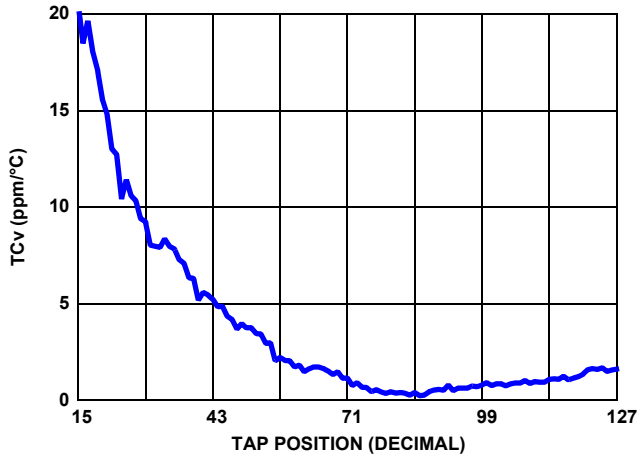


FIGURE 17. 100kΩ TCv vs TAP POSITION, V_{CC} = 3.3V

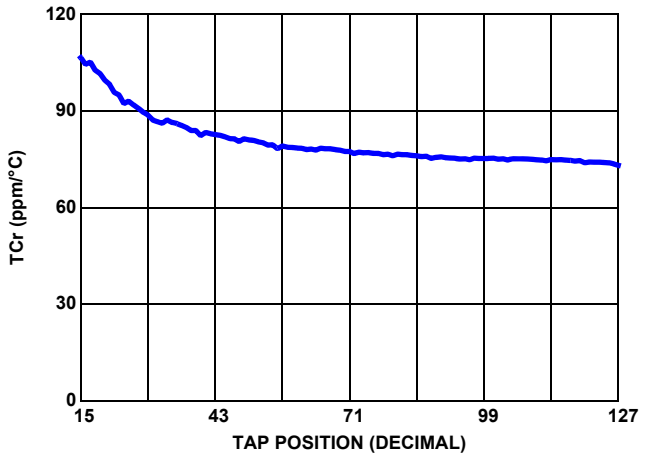


FIGURE 18. 100kΩ TCr vs TAP POSITION, V_{CC} = 3.3V

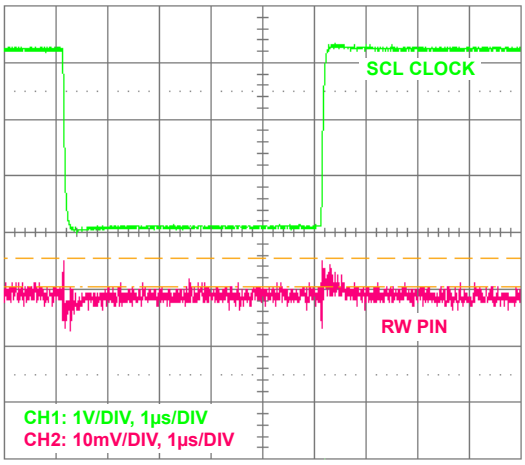


FIGURE 19. WIPER DIGITAL FEED-THROUGH

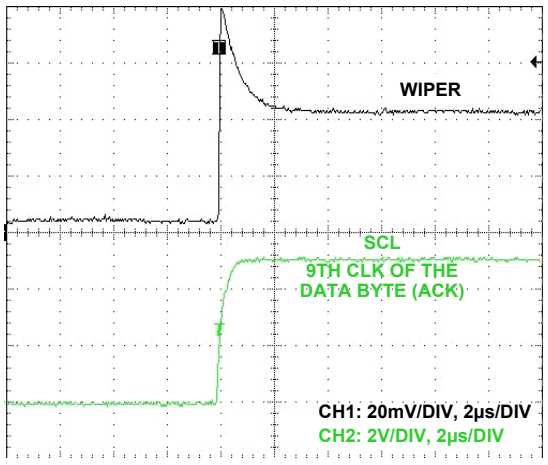


FIGURE 20. WIPER TRANSITION GLITCH

Typical Performance Curves (Continued)

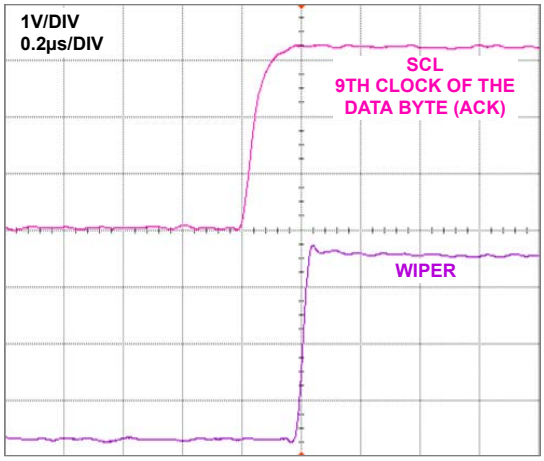


FIGURE 21. WIPER LARGE SIGNAL SETTLING TIME

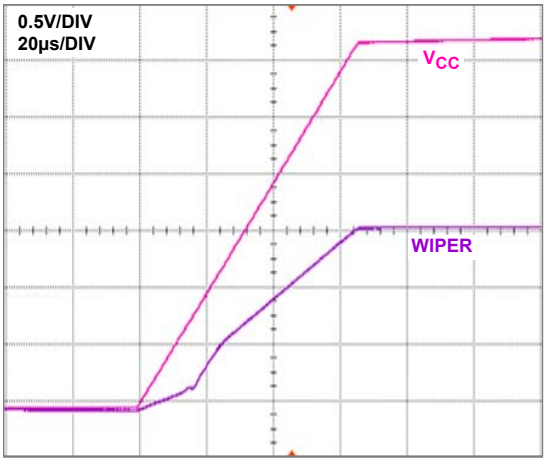


FIGURE 22. POWER-ON START-UP IN VOLTAGE DIVIDER MODE

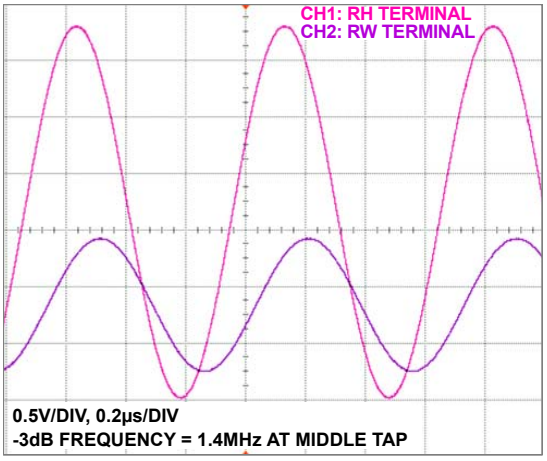


FIGURE 23. 10kΩ -3dB CUT OFF FREQUENCY

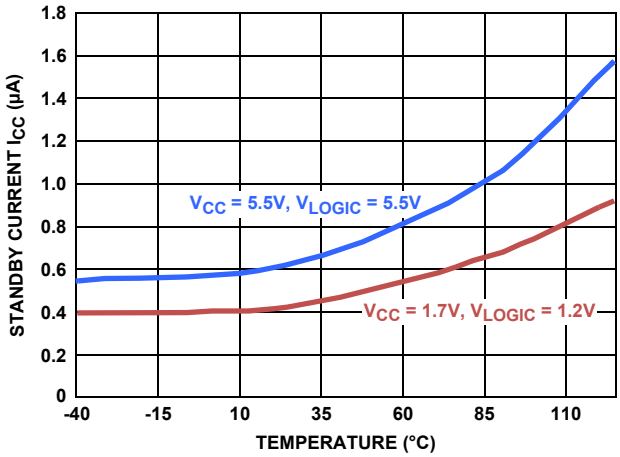


FIGURE 24. STANDBY CURRENT vs TEMPERATURE

Functional Pin Descriptions

Potentiometers Pins

RHi AND RLi

The high (RHi, i = 0, 1) and low (RLi, i = 0, 1) terminals of the ISL23328 are equivalent to the fixed terminals of a mechanical potentiometer. RHi and RLi are referenced to the relative position of the wiper and not the voltage potential on the terminals. With WRi set to 127 decimal, the wiper will be closest to RHi, and with the WR set to 0, the wiper is closest to RLi.

RWi

RWi (i = 0, 1) is the wiper terminal, and it is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the WRi register.

V_{CC}

Power terminal for the potentiometer section analog power source. Can be any value needed to support voltage range of DCP pins, from 1.7V to 5.5V, independent of the V_{LOGIC} voltage.

Bus Interface Pins

SERIAL DATA INPUT/OUTPUT (SDA)

The SDA is a bi-directional serial data input/output pin for I^2C interface. It receives device address, wiper address and data from an I^2C external master device at the rising edge of the serial clock SCL, and it shifts out data after each falling edge of the serial clock.

SDA requires an external pull-up resistor, since it is an open drain input/output.

SERIAL CLOCK (SCL)

This input is the serial clock of the I^2C serial interface. SCL requires an external pull-up resistor, since a master is an open drain output.

DEVICE ADDRESS (A2, A1, A0)

The address inputs are used to set the least significant 3 bits of the 7-bit I^2C interface slave address. A match in the slave address serial data stream must match with the Address input pins in order to initiate communication with the ISL23328. A maximum of eight ISL23328 devices may occupy the I^2C serial bus (see Table 3).

V_{LOGIC}

Digital power source for the logic control section. It supplies an internal level translator for 1.2V to 5.5V serial bus operation. Use the same supply as the I^2C logic source.

Principles of Operation

The ISL23328 is an integrated circuit incorporating two DCPs with its associated registers and an I^2C serial interface providing direct communication between a host and the potentiometer. The resistor array is comprised of individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The electronic switches on the device operate in a "make-before-break" mode when the wiper changes tap positions.

Voltage at any DCP pins, RHi, RLi or RWi, should not exceed V_{CC} level at any conditions during power-up and normal operation.

The V_{LOGIC} pin is the terminal for the logic control digital power source. It should use the same supply as the I^2C logic source which allows reliable communication with a wide range of microcontrollers and is independent from the V_{CC} level. This is extremely important in systems where the master supply has lower levels than DCP analog supply.

DCP Description

Each DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of each DCP are equivalent to the fixed terminals of a mechanical potentiometer (RHi and RLi pins). The RWi pin of the DCP is connected to intermediate nodes, and is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal within the DCP is controlled by an 8-bit volatile Wiper Register (WRi). When the WRi of a DCP contains all zeroes (WRi[7:0] = 00h), its wiper terminal (RWi) is closest to its "Low" terminal (RLi). When the WRi register of a DCP contains all ones (WRi[7:0] = 7Fh), its wiper terminal (RWi) is closest to its "High" terminal (RHi). As the value of the WRi increases from all zeroes (0) to all ones (127 decimal), the wiper moves monotonically from the position closest to RLi to the position closest to RHi. At the same time, the resistance between RWi and RLi increases monotonically, while the resistance between RHi and RWi decreases monotonically.

While the ISL23328 is being powered up, both WR0 and WR1 are reset to 40h (64 decimal), which positions RWi at the center between RLi and RHi.

The WRi can be read or written to directly using the I^2C serial interface as described in the following sections.

Memory Description

The ISL23328 contains three volatile 8-bit registers: Wiper Register WR0, Wiper Register WR1, and Access Control Register (ACR). Memory map of the ISL23328 is shown in Table 1. The Wiper Register WR0 at address 0, contains current wiper position of DCP0; The Wiper Register WR1 at address 1 contains current wiper position of DCP1. The Access Control Register (ACR) at address 10h contains information and control bits described in Table 2.

TABLE 1. MEMORY MAP

ADDRESS (hex)	VOLATILE REGISTER NAME	DEFAULT SETTING (hex)
10	ACR	40
1	WR1	40
0	WR0	40

TABLE 2. ACCESS CONTROL REGISTER (ACR)

BIT #	7	6	5	4	3	2	1	0
NAME/ VALUE	0	$\overline{SHDN}$	0	0	0	0	0	0

Shutdown Function

The $\overline{SHDN}$ bit (ACR[6]) disables or enables shutdown mode for all DCP channels simultaneously. When this bit is 0, i.e., DCP is forced to end-to-end open circuit and RW is connected to RL through a 2kΩ serial resistor as shown in Figure 25. Default value of the $\overline{SHDN}$ bit is 1.

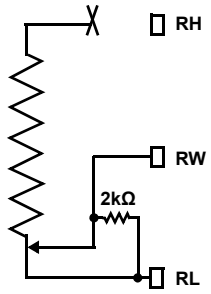


FIGURE 25. DCP CONNECTION IN SHUTDOWN MODE

When the device enters shutdown, all current DCP WR settings are maintained. When the device exits shutdown, the wipers will return to the previous WR settings after a short settling time (see Figure 26).

In shutdown mode, if there is a glitch on the power supply which causes it to drop below 1.3V for more than 0.2 to 0.4µs, the wipers will be RESET to their mid position. This is done to avoid an undefined state at the wiper outputs.

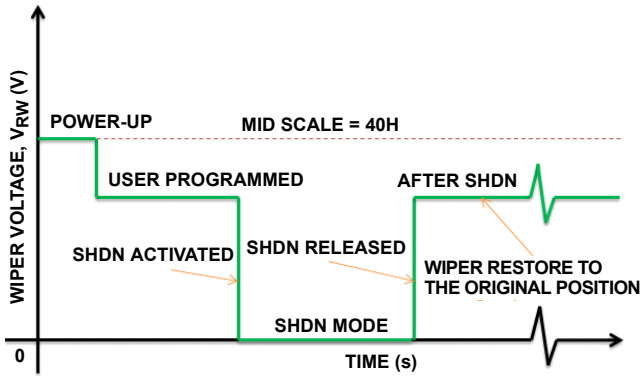


FIGURE 26. SHUTDOWN MODE WIPER RESPONSE

I²C Serial Interface

The ISL23328 supports an I²C bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL23328 operates as a slave device in all applications.

All communication over the I²C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line must change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 27). On power-up of the ISL23328, the SDA pin is in the input mode.

All I²C interface operations must begin with a START condition, which is a HIGH-to-LOW transition of SDA while SCL is HIGH. The ISL23328 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 27). A START condition is ignored during the power-up of the device.

All I²C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 27). A STOP condition at the end of a read operation or at the end of a write operation places the device in its standby mode.

An ACK (Acknowledge) is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 28).

The ISL23328 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL23328 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

A valid Identification Byte contains 1010 as the four MSBs, and the following three bits are matching the logic values present at pins A2, A1 and A0. The LSB is the Read/$\overline{\text{Write}}$ bit. Its value is “1” for a Read operation and “0” for a Write operation (see Table 3).

TABLE 3. IDENTIFICATION BYTE FORMAT

				LOGIC VALUES AT PINS A2, A1 AND A0 RESPECTIVELY			
1	0	1	0	A2	A1	A0	R/$\overline{\text{W}}$
(MSB)							(LSB)

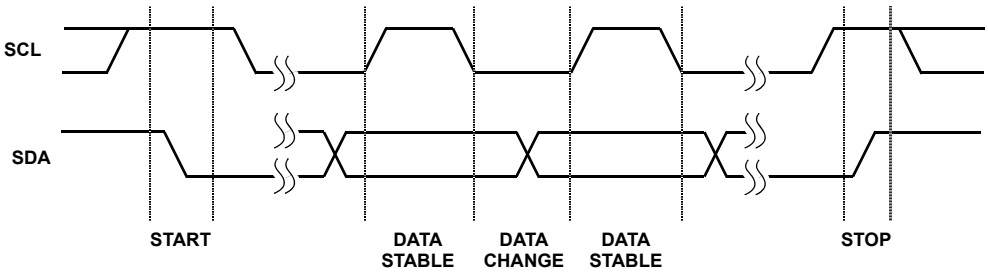


FIGURE 27. VALID DATA CHANGES, START AND STOP CONDITIONS

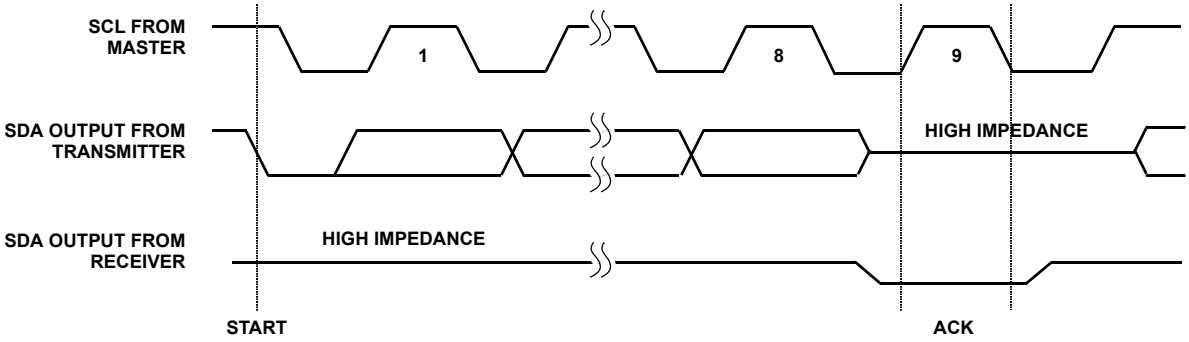


FIGURE 28. ACKNOWLEDGE RESPONSE FROM RECEIVER

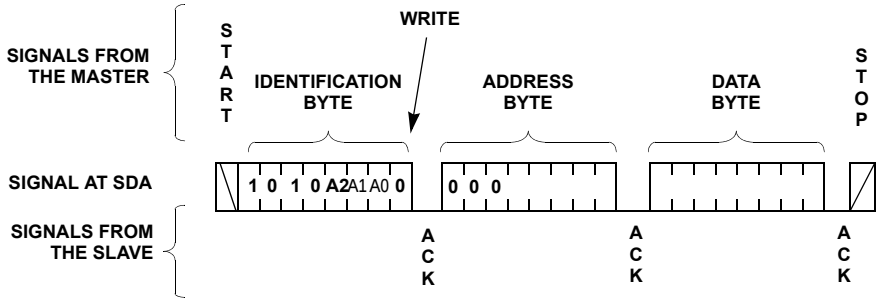


FIGURE 29. BYTE WRITE SEQUENCE

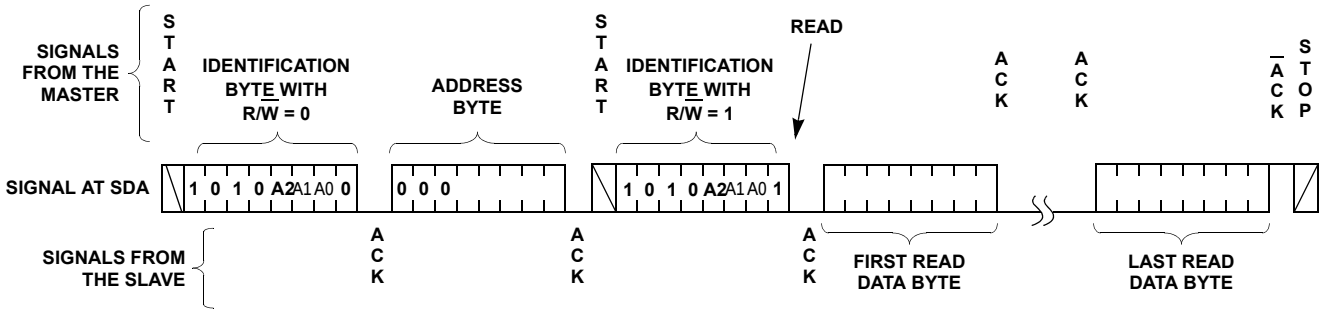


FIGURE 30. READ SEQUENCE

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL23328 responds with an ACK. The data is transferred from I^2C block to the corresponding register at the 9th clock of the data byte and the device enters its standby state (see Figures 28 and 29).

It is possible to perform a sequential Write to all DCP channels via a single Write operation. The command is initiated by sending an additional Data Byte after the first Data byte instead of sending a STOP condition.

Read Operation

A Read operation consists of a three byte instruction followed by one or more Data Bytes (see Figure 30). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/$\overline{W}$ bit set to “0”, an Address Byte, a second START, and a second Identification byte with the R/$\overline{W}$ bit set to “1”. After each of the three bytes, the ISL23328 responds with an ACK; then the ISL23328 transmits Data Byte. The master terminates the read operation issuing a NACK ($\overline{ACK}$) and a STOP condition following the last bit of the last Data Byte (see Figure 30).

Applications Information

V_{LOGIC} Requirements

V_{LOGIC} should be powered continuously during normal operation. In a case where turning V_{LOGIC} OFF is necessary, it is recommended to ground the V_{LOGIC} pin of the ISL23328. Grounding the V_{LOGIC} pin or both V_{LOGIC} and V_{CC} does not affect other devices on the same bus. It is good practice to put a 1µF cap in parallel to 0.1µF as close to the V_{LOGIC} pin as possible.

V_{CC} Requirements and Placement

It is recommended to put a 1µF capacitor in parallel with 0.1µF decoupling capacitor close to the V_{CC} pin.

Wiper Transition

When stepping up through each tap in voltage divider mode, some tap transition points can result in noticeable voltage transients, or overshoot/undershoot, resulting from the sudden transition from a very low impedance “make” to a much higher impedance “break” within a short period of time (<1µs). There are several code transitions such as 0Fh to 10h, 1Fh to 20h,..., 6Fh to 7Fh, which have higher transient glitch. Note, that all switching transients will settle well within the settling time as stated in the datasheet. A small capacitor can be added externally to reduce the amplitude of these voltage transients. However, that will also reduce the useful bandwidth of the circuit, thus may not be a good solution for some applications. It may be a good idea, in that case, to use fast amplifiers in a signal chain for fast recovery.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
September 29, 2015	FN7902.1	Updated Ordering Information Table on page 3. Updated “Product“ section to “About Intersil”. Updated POD L16.2.6x1.8A from rev 5 go rev 6. Change since rev 5: Changed in Note 5 0.30 to 0.25
August 19, 2011	FN7902.0	Initial Release.

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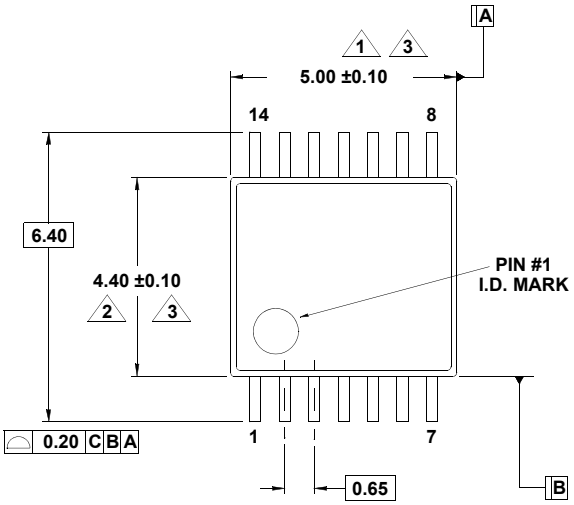
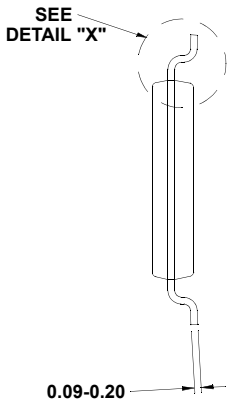
Package Outline Drawing

M14.173

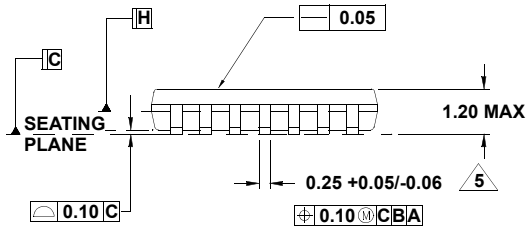
14 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)
Rev 3, 10/09



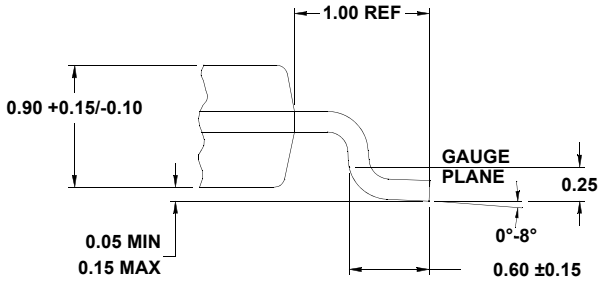
TOP VIEW



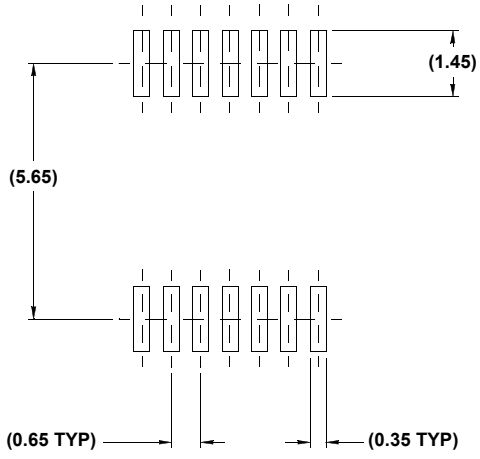
END VIEW



SIDE VIEW



DETAIL "X"

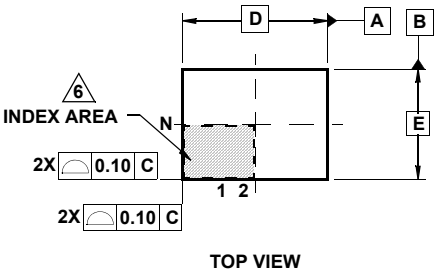


TYPICAL RECOMMENDED LAND PATTERN

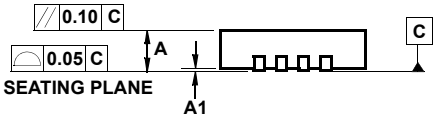
NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.80mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153, variation AB-1.

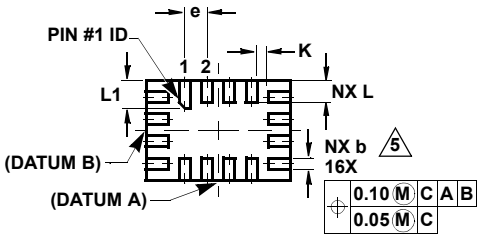
Ultra Thin Quad Flat No-Lead Plastic Package (UTQFN)



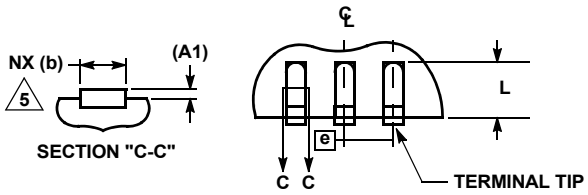
TOP VIEW

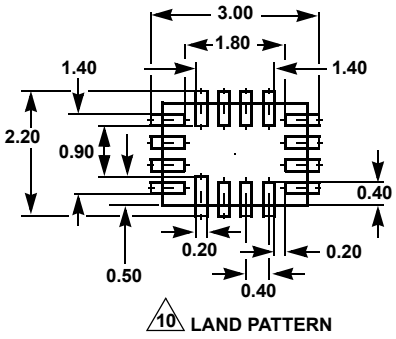


SIDE VIEW



BOTTOM VIEW





L16.2.6x1.8A

16 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.45	0.50	0.55	-
A1	-	-	0.05	-
A3		0.127 REF		-
b	0.15	0.20	0.25	5
D	2.55	2.60	2.65	-
E	1.75	1.80	1.85	-
e		0.40 BSC		-
K	0.15	-	-	-
L	0.35	0.40	0.45	-
L1	0.45	0.50	0.55	-
N		16		2
Nd		4		3
Ne		4		3
θ	0	-	12	4

Rev. 6 1/14

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on D and E side, respectively.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.25mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Maximum package warpage is 0.05mm.
8. Maximum allowable burrs is 0.076mm in all directions.
9. JEDEC Reference MO-255.
10. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.