74AHC273; 74AHCT273

Octal D-type flip-flop with reset; positive-edge trigger

Rev. 03 — 13 May 2008 Product data sheet

1. General description

The 74AHC273; 74AHCT273 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7-A.

The 74AHC273; 74AHCT273 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs.

The common clock (CP) and master reset ($\overline{MR}$) inputs, load and reset (clear) all flip-flops simultaneously.

The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Qn) of the flip-flop.

All outputs will be forced LOW, independent of clock or data inputs, by a LOW on the $\overline{MR}$ input.

The device is useful for applications where only the true output is required and the clock and master reset are common to all storage elements.

2. Features

- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Inputs accept voltages higher than V_{CC}
- Ideal buffer for MOS microcontroller or memory
- Common clock and master reset
- Related product versions:
  - 74AHC377; 74AHCT377 for clock enable version
  - 74AHC373; 74AHCT373 for transparent latch version
  - 74AHC374; 74AHCT374 for 3-state version
- Input levels:
  - For 74AHC273: CMOS level
  - For 74AHCT273: TTL level
- ESD protection:
  - HBM EIA/JESD22-A114E exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
  - CDM EIA/JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC273				
74AHC273D	–40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74AHC273PW	–40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74AHC273BQ	–40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1
74AHCT273				
74AHCT273D	–40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74AHCT273PW	–40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74AHCT273BQ	–40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

4. Functional diagram

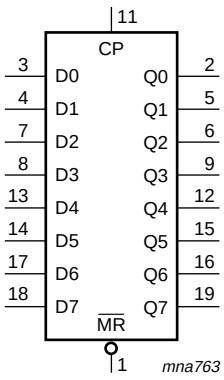


Fig 1. Logic symbol

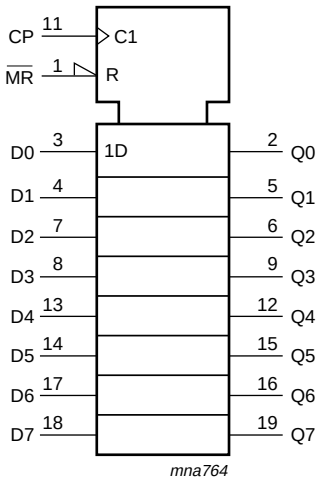


Fig 2. IEC logic symbol

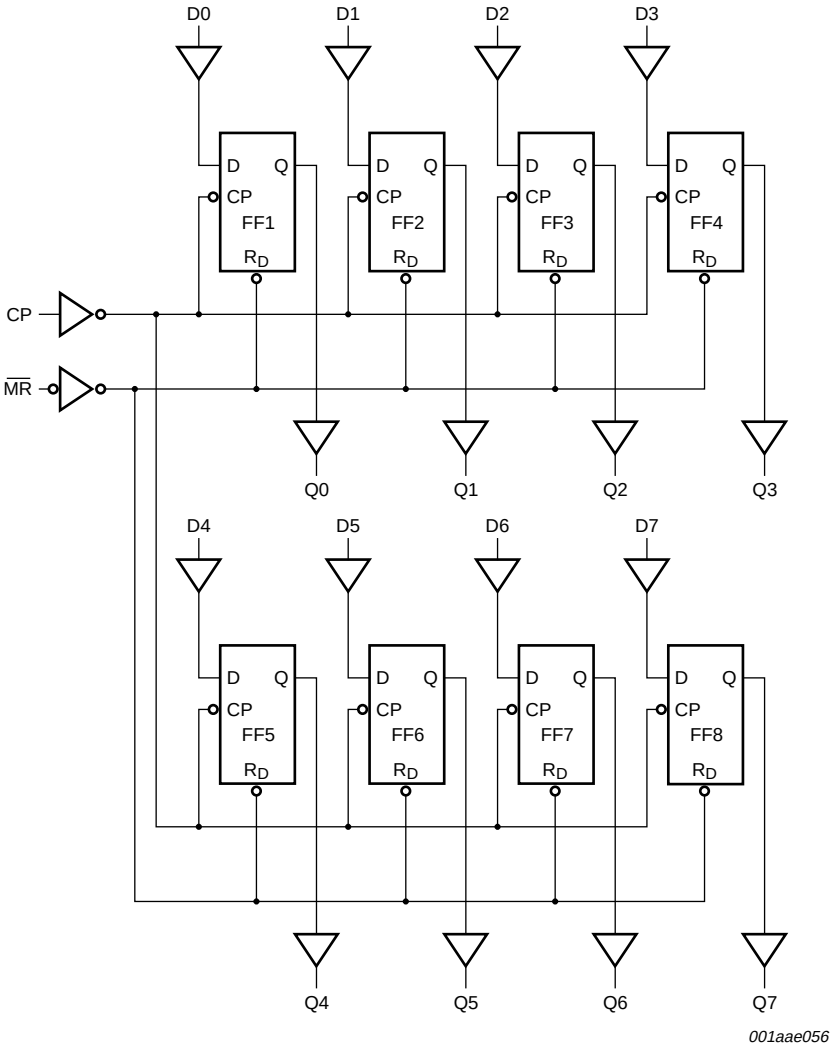


Fig 3. Logic diagram

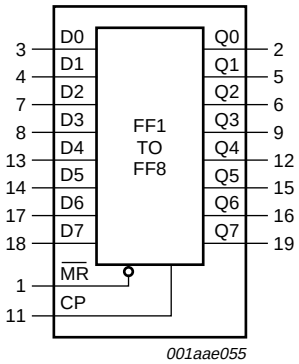


Fig 4. Functional diagram

5. Pinning information

5.1 Pinning

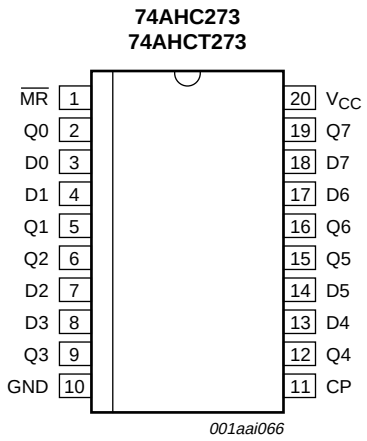
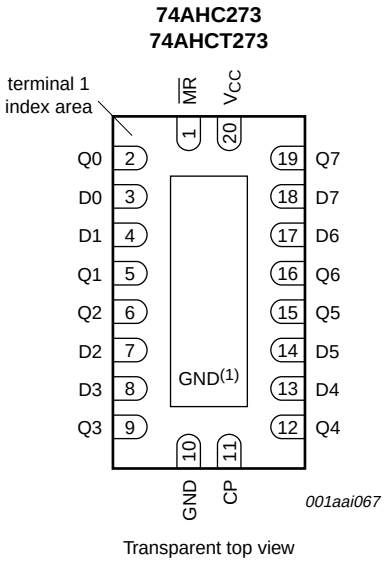


Fig 5. Pin configuration SO20 and TSSOP20



Transparent top view

(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig 6. Pin configuration DHVQFN20

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{MR}$	1	master reset input (active LOW)
Q0	2	flip-flop output
D0	3	data input
D1	4	data input
Q1	5	flip-flop output
Q2	6	flip-flop output
D2	7	data input
D3	8	data input
Q3	9	flip-flop output
GND	10	ground (0 V)
CP	11	clock input (LOW-to-HIGH edge-triggered)
Q4	12	flip-flop output
D4	13	data input
D5	14	data input
Q5	15	flip-flop output
Q6	16	flip-flop output

Table 2. Pin description *...continued*

Symbol	Pin	Description
D6	17	data input
D7	18	data input
Q7	19	flip-flop output
V_{CC}	20	supply voltage

6. Functional description

Table 3. Function table[1]

Operating mode	Control		Input	Output
	$\overline{MR}$	CP	Dn	Qn
Reset (clear)	L	X	X	L
Load '1'	H	↑	h	H
Load '0'	H	↑	l	L

[1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;
↑ = LOW-to-HIGH;
X = don't care.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
V_I	input voltage			–0.5	+7.0	V
I_{IK}	input clamping current	$V_I < –0.5$ V	[1]	–20	-	mA
I_{OK}	output clamping current	$V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	–20	+20	mA
I_O	output current	$V_O = –0.5$ V to ($V_{CC} + 0.5$ V)		–25	+25	mA
I_{CC}	supply current			-	+75	mA
I_{GND}	ground current			–75	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = –40$ °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO20 packages: above 70 °C the value of P_{tot} derates linearly at 8 mW/K.
For TSSOP20 packages: above 60 °C the value of P_{tot} derates linearly at 5.5 mW/K.
For DHVQFN20 packages: above 60 °C the value of P_{tot} derates linearly at 4.5 mW/K.

8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74AHC273						
V_{CC}	supply voltage		2.0	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 3.0 V to 3.6 V	-	-	100	ns/V
		V_{CC} = 4.5 V to 5.5 V	-	-	20	ns/V
74AHCT273						
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 4.5 V to 5.5 V	-	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC273										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V_{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V_{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V_{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V_{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = –50 µA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = –50 µA; V_{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I_O = –50 µA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –4.0 mA; V_{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I_O = –8.0 mA; V_{CC} = 4.5 V	3.94	-	-	3.80	-	3.70	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 50 µA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 50 µA; V_{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 50 µA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I_O = 8.0 mA; V_{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V

Table 6. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	4.0	-	40	-	80	µA
C_I	input capacitance		-	3	10	-	10	-	10	pF
C_O	output capacitance		-	4	-	-	-	-	-	pF
74AHCT273										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		I_O = –50 µA	4.4	-	-	4.4	-	4.4	-	V
		I_O = –8.0 mA	3.94	-	-	3.80	-	3.70	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		I_O = 50 µA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	4.0	-	40	-	80	µA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC}$ – 2.1 V; other pins at V_{CC} or GND; I_O = 0 A; V_{CC} = 4.5 V to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C_I	input capacitance		-	3	10	-	10	-	10	pF
C_O	output capacitance		-	4	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 10.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
74AHC273										
t_{pd}	propagation delay	CP to Qn; see Figure 7 [2]								
		V_{CC} = 3.0 V to 3.6 V								
		C_L = 15 pF	-	6.0	13.6	1.0	16.0	1.0	17.0	ns
		C_L = 50 pF	-	8.6	17.1	1.0	19.5	1.0	21.5	ns
		V_{CC} = 4.5 V to 5.5 V								
		C_L = 15 pF	-	4.2	9	1.0	10.5	1.0	11.5	ns
		C_L = 50 pF	-	6.0	11.0	1.0	12.5	1.0	14.0	ns
		$\overline{MR}$ to Qn; see Figure 8 [3]								
		V_{CC} = 3.0 V to 3.6 V								
		C_L = 15 pF	-	5.1	13.6	1.0	16.0	1.0	17.0	ns
		C_L = 50 pF	-	7.3	17.1	1.0	19.5	1.0	21.5	ns
		V_{CC} = 4.5 V to 5.5 V								
		C_L = 15 pF	-	3.7	8.5	1.0	10.0	1.0	11.0	ns
		C_L = 50 pF	-	5.3	10.5	1.0	12.0	1.0	13.5	ns
f_{max}	maximum frequency	see Figure 7								
		V_{CC} = 3.0 V to 3.6 V								
		C_L = 15 pF	75	120	-	65	-	65	-	MHz
		C_L = 50 pF	50	75	-	45	-	45	-	MHz
		V_{CC} = 4.5 V to 5.5 V								
		C_L = 15 pF	120	165	-	100	-	100	-	MHz
		C_L = 50 pF	80	110	-	70	-	70	-	MHz
t_W	pulse width	CP HIGH or LOW; see Figure 7								
		V_{CC} = 3.0 V to 3.6 V	5.0	-	-	6.5	-	6.5	-	ns
		V_{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
		$\overline{MR}$ LOW; see Figure 8								
		V_{CC} = 3.0 V to 3.6 V	5.0	-	-	6.0	-	6.0	-	ns
		V_{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
t_{su}	set-up time	Dn to CP; see Figure 9								
		V_{CC} = 3.0 V to 3.6 V	3.0	-	-	3.0	-	3.0	-	ns
		V_{CC} = 4.5 V to 5.5 V	3.0	-	-	3.0	-	3.0	-	ns
t_h	hold time	Dn to CP; see Figure 9								
		V_{CC} = 3.0 V to 3.6 V	1.0	-	-	1.0	-	1.0	-	ns
		V_{CC} = 4.5 V to 5.5 V	1.0	-	-	1.0	-	1.0	-	ns

Table 7. Dynamic characteristics *…continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 10.

Symbol	Parameter	Conditions		25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	Min	Max	
t_{rec}	recovery time	$\overline{MR}$ to CP; see Figure 8									
		V_{CC} = 3.0 V to 3.6 V		2.5	-	-	2.5	-	2.5	-	ns
		V_{CC} = 4.5 V to 5.5 V		2.0	-	-	2.0	-	2.0	-	ns
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC}	[4]	-	14	-	-	-	-	-	pF
74AHCT273; V_{CC} = 4.5 V to 5.5 V											
t_{pd}	propagation delay	CP to Qn; see Figure 7	[2]								
		C_L = 15 pF		-	4.0	7.5	1.0	8.8	1.0	9.5	ns
		C_L = 50 pF		-	5.8	9.2	1.0	10.5	1.0	11.5	ns
		$\overline{MR}$ to Qn; see Figure 8	[3]								
		C_L = 15 pF		-	3.9	10.0	1.0	11.6	1.0	12.5	ns
		C_L = 50 pF		-	5.6	11.0	1.0	12.6	1.0	14.0	ns
f_{max}	maximum frequency	see Figure 7									
		C_L = 15 pF		75	120	-	65	-	65	-	MHz
		C_L = 50 pF		50	75	-	45	-	45	-	MHz
t_W	pulse width	CP HIGH or LOW; see Figure 7		5.0	-	-	6.5	-	6.5	-	ns
		$\overline{MR}$ LOW; see Figure 8		5.0	-	-	6.0	-	6.0	-	ns
t_{su}	set-up time	Dn to CP; see Figure 9		3.0	-	-	3.0	-	3.0	-	ns
t_h	hold time	Dn to CP; see Figure 9		1.0	-	-	1.0	-	1.0	-	ns
t_{rec}	recovery time	$\overline{MR}$ to CP; see Figure 8		2.5	-	-	2.5	-	2.5	-	ns
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC}	[4]	-	18	-	-	-	-	-	pF

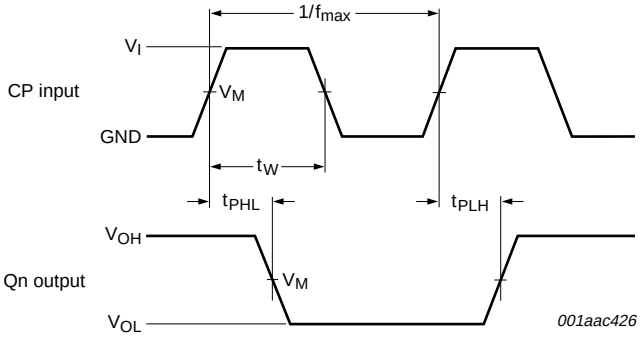
[1] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] t_{pd} is the same as t_{PHL} only.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

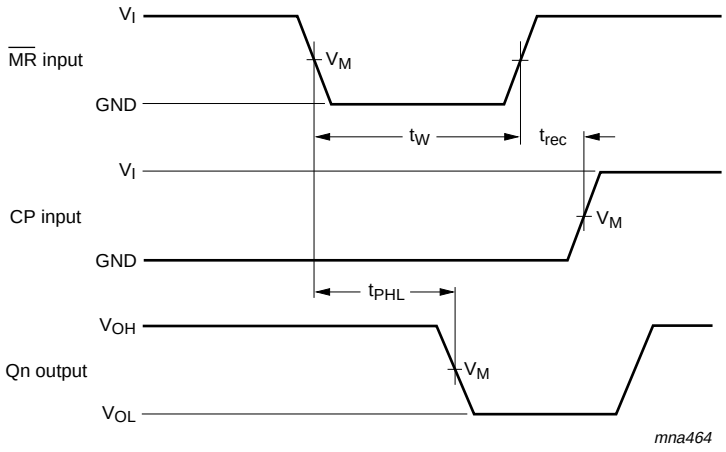
11. Waveforms



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

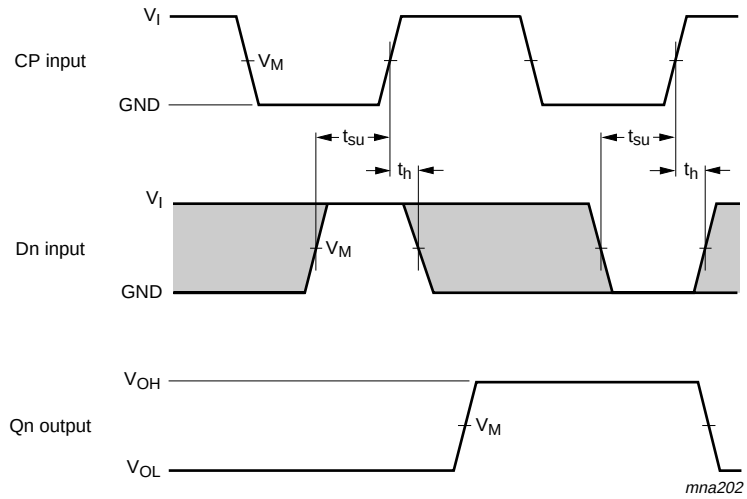
Fig 7. Clock pulse width, maximum frequency and input to output propagation delays



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 8. Master reset pulse width, recovery time and propagation delay



Measurement points are given in Table 8.

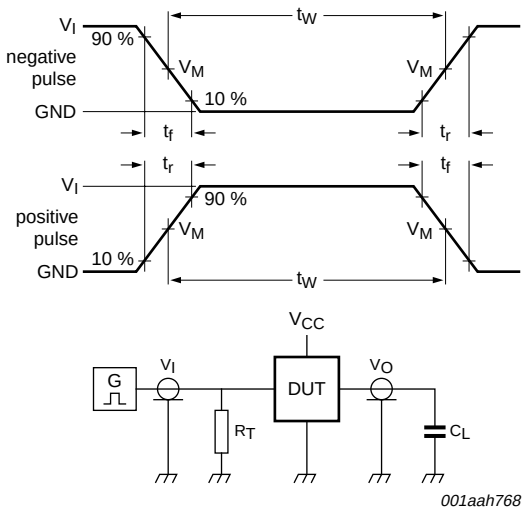
The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 9. Data set-up and hold times

Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74AHC273	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74AHCT273	1.5 V	$0.5 \times V_{CC}$



Test data is given in Table 9.

Definitions test circuit:

R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

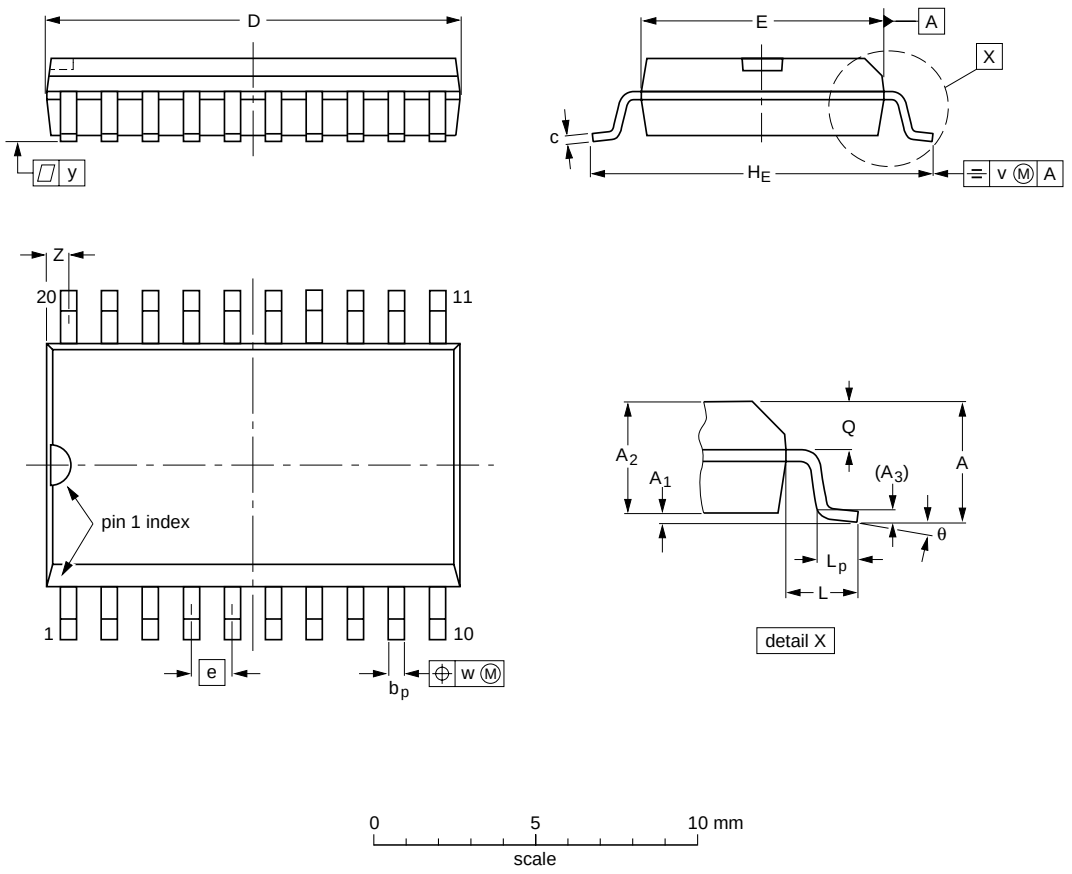
Fig 10. Load circuitry for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74AHC273	V_{CC}	≤ 3.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}
74AHCT273	3.0 V	≤ 3.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

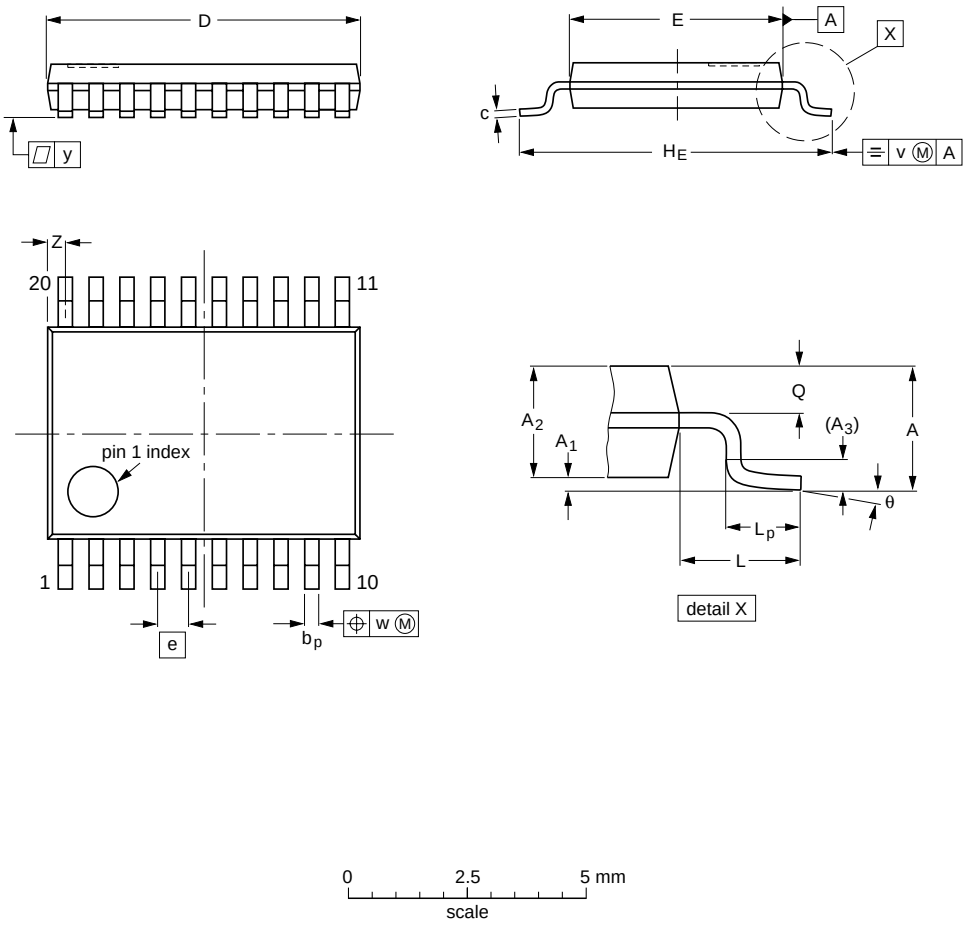
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

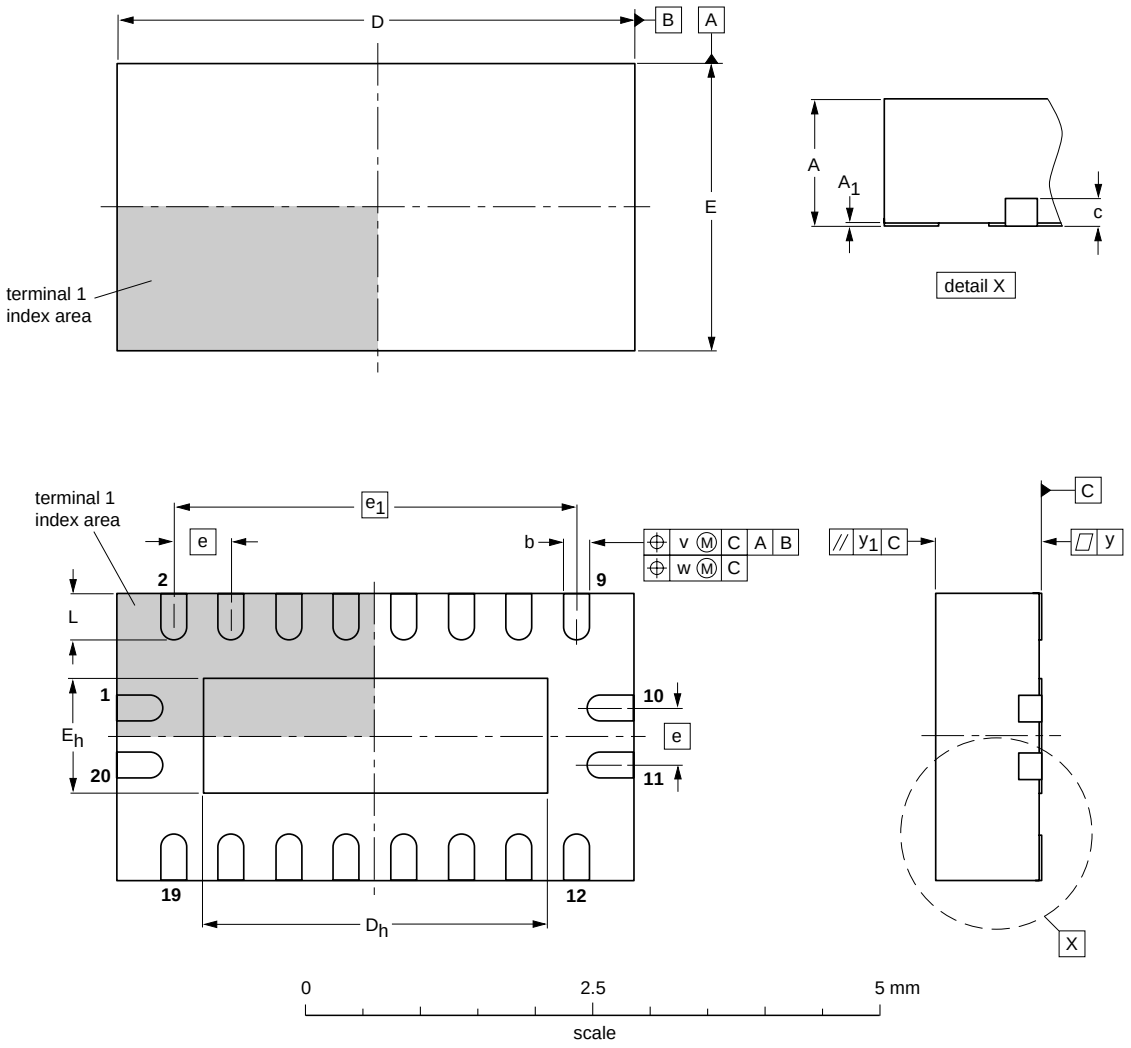
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig 12. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm **SOT764-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	4.6 4.4	3.15 2.85	2.6 2.4	1.15 0.85	0.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT764-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 13. Package outline SOT764-1 (DHVQFN20)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model
MOS	Metal-Oxide Semiconductor

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT273_3	20080513	Product data sheet	-	74AHC_AHCT273_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 6: the conditions for input leakage current have been changed.			
74AHC_AHCT273_2	20030721	Product specification	-	74AHC_AHCT273_1
74AHC_AHCT273_1	19990901	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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17. Contents

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Date of release: 13 May 2008