MAX16812

Integrated High-Voltage LED Driver with Analog and PWM Dimming Control

General Description

The MAX16812 is a peak-current-mode LED driver with an integrated 0.2Ω power MOSFET designed to control the current in a single string of high-brightness LEDs (HB LEDs). The MAX16812 can be used in multiple converter topologies such as buck, boost, or buck-boost. The MAX16812 operates over a 5.5V to 76V wide supply voltage range.

The MAX16812 features a low-frequency, wide-range brightness adjustment (100:1), analog and PWM dimming control input, as well as a resistor-programmable EMI suppression circuitry to control the rise and fall times of the internal switching MOSFET. A high-side LED current-sense amplifier and a dimming MOSFET driver are also included, simplifying the design and reducing the total component count.

The MAX16812 uses peak-current-mode control, adjustable slope compensation that allows for additional design flexibility. The device has two current regulation loops. The first loop controls the internal switching MOSFET peak current, while the second current regulation loop controls the LED current. Switching frequency can be adjusted from 125kHz to 500kHz.

Additional features include adjustable UVLO, soft-start, external enable/disable input, thermal shutdown, a 1.238V 1% accurate buffered reference, and an on-chip oscillator. An internal 5.2V linear regulator supplies up to 20mA to power external devices.

The MAX16812 is available in a thermally enhanced 5mm x 5mm, 28-pin TQFN-EP package and is specified over the automotive -40°C to +125°C temperature range.

Applications

- Architectural and Industrial Lighting

Typical Application Circuit and Pin Configuration appear at end of data sheet.

Features

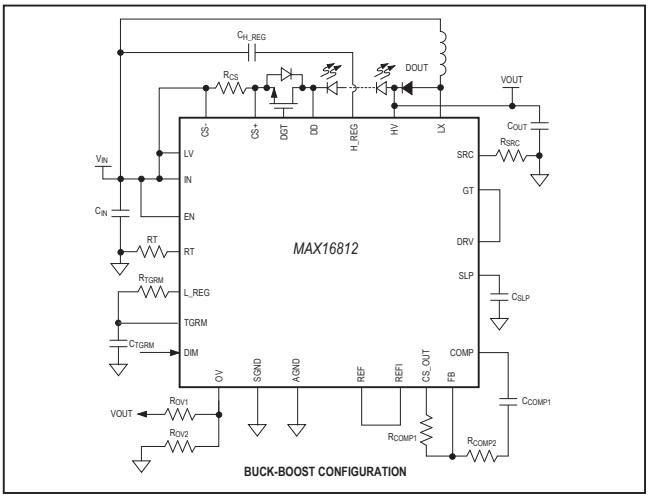
- Integrated 76V, 0.2Ω (typ) Power MOSFET
- 5.5V to 76V Wide Input Range
- Adjustable LED Current with 5% Accuracy
- Floating Differential LED Current-Sense Amplifier
- Floating Dimming N-Channel MOSFET Driver
- PWM LED Dimming with:
  - PWM Control Signal
  - Analog Control Signal
  - Chopped V_{IN} Input
- Peak-Current-Mode Control
- 125kHz to 500kHz Adjustable Switching Frequency
- Adjustable UVLO and Soft-Start
- Output Overvoltage Protection
- 5µs LED Current Rise/Fall Times During Dimming Minimize EMI
- Overtemperature and Short-Circuit Protection

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX16812ATI+	-40°C to +125°C	28 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Simplified Diagram



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Absolute Maximum Ratings

(All voltages are referenced to AGND, unless otherwise noted.)
SGND .....-0.3V to +0.3V
IN, EN, LX, DIM.....-0.3V to +80V
L_REG, GT, DRV .....-0.3V to +6V
RT, REF, REFI, CS_OUT, FB, COMP, SRC,
SLP, TGRM, OV .....-0.3V to +6V
LV, HV, CS-, CS+, DGT, DD, H_REG .....-0.3V to +80V
CS+, DGT, H_REG to LV .....-0.3V to +12V
CS- to LV .....-0.3V to +0.3V
CS+ to CS-.....-0.3V to +12V
DD to LV .....-1V to +80V
Maximum Current into Any Pin (except LX, SRC) .....±20mA
Maximum Current into LX and SRC.....+2A
Continuous Power Dissipation (T_A = +70°C)
28-Pin TQFN 5mm x 5mm
(derate 34.65mW/°C* above +70°C).....2759mW
Operating Temperature Range..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

*As per JEDEC51 standard (multilayer board).

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{IN} = V_{EN} = 12V, C_{L_REG} = 3.3µF, C_{H_REG} = 1µF, C_{REF} = 47nF, V_{TGRM} = 0V, R_{SRC} = 0.2Ω, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}		5.5		76.0	V
Quiescent Supply	I_Q	V_{TGRM} = 1V, V_{DIM} = 0V	0.3		2.5	mA
Shutdown Supply Current	I_{SHDN}	V_{EN} ≤ 300mV		20	45	µA
Internal MOSFET On-Resistance	R_{DSON}	I_{LX} = 1A, V_{IN} > 10V, V_{GT} = V_{DRV} = 5V		0.2	0.4	Ω
Output Current Accuracy	I_{LED}	I_{LED} = 350mA, R_{CS} = 1Ω	-5		+5	%
Peak Switch Current Limit	I_{LXLIM}		2.6	3.1	3.6	A
Hiccup Switch Current				6		A
Switch Leakage Current	I_{LXLEAK}	V_{EN} = 0V, V_{LX} = 76V, V_{GT} = 0V		1	10	µA
UNDERVOLTAGE LOCKOUT						
IN Undervoltage Lockout	UVLO	V_{IN} rising	4.6	4.9	5.3	V
UVLO Hysteresis				100		mV
EN Threshold Voltage	V_{EN_THUP}	V_{EN} rising	1.2	1.38	1.6	V
EN Hysteresis				100		mV
REFERENCE (REF) AND LOW-SIDE LINEAR REGULATOR (L_REG)						
Startup Response Time	t_{POR}	V_{IN} or V_{EN} rising		50		µs
Reference Voltage	V_{REF}	I_{REF} = 10µA	1.190	1.238	1.288	V
Reference Soft-Start Charging Current	I_{REF_SLEW}	V_{REF} = 0V	25	40	60	µA
L_REG Supply Voltage		V_{IN} = 7.5V, I_{L_REG} = 1mA	4.9	5.2	5.5	V
L_REG Load Regulation		I_{L_REG} = 20mA			20	Ω
L_REG Dropout Voltage		I_{L_REG} = 25mA		400		mV

Electrical Characteristics (continued)

(V_{IN} = V_{EN} = 12V, CL_REG = 3.3µF, C_{H_REG} = 1µF, C_{REF} = 47nF, V_{TGRM} = 0V, R_{SRC} = 0.2Ω, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PWM COMPARATOR						
COMP Input Leakage Current	I_{LKCOMP}	V_{COMP} = 1V, V_{SRC} = 0.5V, V_{TGRM} = 1V, V_{DIM} = 0.5V	-0.10		+0.10	µA
SRC Input Leakage Current	I_{LKSRC}	V_{COMP} = 0V, V_{SRC} = 0.5V, V_{TGRM} = 0V, V_{DIM} = 0.5V	-5		+5	µA
Comparator Offset Voltage	$V_{OS(EA)}$	(V_{COMP} - V_{SRC}) = V_{OS}		860		mV
Input Voltage Range	V_{SRC}	V_{COMP} = V_{SRC} + 860mV	0		1.23	V
Propagation Delay	t_{PD}	50mV overdrive		100		ns
ERROR AMPLIFIER						
FB Input Current		V_{FB} = 1V, V_{REFI} = 1.2V	-100		+100	nA
REFI Input Current		V_{FB} = 1V, V_{REFI} = 1V	-100		+100	nA
Error-Amplifier Offset Voltage	V_{OS}	V_{FB} = V_{COMP} = 1.2V	-23		+23	mV
Input Common-Mode Range		V_{FB} = (V_{COMP} - 0.9V)	0		1.5	V
Source Current	I_{COMP}	(V_{REFI} - V_{FB}) ≥ 0.5V	300			µA
Sink Current		(V_{FB} - V_{REFI}) ≥ 0.5V	80			µA
COMP Clamp Voltage	V_{COMP}	V_{REF} = 1.2V, V_{FB} = 0V	1.20		2.56	V
DC Gain				72		dB
Unity-Gain Bandwidth				0.8		MHz

Electrical Characteristics

(V_{IN} = V_{EN} = 12V, C_{L_REG} = 3.3µF, C_{H_REG} = 1µF, C_{REF} = 47nF, V_{TGRM} = 0V, R_{SRC} = 0.2Ω, R_{CS} = 1Ω, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HIGH-SIDE UNDERVOLTAGE LOCKOUT AND LINEAR REGULATOR (H_REG) ((V_{HV} - V_{LV}) = 21V)						
H_REG Input-Voltage Threshold		V_{H_REG} is rising	3.60	3.887	4.20	V
H_REG Supply Voltage		I_{H_REG} = 0	4.75	5	5.40	V
H_REG Load Regulation		I_{H_REG} = 0 to 3mA			80	Ω
Dropout Voltage		I_{H_REG} = 5mA		820		mV
HIGH-SIDE CURRENT-SENSE AMPLIFIERS (V_{HV} - V_{LV}) = 21V						
CS- Input Bias Current	I_{CS-}	V_{CS-} = V_{LV}, (V_{CS+} - V_{CS-}) = -0.1V			500	µA
CS+ Input Bias Current	I_{CS+}	V_{CS-} = V_{LV}, (V_{CS+} - V_{CS-}) = 0.1V	-1		+1	µA
Input Voltage Range		V_{CS-} = V_{LV}	0		0.25	V
Minimum Output Current	I_{CS_OUT}	Sinking	25			µA
		Sourcing	400			
Output Voltage Range	V_{CS_OUT}		0		1.5	V
DC Voltage Gain				4		V/V
Unity-Gain Bandwidth				0.8		MHz
Maximum REFI Input Voltage	V_{REFI}				1.0	V

Electrical Characteristics (continued)

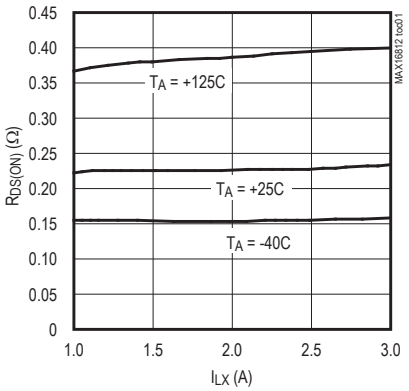
(V_{IN} = V_{EN} = 12V, C_{L_REG} = 3.3µF, C_{H_REG} = 1µF, C_{REF} = 47nF, V_{TGRM} = 0V, R_{SRC} = 0.2Ω, R_{CS} = 1Ω, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HIGH-SIDE DIMMING LINEAR REGULATOR ((V_{HV} - V_{LV}) = 21V)						
Minimum Output Current	I_{DGT}	V_{LV} = V_{CS-}, (V_{CS+} - V_{CS-}) = 0.3V, (V_{DD} - V_{LV}) = 1V, V_{DIM} = 1V, V_{TGRM} = 0V, V_{DGT} = 1V, V_{REFI} = 1.0V, sinking		1.2		mA
		V_{LV} = V_{CS-}, (V_{CS+} - V_{CS-}) = 0.2V, (V_{DD} - V_{LV}) = 1V, V_{TGRM} = 0V, V_{DGT} = 3V, V_{REFI} = 1.0V, V_{DIM} = 1V, sourcing		1.2		
Output Voltage Range			0.2		5.0	V
DC Gain		C_{DGT} = 1nF to LV		60		dB
DD Input Bias Current	I_{DD}	(V_{DD} - V_{CS-}) = 0.5V	-3		+3	µA
DD Input Low Threshold		V_{TGRM} = 0V, V_{DIM} = 1V, V_{REFI} = 1.2V, (V_{DGT} - V_{LV}) > 1.5V, V_{DD} falling	0.25	0.50	0.75	V
DIMMING ((V_{HV} - V_{LV}) = 21V)						
DIM Input Bias Current	I_{DIM}	V_{DIM} = 1.1V	-1		+1	µA
TGRM Input High Threshold			1.18	1.23	1.27	V
TGRM Reset High-to-TGRM Low Pulse Width				1		µs
TGRM Reset Switch $R_{DS(ON)}$		V_{TGRM} = 1.3V			20	Ω
Dimming Rise and Fall LED Current Times				5		µs
OVERVOLTAGE PROTECTION (OV)						
OV Input High Threshold		V_{OV} rising	1.180	1.230	1.292	V
OV Input Threshold Hysteresis				14		mV
OV Input Bias Current	I_{OV}	V_{OV} = 1.1V	-1		+1	µA
INTERNAL OSCILLATOR CLOCK						
Internal Clock Frequency	f_{OSC}	RT = 2MΩ to AGND	470	525	570	kHz
		RT = 50kΩ to AGND	105	125	155	
SLOPE COMPENSATION INPUT (SLP)						
SLP Input Current	I_{SLP}	V_{SLP} = 0V		150		µA
LOW-SIDE GATE DRIVE (DRV)						
DRV Output Low Impedance	R_{DRV_LO}	DRV sinking 20mA	3		30	Ω
DRV Output High Impedance	R_{DRV_HI}	DRV sourcing 20mA	10		45	Ω
INTERNAL POWER MOSFET						
GT Input Leakage Current		V_{GT} = 0 to 5V	-1		+1	µA
Internal MOSFET Gate-to-Source Threshold Voltage	V_{TH}			2.5		V
Internal MOSFET Gate Charge	Q_g	V_{LX} = 50V		8		nC

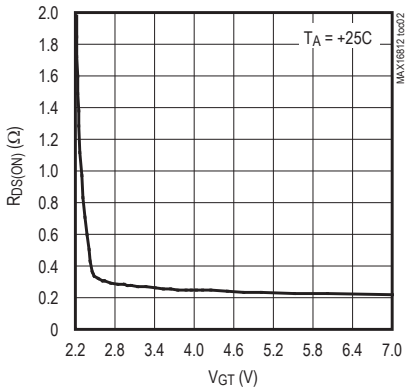
Typical Operating Characteristics

(V_{IN} = V_{EN} = 12V, C_{L_REG} = 3.3µF, C_{H_REG} = 1µF, V_{TGRM} = 0V, T_A = +25°C, unless otherwise noted.)

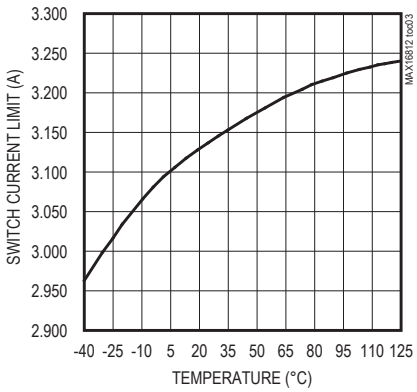
$R_{DS(ON)}$ vs. I_{LX}



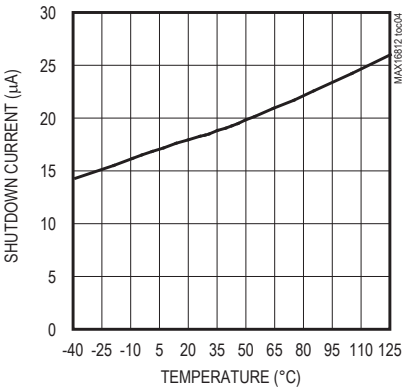
$R_{DS(ON)}$ vs. V_{GT}



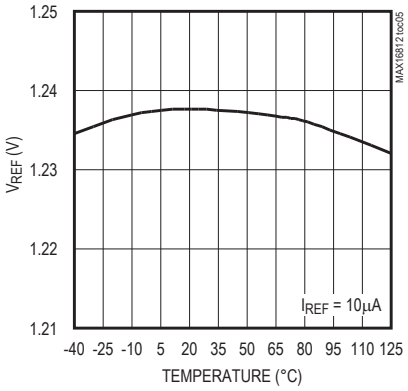
SWITCH CURRENT LIMIT vs. TEMPERATURE



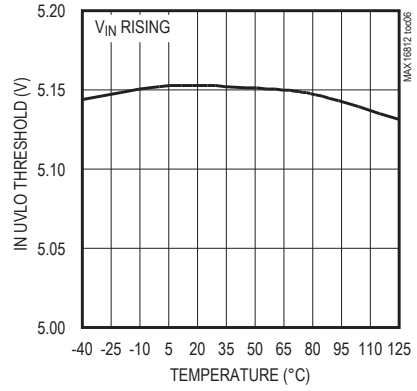
SHUTDOWN CURRENT vs. TEMPERATURE



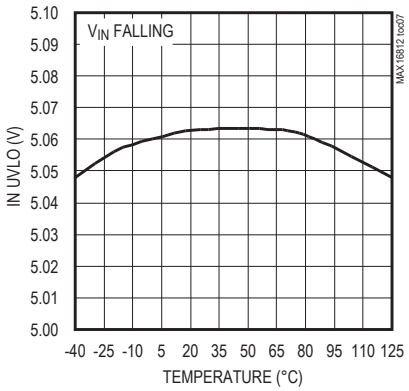
V_{REF} vs. TEMPERATURE



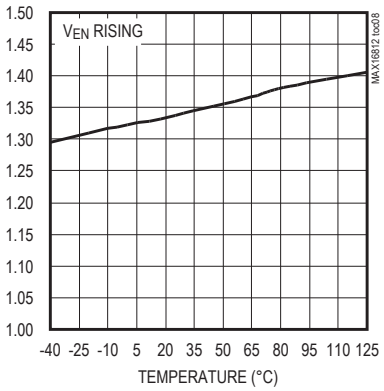
IN UVLO THRESHOLD vs. TEMPERATURE



IN UVLO THRESHOLD vs. TEMPERATURE



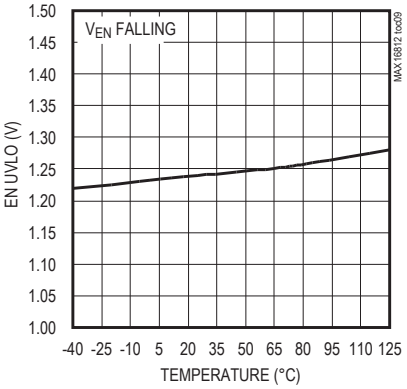
EN UVLO THRESHOLD vs. TEMPERATURE



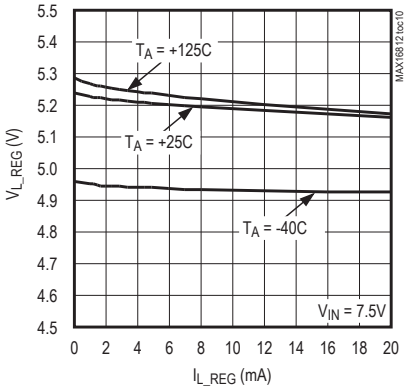
Typical Operating Characteristics (continued)

(V_{IN} = V_{EN} = 12V, C_{L_REG} = 3.3µF, C_{H_REG} = 1µF, V_{TGRM} = 0V, T_A = +25°C, unless otherwise noted.)

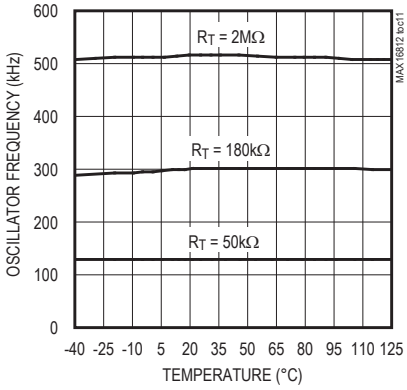
EN UVLO THRESHOLD vs. TEMPERATURE



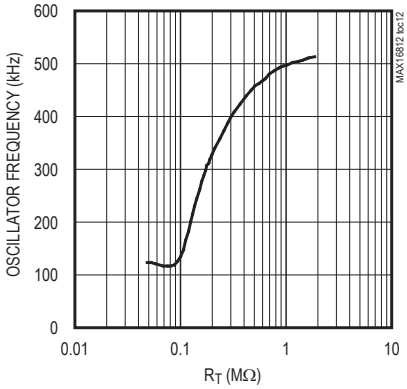
V_{L_REG} vs. I_{L_REG}



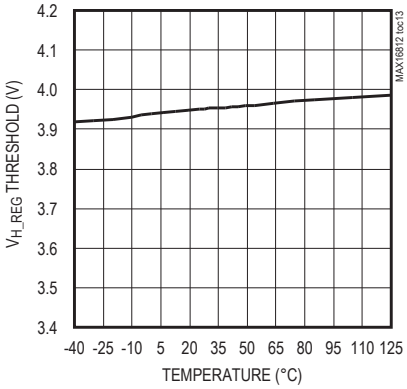
OSCILLATOR FREQUENCY vs. TEMPERATURE



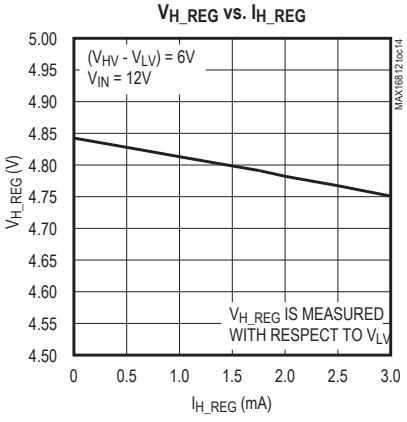
OSCILLATOR FREQUENCY vs. R_T



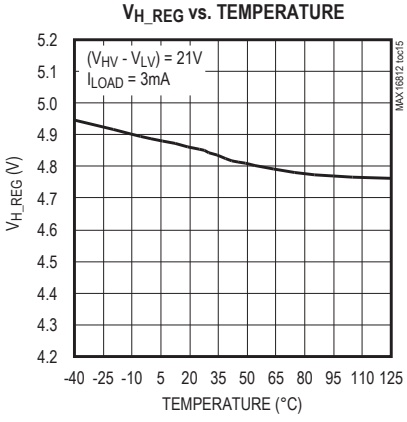
V_{H_REG} THRESHOLD vs. TEMPERATURE



V_{H_REG} vs. I_{H_REG}



V_{H_REG} vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	FB	Low-Side Error Amplifier's Inverting Input
2	COMP	Low-Side Error Amplifier's Output. Connect a compensation network from COMP to FB for stable operation.
3	REFI	Reference Input. V_{REFI} provides the reference voltage for the high-side current-sense amplifier to set the LED current.
4	REF	+1.23V Reference Output. Connect an appropriate soft-start capacitor from REF to AGND.
5	CS_OUT	High-Side Current-Sense Amplifier Output. V_{CS_OUT} is proportional to the current through R_{CS}.
6	AGND	Analog Ground
7	EN	Enable Input/Undervoltage Lockout. Connect EN to IN through a resistive voltage-divider to program the UVLO threshold. Connect EN directly to IN to set up the device for 5V internal threshold. Apply a logic-level input to EN to enable/disable the device.
8	IN	Positive Power-Supply Input. Bypass with a 1µF ceramic capacitor to AGND.
9	L_REG	5V Low-Side Regulator Output. Bypass with a 3.3µF ceramic capacitor to AGND.
10	SGND	Signal Ground
11	DD	MOSFET's Drain Voltage-Sense Input. Connect DD to the drain of the external dimming MOSFET.
12	DGT	External Dimming MOSFET's Gate Drive
13	CS+	High-Side Current-Sense Amplifier's Positive Input. Connect R_{CS} between CS+ and CS-. CS+ is referenced to LV.
14	CS-	High-Side Current-Sense Amplifier's Negative Input. Connect R_{CS} between CS- and CS+. CS- is referenced to LV.
15	LV	High-Side Reference Voltage Input. A DC voltage at LV sets the lowest reference point for the high-side current-sense and dimming MOSFET control circuitry.
16	H_REG	High-Side Regulator Output. H_REG provides a regulated supply for high-side circuitry. Bypass with a 1µF ceramic capacitor to LV.
17	HV	High-Side Positive Supply Voltage Input. HV provides power for dimming and LED current-sense circuitry. HV is referenced to LV.
18	DRV	Internal MOSFET Gate Driver Output. Connect to a resistor between DRV and GT to set the rise and fall times at LX.
19	GT	Internal MOSFET GATE. Connect a resistor between GT and DRV to set the rise and fall times at LX.
20, 21	LX	Internal MOSFET Drain
22, 23	SRC	Internal Power MOSFET Source
24	SLP	Slope Compensation Setting. Connect an appropriate external capacitor from SLP to AGND to generate a ramp signal for stable operation.
25	TGRM	Dimming Comparator's Reference/Ramp Generator
26	DIM	Dimming Control Input
27	RT	Resistor-Programmable Internal Oscillator Setting. Connect a resistor from RT to AGND to set the internal oscillator frequency.
28	OV	Overvoltage Protection Input. Connect OV to HI through a resistive voltage-divider to AGND to set the overvoltage limit for the load. When the voltage at OV exceeds the 1.238V (typ) threshold, the gate drive (DRV) for the switching MOSFET is disabled. Once V_{OV} goes below 1.238V by 14mV, the switching MOSFET turns on again.
—	EP	Exposed Pad. Connect EP to a large-area ground plane for effective power dissipation. Do not use as the IC ground connection.

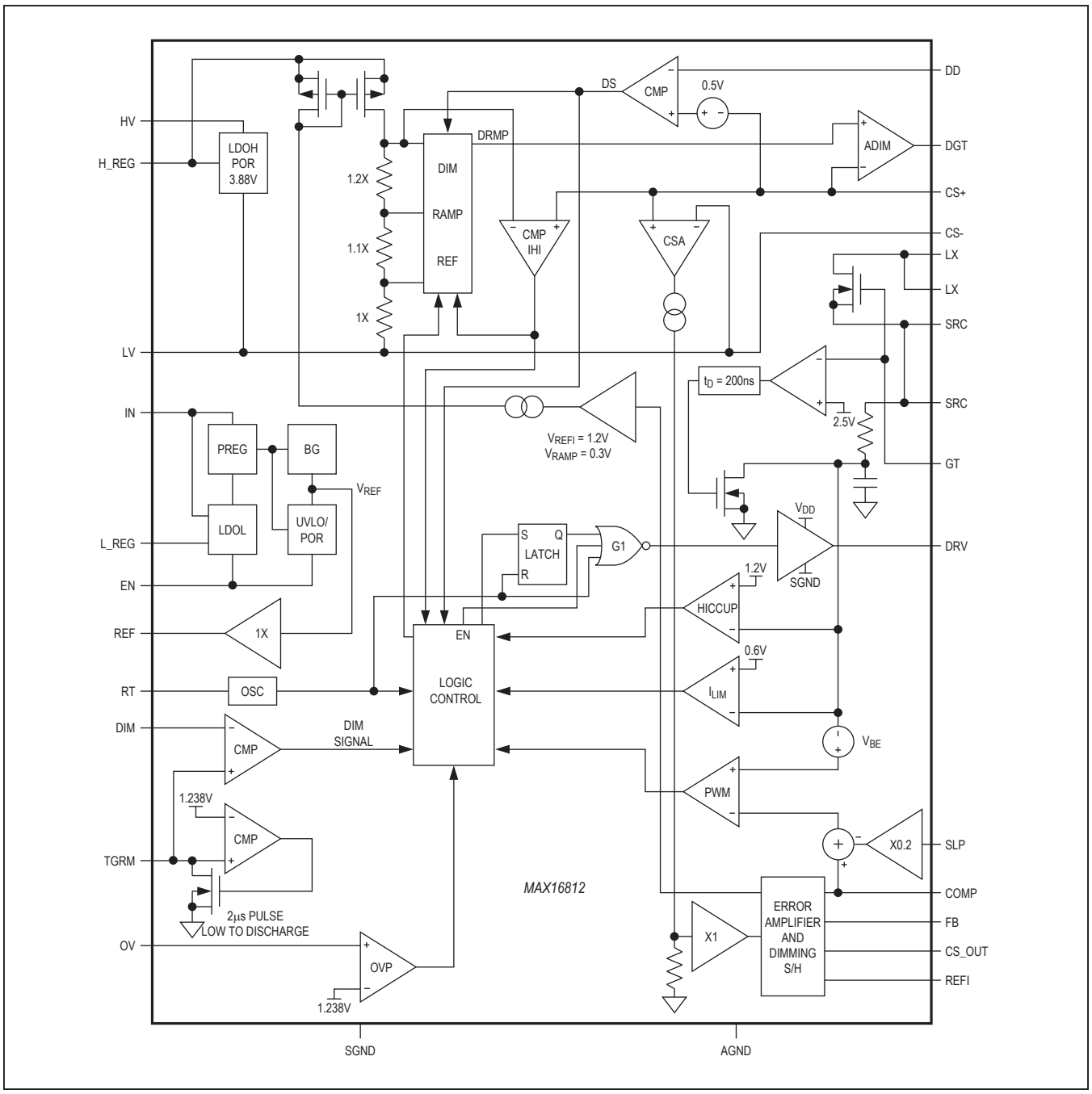


Figure 1. Functional Diagram

Detailed Description

The MAX16812 is a current-mode PWM LED driver with an integrated 0.2Ω power MOSFET for use in driving HB LEDs. By using two current regulation loops, 5% LED current accuracy is achieved. One current regulation loop controls the internal MOSFET peak current through a sense resistor (R_{SRC}) from SRC to ground, while the other current regulation loop controls the average LED current in a single LED string through another sense resistor (R_{CS}) in series with the LEDs.

The MAX16812 includes a cycle-by-cycle current limit that turns off the gate drive to the internal MOSFET during an overcurrent condition. The MAX16812 features a programmable oscillator that simplifies and optimizes the design of magnetics. The MAX16812 is well suited for inputs from 5.5V to 76V. An external resistor in series with the internal MOSFET gate can control the rise and fall times on the drain of the internal switching MOSFET, therefore minimizing EMI problems.

The MAX16812 high-frequency, current-mode PWM HB LED driver integrates all the necessary building blocks for driving a series LED string in an adjustable constant current mode with PWM dimming. Current-mode control with leading-edge blanking simplifies control-loop design, and an external adjustable slope-compensation control stabilizes the inner current-mode loop when operating at duty cycles above 50%.

An input undervoltage lockout (UVLO) programs the input supply startup voltage. An external voltage-divider on EN programs the supply startup voltage. If EN is directly connected to the input, the UVLO is set at 5V. A single external resistor from RT to AGND programs the switching frequency from 125kHz to 500kHz.

Wide contrast (100:1) PWM dimming can be achieved with the MAX16812. A DC input on DIM controls the dimming duty cycle. The dimming frequency is set by the sawtooth ramp frequency on TGRM (see the *PWM Dimming* section). In addition, PWM dimming can be achieved by applying a PWM signal to DIM with TGRM set to a DC voltage less than 1.238V. A floating high-voltage driver drives an external n-channel MOSFET in series with the LED string. REFI allows analog dimming of the LED current, further increasing the effective dimming range over PWM alone. The MAX16812 has a 5µs preprogrammed LED current rise and fall time.

A nonlatching overvoltage protection limits the voltage on the internal switching MOSFET under open-circuit conditions in the LED string. The internal thermal shutdown circuit protects the device if the junction temperature should exceed +165°C.

Current-Mode Control

The MAX16812 offers a current-mode control operation feature with leading-edge blanking that blanks the sensed current signal applied to the input of the PWM current-mode comparator. In addition, a current-limit comparator monitors the same signal at all times and provides cycle-by-cycle current limit. An additional hiccup comparator limits the absolute peak current to two times the cycle-by-cycle current limit. The leading-edge blanking of the current-sense signal prevents noise at the PWM comparator input from prematurely terminating the on-cycle. The switch current-sense signal contains a leading-edge spike that results from the MOSFET gate-charge current, and the capacitive and diode reverse-recovery current of the power circuit. The MAX16812's capacitor-adjustable slope-compensation feature allows for easy stabilization of the inner switching MOSFET current-mode loop. Upon triggering the hiccup current limit, the soft-start capacitor on REF is discharged and the gate drive to DRV is disabled. Once the inductor current falls below the hiccup current limit, the soft-start capacitor is released and it begins to charge after 10µs.

Slope Compensation

The MAX16812 uses an internal ramp generator for slope compensation. The internal ramp signal resets at the beginning of each cycle and slews at the rate programmed by the external capacitor connected at SLP and an internal ISLP current source of 150µA. An internal attenuator attenuates the actual slope compensation signal by a factor of 0.2. Adjust the MAX16812 slew-rate capacitor by using the following equation:

$$C_{SLOPE} = 0.2 \times \frac{SLP}{SR}$$

where I_{SLP} is the charging current in mA and C_{SLOPE} is the slope compensation capacitance on the SLP in µF, and SR is the designed slope in mV/µs.

When using the MAX16812 for internal switching MOSFET duty cycles greater than 50%, the following conditions must be met to avoid current-loop subharmonic oscillations.

$$SR \geq \frac{0.5 \times R_{SRC} \times V_{IND\_OFF}}{L} mV / \mu s$$

where R_{SRC} is in mΩ, V_{IND_OFF} is in volts, and L is in µH. L is the inductor connected to the LX pin of the internal switching MOSFET and V_{IND_OFF} is the voltage across the inductor during the off-time of the internal MOSFET.

Undervoltage Lockout

The MAX16812 features an adjustable UVLO through the enable input (EN). Connect EN directly to IN to use the 5V default UVLO. Connect EN to IN through a resistive divider to ground to set the UVLO threshold. The MAX16812 is enabled when VEN exceeds the 1.38V (typ) threshold.

Calculate the EN UVLO resistor-divider values as follows (see Figure 2):

$$R_{UV1} = R_{UV2} \times \left(\frac{V_{EN}}{V_{UVLO} - V_{EN}} \right)$$

where RUV1 is in the 20kΩ range, VEN is the 1.38V (typ) EN threshold voltage, and V_{UVLO} is the desired input-voltage UVLO threshold in volts. Due to the 100mV hysteresis of the UVLO threshold, capacitor C_{EN} is required to prevent chattering at the UVLO threshold due to line impedance drops at power-up and during dimming. If the undervoltage setting is very close to the required minimum operating voltage, there can be jumps in the voltage at IN while dimming. C_{EN} should be large enough to limit the ripple on EN to less than 100mV (EN hysteresis) under these conditions so that it does not turn on and off due to the ripple on IN.

Soft-Start

The soft-start feature of the MAX16812 allows the LED string current to ramp up in a controlled manner, thus minimizing output-voltage overshoot. While the part is in UVLO, CREF is discharged (Figure 3). Upon coming out of UVLO, an internal current source starts charging CREF during the soft-start cycle. Use the following equation to calculate total soft-start e:

$$t_{ST} = C_{REF} \times \frac{1.238}{I_{REF}}$$

where I_{REF} is 40µA, CREF is in µF, and t_{ST} is in seconds. Operation begins when REF ramps above 0.6V. Once the soft-start is complete, REF is regulated to 1.238V, the internal voltage reference.

Low-Side Internal Switching MOSFET Driver Supply (L_REG)

L_REG is the regulated (5.2V) internal supply voltage capable of delivering 20mA. L_REG provides power to the gate drive of the internal switching power MOSFET. V_{L_REG} is referenced to AGND. Connect a 3.3µF ceramic capacitor from L_REG to AGND.

High-Side Regulator (H_REG)

H_REG is a low-dropout linear regulator referenced to LV. H_REG provides the gate drive for the external n-channel dimming MOSFET and also powers up the MAX16812's LED current-sense circuitry. Bypass H_REG to LV with a 1µF ceramic capacitor.

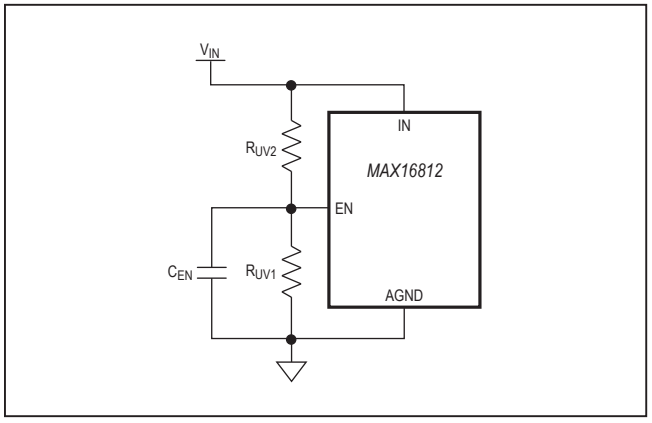


Figure 2. UVLO Threshold Setting

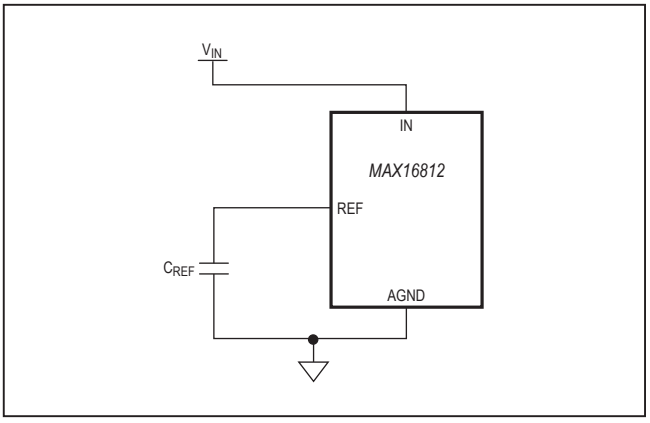


Figure 3. Soft-Start Setting

High-Side Current-Sense Output (CS_OUT)

A high-side transconductance amplifier converts the voltage across the LED current-sense resistor (RCS) into an internal current output. This current flows through an internal resistor connected to AGND. The voltage gain for the LED current-sense signal is 4. The amplified signal is then buffered and connected through an internal switch to CS_OUT.

Internal Error Amplifier

The MAX16812 includes a built-in voltage-error amplifier, which can be used to close the feedback loop. The internal LED current-sense output signal is buffered internally and then connected to CS_OUT through an internal switch. CS_OUT is connected to the inverting input (FB) pin of the error amplifier through a resistor. See Figures 4 and 5. The reference voltage for the output current is connected to REFI, the noninverting input of the error amplifier. When the internal dimming signal is low, COMP is disconnected from the output of the error amplifier and CS_OUT is simultaneously disconnected from the buffered LED current-sense output signal (Figure 5). When the internal dimming signal is high, the output of the op amp is connected to COMP and CS_OUT is connected to the buffered LED current-sense signal at the same time (Figure 4). This enables the compensation capacitor to hold the charge when the DIM signal has turned off the internal switching MOSFET gate drive. To maintain the charge on the compensation capacitors C_{COMP1} and C_{COMP2}, the capacitors should be of the low-leakage ceramic type.

When the internal dimming signal is enabled, the voltage on the compensation capacitor forces the converter into steady state almost instantaneously. The voltage on COMP is subtracted from the internal slope compensation signal and is then connected to one of the inputs of the PWM comparator. The PWM comparator input is of the CMOS type with very low bias currents.

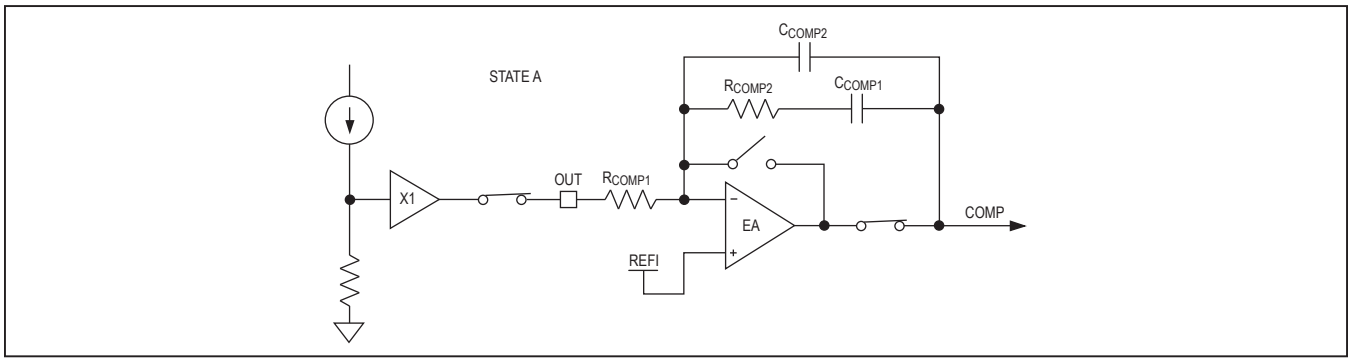


Figure 4. Internal Error Amplifier Connection (Dimming Signal High)

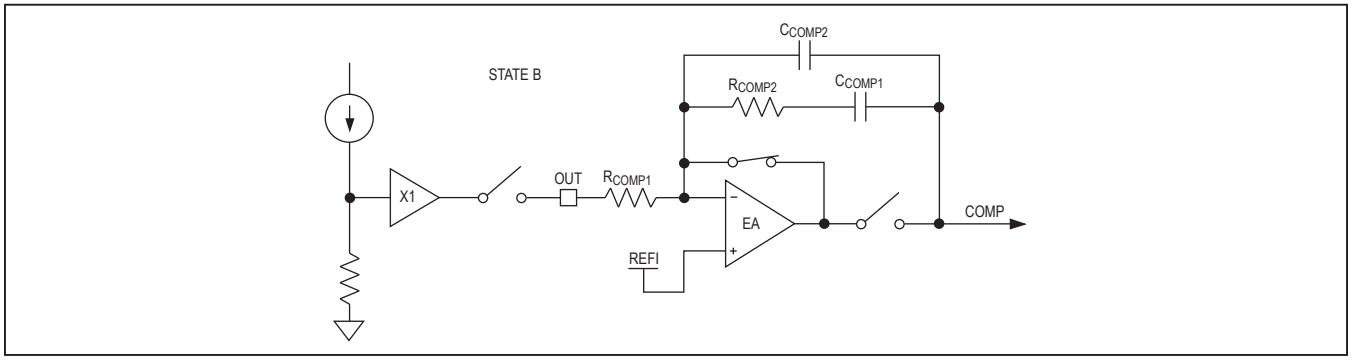


Figure 5. Internal Error Amplifier Connections (Dimming Signal Low)

Analog Dimming

The MAX16812 offers analog dimming of the LED current by allowing the application of an external voltage at REFI. The output current is proportional to the voltage at REFI. Use a potentiometer from REF or directly apply an external voltage source at REFI.

PWM Comparator

The PWM comparator uses the instantaneous switch current, the error-amplifier output, and the slope compensation to determine when the gate drive DRV to the internal n-channel switching MOSFET turns off. In normal operation, gate drive DRV to the n-channel MOSFET turns off when:

$$I_{SW} \times R_{SRC} \geq V_{COMP} - V_{OFFSET} - V_{SCOMP}$$

where I_{SW} is the current through the internal n-channel switching MOSFET, R_{SRC} is the switch current-sense resistor, V_{COMP} is the output voltage of the internal amplifier, V_{OFFSET} is the internal DC offset, which is a V_{BE} drop, and V_{SCOMP} is the ramp function that starts at zero and slews at the programmed slew rate (SR).

Internal Switching MOSFET Current Limit

The current-sense resistor (RSRC), connected between the source of the internal MOSFET and ground, sets the current limit. The SRC input has a voltage trip level (V_{SRC}) of 600mV for the cycle-by-cycle current limit. Use the following equation to calculate the value RSRC:

$$R_{SRC} = \frac{V_{SRC}}{I_{LXLIM}}$$

where I_{LXLIM} is the peak current that flows through the switching MOSFET at full load and low line. When the voltage produced by this current (through the current-sense resistor) exceeds the current-limit (ILIM) comparator threshold, the MOSFET driver (DRV) quickly terminates the current on-cycle. The 200ns leading-edge blanking circuit suppresses the leading-edge spike on the current-sense waveform from appearing at the current-limit comparator. There is also a hiccup comparator (HICCUP) that limits the peak current in the internal switch set at twice the peak limit setting.

Internal n-Channel Switching MOSFET Driver (DRV)

L_REG provides power for the DRV output. Connect a resistor from DRV to gate GT of the internal switching MOSFET to control the switching MOSFET rise and fall times, if necessary.

External Dimming MOSFET Gate Drive (DGT)

DGT is the gate drive to the external dimming MOSFET referenced to LV. H_REG provides the power to the gate drive.

Overvoltage Protection

The overvoltage protection (OVP) comparator compares the voltage at OV with a 1.238V (typ) internal reference. When the voltage at OV exceeds the internal reference, the OVP comparator terminates PWM switching and no further energy is transferred to the load. Connect OV to HV through a resistive voltage-divider to ground to set the overvoltage threshold at the output.

Setting the Overvoltage Threshold

Connect OV to HV or to the high-side of the LEDs through a resistive voltage-divider to set the overvoltage threshold at the output (Figure 6).

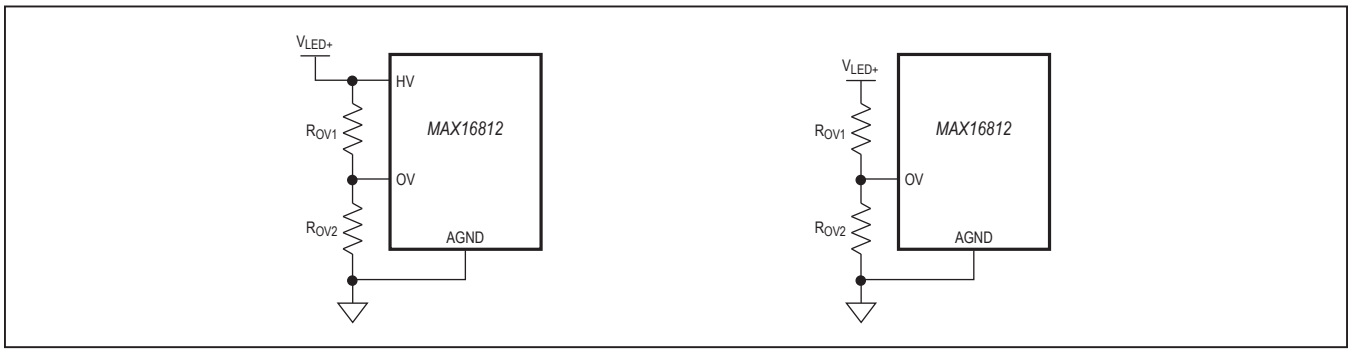


Figure 6. OVP Setting

The overvoltage protection (OVP) comparator compares the voltage at OV with a 1.238V (typ) internal reference. Use the following equation to calculate resistorlues:

$$R_{OV1} = R_{OV2} \times \left(\frac{V_{OV\_LIM} - V_{OV}}{V_{OV}} \right)$$

where V_{OV} is the 1.238V OV threshold. Choose R_{OV1} and R_{OV2} to be reasonably high-value resistors to prevent the discharge of filter capacitors. This prevents degraded performance during dimming.

Internal Oscillator Switching Frequency

The oscillator switching frequency is programmed by a resistor connected from RT to AGND. To program the oscillator frequency above 125kHz, choose the appropriate resistor RT from the curves shown in the Oscillator Frequency vs. RT graph in the T*ypical Operating Characteristics* section.

PWM Dimming

PWM dimming can be achieved by driving DIM with an analog voltage less than V_{REF}. See Figure 7. An external resistor on TGRM from L_REG in conjunction with the ramp capacitor, C_{TGRM}, from TGRM to AGND creates a sawtooth ramp that is compared with the DC voltage on DIM. The output of the comparator is a pulsating dimming signal. The frequency f_{RAMP} of the sawtooth signal on TGRM is given by:

$$f_{RAMP} \cong \frac{3.67}{C_{TGRM} \times R_{TGRM}}$$

Use the following formula to calculate the voltage V_{DIM}, necessary for a given output duty cycle, D:

$$V_{DIM} = D \times 1.238V$$

where V_{DIM} is the DC voltage applied to DIM in volts.

The DC voltage for DIM can also be created by connecting DIM to REF through a resistive voltage-divider. Using the required dimming input voltage, V_{DIM}, calculate the resistor values for the divider string using the following equation:

$$R_{DIM2} = [V_{DIM} / (V_{REF} - V_{DIM})] \times R_{DIM1}$$

where V_{REF} is the voltage on REF.

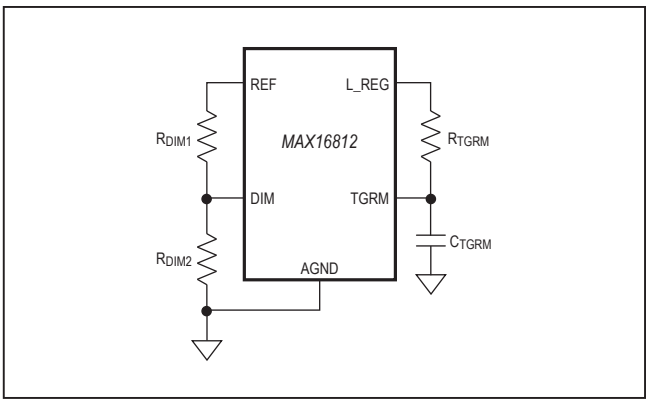


Figure 7. PWM Dimming from REF

PWM dimming can also be achieved by connecting TGRM to a DC voltage less than VREF and applying the PWM signal at DIM. The moment the internal dimming signal goes low, gate drive DRV to the internal switching MOSFET is turned off. The error amplifier goes to state B (see the *Internal Error Amplifier* section and Figures 4 and 5). The peak current in the inductor prior to disabling DRV is I_{LX}. Gate drive DGT to the external dimming MOSFET is held high. Then after a switchover period, gate voltage V_{DGT} on the external dimming MOSFET is linearly controlled to reduce the LED current to 0. The fall time of the LED current is controlled by an internal timing circuit to 5µs for the MAX16812. During this period, the gate (DRV) to the internal switching MOSFET is enabled. After the fall time, the gate drive to the external dimming MOSFET is turned off and the gate drive to the internal switching MOSFET is still held high after the switchover period. The peak current in the inductor is controlled at I_{LX}. Then after a time period of 20µs, the gate drive is disabled. The scope shots in Figures 8–11 show the dimming waveforms.

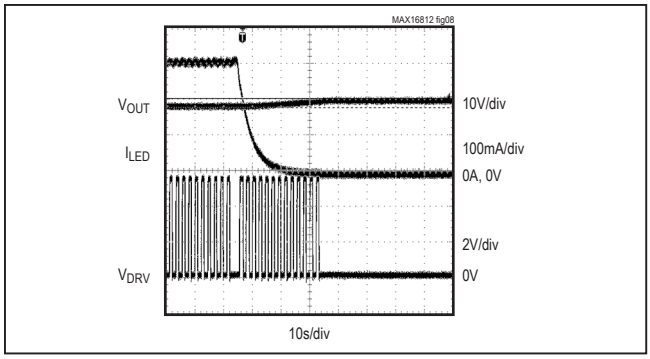


Figure 8. LED Current, Output Voltage, and DRV Waveforms when DIM Signal Goes Low

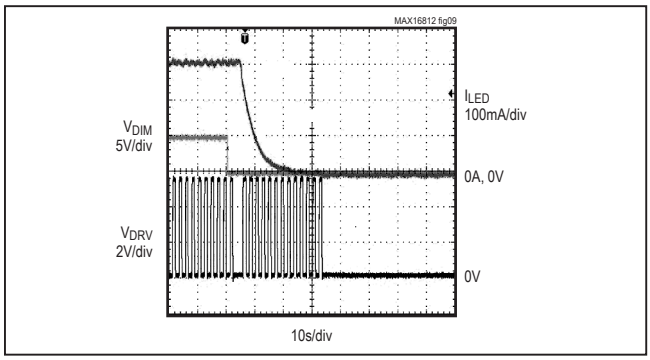


Figure 9. LED Current, DIM Signal, and DRV Waveforms when DIM Signal Goes Low

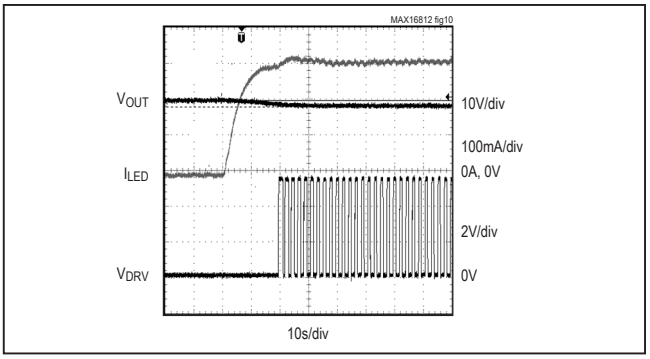


Figure 10. LED Current, Output Voltage, and DRV Waveforms when DIM Signal Goes High

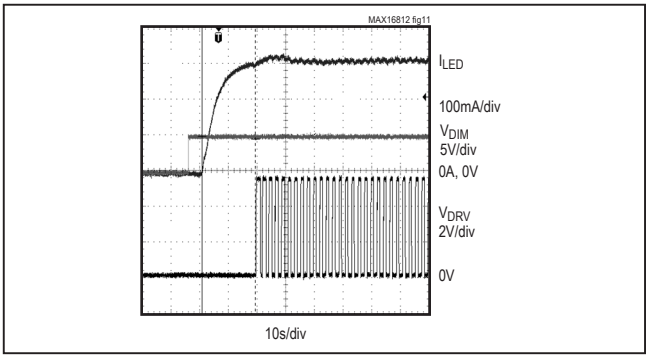


Figure 11. LED Current, DIM Signal, and DRV Waveforms when DIM Signal Goes High

When the DIM signal goes high, the LED current is gradually increased to the programmed value. The rise time of the LED current is controlled to 5µs for the MAX16812 by controlling the voltage on DGT. After the rise time, an internal sensing circuit monitors the voltage across the drain to the source of the external dimming MOSFET. The LED current is now controlled at the programmed value by a linear current regulating circuit. Once the voltage across the drain to source of the dimming MOSFET drops below 0.5V, the reference for the linear current regulating circuit is increased to 1.1 times the programmed value. The gate drive (DRV) to the internal switching MOSFET is enabled and the error amplifier is returned to state A (see the *Internal Error Amplifier* section and Figures 4 and 5).

Fault Protection

The MAX16812 features built-in overvoltage protection and thermal shutdown. Connect a resistive voltage-divider between HV, OV, and AGND to program the overvoltage protection. In the case of a short circuit across the LED string, the temperature of the external dimming MOSFET could exceed the maximum allowable junction temperature. This is due to excess power dissipation in the MOSFET. Use the fault protection circuit shown in Figure 12 to protect the external dimming MOSFET.

Internal thermal shutdown in the MAX16812 safely turns off the IC when the junction temperature exceeds +165°C.

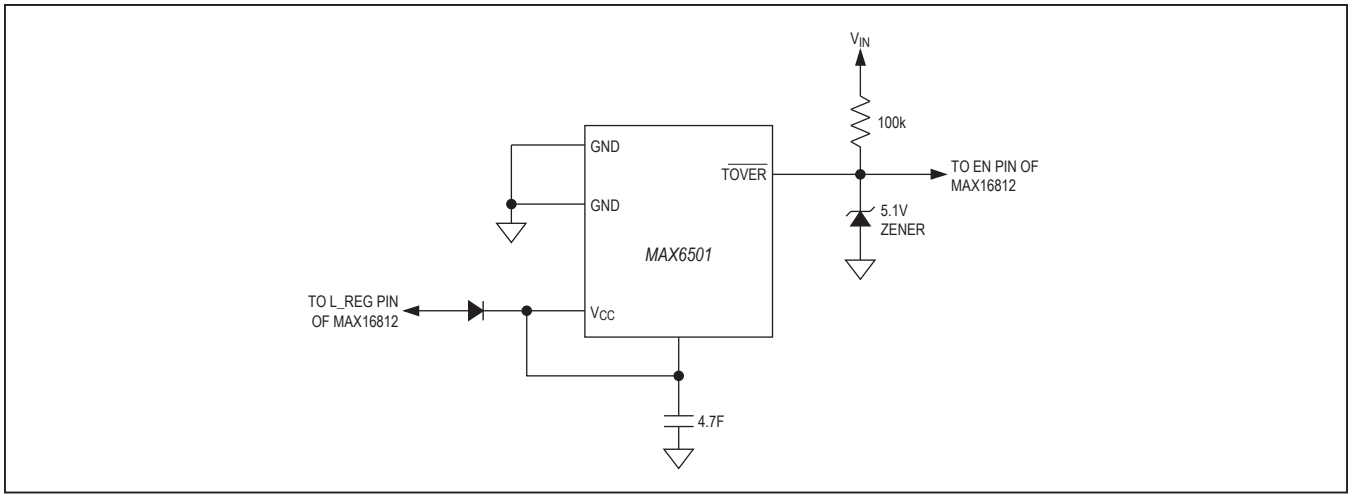


Figure 12. Dimming MOSFET Protection

Inductor Selection

The minimum required inductance is a function of the operating frequency, the input-to-output voltage differential and the peak-to-peak inductor current (ΔI_L). Higher ΔI_L allows for a lower inductor value while a lower ΔI_L requires a higher inductor value. A lower inductor value minimizes size and cost, improves large-signal transient response, but reduces efficiency due to higher peak currents and higher peak-to-peak output ripple voltage for the same output capacitor. On the other hand, higher inductance increases efficiency by reducing the ripple current, ΔI_L. However, resistive losses due to the extra turns can exceed the benefit gained from lower ripple current levels, especially when the inductance is increased without allowing for larger inductor dimensions. A good compromise is to choose ΔI_L equal to 30% of the full load current. The inductor saturating current specification is also important to avoid runaway current during output overload and continuous short-circuit conditions.

Buck Configuration: In a buck configuration (Figure 13), the average inductor current does not vary with the input. The worst-case peak current occurs at the highest input voltage. In this case, the inductance, L, for continuous conduction mode given by:

$$L = \frac{V_{OUT} \times (V_{INMAX} - V_{OUT})}{V_{INMAX} \times f_{SW} \times \Delta I_L}$$

where V_{INMAX} is the maximum input voltage, f_{SW} is the switching frequency, and V_{OUT} is the output voltage.

Boost Configuration: In the boost converter, the average inductor current varies with the input voltage and the maximum average current occurs at the lowest input voltage. For the boost converter, the average inductor current is equal to the input current. In this case, the inductance, L, is calculated as:

$$L = \frac{V_{INMIN} \times (V_{OUT} - V_{INMIN})}{V_{OUT} \times f_{SW} \times \Delta I_L}$$

where V_{INMIN} is the minimum input voltage, V_{OUT} is the output voltage, and f_{SW} is the switching frequency. See Figure 14.

Buck-Boost Configuration: In a buck-boost converter (see the *Typical Application Circuit*), the average inductor current is equal to the sum of the input current and the LED current. In this case, the inductance, L, is:

$$L = \frac{V_{OUT} \times V_{INMIN}}{(V_{OUT} + V_{INMIN}) \times f_{SW} \times \Delta I_L}$$

where V_{INMIN} is the minimum input voltage, V_{OUT} is the output voltage, and f_{SW} is the switching frequency.

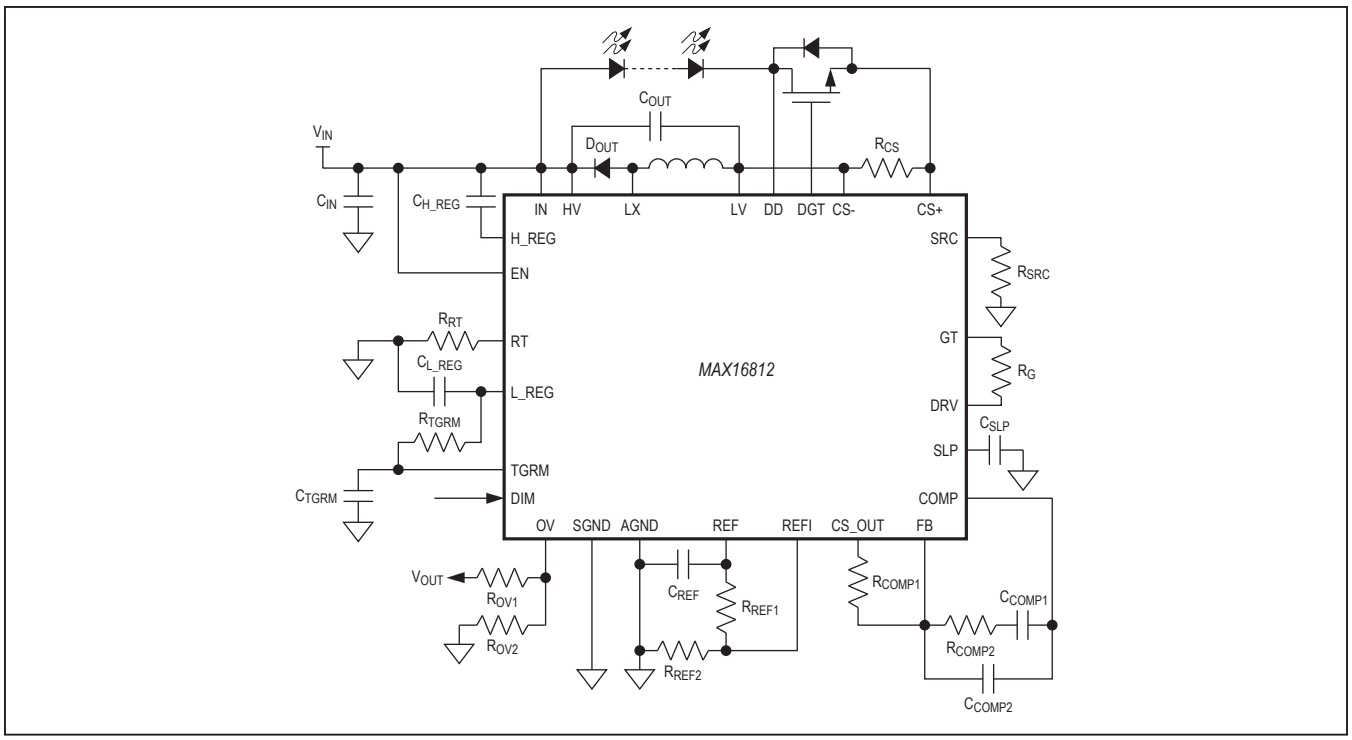


Figure 13. Buck Configuration

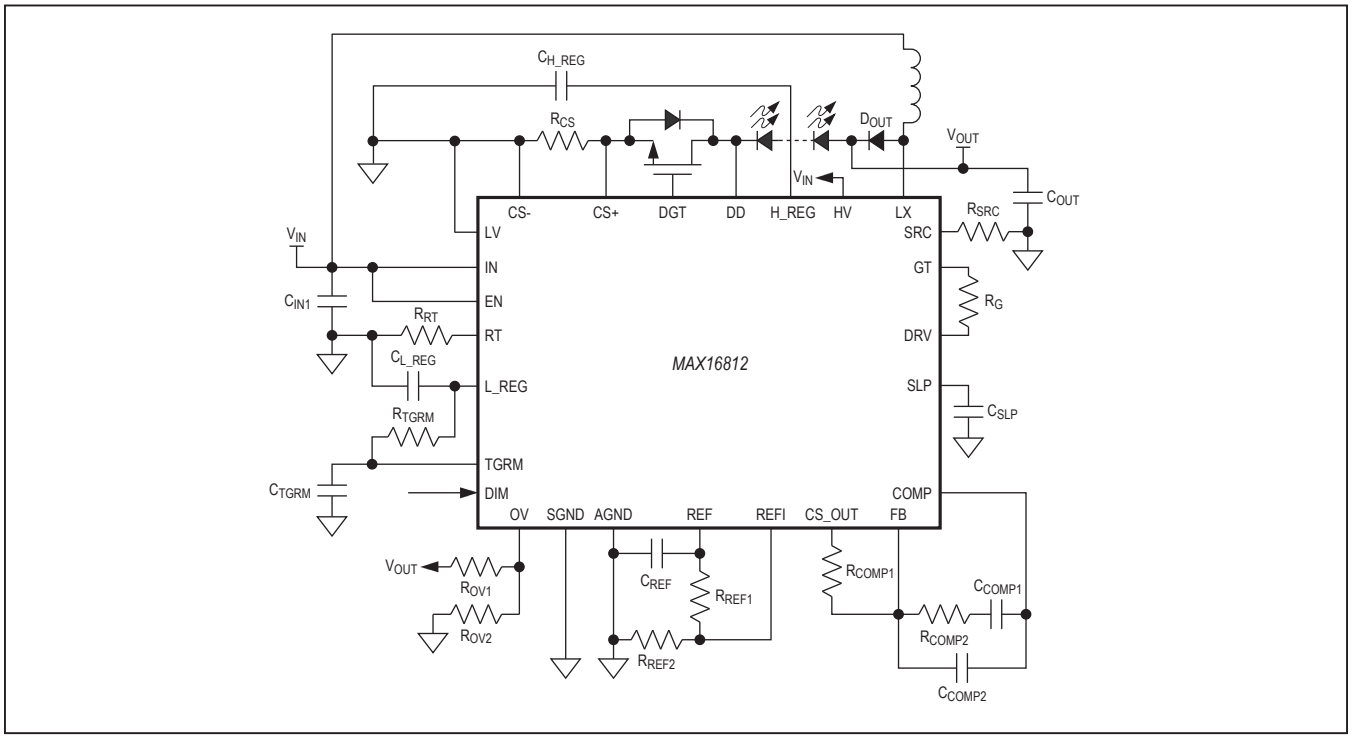


Figure 14. Boost Configuration

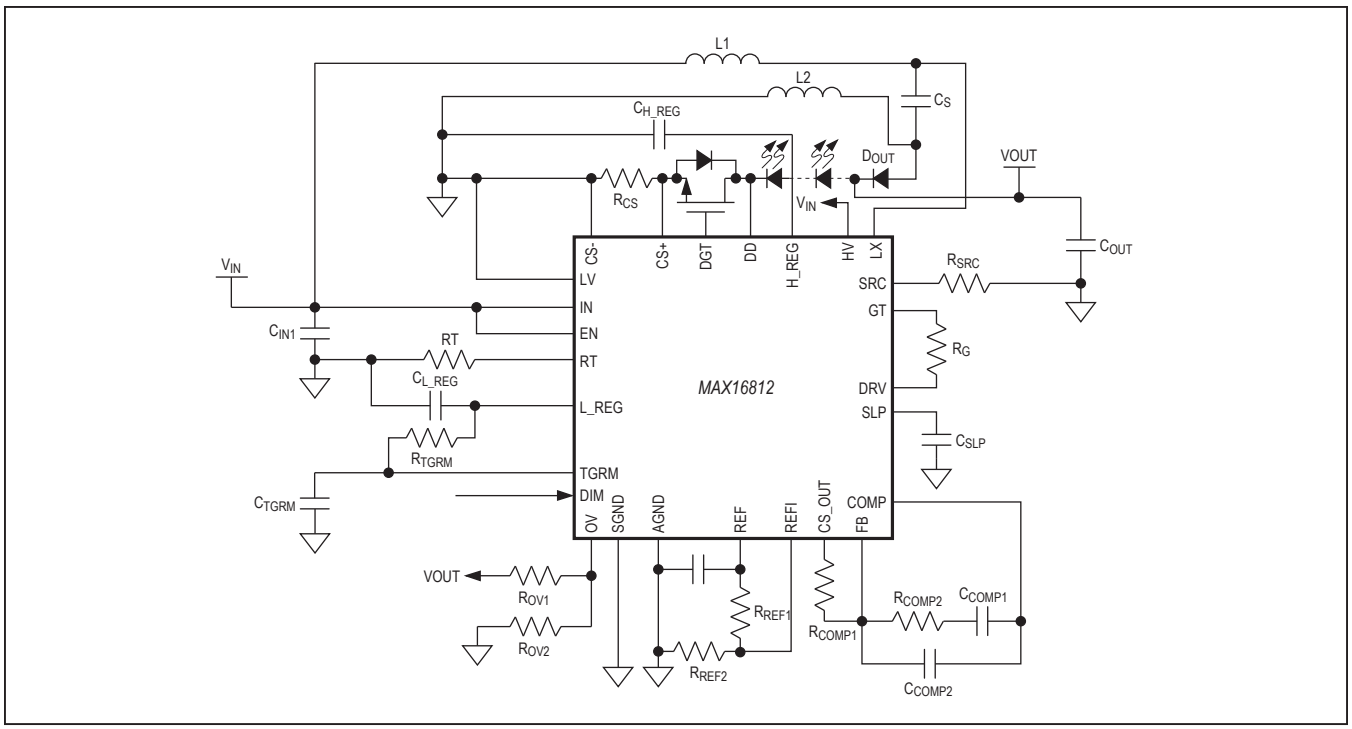


Figure 15. SEPIC Configuration

Output Capacitor

The function of the output capacitor is to reduce the output ripple to acceptable levels. The ESR, ESL, and the bulk capacitance of the output capacitor contribute to the output ripple. In most of the applications, the output ESR and ESL effects can be dramatically reduced by using low-ESR ceramic capacitors. To reduce the ESL effects, connect multiple ceramic capacitors in parallel to achieve the required capacitance.

In a buck configuration, the output capacitance, C_{OUT}, is calculated using the follow equation:

$$C_{OUT} \geq \frac{(V_{INMAX} - V_{OUT}) \times V_{OUT}}{\Delta V_R \times 2 \times L \times V_{INMAX} \times f_{SW}^2}$$

where ΔVR is the maximum allowable output ripple.

In a boost configuration, the output capacitance, C_{OUT}, is calculated as:

$$C_{OUT} \geq \frac{(V_{OUT} - V_{INMIN}) \times 2 \times I_{OUT}}{\Delta V_R \times V_{OUT} \times f_{SW}}$$

where C_{OUT} is the output capacitor.

In a buck-boost configuration, the output capacitance, C_{OUT} is:

$$C_{OUT} \geq \frac{2 \times V_{OUT} \times I_{OUT}}{\Delta V_R \times (V_{OUT} + V_{INMIN}) \times f_{SW}}$$

where V_{OUT} is the voltage across the load and I_{OUT} is the output current.

Input Capacitor

An input capacitor connected between IN and ground must be used when configuring the MAX16812 as a buck converter. Use a low-ESR input capacitor that can handle the maximum input RMS ripple current. Calculate the maximum RMS ripple using the follow equation:

$$I_{IN(RMS)} = \frac{I_{OUT} \times \sqrt{V_{OUT} \times (V_{INMIN} - V_{OUT})}}{V_{INMIN}}$$

When using the MAX16812 in a boost or buck-boost configuration, the input capacitor's RMS current is low and the input capacitance can be small. However, an additional electrolytic capacitor may be required to prevent oscillations due to line impedances.

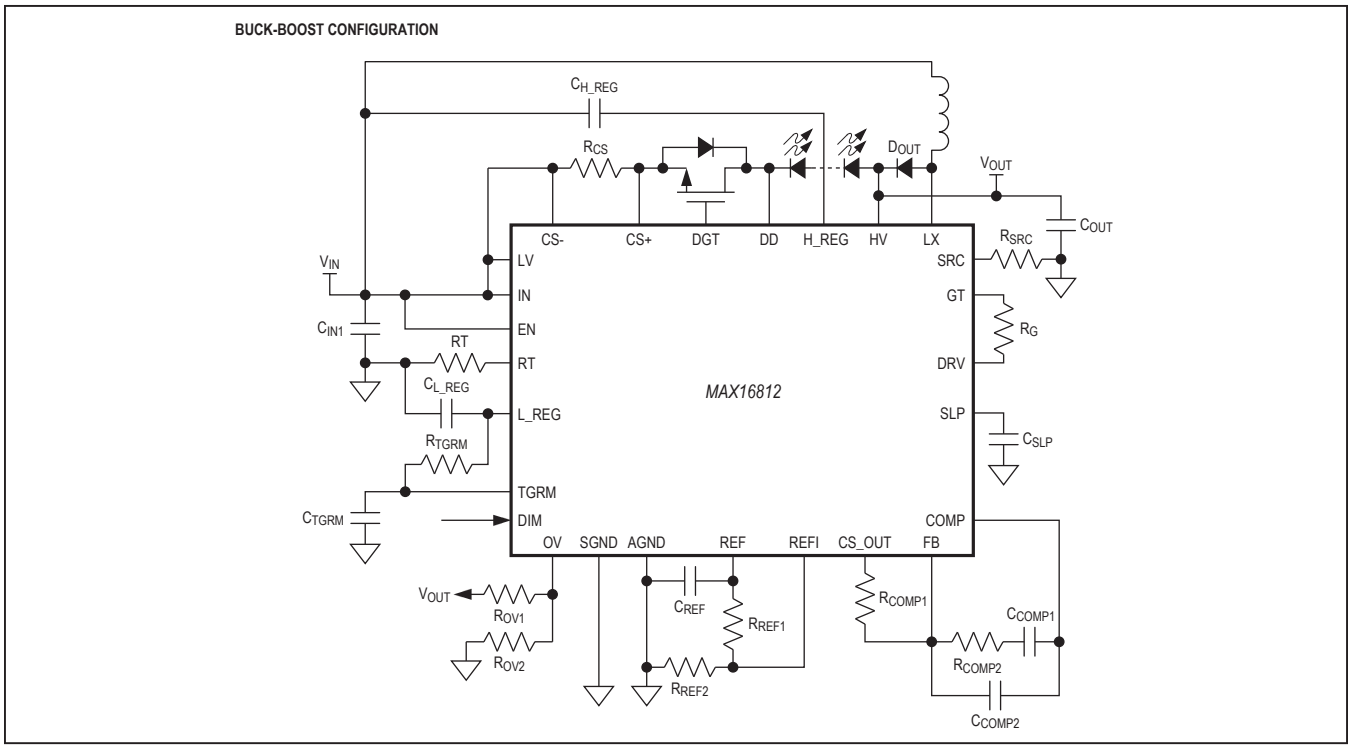
Layout Recommendations

Typically, there are two sources of noise emission in a switching power supply: high di/dt loops and high dv/dt surfaces. For example, traces that carry the drain current often form high di/dt loops. Similarly, the drain of the internal MOSFET connected to the LX pin presents a dv/dt source. Keep all PCB traces carrying switching currents as short as possible to minimize current loops. Use ground planes for best results.

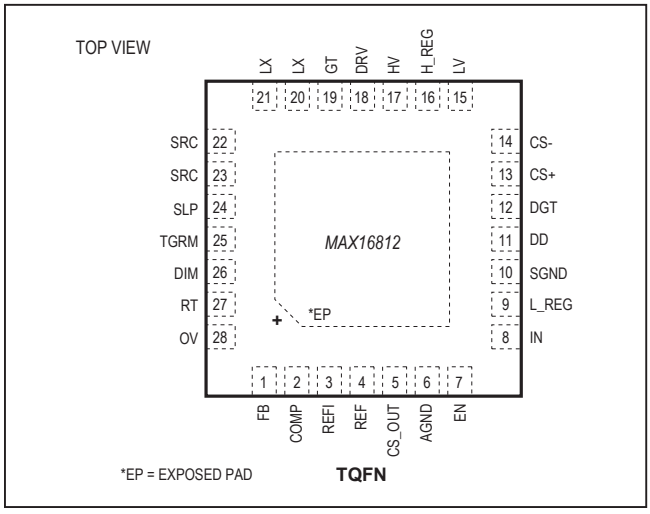
Careful PCB layout is critical to achieve low switching losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity and power dissipation. Follow these guidelines for good PCB layout:

- Use a large copper plane under the MAX16812 package. Ensure that all heat-dissipating components have adequate cooling. Connect the exposed pad of the device to the ground plane.
- Isolate the power components and high-current paths from sensitive analog circuitry.
- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. Keep switching loops short.
- Connect AGND and SGND to a ground plane. Ensure a low-impedance connection between all ground points.
- Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PCBs to enhance full-load efficiency.
- Ensure that the feedback connection to FB is short and direct.
- Route high-speed switching nodes away from the sensitive analog areas.
- To prevent discharge of the compensation capacitors, C_{COMP1} and C_{COMP2}, during the off-time of the dimming cycle, ensure that the PCB area close to these components has extremely low leakage.

Typical Application Circuit



Pin Configuration



Chip Information

PROCESS: BiCMOS

TRANSISTOR COUNT: 8699

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
28 TQFN-EP	T2855+8	**21-0140**	**90-0028**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/07	Initial release	—
1	4/14	No /V OPNs; removed Automotive reference from *Applications* section	1

