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FPF2488 Dual Channel Over-Voltage Protection Load Switch

Features

- Dual Channel Power Switch (V_{BUS} and V_{IF})
- Surge Protection under IEC 61000-4-5
 - V_{BUS} : ± 100 V
 - V_{IF} : ± 40 V
- Input Voltage Range
 - V_{BUS} : 2.5 V ~ 23 V
 - V_{IF} : 3.1 V ~ 5.5 V
- Max Continuous Current Capability
 - V_{BUS} : 2.5 A
 - V_{IF} : 6 A
- Ultra Low On-Resistance
 - V_{BUS} : Typ. 33 m Ω
 - V_{IF} : Typ. 10 m Ω
- Over Voltage Protection
 - V_{BUS} : 10 V \pm 100 mV
 - V_{IF} : 5.25 V \pm 250 mV
- LDO Output based V_{BUS_DET} for V_{BUS} Detection
- Active Low Control for V_{BUS} Path
- OTG Functionality on V_{BUS} Path
- Conditional Active High Control for V_{IF} Path
- Reverse-Current Blocking for V_{IF} Path

Applications

- Mobile Handsets and Tablets
- Wearable Devices

Description

The FPF2488 features a 2-channel power switch, which offers surge protection and Over-Voltage Protection (OVP), to protect downstream components and enhancing overall system robustness.

Channel one (V_{BUS}) is an active-low, 28 V/2.5 A rated, power MOSFET switch with an internal clamp supporting ± 100 V surge protection, highly accurate fixed OVP at 10.0 V (± 100 mV), and OTG functionality. Channel two (V_{IF}) is a conditional active-high, 6 V/6 A rated, power MOSFET switch with an integrated TVS supporting ± 40 V surge protection and fixed OVP at 5.25 V (± 250 mV). V_{IF} also provides Reverse Current Blocking (RCB) during its OFF state to minimize leakage current.

V_{BUS_DET} is paired with always ON LDO to power downstream devices even with V_{BUS} is greater than 2.5 V, even when disabled through the ONB pin. This provides power sequence control or a host controlled configuration in system.

The FPF2488 is available in a 15-bump, 1.6 mm x 2.2 mm Wafer-Level Chip-Scale Package (WLCSP) with 0.4 mm pitch.

Related Resources

- <http://www.fairchildsemi.com/>

Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package	Packing Method
FPF2488UCX	-40°C – +85°C	GW	15-Ball, 0.4 mm Pitch WLCSP	Tape & Reel

Application Diagram

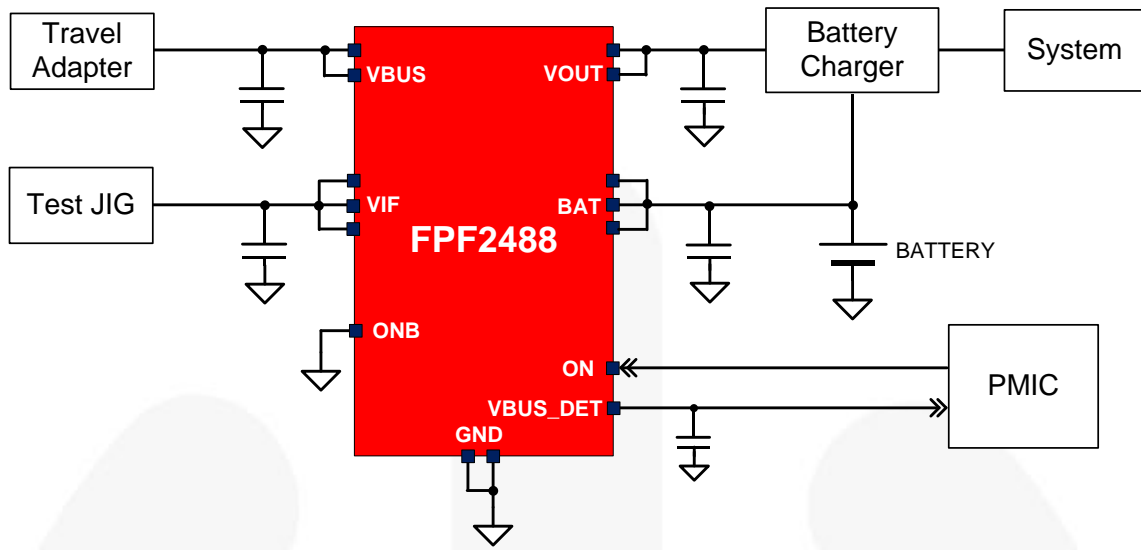


Figure 1. Typical Application

Block Diagram

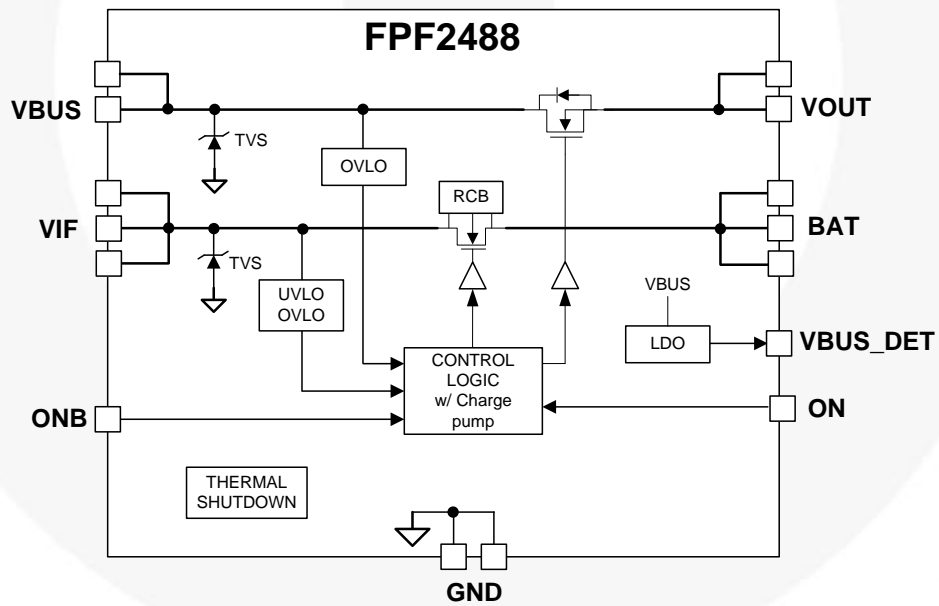


Figure 2. Functional Block Diagram

Pin Configuration

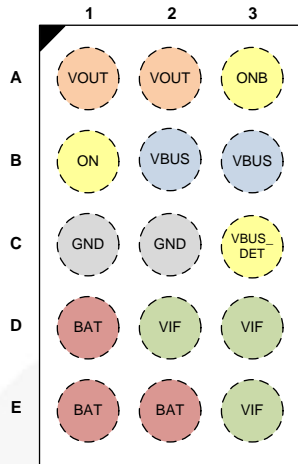


Figure 3. Pin Configuration (Top View)

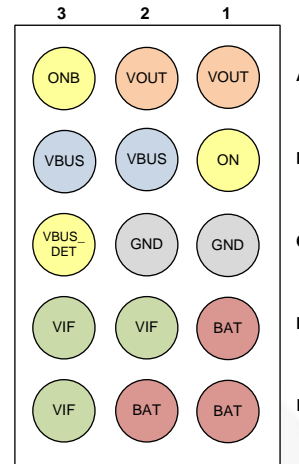


Figure 4. Pin Configuration (Bottom View)

Pin Definitions

Name	Bump	Type	Description
V_{BUS}	B2, B3	Input/Supply	Switch Input and Device Supply
VOUT	A1, A2	Output	Switch Output to Load
V_{IF}	D2, D3, E3	Input/Supply	Switch Input and Device Supply
BAT	D1, E1, E2	Output	Switch Output to Battery
V_{BUS_DET}	C3	Output	Regulated Output according to V_{BUS}
ON	B1	Input	Active HIGH: V_{IF} path only and when BAT is valid prior to V_{IF}
ONB	A3	Input	Active LOW: V_{BUS} path only
GND	C1, C2	GND	Ground

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit	
V _{BUS}	V _{BUS} to GND & V _{BUS} to V _{OUT} =GND or Float		-0.3	29.0	V	
V _{IF}	V _{IF} to GND		-2 ⁽¹⁾	6	V	
V _{OUT}	V _{OUT} to GND		-0.3	V _{IN} + 0.3	V	
BAT	BAT to GND		-0.3	V _{IF} + 0.3	V	
V _{BUS_DET}	V _{BUS_DET} to GND			8	V	
V _{ON(B)}	ONB or ON to GND			6	V	
I _{IN_VBUS}	Continuous V _{BUS} Current			2.5	A	
	Peak V _{BUS} Current (5 ms)			5	A	
I _{IN_VIF}	Continuous V _{IF} Current			6	A	
	Peak V _{IF} Current (5 ms)			12	A	
I _{IN_VBUS_DET}	Continuous V _{BUS_DET} Current			1	mA	
t _{PD}	Total Power Dissipation at T _A =25°C			1.54	W	
T _{STG}	Storage Temperature Range		-65	+150	°C	
T _J	Maximum Junction Temperature			+150	°C	
T _L	Lead Temperature (Soldering, 10 Seconds)			+260	°C	
θ _{JA}	Thermal Resistance, Junction-to-Ambient ⁽²⁾ (1-in. ² Pad of 2-oz. Copper)			81 ⁽²⁾	°C/W	
ESD	Electrostatic Discharge Capability	IEC 61000-4-2 System Level ESD	Air Discharge	15.0		kV
			Contact Discharge	8.0		
		Human Body Model, ANSI/ESDA/JEDEC JS-001-2012	All Pins	2		
			Charged Device Model, JESD22-C101	All Pins	1	
Surge		IEC 61000-4-5, Surge Protection	V _{BUS}	±100		V
			V _{IF}	±40		

Notes:

1. Pulsed, 50 ms maximum non-repetitive.
2. Measured using 2S2P JEDEC std. PCB.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V _{BUS}	Supply Voltage, V _{BUS}	2.5	23.0	V
V _{IF}	Supply Voltage, V _{IF}	3.1	5.5	V
C _{IN} / C _{OUT}	Input and Output Capacitance	0.1		μF
C _{VBUS_DET}	Output Capacitance	0.47		μF
T _A	Operating Temperature	-40	+85	°C

Electrical Characteristics

Unless otherwise noted, $V_{BUS}=2.5$ to 23 V, $V_{IF}=3.1$ to 5.5 V, $T_A=-40$ to 85°C ; Typical values are at $V_{BUS}=5$ V, $I_{IN} \leq 2$ A, $V_{IF}=4$ V, $C_{IN}=0.1$ μF and $T_A=25^\circ\text{C}$.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Basic Operation						
I_Q	Input Quiescent Current	$V_{BUS}=5$ V, $ONB=0$ V, V_{BUS_DET} =Floating		160	250	μA
		$V_{IF}=4$ V		100	150	μA
I_{IN_Q}	OVLO Supply Current	$V_{BUS}=12$ V, $V_{OUT}=0$ V, V_{BUS_DET} =Floating		150	205	μA
		$V_{IF}=5.5$ V, $BAT=0$ V		100	180	μA
T_{SDN}	Thermal Shutdown ⁽³⁾			140		$^\circ\text{C}$
T_{SDN_HYS}	Thermal Shutdown Hysteresis ⁽³⁾			20		$^\circ\text{C}$
V_{BUS} to V_{OUT} Switch						
V_{BUS_CLAMP}	Input Clamping Voltage	$I_{IN}=10$ mA		35		V
V_{BUS_OVLO}	Over-Voltage Trip Level	V_{BUS} Rising, $T_A=-40$ to 85°C	9.9	10.0	10.1	V
		V_{BUS} Falling, $T_A=-40$ to 85°C	9.8			V
R_{ON_VBUS}	On-Resistance	$V_{BUS}=5$ V, $I_{OUT}=1$ A, $T_A=25^\circ\text{C}$		33	39	$\text{m}\Omega$
		$V_{BUS}=9$ V, $I_{OUT}=1$ A, $T_A=25^\circ\text{C}$		33	39	$\text{m}\Omega$
t_{DEB_VBUS}	Debounce Time	Time from $V_{BUS_MIN} < V_{BUS} < V_{BUS_OVLO}$ to $V_{OUT}=0.1 \times V_{BUS}$		15		ms
t_{START_VBUS}	Soft-Start Time	Time from $V_{BUS}=V_{BUS_MIN}$ to $0.1 \times V_{BUS_DET}$		30		ms
t_{ON_VBUS}	Switch Turn-On Time	$R_L=100$ Ω , $C_L=22$ μF , V_{OUT} from $0.1 \times V_{BUS}$ to $0.9 \times V_{BUS}$		3		ms
t_{OFF_VBUS}	Switch Turn-Off Time	$R_L=100$ Ω , No C_L , $V_{BUS} > V_{BUS_OVLO}$ to $V_{OUT}=0.8 \times V_{BUS}$			150	ns
V_{IF} to BAT Switch						
V_{IF_CLAMP}	Input Clamping Voltage	$I_{IN}=10$ mA		6.4		V
V_{IF_UVLO}	Under-Voltage Trip Level	V_{IF} Rising, $T_A=-40$ to 85°C		2.85	3.05	V
		V_{IF} Falling, $T_A=-40$ to 85°C		2.7		V
V_{IF_OVLO}	Over-Voltage Trip Level	V_{IF} Rising, $T_A=-40$ to 85°C	5.00	5.25	5.50	V
		V_{IF} Falling, $T_A=-40$ to 85°C	4.8			V
R_{ON_VIF}	On-Resistance	$V_{IF}=3.1$ V, $I_{OUT}=1$ A, $T_A=25^\circ\text{C}$		10	15	$\text{m}\Omega$
I_{RCB}	Reverse Current	$V_{IF}=0$ V, $BAT=4.4$ V		3	7	μA
t_{DEB_VIF}	Debounce Time	Time from $V_{IF_UVLO} < V_{IF} < V_{IF_OVLO}$ to $BAT=0.1 \times V_{IF}$		15		ms
t_{QUAL_VIF}	Qualification Time	$BAT > V_{IH_BAT}$ First, Time from $ON > V_{IH_ON(B)}$ to BAT Voltage Increase		30		ms
t_{ON_VIF}	Switch Turn-On Time	$R_L=100$ Ω , $C_L=22$ μF , V_{OUT} from $0.1 \times V_{IF}$ to $0.9 \times V_{IF}$		3		ms
t_{OFF_VIF}	Switch Turn-Off Time	$R_L=100$ Ω , No C_L , $V_{IN} > V_{OVLO}$ to $V_{OUT}=0.8 \times V_{IF}$			150	ns

Note:

- Guaranteed by characterization and design.

Continued on the following page...

Electrical Characteristics

Unless otherwise noted, $V_{BUS}=2.5$ to 23 V, $V_{IF}=3.1$ to 5.5 V, $T_A=-40$ to 85°C ; Typical values are at $V_{BUS}=5$ V, $I_{IN} \leq 2$ A, $V_{IF}=4$ V, $C_{IN}=0.1$ μF and $T_A=25^{\circ}\text{C}$.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{BUS_DET}						
V_{BUS_DET}	V_{BUS_DET} Output Voltage	$V_{BUS}=6.5$ V, $I_{BUS_DET}=0$ mA, $T_A=25^{\circ}\text{C}$	6.0		6.5	V
		$V_{BUS}=15$ V, $I_{BUS_DET}=0$ mA, $T_A=25^{\circ}\text{C}$	6.0	7.0	7.9	V
		$V_{BUS}=6.5$ V, $I_{BUS_DET}=1$ mA, $T_A=25^{\circ}\text{C}$	6.0	6.3	6.5	V
		$V_{BUS}=15$ V, $I_{BUS_DET}=1$ mA, $T_A=25^{\circ}\text{C}$	6.0	7.0	7.9	V
Digital Signals						
$V_{IH_ON(B)}$	Enable HIGH Voltage	V_{BUS} , V_{IF} Operating Range	1.2			V
$V_{IL_ON(B)}$	Enable LOW Voltage	V_{BUS} , V_{IF} Operating Range			0.5	V
V_{IH_BAT}	BAT Presence HIGH Voltage	BAT Rising	2.6			V
V_{IL_BAT}	BAT Presence Low Voltage	BAT Falling			1.7	V
$I_{VBUS_DET_LEAK}$	V_{BUS_DET} Leakage Current	$V_{VBUS_DET}=5$ V, $V_{BUS}=0$ V			1	μA
O_{NB_Leak}	ONB Leakage Current	$V_{BUS}=5$ V, $V_{OUT}=\text{Float}$			1	μA

Timing Diagrams

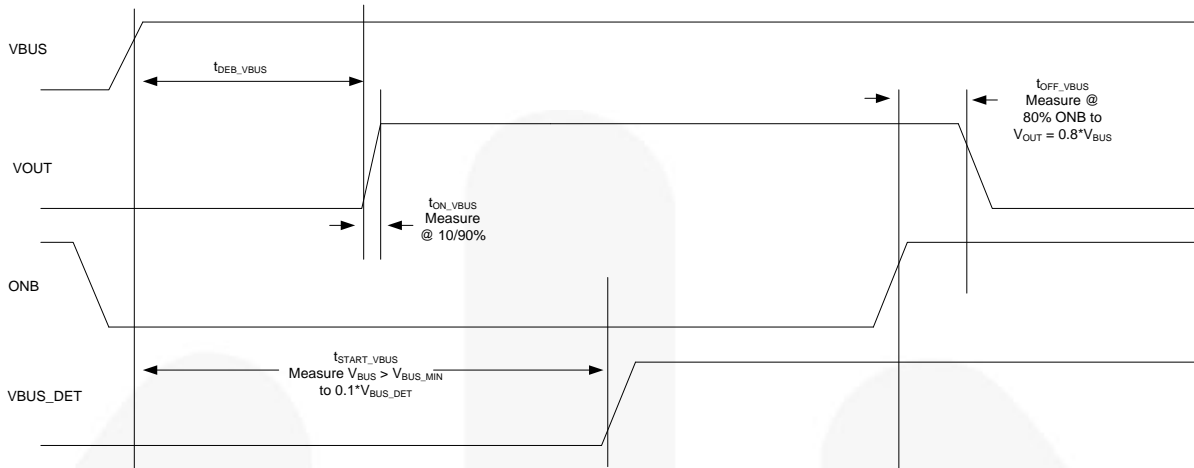


Figure 5. Timing for V_{BUS} Power Up/Down and Normal Operation

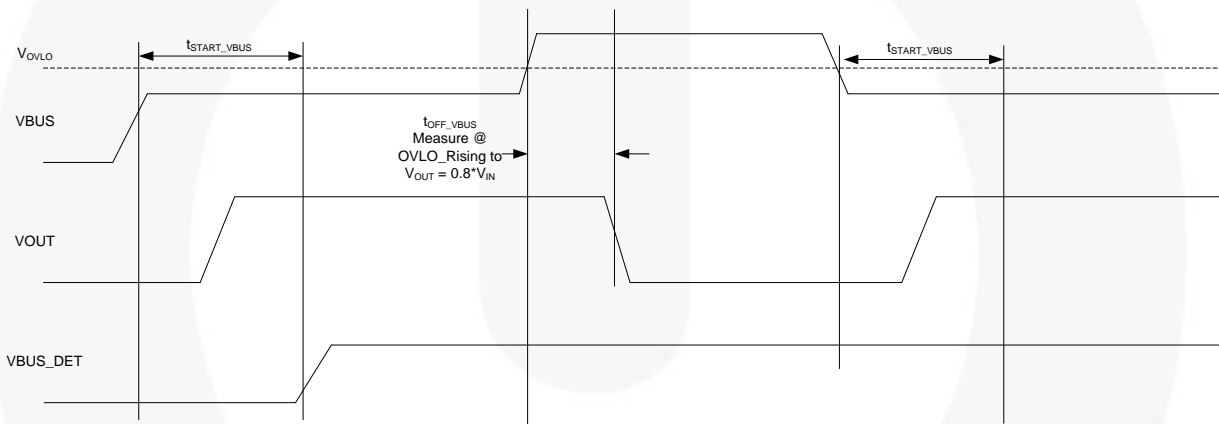


Figure 6. Timing for V_{BUS} OVLO Operation (ONB=LOW)

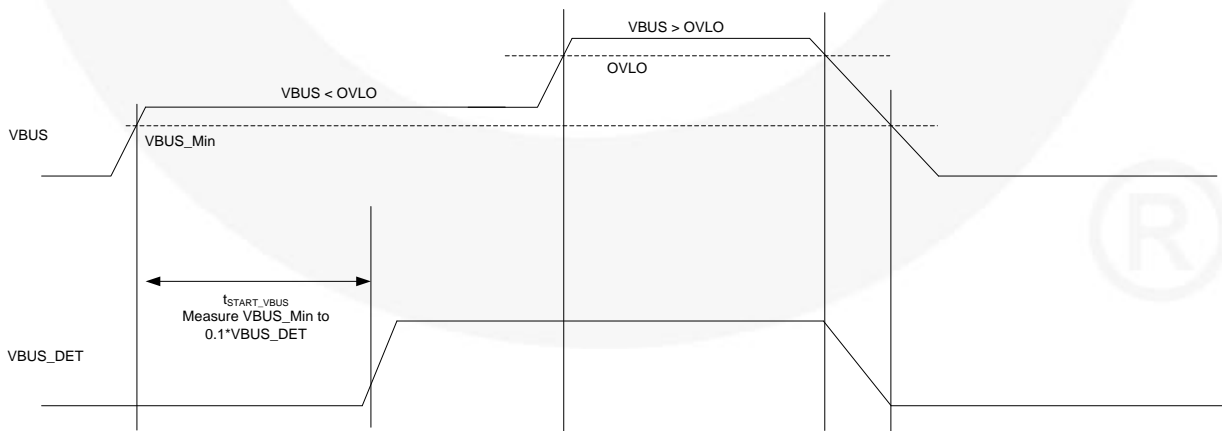


Figure 7. Always ON V_{BUS_DET} Operation (ONB=HIGH)

Timing Diagrams (Continued)

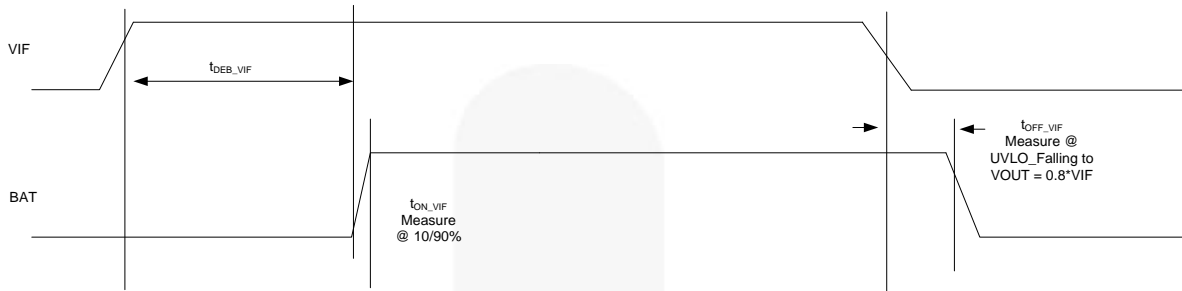


Figure 8. Timing for V_{IF} Power Up/Down and Normal Operation (ON=Don't Care)

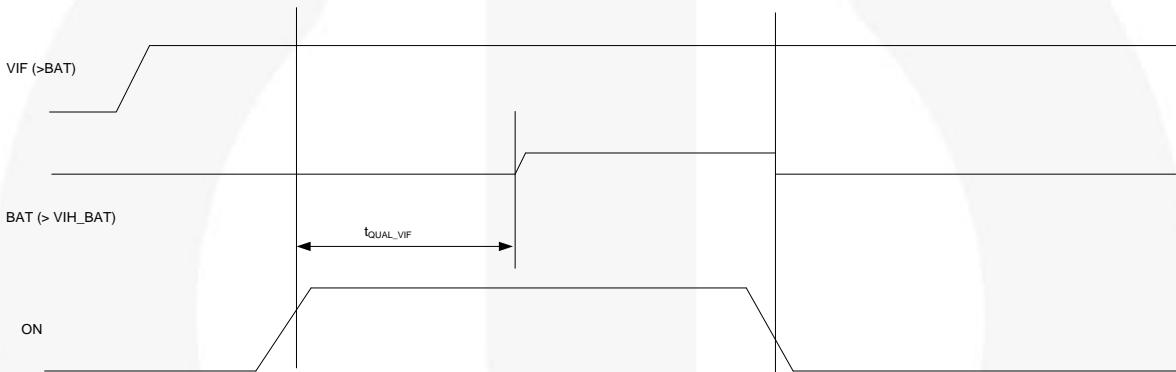


Figure 9. Timing for V_{IF} Power Up/Down and Normal Operation with ON Pin

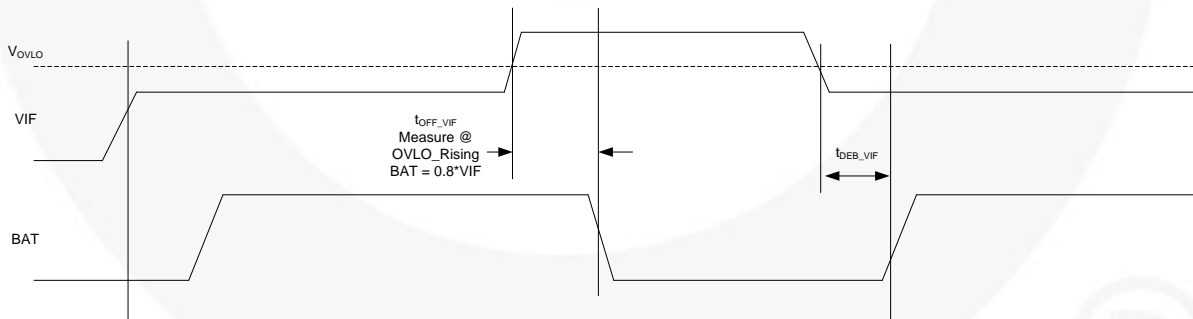


Figure 10. Timing for V_{IF} OVLO Operation (ON=Don't Care)

V_{IF} Turn-On Qualification State Diagram

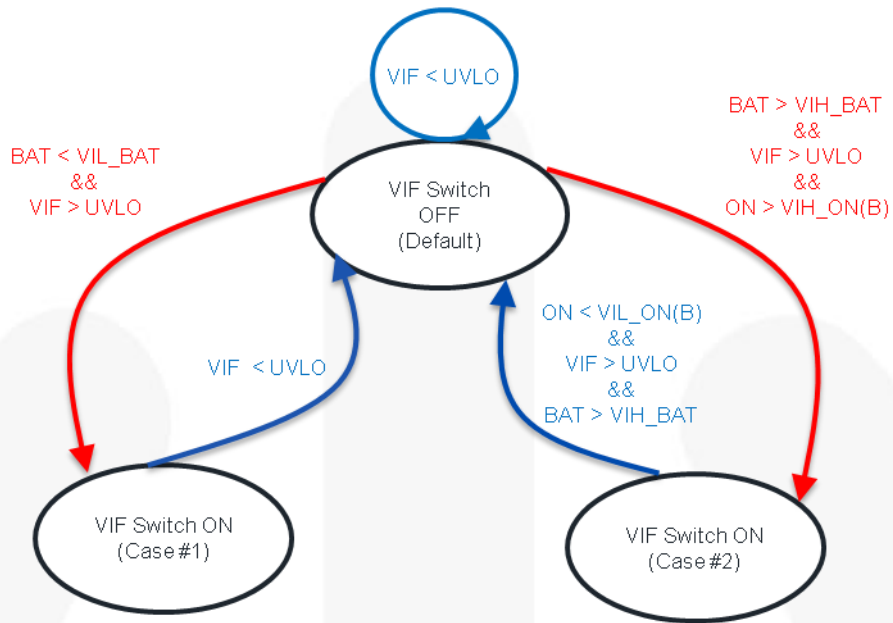


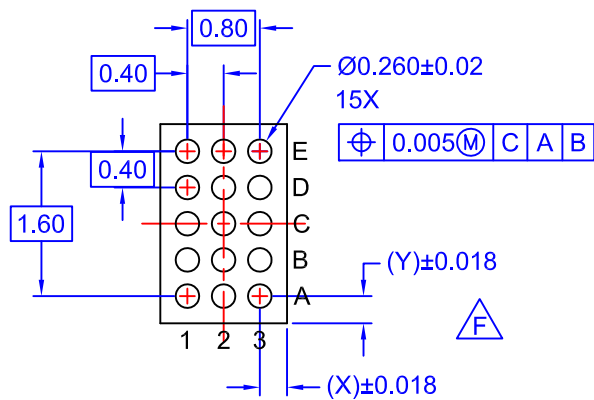
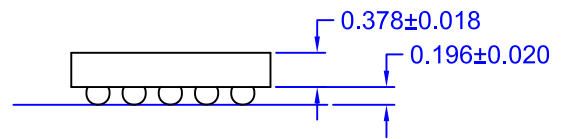
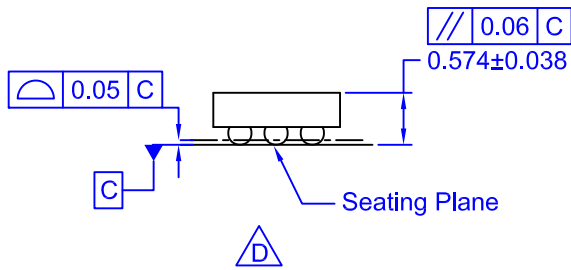
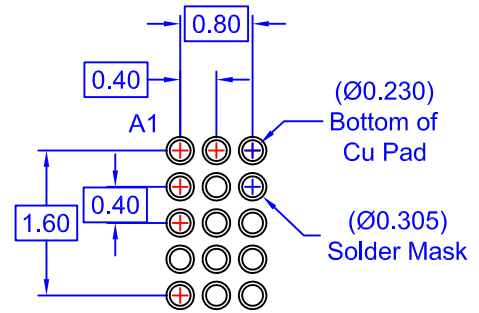
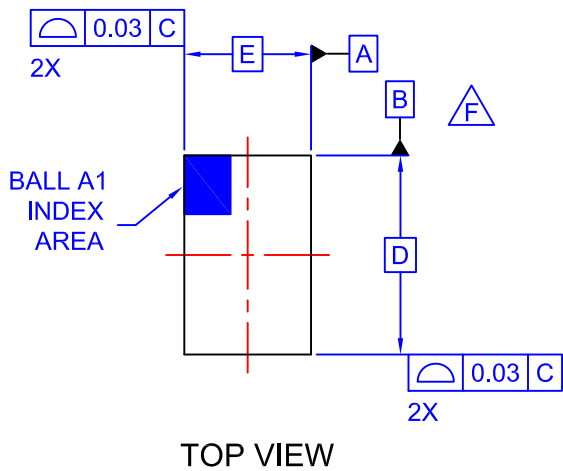
Figure 11. V_{IF} Turn-On Qualification State Diagram

Notes:

- 4. Case #1 is reflecting removable battery system without ON signal.
- 5. Case #2 is reflecting embedded battery system with ON signal.

Product-Specific Dimensions

D	E	X	Y
2200 μm ±30 μm	1600 μm ±30 μm	400 μm ±18 μm	300 μm ±18 μm



NOTES

- A. NO JEDEC REGISTRATION APPLIES.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 2009.
- D.** DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
- E.** PACKAGE NOMINAL HEIGHT IS 574 ± 38 MICRONS (536-612 MICRONS).
- F.** FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.
- G. DRAWING FILNAME: MKT-UC015AC REV2.



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