RFMD + TriQuint = Qorvo

TQF6297H

B7/B30/B38/B40/B41N Front-End Module (FEM)

Applications

- TD-LTE Smartphones, Tablets and Handsets
- Datacards

Product Features

- Single Device for FDD-LTE and TD-LTE Bands
- Module Contains Band 40 and Band 41N Filters
  - B41N Meets China Market Requirements
- LTE Bands and Output Power
  - 7 (2500 – 2570 MHz) +27.5 dBm
  - 30 (2305 – 2315 MHz) +27.5 dBm
  - 38 (2570 – 2620 MHz) +27.5 dBm
  - 40 (2300 – 2400 MHz) +25.0 dBm
  - 41N (2555 – 2655 MHz) +25.0 dBm
- High Efficiency
- 4.0 x 3.0 mm, 24-pin Module

General Description

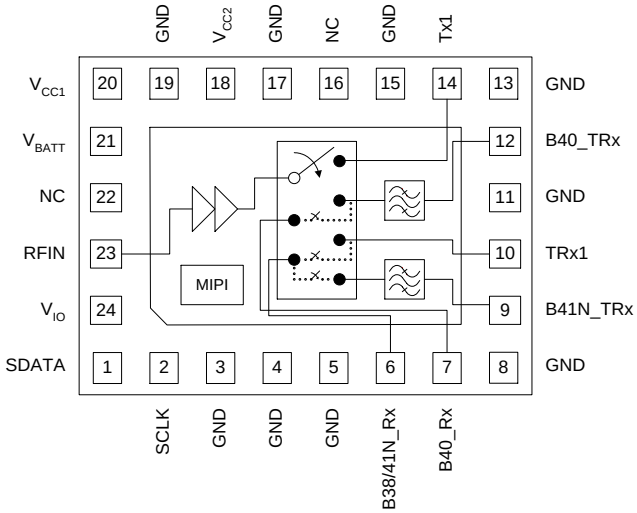
The TQF6297H front-end power amplifier module merges TriQuint's HBT power amplifier, CuFlip®, and BAW filter technologies into one product. This increases module circuit integration which yields an ultra-compact package. The small size and integration allows phone board designer to take one step closer to a small RF solution.

The UHB LTE module's primary bands are Band 40 and Band 41N, while Band 7, Band 30, and Band 38 are auxiliary bands. Band 40 and Band 41N filters meet tough WiFi co-exist specification requirements. Band 38/40/41N Rx is passed through a cross-point switch to reduce the number of filters required for TD-LTE solutions.

Key Performance Specifications

Parameter	B7	B38	B40	B41N	Units
Gain HPM	29	29	26.5	26.5	dB
Output Power	+27.5	+27.5	+25.0	+25.0	dBm
Current (Pmax)	480	480	450	500	mA

Functional Block Diagram



Pin Configuration

Pin No.	Label
1	SDATA
2	SCLK
6	B38/41N_Rx
7	B40_Rx
9	B41N_TRx
10	TRx1
12	B40_TRx
14	Tx1
18	V_{CC2}
20	V_{CC1}
21	V_{BATT}
23	RFIN (B7/B30/B38/B40/B41N)
24	V_{IO}
16,22	NC
3,4,5,8,11,13,15,17,19	GND
Backside Pad	GND

Ordering Information

Part No.	Description
TQF6297H	B7//30/38/40/41 Front-End Module (FEM)

Standard T/R size = 5000 pieces on a 13" reel.

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−40 to +150°C
RF Input Power, CW, 50 Ω, T = 25°C	+15 dBm
Supply Voltage, V_{CC1}, V_{CC2}	−1.0 V to +6 V
Battery Voltage, V_{BATT}	−1.0V to +6 V
Digital Control Voltage (MIPI)	−0.5 to +2.2 V

Operation of this device outside the parameter ranges given above or with multiple absolute maximum ratings applied simultaneously may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{BATT}	+3.0	+3.5	+4.6	V
V_{CC1}, V_{CC2}	+0.8	+3.4	+4.6	V
Interface Supply Voltage VIO	+1.65	+1.8	+1.95	V
Logic Low	0	0	0.2*VIO	V
Logic High	0.8*VIO	+1.8	+1.95	V
Case Temperature	−20		+85	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications: Band 7

Test conditions unless otherwise noted: $V_{CC1} = V_{CC2} = +3.4$ V, V_{BATT}=+3.4, P_{MAX} = min., Temp = 25 °C, $Z_S = Z_L = 50$ Ω, LTE modulation = QPSK, 10M12RB

Parameter	Conditions	Min	Typ	Max	Units
P_{MAX}	QPSK, 10M12RB	+27.5	+28.5		dBm
HPM Gain			29		dB
HPM Gain over Temp	-20°C to 85°C, Vcc = 3.0V to 4.6V	25.75		31	
LPM Gain	$P_{OUT} \leq$ +16 dBm		22.7		dB
LPM Gain over Temp	$P_{OUT} \leq$ +16 dBm, -20°C to 85°C	20.5		25	
Gain Linearity	0 ≤ $P_{OUT} \leq$ +16dBm LPM / 27.5dBm HPM	-1	+/-0.5	1	dB
EUTRA ACLR	$P_{OUT} \leqq P_{MAX}$		−37	−34	dBc
UTRA ACLR1	$P_{OUT} \leqq P_{MAX}$		−38	−35	dBc
UTRA ACLR2	$P_{OUT} \leqq P_{MAX}$		−42	−41	dBc
EVM	$P_{OUT} \leqq P_{MAX}$, all modulations		3	5	%
Current at P_{max}	Vcc = 3.4V, Ibatt + I_{CC1} + I_{CC2}		495	550	mA
Current at +16 dBm	Ibatt + I_{CC1} + I_{CC2}		150	185	mA
Current at 0 dBm	Ibatt + I_{CC1} + I_{CC2}		35		mA
Quiescent current IcQ	LPM Ibatt + I_{CC1} + I_{CC2}, no RF	45	70	105	mA
	HPM Ibatt + I_{CC1} + I_{CC2}, no RF	75	120	145	mA
Phase Variation	Phase shift at 16dBm when switching from HPM to LPM			30	deg
Rx Band Gain	2620 – 2690 MHz		29	31	dB
RX Band Noise Power	20 MHz FRB		-130	−126	dBm/Hz
ISM Band Noise Power	Ch1 – Ch6, 20 MHz FRB		-125	-120	dBm/Hz
	Ch11-Ch12, 20 MHz FRB		-107	-105	
	Ch13, 20 MHz FRB		-102	-98	
GPS Band Noise Power	1563 – 1587 MHz, 20 MHz FRB		-147	−140	dBm/Hz
GLONASS Band Noise Power	1593 – 1606 MHz, 20 MHz FRB		-147	-140	dBm/Hz
BeiDou Band Noise Power	1559 – 1591 MHz, 20MHz FRB		-147	-140	dBm/Hz
2nd Harmonic Power	Pout ≦ P_{max}		-22	−15	dBm
3rd Harmonic Power	Pout ≦ P_{max}		-40	−20	dBm
Input VSWR			2.3:1	3:1	

Electrical Specifications: Band 7 (cont.)

Stability	Load VSWR ≤ 6:1			−36	dBm
Ruggedness[1]	All phases, Pout ≤ maxPout, ETC			8:1	VSWR

Notes:
1. B7, B30, and B38 Load VSWR=8:1 all phases, LTE 5M8RB QPSK U/D config.=0, forward Pout≤+27.5dBm

Electrical Specifications: Band 30

Test conditions unless otherwise noted: V_{CC1} = V_{CC2} = +3.4 V, V_{BATT}=+3.4, P_{MAX} = min., Temp = 25 °C, $Z_S = Z_L$ = 50 Ω, LTE modulation = QPSK, 10M12RB

Parameter	Conditions	Min	Typ	Max	Units
P_{MAX}	QPSK, 10M12RB	+27.5	+28.5		dBm
HPM Gain			27		dB
HPM Gain over Temp	-20°C to 85°C, Vcc = 3.0V to 4.6V	24.25		29.5	dB
LPM Gain	P_{OUT} ≤ +16 dBm		21.2		dB
LPM Gain over Temp	P_{OUT} ≤ +16 dBm, -20°C to 85°C	19.5		23.5	dB
Gain Linearity	0 ≤ P_{OUT} ≤ +16dBm LPM / 27.5dBm HPM	-1	+/-0.5	1	dB
EUTRA ACLR	P_{OUT} ≦ P_{MAX}		−38	−34	dBc
UTRA ACLR1	P_{OUT} ≦ P_{MAX}		−40	−35	dBc
UTRA ACLR2	P_{OUT} ≦ P_{MAX}		−42	−41	dBc
EVM	P_{OUT} ≦ P_{MAX} , all modulations		3	5	%
Current at P_{max}	Vcc = 3.4V, Ibatt + I_{CC1} + I_{CC2}		490	570	mA
Current at +16 dBm	Ibatt + I_{CC1} + I_{CC2}		150	175	mA
Current at 0 dBm	Ibatt + I_{CC1} + I_{CC2}		30		mA
Quiescent current IcQ	LPM Ibatt + I_{CC1} + I_{CC2}, no RF	45	80	105	mA
	HPM Ibatt + I_{CC1} + I_{CC2}, no RF	75	110	145	mA
Rx Band Gain	2350 – 2360 MHz		27	29.5	dB
RX Band Noise Power	10 MHz FRB		-121	−115	dBm/Hz
GPS Band Noise Power	1563 – 1587 MHz, 20 MHz FRB		-149	−145	dBm/Hz
GLONASS Band Noise Power	1593 – 1606 MHz, 20 MHz FRB		-149	−145	dBm/Hz
BeiDou Band Noise Power	1559 – 1591 MHz, 20MHz FRB		-149	-145	dBm/Hz
2nd Harmonic Power	Pout ≦ P_{max}		-20	−14	dBm
3rd Harmonic Power	Pout ≦ P_{max}		-33	−20	dBm
Input VSWR			3.1:1	3.3:1	
Stability	Load VSWR ≤ 6:1			−36	dBm
Ruggedness[1]	All phases, Pout ≤ maxPout			8:1	VSWR

Notes:
1. B7 and B38 Load VSWR=8:1 all phases, LTE 5M8RB QPSK U/D config.=0, forward Pout≤+27.5dBm

Electrical Specifications: Band 38

Test conditions unless otherwise noted: $V_{CC1} = V_{CC2}$ = +3.4 V, V_{BATT}=+3.4 V, P_{MAX} = min., Temp. = 25 °C, $Z_S = Z_L$ = 50 Ω, LTE modulation = QPSK, 10M12RB

Parameter	Conditions	Min	Typ	Max	Units
P_{MAX}	QPSK, 10M12RB	+27.5	+29		dBm
HPM Gain			30		dB
HPM Gain over Temp	-20°C to 85°C	26		31.50	
LPM Gain	$P_{OUT} \leq$ +16 dBm		22.5		dB
LPM Gain over Temp	$P_{OUT} \leq$ +16 dBm, -20°C to 85°C, Vcc = 3.0V to 4.6V	20.5		25	
Gain Linearity	0 ≤ $P_{OUT} \leq$ +16dBm LPM / 27.5dBm HPM	-1	+/-0.5	1	dB
EUTRA ACLR	$P_{OUT} \leqq P_{MAX}$		−37	−34	dBc
UTRA ACLR1	$P_{OUT} \leqq P_{MAX}$		−38	−35.5	dBc
UTRA ACLR2	$P_{OUT} \leqq P_{MAX}$		−42	−40	dBc
EVM	$P_{OUT} \leqq P_{MAX}$, all modulations		3	5	%
Current at P_{max}	Vcc = 3.4V, Ibatt + I_{CC1} + I_{CC2}		530	580	mA
Current at +16 dBm	Ibatt + I_{CC1} + I_{CC2}		155	185	mA
Current at 0 dBm	Ibatt + I_{CC1} + I_{CC2}		36		mA
Quiescent current IcQ	LPM Ibatt + I_{CC1} + I_{CC2}, no RF	45	70	105	mA
	HPM Ibatt + I_{CC1} + I_{CC2}, no RF	145	180	230	mA
Phase Variation	Phase shift at 16dBm when switching from HPM to LPM			30	deg
ISM Band Noise Power	Ch1 – Ch6, 20 MHz FRB		−135	-130	dBm/Hz
	Ch11-Ch12, 20 MHz FRB		-131	-128	
	Ch13, 20 MHz FRB		-130	-125	
B1 Rx Noise Power	2110 – 2170 MHz, 20 MHz FRB		-138	−134	dBm/Hz
GPS Band Noise Power	1563 – 1587 MHz, 20 MHz FRB		-146	−140	dBm/Hz
GLONASS Band Noise Power	1593 – 1606 MHz, 20 MHz FRB		-146	−140	dBm/Hz
BeiDou Band Noise Power	1559 – 1591 MHz, 20MHz FRB		-146	-140	dBm/Hz
2nd Harmonic Power	Pout ≦ P_{max}		-24	−15	dBm
3rd Harmonic Power	Pout ≦ P_{max}		-37	−20	dBm
Input VSWR			1.4:1	3:1	
Stability	Load VSWR ≤ 6:1			−36	dBm
Ruggedness[1]	All phases, Pout ≤ max Pout			8:1	VSWR

Notes:
1. B7, B30, and B38 Load VSWR=8:1 all phases, LTE 5M8RB QPSK U/D config.=0, forward Pout ≤ +27.5dBm

Electrical Specifications: Band 40

Test conditions unless otherwise noted: V_{CC1} = V_{CC2} = +3.4 V, V_{BATT}=+3.4 V, P_{MAX} = min., Temp = 25 °C, Z_S = Z_L = 50 Ω, LTE modulation = QPSK, 10M12RB

Parameter	Conditions	Min	Typ	Max	Units
P_{MAX}	QPSK, 10M12RB	+25	+26		dBm
HPM Gain	Pout ≤ max Pout		25		dB
HPM Gain over Temp	Pout ≤ max Pout, -20°C to 85°C	21.25		28.75	
LPM Gain	Pout ≤ +14 dBm		19		dB
LPM Gain over Temp	Pout ≤ +14 dBm, -20°C to 85°C	16.5		23	
Gain Linearity	0 ≤ P_{OUT} ≤ +14dBm LPM / 25dBm HPM	-1	+/-0.5	1	dB
EUTRA ACLR	P_{OUT} ≦ P_{MAX}		−36	−34	dBc
UTRA ACLR1	P_{OUT} ≦ P_{MAX}, Cf<2305MHz		−36	−35.5	dBc
	P_{OUT} ≦ P_{MAX}, 2307.5MHz<Cf<2397.5MHz		-39	-35.5	dBc
UTRA ACLR2	P_{OUT} ≦ P_{MAX}		−41	−39	dBc
EVM	P_{OUT} ≦ P_{MAX} , all modulations		3	5	%
Current at P_{max}	Vbatt = 3.4V, Ibatt + I_{CC1} + I_{CC2}		450	600	mA
Current at +14 dBm	Ibatt + I_{CC1} + I_{CC2}		150	195	mA
Current at 0 dBm	Ibatt + I_{CC1} + I_{CC2}		35		mA
Quiescent current IcQ	LPM Ibatt + I_{CC1} + I_{CC2}, no RF	45	70	105	mA
	HPM Ibatt + I_{CC1} + I_{CC2}, no RF	75	120	145	mA
Phase variation	Phase shift at 14dBm when switching from HPM to LPM		10	30	Deg.
ISM Band Noise Power	Ch1, 20 MHz FRB		-103	-100	dBm/Hz
	Ch3, 20 MHz FRB		-118	-115	dBm/Hz
	Ch6, 20 MHz FRB		-138	-135	dBm/Hz
	Ch11-Ch12		-164	-160	dBm/Hz
B1 Rx Noise Power	2110 – 2170 MHz, 20 MHz FRB		-160	-155	dBm/Hz
GPS Band Noise Power	1563 – 1587 MHz, 20 MHz FRB		-166	-160	dBm/Hz
GLONASS Band Noise Power	1593 – 1606 MHz, 20 MHz FRB		-166	-160	dBm/Hz
BeiDou Band Noise Power	1559 – 1591 MHz, 20MHz FRB		-166	-160	dBm/Hz
2nd Harmonic Power	Pout ≦ P_{max}		-42	−34	dBm
3rd Harmonic Power	Pout ≦ P_{max}		-58	-40	dBm
Input VSWR	Cf=2320-2397.5MHz		2:1	3:1	
	Cf<2320MHz		3:1	3.5:1	
Stability	Load VSWR ≤ 10:1			−36	dBm
Ruggedness[1]	All phases, Pout ≤ max Pout			10:1	VSWR

Notes:

1. B40 and B41N Load VSWR=10:1 all phases, LTE 5M8RB QPSK U/D config.=0, forward Pout ≤ +25dBm

Electrical Specifications: Band 41N

Test conditions unless otherwise noted: $V_{CC1} = V_{CC2}$ = +3.4 V, V_{BATT}=+3.4 V, P_{MAX} = min, Temp = 25 °C, $Z_S = Z_L$ = 50 Ω, LTE modulation = QPSK, 10M12RB

Parameter	Conditions	Min	Typ	Max	Units
P_{MAX}	QPSK, 10M12RB	+25	+26		dBm
HPM Gain	$P_{OUT} \leqq P_{MAX}$		27		dB
HPM Gain over Temp	$P_{OUT} \leqq P_{MAX}$, -20°C to 85°C	23.7		30.25	
LPM Gain	Pout≤14dBm		20		dB
LPM Gain over Temp	Pout≤14dBm, -20°C to 85°C	17		23	
Gain Linearity	$0 \leq P_{OUT} \leq$ +14dBm LPM / 25dBm HPM	-1	+/-0.5	1	dB
EUTRA ACLR	$P_{OUT} \leqq P_{MAX}$		-37	-34	dBc
UTRA ACLR1	$P_{OUT} \leqq P_{MAX}$		-38	-36	dBc
UTRA ACLR2	$P_{OUT} \leqq P_{MAX}$		-43	-40	dBc
EVM	$P_{OUT} \leqq P_{MAX}$, all modulations		3	5	%
Current at P_{max}	Vcc = 3.4V, Ibatt + I_{CC1} + I_{CC2}		500	615	mA
Current at +14 dBm	Ibatt + I_{CC1} + I_{CC2}		156	200	mA
Current at 0 dBm	Ibatt + I_{CC1} + I_{CC2}		40		mA
Quiescent current IcQ	LPM Ibatt + I_{CC1} + I_{CC2}, no RF	55	90	120	mA
	HPM Ibatt + I_{CC1} + I_{CC2}, no RF	145	190	230	mA
Phase variation	Phase shift at 14dBm when switching from HPM to LPM		7	30	Deg.
ISM Band Noise Power	Ch1 – Ch6, 20 MHz FRB		-170	-165	dBm/Hz
	Ch11-Ch12, 20 MHz FRB		-166	-164	
	Ch13, 20 MHz FRB		-148	-145	
B1 Rx Noise Power	2110 – 2170MHz, 20MHz FRB		-148	-145	dBm/Hz
GPS Band Noise Power	1563 – 1587MHz, 20MHz FRB		-170	-165	dBm/Hz
GLONASS Band Noise Power	1597 – 1606MHz, 20MHz FRB		-170	-165	dBm/Hz
BeiDou Band Noise Power	1559 – 1591MHz, 20MHz FRB		-170	-165	dBm/Hz
2nd Harmonic Power	Pout ≦ P_{max}		-47	−40	dBm
3rd Harmonic Power	Pout ≦ P_{max}		-66	−40	dBm
Input VSWR			1.5:1	3:1	
Stability	Load VSWR ≤ 10:1			−36	dBm
Ruggedness[1]	All phases, Pout ≤ maxPout			10:1	VSWR

Notes:
1. B40 and B41N Load VSWR=10:1 all phases, LTE 5M8RB QPSK U/D config.=0, forward Pout ≤ +25dBm

Electrical Specifications: Rx Band 38

Test conditions unless otherwise noted: $V_{CC1} = V_{CC2}$ = +3.4 V , V_{BATT}=+3.4 V, P_{MAX} = min, Temp = 25 °C, $Z_S = Z_L$ = 50 Ω, LTE modulation = QPSK, 10M12RB

Parameter	Conditions	Min	Typ	Max	Units
Insertion Loss	2570 – 2620 MHz, Ta=+25C		0.6	0.8	dB
Rx VSWR	2300 – 2400 MHz, Typical at +25 °C		1.2	2	VSWR

Electrical Specifications: Rx Band 40

Test conditions unless otherwise noted: $V_{CC1} = V_{CC2}$ = +3.4 V , V_{BATT}=+3.4 V, P_{MAX} = min, Temp = 25 °C, $Z_S = Z_L$ = 50 Ω

Parameter	Conditions	Min	Typ	Max	Units
Insertion Loss[1]	2300 – 2310 MHz		2.3	3.3	dB
	2310-2390 MHz		1.9	3.0	
	2390-2400 MHz		2.3	3.6	
Integrated Insertion Loss[2]	2300 – 2310 MHz		2.3	3.0	dB
	2310 – 2320 MHz		1.8	2.5	
	2320 – 2330 MHz		1.8	2.6	
	2330 - 2340 MHz		1.9	2.8	
	2340 - 2350 MHz		2.0	2.9	
	2350 - 2360 MHz		1.9	2.9	
	2360 – 2370 MHz		1.9	2.9	
	2370 - 2380 MHz		1.8	2.8	
	2380 - 2390 MHz		2.0	3.0	
	2390 - 2400 MHz		2.3	3.3	
Input / Output VSWR	2300 – 2400 MHz		1.9	2.2	
Attenuation	10 – 1574 MHz	35	37		dB
	1574 – 1577 MHz	35	37		
	1577 – 1680 MHz	33	35		
	1845 – 1880 MHz	30	33		
	2110 – 2170 MHz	30	32		
	2420 – 2427 MHz	26	32		
	2427 – 2460 MHz	45	55		
	2460 – 2500 MHz	40	42		
	4600 – 4800 MHz	38	41		
	6900 – 7200 MHz	20	23		

Note:
1. Typical values are derived from the integration of the specified band in the “Conditions” column.
2. Typical values are derived through integration of the linear s-parameters over a 10MHz frequency span. Values were derived from Trim 2 simulations.

Electrical Specifications: Rx Band 41N

Test conditions unless otherwise noted: $V_{CC1} = V_{CC2}$ = +3.4 V, V_{BATT}=+3.4 V, P_{MAX} = min, Temp = 25 °C, $Z_S = Z_L$ = 50 Ω, LTE modulation = QPSK, 10M12RB

Parameter	Conditions	Min	Typ	Max	Units
B41N Insertion Loss[1]	2555 – 2655 MHz		2.9	3.3	dB
Integrated Insertion Loss[2]	2.555 – 2.655 MHz		2.9	3.4	dB
	2.555 – 2.565 MHz		2.9	3.4	dB
	2.565 – 2.575 MHz		2.9	3.4	dB
	2.575 – 2.585 MHz		2.8	3.4	dB
	2.585 – 2.595 MHz		2.9	3.4	dB
	2.595 – 2.605 MHz		2.9	3.4	dB
	2.605 – 2.615 MHz		2.9	3.4	dB
	2.615 – 2.625 MHz		2.9	3.4	dB
	2.625 – 2.635 MHz		2.8	3.3	dB
	2.635 – 2.645 MHz		2.9	3.3	dB
	2.645 – 2.655 MHz		2.8	3.3	dB
Input / Output VSWR	2555 – 2655 MHz		1.6	2	
Attenuation	10 – 1564 MHz	36	39		dB
	1565 – <1710MHz	35	38		
	1710 – 1980MHz	15	19.6		
	>1980 – 2300MHz	5	7.8		
	>2300 – 2400MHz	9	10.6		
	2401 – 2468 MHz (WiFi Ch1 – Ch10)	39	41		
	2451 – 2473 MHz (WiFi Ch11)	38	44		
	2456 – 2478 MHz (WiFi Ch12)	36	52		
	2461 – 2483 MHz (WiFi Ch13)	25	35.3		
	2775 – 4991 MHz	12	14		
	4992 – 5380 MHz	30	33		
	5381 – 7487 MHz	21	22		
	7488 – 8000 MHz	22	24		

Notes:
1. Typical values are derived from the integration of the specified band in the “Conditions” column.
2. Typical values are derived through integration of the linear s-parameters over a 10MHz frequency span.

Module Port Isolation Specification

Test conditions: V_{CC1} = V_{CC2} = +3.4 V, V_{BATT}=+3.4 V, P_{MAX} = min, Temp = -20 °C to +85 °C, Z_S = Z_L = 50 Ω

	Tx1	TRx1	B40_TRx	B41_TRx	B40_Rx	B38/41_Rx
B7 Transmit (Tx1)	Active	25dB	30dB	38dB	27dB	23dB
B30 Transmit (TRx1)	28dB	Active	30dB	25dB	25dB	21dB
B38 Transmit (TRx1)	27dB	Active	39dB	26dB	28dB	21dB
B40 Transmit (B40_TRx)	25dB	25dB	Active	31dB	24dB	24dB
B41 Transmit (B41_TRx)	32dB	21	47	Active	28dB	21dB
B38 Receive (B38/41_Rx)	35dB	Active	40dB	30dB	36dB	Active
B40 Receive (B40_Rx)	27dB	35dB	Active	35dB	Active	27dB
B41 Receive (B38/41_Rx)	48dB	29dB	58dB	Active	25dB	Active

Electrical Specifications: Common Parameters

Test conditions unless otherwise noted: Rel99, V_{CC1} = V_{CC2} = +3.4 V , V_{BATT}=+3.8 V, Temp.=+25 °C

Parameter	Conditions	Min	Typ	Max	Units
Ibatt Leakage Current	Vbatt = 5.0V; Vcc1, Vcc2 = 0			5	µA
Sleep Mode Current	Vbatt = 5.0V; Vcc1, Vcc2 = 5.0V			10	µA
Enable ON Time[1]	Time between falling edge of SCLK during Bus Park and module ready for RFIN			5	µS
Enable OFF Time[2]	Time to sleep mode following falling edge of SCLK during Bus Park with x00 write to Reg0			5	µS
Mode Switching Time	Time between falling edge of SCLK during Bus Park and HPM to LPM or LPM to HPM transition			2	µS

Notes:

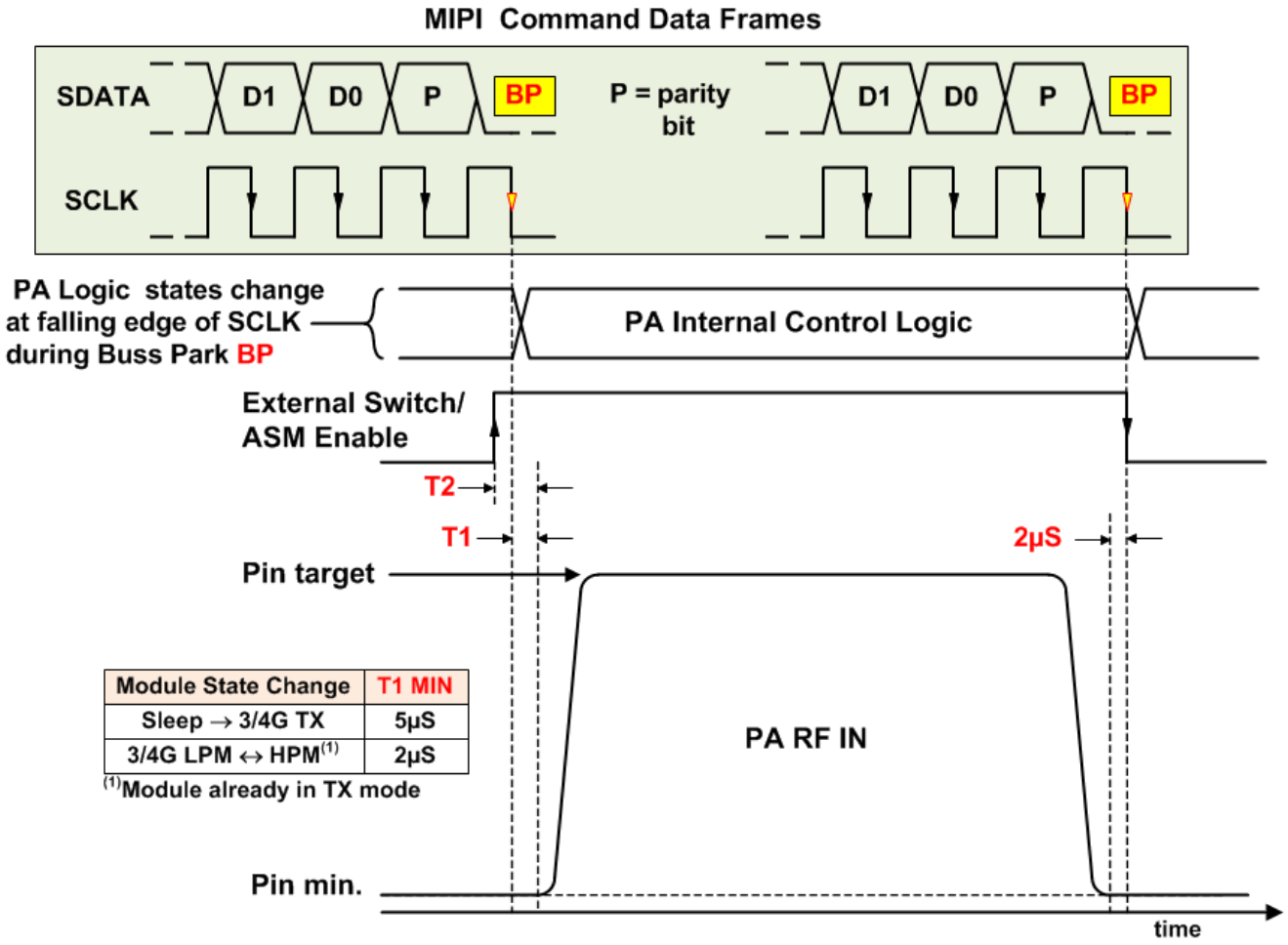
1: Enable ON time is the minimum recommended wait time between the MIPI write to Reg 0 enabling the PA (as defined by the SCLK transition at Bus Park) and the application of RF input. Metric: Time for RF output to settle within +/-1dB of final value for a constant RF input 6dB below (to prevent PA damage) that required to deliver rated maximum output power, with time referenced to the rising edge of LB or HB_EN. ***Failure to comply with this specification may result in RF output distortion and module damage.***

2: Enable OFF time is the minimum recommended wait time between the removal of RF input and the MIPI write to Reg 0 putting the part in sleep mode (as defined by the SCLK transition at Buss Park). ***Failure to comply with this specification may result in RF output distortion and module damage.***

MIPI RFFE Operation

MIPI RFFE Interface	Min	Typ	Max	Units
Interface Supply Voltage VIO	+1.65	+1.8	+1.95	V
Logic Low	0	0	0.2 * VIO	V
Logic High	0.8 * VIO	+1.8	+1.95	V
Active Mode VIO current			1.25	mA
SHUTDOWN Mode VIO current			5	uA
SCLK write frequency	0.03	26	29	MHz
SCLK read frequency	0.03	13	14.5	MHz
SDATA/SCLK input capacitance		2	3	pF
SDATA/SCLK load capacitance	10		50	pF
Delay of data line at the slave's pad output with respect to SCLK for Full-Rate (Td)			10.25	nS
Delay of data line at the slave's pad output with respect to SCLK for Half-Rate (Td)			22	nS
T(SDataOTR) (Full-Rate)	2.1		6.5	nS
T(SDataOTR) (Half-Rate)	2.1		10	nS
Data setup time (Ts)	1			nS
Data hold time (Th)	5			nS

Timing Diagram



Module State Change	T1 MIN
Sleep → 3/4G TX	5µS
3/4G LPM ↔ HPM(1)	2µS

(1)Module already in TX mode

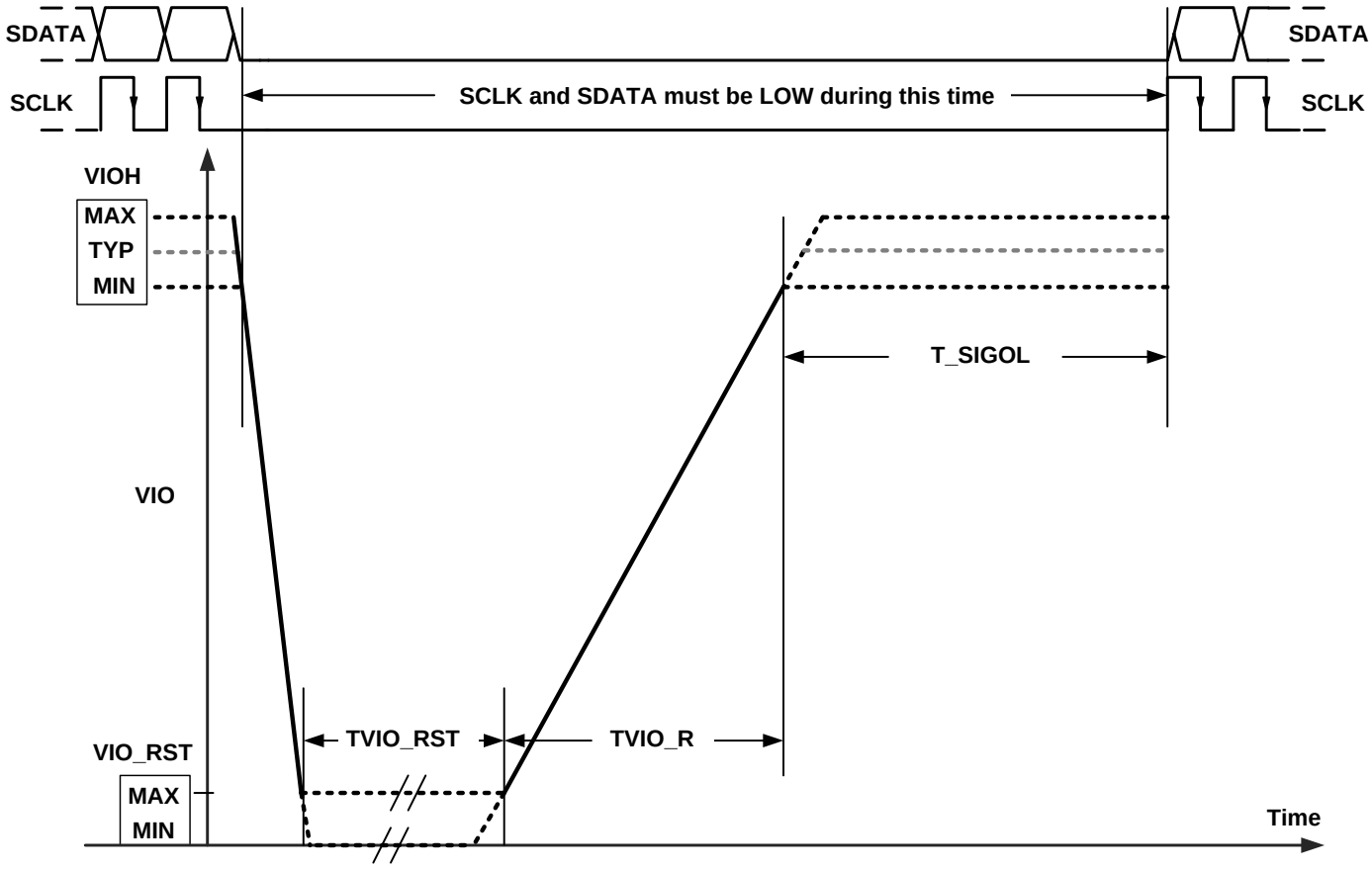
Delay application of PA RF IN by at least T1 µS after PA MIPI Data Frame Buss Park BP
Do not transition logic states until 2µS *after* RF input has been removed (PA RF IN = Pin min.)
Enable External Switch/ ASM T2 uS before PA RF IN. T2 = maximum Switch/ ASM turn on time.

Failure to comply with this specification may result in RF output distortion or module damage

VIO Power On Reset (POR)Timing

For applications where MIPI VIO is turned ON/ OFF in accordance with MIPI buss activity, the timing recommendations below should be used to ensure error-free MIPI register writes following VIO power on reset (POR)

Parameter	Description	MIN	TYP	MAX
VIOH	VIO HIGH Voltage	1.65V	1.80V	1.95V
VIO_RST	VIO Reset Voltage	0V	0V	0.2V
TVIO_RST	Time to hold VIO L for proper MIPI reset	10µS	-	-
TVIO_R	Restriction on VIO Rise Time	1µS	-	400µS
T_SIGOL	Time to wait after TVIO_R before writing to MIPI registers	560µS	-	-



MIPI Description

The RFFE interface implemented in the TQF6297H is described in detail in the MIPI Alliance Specification for RF Front-End Control Interface, as shown in [1].

Referenced Documents

[1] MIPI Alliance Specification for RF Front-End Control Interface, Version 1.10a – 26 July 2011

Register Map Overview

RW Type	Register Address	Name	Description
R/W	0x00	PA_CNTRL0	PA_CTRL0
R/W	0x01	PA_CNTRL1	PA_BIAS ADJUST (bits 7:4 DAC1, bits 3:0 DAC2)
R/W	0x02	PA_CNTRL2	PA Turn-on delay
N/A	0x1A	Reserved	Reserved
RW	0x1B	GSID	Group Slave ID register requires USID as slave address to program;
R/W	0x1C	PM_TRIG	Power Mode and Trigger Register
R	0x1D	PRODUCT_ID	read-only product ID, settable in metal
R	0x1E	MANUFACTURER_ID	read-only manufacturer ID (0x86 for TQS)
R/W	0x1F	SPARE(1:0) MANUFACTURER_ID(9:8) USID(3:0)	MIPI Logic Input – Sets LSB of USID Manufacturer ID 9:8 (0x2 for TQS)

Note: RW = read / write capable
R = read only

Applying VIO to the RFFE Bus shall power on the slave interfaces and set the registers to default state as described below

Register_1A, Reserved, 0x1A, 00011010_B

Bit	Function	Broadcast Support	GSID Support	Trigger Support	R/W	Default
7:0	Reserved	N/A	N/A	N/A	N/A	N/A

Register_0, PA_CTRL0, 0x00, 00000000_B, read/write

Register 0, if accessed by a register 0 write command, has the shortest telegram length. However, a “Register 0 Write” command only writes the 7 LSBs of Register 0. Bit 7 of register 0 can only be written with a standard register write, short register 0 write is not recommended. The content of these bits is used for most critical timing signals.

Bit	Function	Broadcast Support	GSID Support	Trigger Support	R/W	Default
7	Unused, read 0 write ignored	yes*	yes*	yes	R/W	
6	Two PA support, not applicable for TQF6297H	yes*	yes*	yes	R/W	0
5	Tx/Rx Mode Select - TxRx_2 (MSB), see truth table	yes*	yes*	yes	R/W	0
4	Tx/Rx Mode Select - TxRx_1, see truth table	yes*	yes*	yes	R/W	0
3	Tx/Rx Mode Select - TxRx_0, see truth table	yes*	yes*	yes	R/W	0
2	PA Enable – 0 = PA Off, 1 = PA On	yes*	yes*	yes	R/W	0
1:0	00 – High Power Mode (HPM)	yes*	yes*	yes	R/W	10
	01 – High Power Mode (HPM)	yes*	yes*	yes		
	10 – Low Power Mode (LPM)	yes*	yes*	yes		
	11 – Unused, neither bias mode will be on	yes*	yes*	yes*		
	11 – Unused, neither bias mode will be on					

Note: yes* means: only valid, if broadcast_en bit (register GSID, 0x1B, bit D[4] is set to “1”, otherwise no.

Register_1, PA_CTRL1, 0x01, 00000001B, read/write

Bit	Function	Broadcast Support	GSID Support	Trigger Support	R/W	Default
7:4	PA Driver stage bias adjust, DAC1, 0000 = min Icq, 1111 = max Icq	yes*	yes*	yes	R/W	0000
3:0	PA Final stage bias adjust, DAC2, 0000 = min Icq, 1111 = max Icq	yes*	yes*	yes	R/W	0000

Register_2, PA_CTRL2, 0x02, 00000010B, read/write

A programmable delay between application of the SOI output switch supply voltage and PA bias is included to reduce the chances of PA damage due to incorrect control timing. This delay can be used to prevent the PA from delivering RF output into the switch before it has settled. The delay is set via the PA_CNTRL2 register, with default value of 0.75uS

Bit	Function	Broadcast Support	GSID Support	Trigger Support	R/W	Default
7:2	Unused	yes*	yes*	yes	R/W	000000
1:0	PA turn-on delay as shown in table below	yes*	yes*	yes	R/W	00

PA_CNTRL2 (0x02) Setting	Min	Typ	Max	Units
0x00		0.53		µS
0x01		1.21		µS
0x02		1.66		µS
0x03		2.14		µS

Register_GSID, 0x1B, 00000011B, read/write

This register contains the Group Slave ID and additional options for the MIPI RFFE Slave configuration. Note: This register may only be written with the current USID, per paragraph 287 of [1].

Additional options for the MIPI RFFE interface configuration:

- The broadcast_en bit determines whether the part will respond to Broadcast ID or GSID commands on all registers or only the PM_TRIG register (default).
  - Note that the Slave will never respond to reads with either the Broadcast ID or GSID.
  - There are four registers that will not respond to writes with the Broadcast ID or GSID.
    1. The read-only PRODUCT_ID register 0x1D will never respond to Broadcast ID or GSID reads.
    2. The read-only MANUFACTURER_ID register 0x1E will never respond to Broadcast ID or GSID reads.
    3. The GSID register 0x1B can only be updated by writes using the current USID.
    4. The USID register can only be written by following the specified MIPI USID programming sequence using the USID.

Bit	Function	R/W	Default
7:5	Spare Bits (not used)	R/W	0
4	Broadcast enable: 0 – broadcasts and GSID programming can only access PM_TRIG (0x1c) 1 – broadcasting and GSID programming can access all registers	R/W	0
3:0	Group Slave ID	R/W	0000

Register PM_TRIG, 0x1C, 00011100_B, read/write

This register is broadcast capable, however, this applies to the PWR_MODE[1:0] bits and the Triggers, but not the Trigger Masks. See [1], sections 6.5 and 6.9.

The PWR_MODE[1:0] bits determine the operating mode of the IC via the output values from the MIPI RFFE interface. These provide:

- A full reset, returning the part to the Default Settings (PWR_MODE=01).
- A low power mode wherein all register outputs to the IC are gated to 0 (PWR_MODE=10).

Notes on power modes:

- The PWR_MODE bits can be written with any valid ID (SA), including the current USID, GSID and Broadcast ID.

The Trigger Mask and Trigger bits provide a method of pre-loading the next register values and holding the update, leaving the previous values at the outputs, until the Trigger bit is written. In this MIPI RFFE Slave implementation, all user defined registers are responsive to all three triggers and masks. These are Registers 0, 1, 2, 3 and 4. The Trigger Mask bits can be accessed only with a write using the current USID per paragraph 315 of the MIPI Specification [1]. The MIPI system registers, 0x1A through 0x1F are not shadowed and are unaffected by the Trigger.

NOTE: Per [1], the Triggers are active by default. After a reset, updates to user registers will not take effect until the Trigger is written, or until the Trigger Mask bit is set to 1.
NOTE: Per the MIPI RFFE Specification [1] paragraph 315, the Trigger Mask bits may only be written with the USID address.
NOTE: For clarity: When a Trigger is masked/disabled, write data goes directly to the destination register. By default the Trigger is Enabled (Mask==0 /not masked) and writes to user registers **DO NOT** take effect until the Trigger is written.

Bit	Function	Broadcast Support	GSID Support	Trigger Support	R/W	Default
7:6	pwr_mode[1:0] 00 = Normal Operation Mode 01 = Default Settings (STARTUP); returns the part to default settings 10 = LOW POWER Mode 11 = Reserved	yes	yes	yes	R/W	00
5	trig_mask2 0=Trigger 2 Mask disabled / Trigger 2 Enabled (not Masked off). 1=Trigger 2 Mask enabled / Trigger 2 is Disabled (Masked off).	no	no	no	R/W	0
4	trig_mask1 0=Trigger 1 Mask disabled / Trigger 1 Enabled (not Masked off). 1=Trigger 1 Mask enabled / Trigger 1 Disabled (Masked off).	no	no	no	R/W	0
3	trig_mask0 0=Trigger 0 Mask disabled / Trigger 0 Enabled (not Masked off). 1=Trigger 0 Mask enabled / Trigger 0 Disabled (Masked off). When a Trigger is masked/disabled, write data goes directly to the destination. By default the Trigger is Enabled (Mask==0 /not masked) and writes to user registers DO NOT take effect until the Trigger is written.	no	no	no	R/W	0
2	Trigger[2] A write of a 1 to this bit loads any pending user register updates if Trigger Mask 2 == 0. This bit always reads as a 0, and it automatically returns to 0 when written.	yes	yes	no	R/W	0
1	Trigger[1] A write of a 1 to this bit loads any pending user register updates if Trigger Mask 1 == 0. This bit always reads as a 0, and it automatically returns to 0 when written.	yes	yes	no	R/W	0
0	Trigger[0] A write of a 1 to this bit loads any pending user register updates if Trigger Mask 0 == 0. This bit always reads as a 0, and it automatically returns to 0 when written.	yes	yes	no	R/W	0

Register PRODUCT_ID, 0x1d, 00011101_B, read only

The Product_ID indicates which revision CMOS is used in the next level product.

Bit	Function	Broadcast Support	GSID Support	Trigger Support	R/W	Default
7:0	Product ID (0x 1C)	no	no	no	R	00011100

Register MANUFACTURER_ID, 0x1E, 00011110_B, read only

Manufacturer ID: Manufacturer ID is read by the master to determine which components reside on the board. For TriQuint, this ID, defined by TriQuint's MIPI Membership, will be:
{D9,D8,D7,D6,D5,D4,D3,D2,D1,D0}={1,0,1,0,0,0,0,1,1,0} = 0x286
The 8 LSBs of this number are contained in this register. The two MSBs are in register 0x1F (below)

Bit	Function	Broadcast Support	GSID Support	Trigger Support	R/W	Default
7:0	Low 8 bits of TQS Manufacturer ID (0x86)	no	no	no	R	00011100

Register USID, 0x1F, 00011111_B

The USID register holds the current USID (Unique slave ID) and must be programmed with the special USID programming sequence outlined in the MIPI specification [1]. In addition the two most-significant bits of the MANUFACTURER_ID are located in this register. The spare bits in this register may be accessed with any valid ID. The USID bits may only be accessed via the special programming sequence. Note that the sequence is aborted if interrupted with either a command using either the broadcast ID or the current GSID.

Bit	Function	Broadcast Support	GSID Support	Trigger Support	R/W	Default
7:6	Spare	no	no	no	R/W	00
5:4	Upper 2 bits <9:8> of the TQS Manufacture ID (0x2)	no	no	no	R	10
3:0	Programmable USID (0xE)	no	no	no	R/W	1110

Recommended MIPI Register Settings (1)

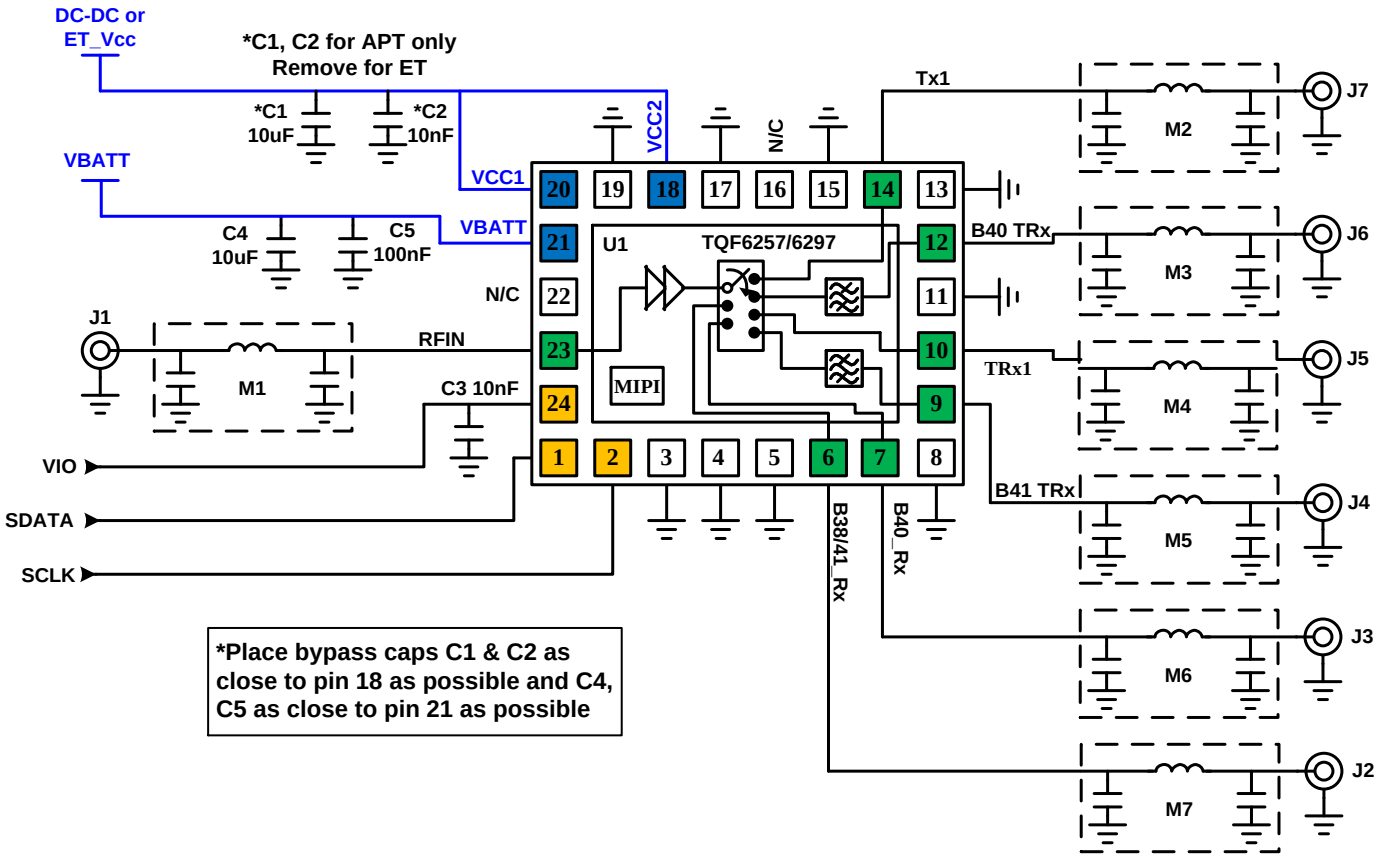
Mode of Operation	Pin Routing	Register 0	Register 1	Register 2	Vcc (v)
Sleep	N/A	0x00	X = Don't care		3.4
Band 7 TX HPM (Tx1)	14	0x24	0xF4		3.4
Band 7 TX LPM (Tx1)	14	0x26	0xF9		1.2
Band 7 TX LPM (Tx1, 0dBm)	14	0x26	0x43		0.6
Band 30 HPM (TRx1)	10	0x14	0xC3		3.4
Band 30 LPM (TRx1)	10	0x16	0x9B		1.2
Band 30 LPM (TRx1, 0dBm)	10	0x16	0x42		0.6
Band 38 TX HPM (TRx1)	10	0x14	0x9F		3.4
Band 38 TX LPM (TRx1)	10	0x16	0xF9		1.2
Band 38 TX LPM (TRx1, 0dBm)	10	0x16	0x53	0x00	0.6
Band 40 TX HPM	12	0x0C	0xB4		3.4
Band 40 TX LPM	12	0x0E	0xA9		1.3
Band 40 TX LPM (0dBm)	12	0x0E	0x32		0.6
Band 41N TX HPM	9	0x1C	0xBF		3.4
Band 41N TX LPM	9	0x1E	0X9D		1.3
Band 41N TX LPM (0dBm)	9	0x1E	0x53		0.6
Band 38 RX	10 to 6	0x30	X = Don't care		3.4
Band 40 RX	12 to 7	0x28	X = Don't care		3.4
Band 41N RX	9 to 6	0x38	X = Don't care		3.4

Notes:
Listed MIPI settings represent APT values; ET MIPI values may be different

Application Circuit Recommendations (APT/ET)

APT and ET Application Circuit: APT with DC – DC Converter or ET Applied to Vcc1, 2

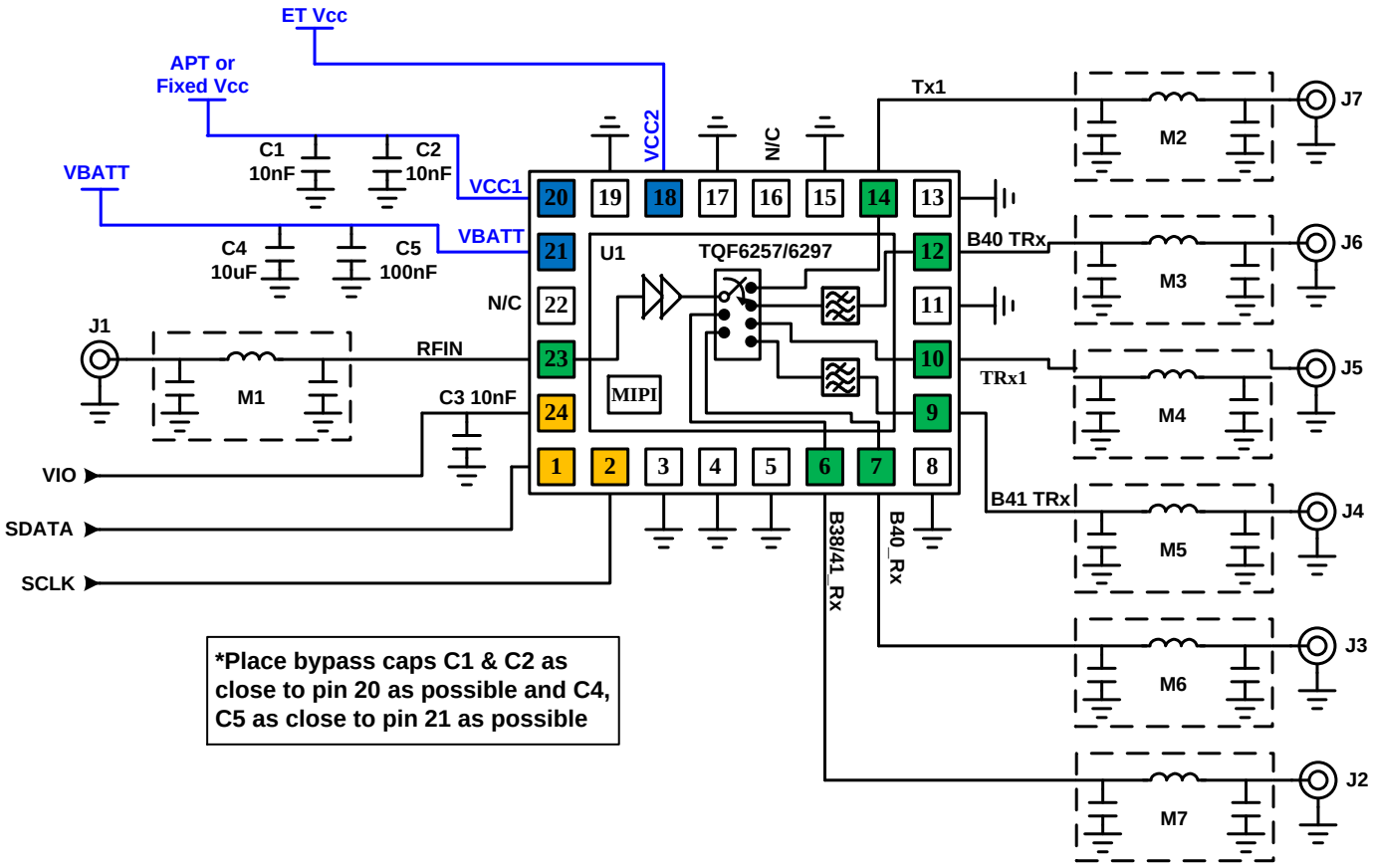
Vbatt connected to the battery supply/ Vcc_1/2 connected to a DC-DC converter.



Application Circuit Recommendations (ET)

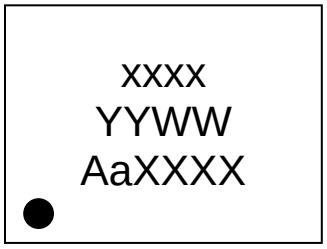
ET Application Circuit: ET Applied to Vcc2 and APT or Fixed Supply for Vcc1

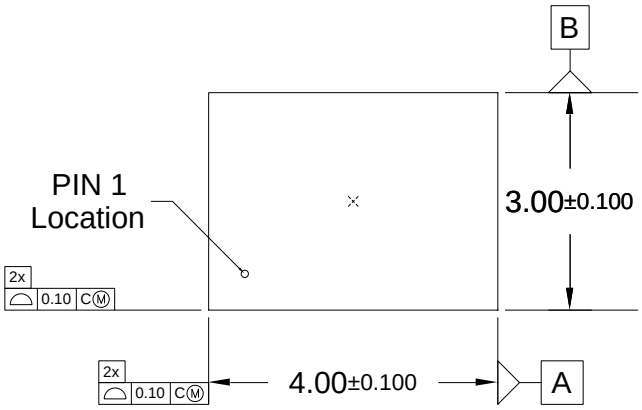
Vbatt connected to the battery supply/ Vcc_1/2 connected to a DC-DC converter.



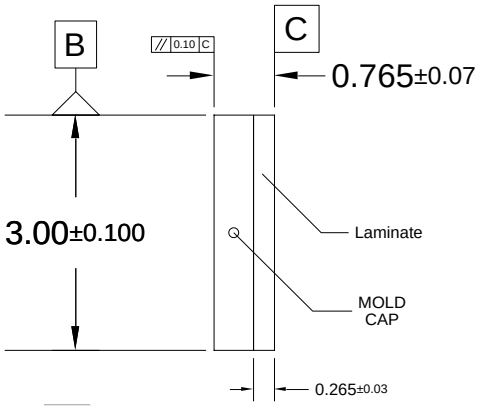
Package Marking and Dimensions

Marking: Product Code: xxxx
Date Code: YYWW
Assembly Code: AaXXXX

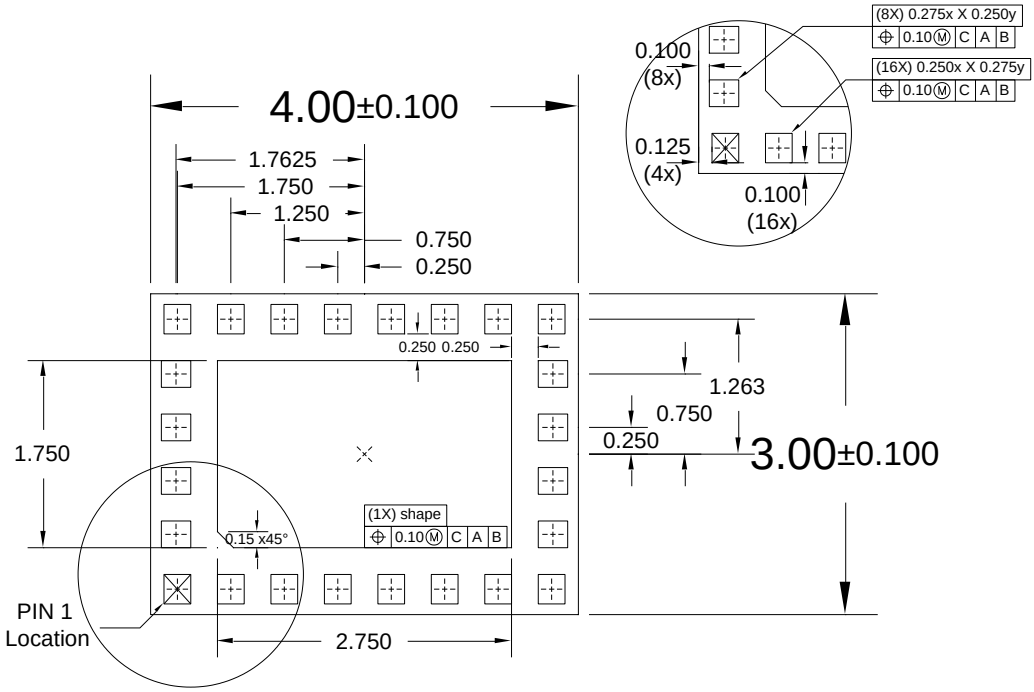




Top View (dimensions in mm)

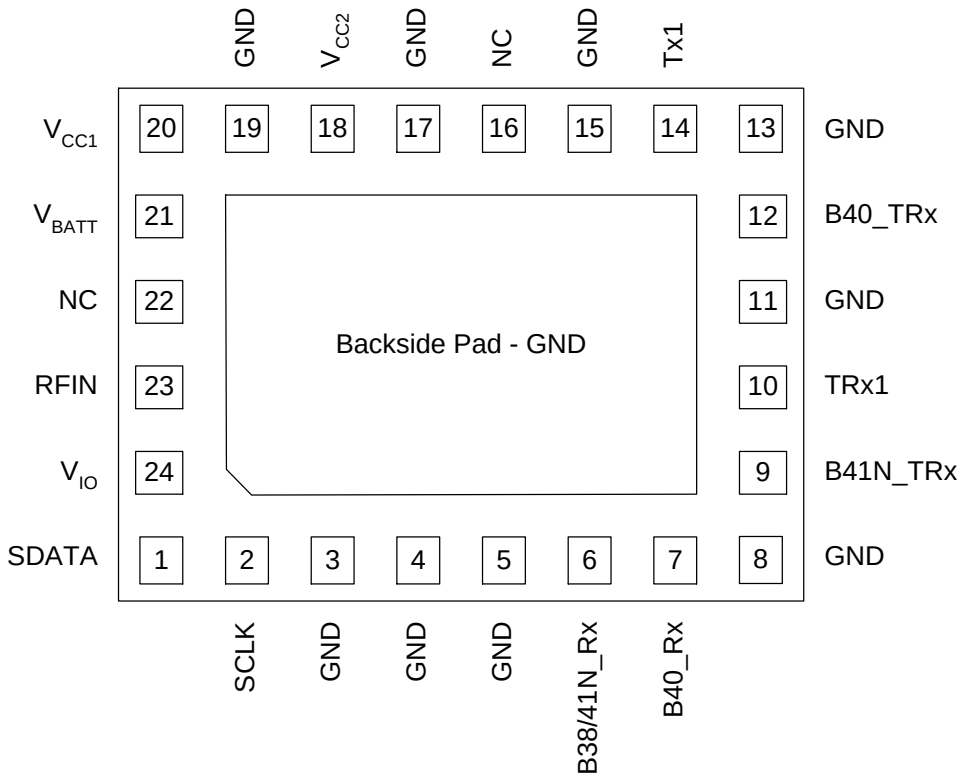


Side View through module (dimensions in mm)



Top View through module (dimensions in mm)

Pin Configuration and Description

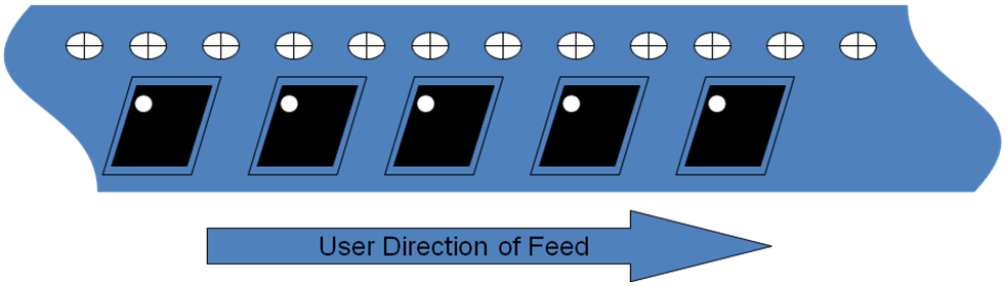


Top View Looking Through Module

Pin	Label	Description
1	SDATA	Data to MIPI controller
2	SCLK	Clock signal for MIPI controller
6	B38/41N_RX	B38/B41N receive signal to transceiver
7	B40_RX	B40 receive signal to transceiver
9	B41N_TRx	Tx Output covering B41N
10	TRx1	Tx and Rx Signal, commonly used for B38
12	B40_TRx	Tx Output covering B40
14	Tx1	Tx output, FDD port, commonly used for B7
16, 22	NC	Not Connected
18	V_{CC2}	Supply2 voltage for TDD/FDD PA
20	V_{CC1}	Supply1 voltage for TDD/FDD PA
21	V_{BATT}	Battery Voltage
23	RFIN	Tx Input
24	V_{IO}	Supply for MIPI/RFFE controller
3-5, 8, 11, 13, 15, 17, 19	GND	Ground
Backside Pad	GND	Ground

Tape and Reel Information – Carrier and Cover Tape Dimensions

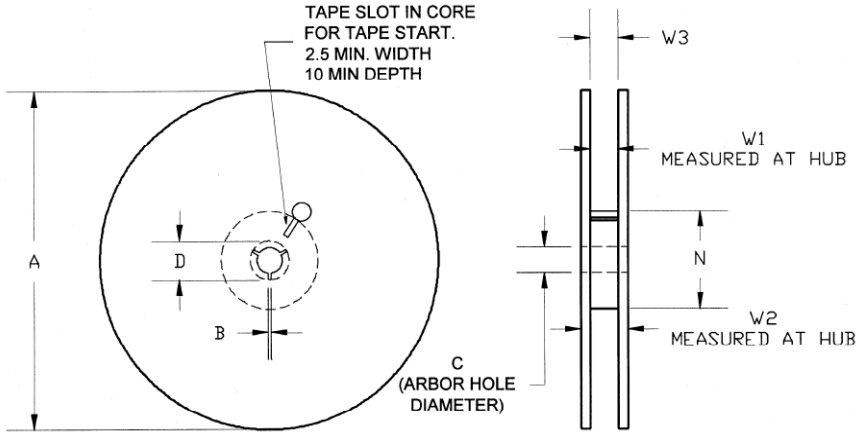
Tape and reel specifications for this part are also available on the TriQuint website.
Standard T/R size = 2500 pieces on a 13” reel.



CAVITY (mm)				DISTANCE BETWEEN CENTERLINE (mm)		CARRIER TAPE (mm)	COVER TAPE (mm)
Length (A0)	**Width (B0)**	**Depth (K0)**	**Pitch (P1)**	**Length direction (P2)**	**Width Direction (F)**	**Width (W)**	**Width (W)**
3.40	4.40	1.30	8.0	2.00	5.50	12.0	9.20

Tape and Reel Information – Reel Dimensions

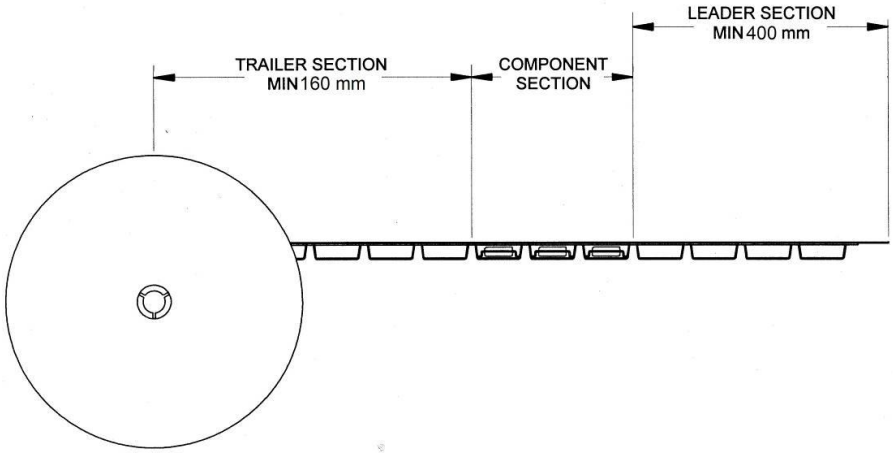
Packaging reels are used to prevent damage to devices during shipping and storage, loaded carrier tape is typically wound onto a plastic take-up reel. The reel size is 13" diameter. The reels are made from high-impact injection-molded polystyrene (HIPS), which offers mechanical and ESD protection to packaged devices.

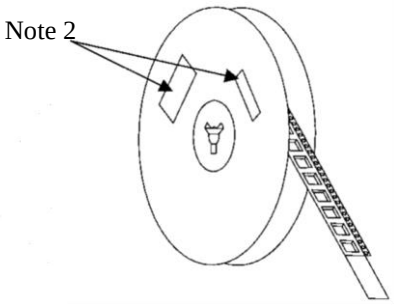


Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	12.992	330.0
	Thickness	W2	0.559	14.2
	Space Between Flange	W1	0.346	8.8
Hub	Outer Diameter	N	4.016	102.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.795	20.2

Tape and Reel Information – Tape Length and Label Placement

Tape and reel specifications for this part are also available on the TriQuint website.
Standard T/R size = 5000 pieces on a 13” reel.





Notes:

1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.

Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating: Class 2
Value: 2000V < V_{ESD} ≤ 2500 V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class C3
Value: 1000V < V_{ESD} ≤ 1500 V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating

MSL Rating: MSL3
Test: 260°C convection reflow
Standard: JEDEC Standard IPC/JEDEC J-STD-020

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Contact plating: Electrolytic plated AU over NI

RoHs Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU

This product also has the following attributes:

- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.Qorvo.com **Tel:** +1.503.615.9000
Email: info-sales@Qorvo.com **Fax:** +1.503.615.8902

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