NB3W800L

3.3 V 100/133 MHz Differential 1:8 HCSL-Compatible Push-Pull Clock ZDB/Fanout Buffer for PCIe®

ON Semiconductor®

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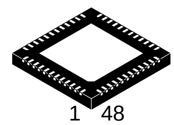
Description

The NB3W800L is a low−power 8−output differential buffer that meets all the performance requirements of the DB800ZL specification. The NB3W800L is capable of distributing the reference clocks for Intel® QuickPath Interconnect (Intel QPI), PCIe Gen1/Gen2/Gen3, SAS, SATA, and Intel Scalable Memory Interconnect (Intel SMI) applications. A fixed, internal feedback path maintains low drift for critical QPI applications.

Features

- 8 Differential Clock Output Pairs @ 0.7 V
- Low−power NMOS Push−pull HCSL Compatible Outputs
- Cycle−to−cycle Jitter <50 ps
- Output−to−output Skew <50 ps
- Input−to−output Delay Variation <100 ps
- PCIe Gen3 Phase Jitter <1.0 ps RMS
- QPI 9.6GT/s 12UI Phase Jitter <0.2 ps RMS
- Pseudo−External Fixed Feedback for Lowest Input−to−output Delay
- Individual OE Control; Hardware Control of Each Output
- PLL Configurable for PLL Mode or Bypass Mode (Fanout Operation)
- 100 MHz or 133 MHz PLL Mode Operation; Supports PCIe and QPI Applications
- Selectable PLL Bandwidth; Minimizes Jitter Peaking in Downstream PLL's
- SMBus Programmable Configurations
- Spread Spectrum Compatible; Tracks Input Clock Spreading for Low EMI
- These are Pb−Free Devices

MARKING DIAGRAM



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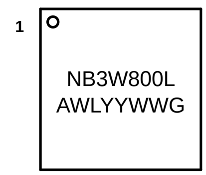


NB3W800L	=	Specific Device Code
A	=	Assembly Location
WL	=	Wafer Lot
YY	=	Year
WW	=	Work Week
G	=	Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NB3W800LMNG	QFN48 (Pb−Free)	490 / Tray
NB3W800LMNTXG	QFN48 (Pb−Free)	2500 / Tape & Reel
NB3W800LMNTWG	QFN48 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

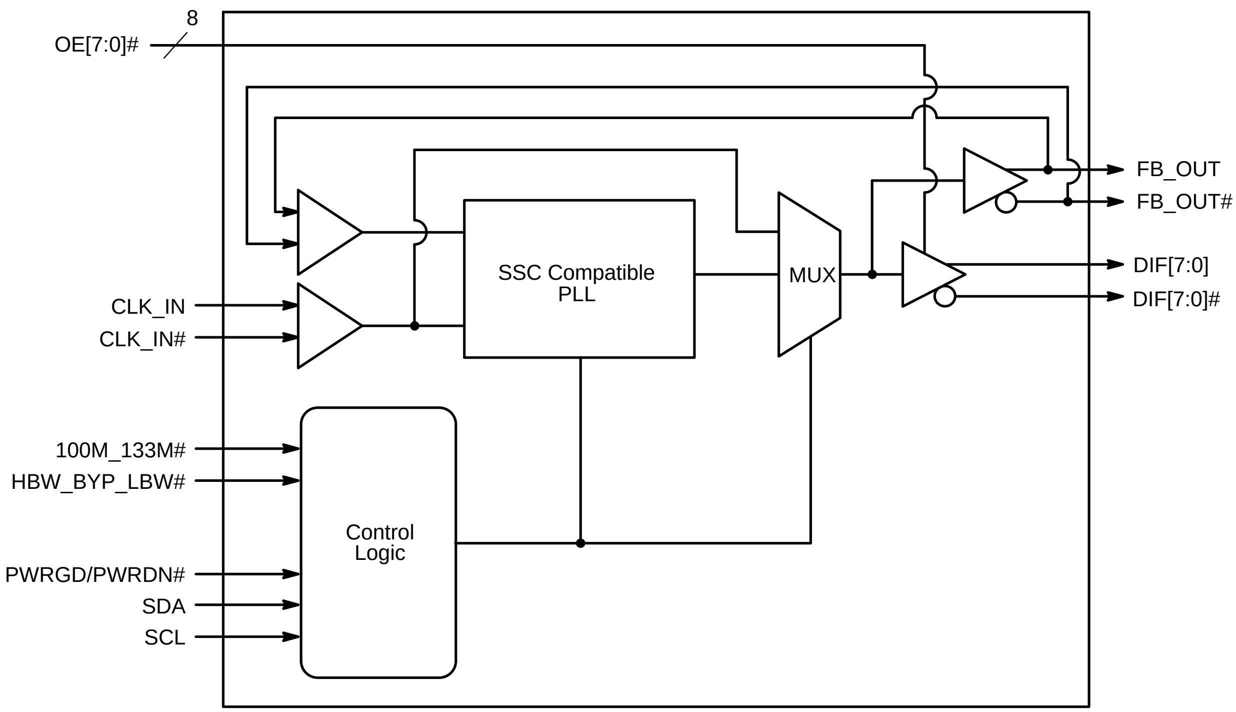


Figure 1. Simplified Block Diagram

Table 1. OE AND POWER PIN TABLE

Inputs		OE# Hardware Pins & Control Register Bits			Outputs	
PWRGD/ PWRDN#	CLK_IN/ CLK_IN#	SMBUS Enable Bit	OE# Pin	DIF/DIF# [7:0]	FB_OUT/ FB_OUT#	PLL State
0	X	X	X	Hi−Z	Hi−Z	OFF
1	Running	0	X	Hi−Z	Running	ON
		1	0	Running	Running	ON
		1	1	Hi−Z	Running	ON

Table 2. FUNCTIONALITY AT POWER−UP (PLL MODE)

100M_133M#	CLK_IN MHz	DIF(7:0)
1	100.00	CLK_IN
0	133.33	CLK_IN

Table 3. POWER CONNECTIONS

Pin Number		Description
VDD	GND	
44	49	Analog PLL
3	2	Analog Input
10, 15, 19, 27, 34, 38, 42	49	DIF clocks

Table 4. SMBus ADDRESS

Address	+ Read/Write bit
D8	R

Table 5. PLL OPERATING MODE READBACK TABLE

HBW_BYP_LBW#	Byte0, bit 7	Byte 0, bit 6
Low (Low BW)	0	0
Mid (Bypass)	0	1
High (High BW)	1	1

Table 6. TRI−LEVEL INPUT THRESHOLDS

Level	Voltage
Low	<0.8 V
Mid	1.2<Vin<1.8 V
High	Vin > 2.2 V

Table 7. PLL OPERATING MODE

HBW_BYP_LBW#	Mode
Low	PLL Lo BW
Mid	Bypass
High	PLL Hi BW

NOTE: PLL is OFF in Bypass Mode

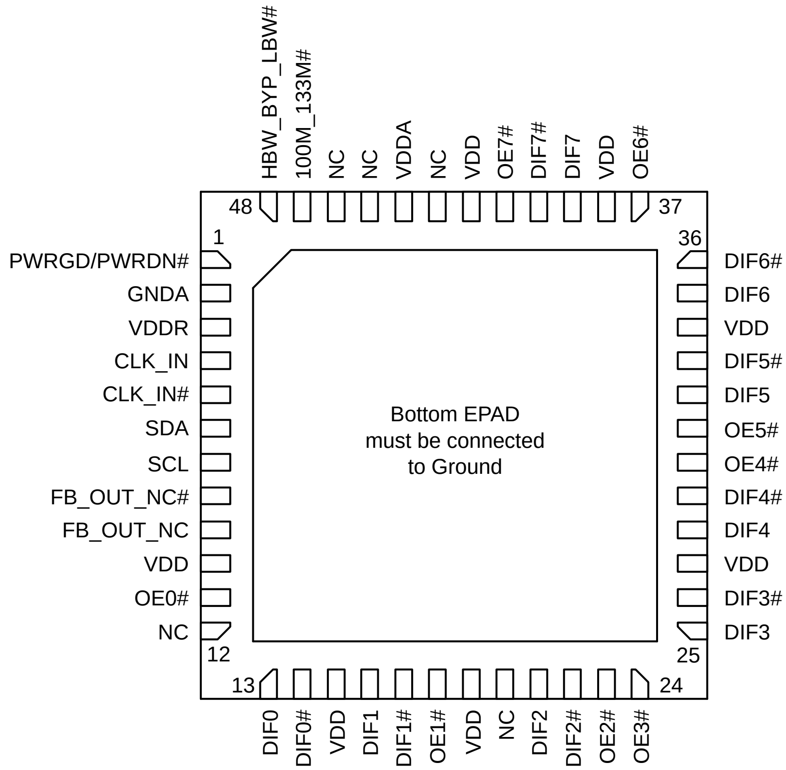


Figure 2. Pin Configuration

Table 8. PIN DESCRIPTIONS

Pin #	Pin Name	Type	Description
1	PWRGD/PWRDN#	IN	3.3 V Input notifies device to sample latched inputs and start up on first high assertion, or exit Power Down Mode on subsequent assertions. Low enters Power Down Mode.
2	GNDA	GND	Ground for Input Receiver and PLL Core
3	VDDR	PWR	3.3 V power for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately.
4	CLK_IN	IN	0.7 V Differential true input
5	CLK_IN#	IN	0.7 V Differential complementary Input
6	SDA	I/O	Data pin of SMBus circuitry
7	SCL	IN	Clock pin of SMBus circuitry
8	FB_OUT_NC#	OUT	Complementary half of differential feedback output provides feedback signal to the PLL for synchronization with input clock to eliminate phase error. This pin should NOT be connected on the circuit board; the feedback is internal to the package.
9	FB_OUT_NC	OUT	True half of differential feedback output provides feedback signal to the PLL for synchronization with the input clock to eliminate phase error. This pin should NOT be connected on the circuit board; the feedback is internal to the package.
10	VDD	PWR	Power supply, nominal 3.3 V
11	OE0#	IN	Active low input for enabling DIF pair 0. This pin has an internal pull−down. 1 = disable outputs, 0 = enable outputs
12	NC	N/A	No Connection.
13	DIF0	OUT	0.7 V differential true clock output
14	DIF0#	OUT	0.7 V differential complementary clock output
15	VDD	PWR	Power supply, nominal 3.3 V
16	DIF1	OUT	0.7 V differential true clock output

Table 8. PIN DESCRIPTIONS

Pin #	Pin Name	Type	Description
17	DIF1#	OUT	0.7 V differential complementary clock output
18	OE1#	IN	Active low input for enabling DIF pair 1. This pin has an internal pull−down. 1 =disable outputs, 0 = enable outputs
19	VDD	PWR	Power supply, nominal 3.3 V
20	NC	N/A	No Connection.
21	DIF2	OUT	0.7 V differential true clock output
22	DIF2#	OUT	0.7 V differential complementary clock output
23	OE2#	IN	Active low input for enabling DIF pair 2. This pin has an internal pull−down. 1 = disable outputs, 0 = enable outputs
24	OE3#	IN	Active low input for enabling DIF pair 3. This pin has an internal pull−down. 1 = disable outputs, 0 = enable outputs
25	DIF3	OUT	0.7 V differential true clock output
26	DIF3#	OUT	0.7 V differential complementary clock output
27	VDD	PWR	Power supply, nominal 3.3 V
28	DIF4	OUT	0.7 V differential true clock output
29	DIF4#	OUT	0.7 V differential complementary clock output
30	OE4#	IN	Active low input for enabling DIF pair 4. This pin has an internal pull−down. 1 = disable outputs, 0 = enable outputs
31	OE5#	IN	Active low input for enabling DIF pair 5. This pin has an internal pull−down. 1 =disable outputs, 0 = enable outputs
32	DIF5	OUT	0.7 V differential true clock output
33	DIF5#	OUT	0.7 V differential complementary clock output
34	VDD	PWR	Power supply, nominal 3.3 V
35	DIF6	OUT	0.7 V differential true clock output
36	DIF6#	OUT	0.7 V differential complementary clock output
37	OE6#	IN	Active low input for enabling DIF pair 6. This pin has an internal pull−down. 1 = disable outputs, 0 = enable outputs
38	VDD	PWR	Power supply, nominal 3.3 V
39	DIF7	OUT	0.7 V differential true clock output
40	DIF7#	OUT	0.7 V differential complementary clock output
41	OE7#	IN	Active low input for enabling DIF pair 7. This pin has an internal pull−down. 1 = disable outputs, 0 = enable outputs
42	VDD	PWR	Power supply, nominal 3.3 V
43	NC	N/A	No Connection.
44	VDDA	PWR	3.3 V power for the PLL core.
45	NC	N/A	No Connection.
46	NC	N/A	No Connection.
47	100M_133M#	IN	3.3 V Input to select operating frequency. See Functionality Table for Definition
48	HBW_BYP_LBW#	IN	Trilevel input to select High BW, Bypass or Low BW mode. See PLL Operating Mode Table for Details.
49	GND	PWR	EPAD, must be connected to Ground

Table 9. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VDD, VDDA	3.3 V Supply Voltage (Notes 1, 2)	VDD for core logic and PLL			4.6	V
V_{IL}	Input Low Voltage (Note 1)		GND−0.5			V
V_{IH}	Input High Voltage (Note 1)	Except for SMBus interface			V_{DD} + 0.5	V
V_{IHSMB}	Input High Voltage (Note 1)	SMBus clock and data pins			5.5	V
Ts	Storage Temperature (Note 1)		−65		150	°C
Tj	Junction Temperature (Note 1)				125	°C
ESD prot	Input ESD protection (Note 1)	Human Body Model	2000			V
θ_{JA}	Thermal Resistance, Junction−to−Ambient	Still air		17		°C/W
θ_{JC}	Thermal Resistance, Junction−to−Case			7		°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Guaranteed by design and characterization, not tested in production.
2. Operation under these conditions is neither implied nor guaranteed.

Table 10. ELECTRICAL CHARACTERISTICS–CLOCK INPUT PARAMETERS (HCSL−COMPATIBLE)
(V_{DD} = V_{DDA} = 3.3 V ±5%, T_A = 0°C – 70°C), See Test Loads for Loading Conditions. (Note 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IHCLK_IN}	Input High Voltage - CLK_IN (Note 3)	Differential inputs (single−ended measurement)	600	800	1150	mV
V_{ILCLK_IN}	Input Low Voltage - CLK_IN (Note 3)	Differential inputs (single−ended measurement)	V_{SS} - 300	0	300	mV
V_{COM}	Input Common Mode Voltage - CLK_IN (Note 3)	Common Mode Input Voltage (Single−ended measurement)	300		1000	mV
V_{SWING}	Input Amplitude - CLK_IN (Note 3)	Peak to Peak (differential)	300		1450	mV
dv/dt	Input Slew Rate - CLK_IN (Notes 3, 4)	Measured differentially	0.35		8	V/ns
I_{IN}	Input Leakage Current (Note 3)	V_{IN} = V_{DD} , V_{IN} = GND	−5		5	μA
d_{tin}	Input Duty Cycle (Note 3)	Measurement from differential waveform	45		55	%
J_{DIFIn}	Input Jitter - Cycle to Cycle (Note 3)	Differential Measurement			125	ps

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
3. Guaranteed by design and characterization, not tested in production.
4. Slew rate measured through ±75 mV window centered around differential zero.
5. Test configuration is; Rs = 27 Ω, 2 pF for 85 Ω transmission line.

Table 11. ELECTRICAL CHARACTERISTICS – Input/Supply/Common Parameters
(V_{DD} = V_{DDA} = 3.3 V ±5%, T_A = 0°C – 70°C), See Test Loads for Loading Conditions. (Note 11)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Voltage (Note 6)	Single−ended inputs, except SMBus, low threshold and tri−level inputs	2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage (Note 6)	Single−ended inputs, except SMBus, low threshold and tri−level inputs	GND − 0.3		0.8	V
I_{IN}	Input Current (Note 6)	Single−ended inputs, V_{IN} = GND, V_{IN} = V_{DD}	−5		5	μA
I_{INP}		Single−ended inputs V_{IN} = 0 V; Inputs with internal pull−up resistors V_{IN} = V_{DD}; Inputs with internal pull−down resistors	−200		200	μA
F_{ibyp}	Input Frequency (Note 7)	V_{DD} = 3.3 V, Bypass mode	33		150	MHz
F_{ipll}		V_{DD} = 3.3 V, 100 MHz PLL mode	99	100.00	101	MHz
F_{ipll}		V_{DD} = 3.3 V, 133.33 MHz PLL mode	132.33	133.33	134.33	MHz
L_{pin}	Pin Inductance (Note 6)				7	nH
C_{IN}	Capacitance (Note 6)	Logic Inputs, except CLK_IN	1.5		4.5	pF
C_{INCLK_IN}		CLK_INdifferential clock inputs (Note 9)	1.5		2.7	pF
C_{OUT}		Output pin capacitance			4.5	pF
f_{MODIN}	Input SS Modulation Frequency (Note 6)	Allowable Frequency (Triangular Modulation)	30		33	kHz
$t_{LATOE\#}$	OE# Latency (Notes 6. 8)	DIF start after OE# assertion DIF stop after OE# deassertion	4		8	cycles
t_{DRVPD}	Tdrive_PD# (Notes 6, 8)	DIF output enable after PD# de−assertion			300	μs
t_F	Tfall (Notes 6, 7)	Fall time of control inputs			10	ns
t_R	Trise (Notes 6, 7)	Rise time of control inputs			10	ns
V_{ILSMB}	SMBus Input Low Voltage (Note 6)				0.8	V
V_{IHSMB}	SMBus Input High Voltage (Note 6)		2.1		V_{DDSMB}	V
V_{OLSMB}	SMBus Output Low Voltage (Note 6)	@ I_{PULLUP}			0.4	V
I_{PULLUP}	SMBus Sink Current (Note 6)	@ V_{OL}	4			mA
V_{DDSMB}	Nominal Bus Voltage (Note 6)	3 V to 5 V ±10%	2.7		5.0	V
t_{RSMB}	SCL/SDA Rise Time (Note 6)	(Max V_{IL} - 0.15) to (Min V_{IH} + 0.15)			1000	ns
t_{FSMB}	SCL/SDA Fall Time (Note 6)	(Min V_{IH} + 0.15) to (Max V_{IL} - 0.15)			300	ns
f_{MAXSMB}	SMBus Operating Frequency (Notes 6, 10)	Maximum SMBus operating frequency			100	kHz

6. Guaranteed by design and characterization, not tested in production.
7. Control input must be monotonic from 20% to 80% of input swing.
8. Time from deassertion until outputs are >200 mV
9. CLK_IN input
10. The differential input clock must be running for the SMBus to be active
11. Test configuration is; Rs = 27 Ω, 2 pF for 85 Ω transmission line.

Table 12. DIF 0.7 V AC TIMING CHARACTERISTICS (Non−Spread or −0.5% Spread Spectrum Mode)
(V_{DD} = V_{DDA} = 3.3 V ±5%, T_A = 0°C – 70°C), See Test Loads for Loading Conditions.

Symbol	Parameter		CLK = 100 MHz, 133.33 MHz		Unit
			Min	Max	
Tstab (Note 32)	Clock Stabilization Time			1.8	ms
Laccuracy (Notes 15, 19, 27, 33)	Long Accuracy			100	ppm
Tabs (Notes 15, 16, 19)	Absolute Min/Max Host CLK Period	No Spread	9.94900 for 100 MHz	10.05100 for 100 MHz	ns
			7.44925 for 133 MHz	7.55075 for 133 MHz	
		−0.5% Spread	9.49900 for 100 MHz	10.10126 for 100 MHz	
			7.44925 for 133 MHz	7.58845 for 133 MHz	
Slew_rate (Notes 13, 15, 19)	DIFF OUT Slew_rate		1.0	4.0	V/ns
ΔTrise / ΔTfall (Notes 15, 19, 29)	Rise and Fall Time Variation			125	ps
Rise/Fall Matching (Notes 15, 19, 30, 31)				20	%
VHigh (Notes 15, 18, 21)	Voltage High (typ 0.70 Volts)		660	850	mV
VLow (Notes 15, 18, 22)	Voltage Low (typ 0.0 Volts)		−150	150	mV
Vmax (Note 18)	Maximum Voltage			1150	mV
Vcross absolute (Notes 12, 14, 15, 18, 25)	Absolute Crossing Point Voltages		250	550	mV
Vcross relative (Notes 15, 17, 18, 25)	Relative Crossing Point Voltages		Calc	Calc	
Total Δ Vcross (Notes 15, 18, 26)	Total Variation of Vcross Over All Edges			140	mV
Vovs (Notes 15, 18, 23)	Maximum Voltage (Overshoot)			Vhigh + 0.3	V
Vuds (Notes 15, 18, 24)	Maximum Voltage (Undershoot)			Vlow − 0.3	V

12. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLK#.
13. Measurment taken from differential waveform on a component test board. The slew rate is measured from −150 mV to +150 mV on the differential waveform. Scope is set to average because the scope sample clock is making most of the dynamic wiggles along the clock edge Only valid for Rising CLK_IN and Falling CLK_IN#. Signal must be monotonic through the Vol to Voh region for Trise and Tfall.
14. This measurement refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing.
15. Test configuration is; Rs = 27 Ω, 2 pF for 85 Ω transmission line.
16. The average period over any 1 μs period of time must be greater than the minimum and less than the maximum specified period.
17. Vcross(rel) Min and Max are derived using the following, Vcross(rel) Min = 0.250 + 0.5 (Vhavg − 0.700), Vcross(rel) Max = 0.550 − 0.5 (0.700 – Vhavg)
18. Measurement taken from Single Ended waveform.
19. Measurement taken from differential waveform. Bypass mode, input duty cycle = 50%.
20. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
21. VHigh is defined as the statistical average High value as obtained by using the Oscilloscope VHigh Math function.
22. VLow is defined as the statistical average Low value as obtained by using the Oscilloscope VLow Math function.
23. Overshoot is defined as the absolute value of the maximum voltage.
24. Undershoot is defined as the absolute value of the minimum voltage.
25. The crossing point must meet the absolute and relative crossing point specifications simultaneously.
26. ΔVcross is defined as the total variation of all crossing voltages of Rising DIF and Falling DIF#. This is the maximum allowed variance in Vcross for any particular system.
27. Using frequency counter with the measurement interval equal or greater than 0.15 s, target frequencies are 100,000,000 Hz, 133,333,333 Hz.
28. Using frequency counter with the measurement interval equal or greater than 0.15 s, target frequencies are 99,750,00 Hz, 133,000,000 Hz.
29. Measured with oscilloscope, averaging off, using min max statistics. Variation is the delta between min and max.
30. Measured with oscilloscope, averaging on, The difference between the rising edge rate (average) of DIF versus the falling edge rate (average) of DIF#. Measured in a ±75 mV window around the crosspoint of DIF and DIF#.
31. Rise/Fall matching is derived using the following, 2*(Trise – Tfall) / (Trise + Tfall).
32. This is the time from the valid CLK_IN input clocks and the assertion of the PWRGD signal level at 1.8 V – 2.0 V to the time that stable clocks are output from the buffer chip (PLL locked).
33. All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK410B+/CK420BQ accuracy requirements. The NB3W800L itself does not contribute to ppm error.

Table 13. ELECTRICAL CHARACTERISTICS – Current Consumption
(V_{DD} = V_{DDA} = 3.3 V ±5%, T_A = 0°C − 70°C), See Test Loads for Loading Conditions. (Note 35)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DDVDD}	Operating Current (Note 34)	133 MHz, VDD rail		94	105	mA
I_{DDVDDA}		133 MHz, VDDA + VDDR rail, PLL Mode		38	50	mA
$I_{DDVDDPD}$	Powerdown Current (Note 34)	Power Down, VDD Rail		2.0	3.5	mA
$I_{DDVDDAPD}$		Power Down, VDDA Rail		0.5	1.0	mA

34. Guaranteed by design and characterization, not tested in production.
35. C_L = 2 pF with RS = 27 Ω for Zo = 85 Ω differential trace impedance.

Table 14. ELECTRICAL CHARACTERISTICS – Skew and Differential Jitter Parameters
(V_{DD} = V_{DDA} = 3.3 V ±5%, T_A = 0°C − 70°C), See Test Loads for Loading Conditions.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{SPO_PLL}	CLK_IN, DIF[x:0] (Notes 36, 37, 39, 40, 43)	Input−to−Output Skew in PLL mode nominal value @ 25°C, 3.3 V	−100		100	ps
t_{PD_BYP}	CLK_IN, DIF[x:0] (Notes 36, 37, 39, 40, 43)	Input−to−Output Skew in Bypass mode nominal value @ 25°C, 3.3 V	2.5		4.5	ns
t_{DSPO_PLL}	CLK_IN, DIF[x:0] (Notes 36, 37, 39, 40, 43)	Input−to−Output Skew Varation in PLL mode across voltage and temperature	−100		100	ps
t_{DSPO_BYP}	CLK_IN, DIF[x:0] (Notes 36, 37, 39, 40, 43)	Input−to−Output Skew Varation in Bypass mode across voltage and temperature	−250		250	ps
t_{SKEW_ALL}	DIF{x:0] (Notes 36, 37, 39, 43)	Output−to−Output Skew across all outputs (Common to Bypass and PLL mode)			50	ps
$j_{peak-hbw}$	PLL Jitter Peaking (Notes 36, 42, 43)	HBW_BYP_LBW# = 1			2.5	dB
$j_{peak-lbw}$	PLL Jitter Peaking (Notes 36, 42, 43)	HBW_BYP_LBW# = 0			2	dB
pll_{HBW}	PLL Bandwidth (Notes 36, 43, 44)	HBW_BYP_LBW# = 1	2	3	4	MHz
pll_{LBW}	PLL Bandwidth (Notes 36, 43, 44)	HBW_BYP_LBW# = 0	0.7	1	1.4	MHz
t_{DC}	Duty Cycle (Note 36, 46)	Measured differentially, PLL and Bypass Mode	45	50	55	%
t_{DCD}	Duty Cycle Distortion (Notes 36, 45)	Measured differentially, Bypass Mode @ 100 MHz	−2	0	2	%
$t_{jcyc-cyc}$	Jitter, Cycle to cycle (Notes 36, 46)	PLL mode			50	ps
		Additive Jitter in Bypass Mode			50	ps

36. C_L = 2 pF with RS = 27 Ω for Zo = 85 Ω differential trace impedance. Input to output skew is measured at the first output edge following the corresponding input.
37. Measured from differential cross−point to differential cross−point. This parameter can be tuned with external feedback path, if present.
38. All Bypass Mode Input−to−Output specs refer to the timing between an input edge and the specific output edge created by it.
39. This parameter is deterministic for a given device
40. Measured with scope averaging on to find mean value.
41. t is the period of the input clock
42. Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.
43. Guaranteed by design and characterization, not tested in production.
44. Measured at 3 db down or half power point.
45. Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.
46. Measured from differential waveform. Bypass mode, input duty cycle = 50%.

Table 15. ELECTRICAL CHARACTERISTICS – PHASE JITTER PARAMETERS
(V_{DD} = V_{DDA} = 3.3 V ±5%, TA = 0°C − 70°C), See Test Loads for Loading Conditions. (Note 35)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{jphPCIeG1}$	Phase Jitter, PLL Mode (Note 47)	PCIe Gen 1 (Notes 48, 49)			86	ps (p−p)
$t_{jphPCIeG2}$		PCIe Gen 2 Lo Band 10 kHz < f < 1.5 MHz (Note 48)			3	ps (rms)
		PCIe Gen 2 High Band 1.5 MHz < f < Nyquist (50 MHz) (Note 48)			3.1	ps (rms)
$t_{jphPCIeG3}$		PCIe Gen 3 (PLL BW of 2−4 MHz, CDR = 10 MHz) (Notes 48, 50)			1	ps (rms)
t_{jphQPI_SMI}		QPI & SMI (100 MHz or 133 MHz, 4.8 Gb/s, 6.4 Gb/s 12 UI) (Note 51)			0.5	ps (rms)
		QPI & SMI (100 MHz, 8.0 Gb/s, 12 UI) (Note 51)			0.3	ps (rms)
		QPI & SMI (100 MHz, 9.6 Gb/s, 12 UI) (Note 51)			0.2	ps (rms)
$t_{jphPCIeG1}$	Additive Phase Jitter, Bypass mode (Note 47)	PCIe Gen 1 (Notes 48, 49)			10	ps (p−p)
$t_{jphPCIeG2}$		PCIe Gen 2 Lo Band 10 kHz < f < 1.5 MHz (Notes 48, 52)			0.3	ps (rms)
		PCIe Gen 2 High Band 1.5 MHz < f < Nyquist (50 MHz) (Notes 48, 52)			0.6	ps (rms)
$t_{jphPCIeG3}$		PCIe Gen 3 (PLL BW of 2−4 MHz, 2−5 MHz, CDR = 10 MHz) (Notes 48, 50, 52)			0.2	ps (rms)
t_{jphQPI_SMI}		QPI & SMI (100 MHz or 133 MHz, 4.8 Gb/s, 6.4 Gb/s 12 UI) (Notes 51, 52)			0.2	ps (rms)
		QPI & SMI (100 MHz, 8.0 Gb/s, 12 UI) (Notes 51, 52)			0.1	ps (rms)
		QPI & SMI (100 MHz, 9.6 Gb/s, 12 UI) (Notes 51, 52)			0.1	ps (rms)

47. Applies to all outputs.
48. See http://www.pcisig.com for complete specs
49. Sample size of at least 100K cycles. This figures extrapolates to 108ps pk−pk @ 1M cycles for a BER of 1−12.
50. Subject to final ratification by PCI SIG.
51. Calculated from Intel−supplied Clock Jitter Tool v 1.6.3
52. For RMS figures, additive jitter is calculated by solving the following equation: $(\text{Additive jitter})^2 = (\text{total jittter})^2 - (\text{input jitter})^2$

Table 16. CLOCK PERIODS – Differential Outputs with Spread Spectrum Disabled

SSC OFF	Center Freq. MHz	Measurement Window 1 Clock −c2c Jitter Abs Per Min	1 µs −SSC Short−Term Average Min	0.1 s − ppm Long−Term Average Min	0.1 s 0 ppm Period Nominal	0.1 s + ppm Long−Term Average Max	1 µs +SSC Short−Term Average Max	1 Clock +c2c Jitter Abs Per Max	Units
DIF (Notes 53, 54, 55)	100.00	9.94900		9.99900	10.00000	10.00100		10.05100	ns
DIF (Notes 53, 54, 56)	133.33	7.44925		7.49925	7.50000	7.50075		7.55075	ns

Table 17. CLOCK PERIODS – Differential Outputs with Spread Spectrum Enabled

SSC ON	Center Freq. MHz	Measurement Window 1 Clock −c2c Jitter Abs Per Min	1 µs −SSC Short−Term Average Min	0.1 s − ppm Long−Term Average Min	0.1 s 0 ppm Period Nominal	0.1 s + ppm Long−Term Average Max	1 µs +SSC Short−Term Average Max	1 Clock +c2c Jitter Abs Per Max	Units
DIF (Notes 53, 54, 55)	99.75	9.94906	9.99906	10.02406	10.02506	10.02607	10.05107	10.10107	ns
DIF (Notes 53, 54, 56)	133.00	7.44930	7.49930	7.51805	7.51880	7.51955	7.53830	7.58830	ns

53. Guaranteed by design and characterization, not tested in production.
54. All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK420BQ/CK410B+ accuracy requirements (±100 ppm). The device itself does not contribute to ppm error.
55. Driven by SRC output of main clock, 100 MHz PLL Mode or Bypass mode
56. Driven by CPU output of main clock, 133 MHz PLL Mode or Bypass mode

Measurement Points for Differential

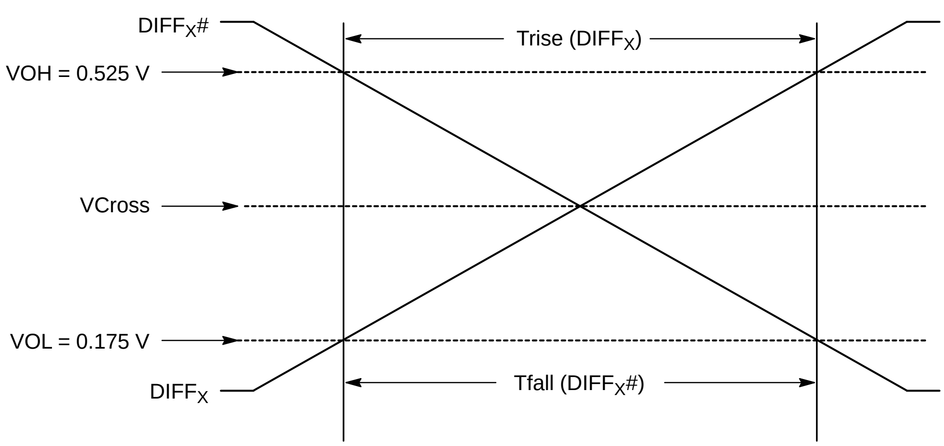


Figure 3. Single−Ended Measurement Points for Trise, Tfall

Measurement Points for Differential

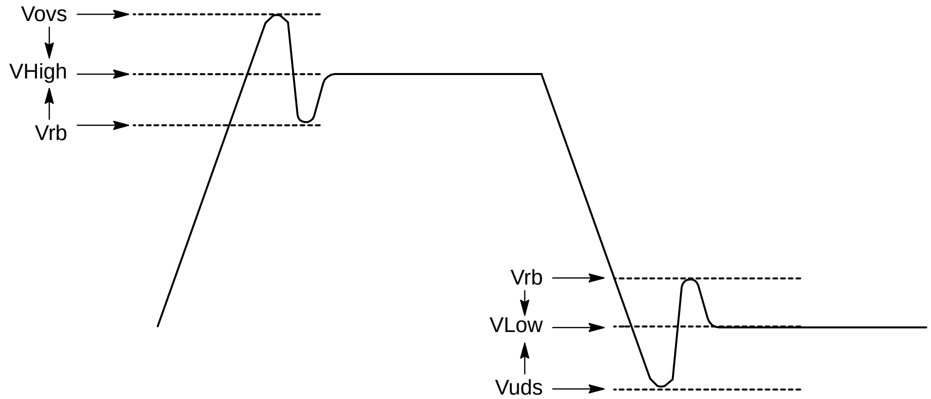


Figure 4. Single−Ended Measurement Points for Vovs, Vuds, Vrb

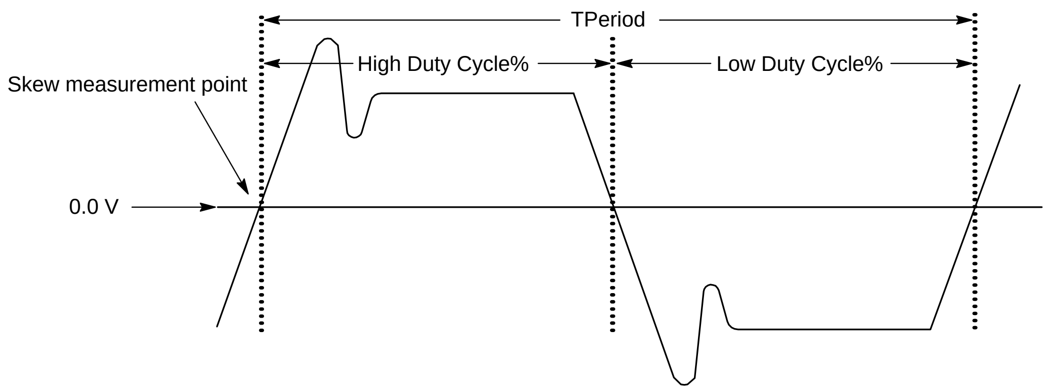


Figure 5. Differential ($DIFF_X$ – $DIFF_X$#) Measurement Points (Tperiod, Duty Cycle, Jitter)

Test Loads

Differential Output Terminations	
DIF Zo (Ω)	Rs (Ω)
100	33
85	27

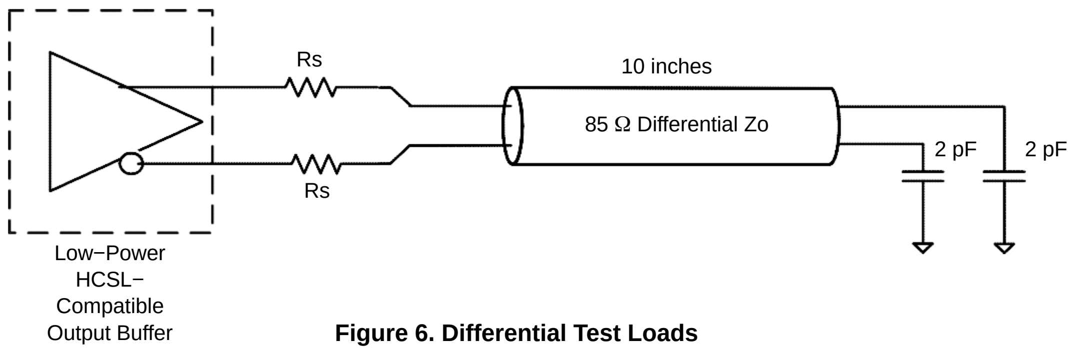


Figure 6. Differential Test Loads

SIGNAL AND FEATURE OPERATION

CLK_IN, CLK_IN#

The differential input clock is expected to be sourced from a clock synthesizer with an HCSL−compatible output, e.g. CK420BQ, CK−NET, CK−uS, or CK509B or another driver.

OE# and Output Enables (Control Registers)

Each output can be individually enabled or disabled by SMBus control register bits. Additionally, each output of the DIF[7:0] has a dedicated OE# pin. The OE# pins are asynchronous asserted−low signals. The Output Enable bits in the SMBus registers are active high and are set to enable by default.

The disabled state for the NB3W800L low power NMOS Push−Pull outputs is Low/Low.

Please note that the logic level for assertion or deassertion is different in software than it is on hardware. Output is enabled if OE# pin is pulled low and still maintains software programming logic with output enabled if OE register is true.

The assertion and de−assertion of this signal is absolutely asynchronous.

OE# Assertion (Transition from ‘1’ to ‘0’)

All differential outputs that were tristated will resume normal operation in a glitch free manner.

OE# De−Assertion (Transition from ‘0’ to ‘1’)

Corresponding output will transition from normal operation to tri−state in a glitch free manner.

100M_133M# − Frequency Selection

The 100M_133M# is a hardware pin, which programs the appropriate output frequency of the DIF pairs. Note that the CLK_IN frequency is equal to CLK_OUT frequency. An external pull−up or pull−down resistor is attached to this pin to select the input/output frequency.

PWRGD / PWRDN#

PWRGD is asserted high and de−asserted low. De−assertion of PWRGD (pulling the signal low) is equivalent to indicating a powerdown condition. PWRGD (assertion) is used by the NB3W800L to sample initial configurations such as frequency select condition.

After PWRGD has been asserted high for the first time, the pin becomes a PWRDN# (Power Down) pin that can be used to shut off all clocks cleanly and instruct the device to invoke power savings mode. PWRDN# is a completely asynchronous active low input. When entering power savings mode, PWRDN# should be asserted low prior to shutting off the input clock or power to ensure all clocks shut down in a glitch free manner.

The assertion and de−assertion of PWRDN# is absolutely asynchronous.

When PWRDN# is sampled low by two consecutive rising edges of DIF#, all differential outputs are held tri−stated on the next DIF# high to low transition.

HBW_BYPASS_LBW#

The HBW_BYPASS_LBW# is a tri level function input pin. It is used to select between PLL high bandwidth, bypass mode and PLL low bandwidth mode.

Device Power Up Sequence

The device power up should follow the sequence mentioned below for proper functioning of the device: PWRGD/PWRDN# should be asserted Low. All other Control pins should be defined to the required state. Power should be given to the device. PWRGD/PWRDN# should be asserted High.

Note: if no clock is present on the CLK_IN/CLK_IN# pins, whenever device is Powered Up,there will be no clock on DIF/DIF# outputs

POWER FILTERING EXAMPLE

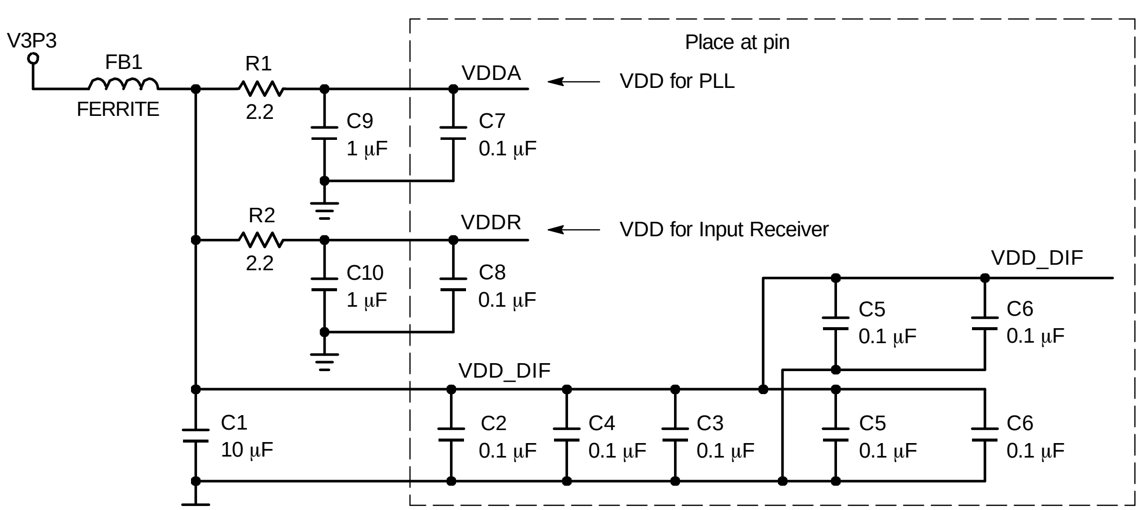


Figure 7. Schematic Example of the NB3W800L Power Filtering

General SMBus Serial Interface Information for NB3W800L

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- Clock(device) will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Clock(device) will **acknowledge**
- Controller (host) sends the byte count = X
- Clock(device) will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X−1**
- Clock(device) will **acknowledg**e each byte **one at a time**
- Controller (host) sends a Stop bit

Index Block Write Operation			
Controller (Host)			**Clock (Device)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N			
			ACK
O			
O		X Byte	O
O			O
			O
Byte N + X − 1			
			ACK
P	stoP bit		

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- Clock(device) will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Clock(device) will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- Clock(device) will **acknowledge**
- Clock(device) will send the data byte count = X
- Clock(device) sends Byte **N+X−1**
- Clock(device) sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**Clock (Device)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count = X
ACK			
			Beginning Byte N
ACK			
			O
O		X Byte	O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

Table 18. SMBus TABLE: PLL MODE, AND FREQUENCY SELECT REGISTER

Byte 0	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	48	PLL Mode 1	PLL Operating Mode Rd back 1	R	See PLL Operating Mode Readback Table		Latched at power up
Bit 6	48	PLL Mode 0	PLL Operating Mode Rd back 0	R			Latched at power up
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		PLL_SW_EN	Enable S/W control of PLL BW	RW	HW Latch	SMBus Control	0
Bit 2		PLL Mode 1	PLL Operating Mode 1	RW	See PLL Operating Mode Readback Table		1
Bit 1		PLL Mode 0	PLL Operating Mode 0	RW			1
Bit 0	47	100M_133M#	Frequency Select Readback	R	133 MHz	100 MHz	Latched at power up

NOTE: Setting bit 3 to ‘1’ allows the user to overide the Latch value from pin 48 via use of bits 2 and 1. Use the values from the PLL Operating Mode Readback Table. Note that Bits 7 and 6 will keep the value originally latched on pin 48. A warm reset of the system will have to accomplished if the user changes these bits.

Table 19. SMBus TABLE: OUTPUT CONTROL REGISTER

Byte 1	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	32/33	DIF_5_En	Output Control - ‘0’ overrides OE# pin	RW	Low/Low	Enable	1
Bit 6	28/29	DIF_4_En	Output Control - ‘0’ overrides OE# pin	RW			1
Bit 5	25/26	DIF_3_En	Output Control - ‘0’ overrides OE# pin	RW			1
Bit 4	21/22	DIF_2_En	Output Control - ‘0’ overrides OE# pin	RW			1
Bit 3		Reserved					1
Bit 2	16/17	DIF_1_En	Output Control - ‘0’ overrides OE# pin	RW	Low/Low	Enable	1
Bit 1	13/14	DIF_0_En	Output Control - ‘0’ overrides OE# pin	RW			1
Bit 0		Reserved					1

Table 20. SMBus TABLE: OUTPUT CONTROL REGISTER

Byte 2	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		Reserved					1
Bit 2	39/40	DIF_7_En	Output Control - ‘0’ overrides OE# pin	RW	Low/Low	Enable	1
Bit 1		Reserved					1
Bit 0	35/36	DIF_6_En	Output Control - ‘0’ overrides OE# pin	RW	Low/Low	Enable	1

Table 21. SMBus TABLE: RESERVED REGISTER

Byte 3	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		Reserved					0
Bit 2		Reserved					0
Bit 1		Reserved					0
Bit 0		Reserved					0

Table 22. SMBus TABLE: RESERVED REGISTER

Byte 4	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		Reserved					0
Bit 2		Reserved					0
Bit 1		Reserved					0
Bit 0		Reserved					0

Table 23. SMBus TABLE: VENDOR & REVISION ID REGISTER

Byte 5	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	−	RID3	REVISION ID	R	A rev = 0000		0
Bit 6	−	RID2		R			0
Bit 5	−	RID1		R			0
Bit 4	−	RID0		R			0
Bit 3	−	VID3	VENDOR ID	R	−	−	1
Bit 2	−	VID2		R	−	−	1
Bit 1	−	VID1		R	−	−	1
Bit 0	−	VID0		R	−	−	1

Table 24. SMBus TABLE: DEVICE ID

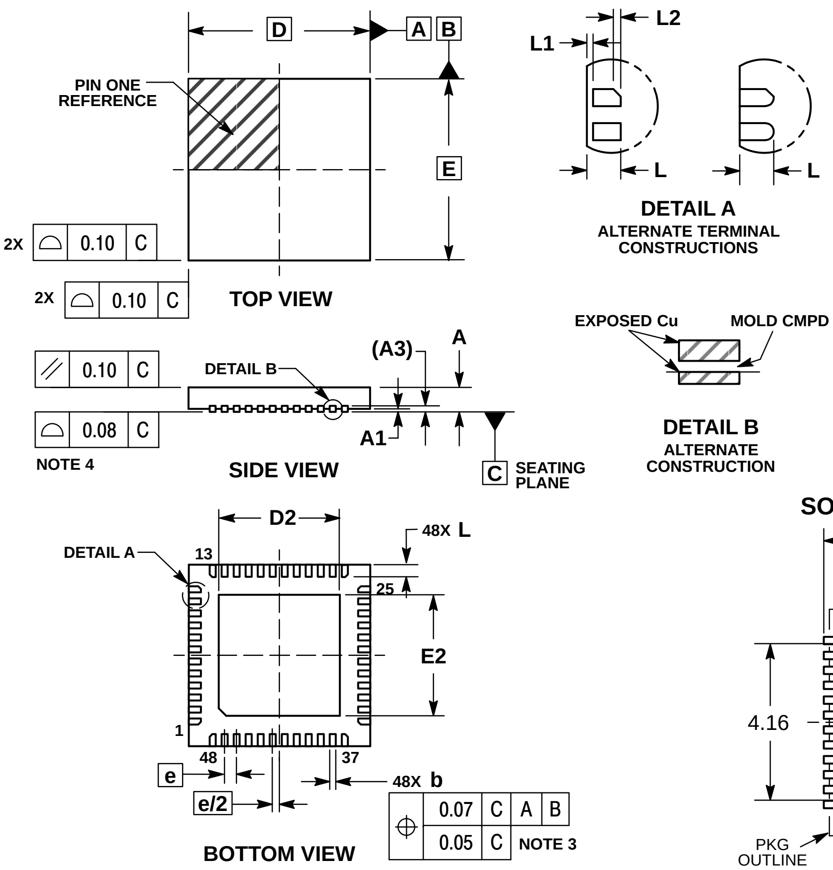
Byte 6	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	−	Device ID 7 (MSB)		R			1
Bit 6	−	Device ID 6		R			1
Bit 5	−	Device ID 5		R			1
Bit 4	−	Device ID 4		R			0
Bit 3	−	Device ID 3		R			0
Bit 2	−	Device ID 2		R			1
Bit 1	−	Device ID 1		R			1
Bit 0	−	Device ID 0		R			1

Table 25. SMBus TABLE: BYTE COUNT REGISTER

Byte 7	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4	−	BC4	Writing to this register configures how many bytes will be read back.	RW	Default value is 8 hex, so 9 bytes (0 to 8) will be read back by default.		0
Bit 3	−	BC3		RW			1
Bit 2	−	BC2		RW			0
Bit 1	−	BC1		RW			0
Bit 0	−	BC0		RW			0

PACKAGE DIMENSIONS

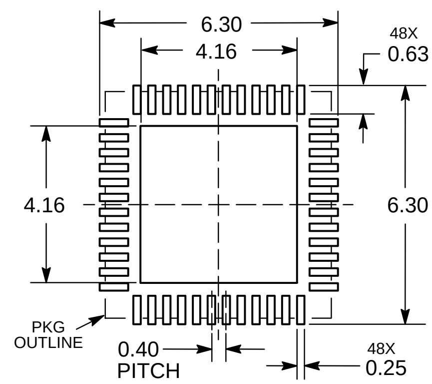
QFN48 6x6, 0.4P
CASE 485DP
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.15	0.25
D	6.00 BSC	
D2	3.90	4.10
E	6.00 BSC	
E2	3.90	4.10
e	0.40 BSC	
L	0.30	0.50
L1	0.00	0.15
L2	0.08 REF	

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and

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