

June 2010

# FQD12N20LTM\_F085

# 200V Logic Level N-Channel MOSFET

## **General Description**

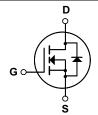
These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switching DC/DC converters, switch mode power supply, motor control.

## **Features**

- 9.0A, 200V,  $R_{DS(on)} = 0.28\Omega @V_{GS} = 10 V$
- Low gate charge (typical 16 nC)
- Low Crss (typical 17 pF)
- Fast switching
- · 100% avalanche tested
- · Improved dv/dt capability
- Low level gate drive requirement allowing direct opration from logic drivers
- Qualified to AEC Q101
- RoHS Compliant





# Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted

Symbol	Parameter		FQD12N20LTM_F085	Units	
$V_{DSS}$	Drain-Source Voltage		200	V	
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C)		9.0	Α	
	- Continuous (T <sub>C</sub> = 100°C)		5.7	Α	
I <sub>DM</sub>	Drain Current - Pulsed	(Note 1)	36	Α	
V <sub>GSS</sub>	Gate-Source Voltage		± 20	V	
I <sub>AR</sub>	Avalanche Current	(Note 1)	9.0	Α	
dv/dt	Peak Diode Recovery dv/dt	(Note 2)	5.5	V/ns	
P <sub>D</sub>	Power Dissipation (T <sub>A</sub> = 25°C) *		2.5	W	
	Power Dissipation (T <sub>C</sub> = 25°C)		55	W	
	- Derate above 25°C		0.44	W/°C	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range		-55 to +150	°C	
T <sub>L</sub>	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C	

## **Thermal Characteristics**

Symbol	Parameter	Тур	Max	Units	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case		2.27	°C/W	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *		50	°C/W	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient		110	°C/W	

<sup>\*</sup> When mounted on the minimum pad size recommended (PCB Mount)

36

1.5

128

0.56

(Note 3)

Α

٧

ns

μС

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Cha	racteristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	200			V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C		0.14		V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V			1	μА
		V <sub>DS</sub> = 160 V, T <sub>C</sub> = 125°C			10	μΑ
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0 V			-100	nA
On Cha	racteristics				•	
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	1.0		2.0	V
R <sub>DS(on)</sub>	Static Drain-Source $V_{GS} = 10 \text{ V}, I_D = 4.5 \text{ A}$			0.22	0.28	
	On-Resistance	$V_{GS} = 5 \text{ V}, I_D = 4.5 \text{ A}$		0.25	0.32	Ω
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 4.5 A (Note 3)		11.6		S
Dynam	ic Characteristics				•	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V,		830	1080	pF
C <sub>oss</sub>	Output Capacitance	f = 1.0 MHz		120	155	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			17	22	pF
Switchi	ng Characteristics					
t <sub>d(on)</sub>	Turn-On Delay Time	V = 100 V I = 11 6 A		15	40	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{DD} = 100 \text{ V}, I_{D} = 11.6 \text{ A},$ $R_{G} = 25 \Omega$		190	390	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			60	130	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 3, 4)		120	250	ns
Qg	Total Gate Charge	V <sub>DS</sub> = 160 V, I <sub>D</sub> = 11.6 A,		16	21	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = 5 V		2.8		nC
Q <sub>gd</sub>	Gate-Drain Charge	(Note 3, 4)		7.6		nC
D' 6	District Clarify	- 1 M 2				
	Ource Diode Characteristics at				9.0	Α
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				9.0	A

# Q<sub>rr</sub>

 $I_{SM}$ 

 $V_{SD}$ 

 $\mathsf{t}_{\mathsf{rr}}$ 

Notes: Notes: Notes: A specific Notes: Pulse width limited by maximum junction temperature 2.  $I_{SD} \leq 11.6A$ , di/dt  $\leq 300$ A/ $\mu$ s,  $V_{DD} \leq BV_{DSS}$ , Starting  $T_J$  = 25°C 3. Pulse Test: Pulse width  $\leq 300$  $\mu$ s, Duty cycle  $\leq 2$ % 4. Essentially independent of operating temperature

Drain-Source Diode Forward Voltage

Maximum Pulsed Drain-Source Diode Forward Current

Reverse Recovery Time

Reverse Recovery Charge

 $V_{GS} = 0 \text{ V}, I_{S} = 9.0 \text{ A}$ 

 $V_{GS} = 0 \text{ V}, I_{S} = 11.6 \text{ A},$   $dI_{F} / dt = 100 \text{ A/}\mu\text{s}$ 

# **Typical Characteristics**

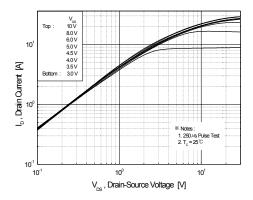


Figure 1. On-Region Characteristics

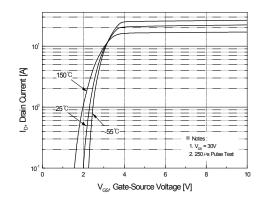


Figure 2. Transfer Characteristics

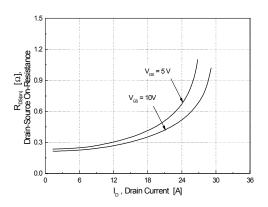


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

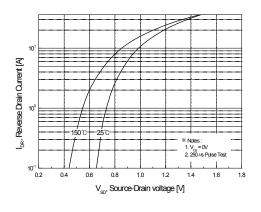


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

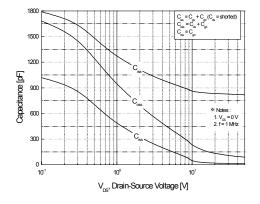


Figure 5. Capacitance Characteristics

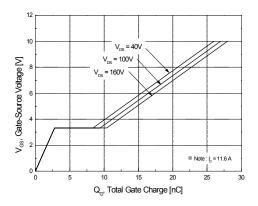


Figure 6. Gate Charge Characteristics

# Typical Characteristics (Continued)

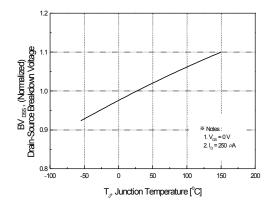
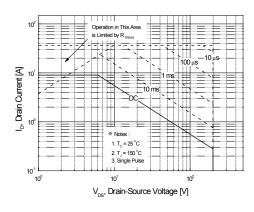


Figure 7. Breakdown Voltage Variation vs. Temperature

Figure 8. On-Resistance Variation vs. Temperature



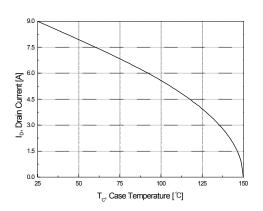


Figure 9. Maximum Safe Operating Area

Figure 10. Maximum Drain Current vs. Case Temperature

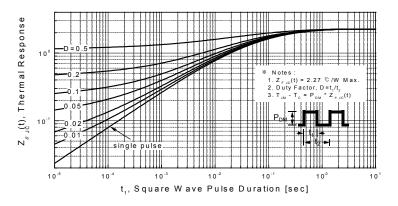


Figure 11. Transient Thermal Response Curve

# **Typical Characteristics**

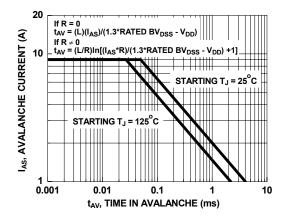
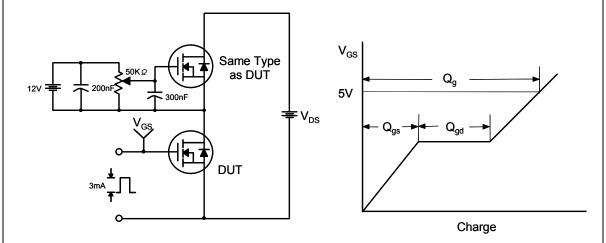
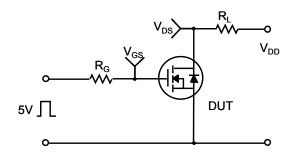


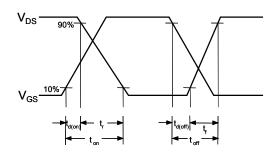
Figure 12. Unclamped Inductive Switching Capability

# **Gate Charge Test Circuit & Waveform**

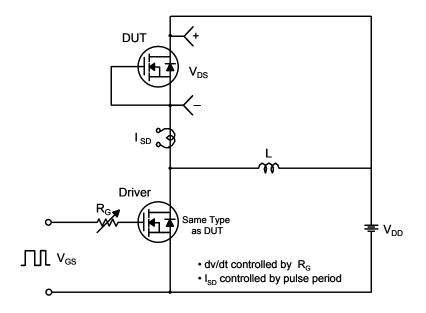


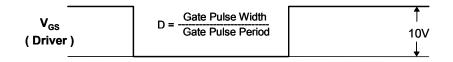
## **Resistive Switching Test Circuit & Waveforms**

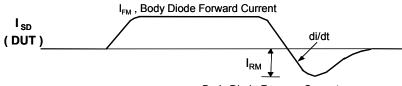




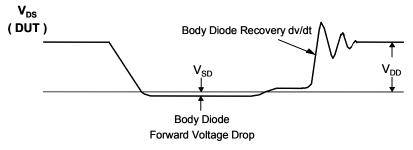
## Peak Diode Recovery dv/dt Test Circuit & Waveforms

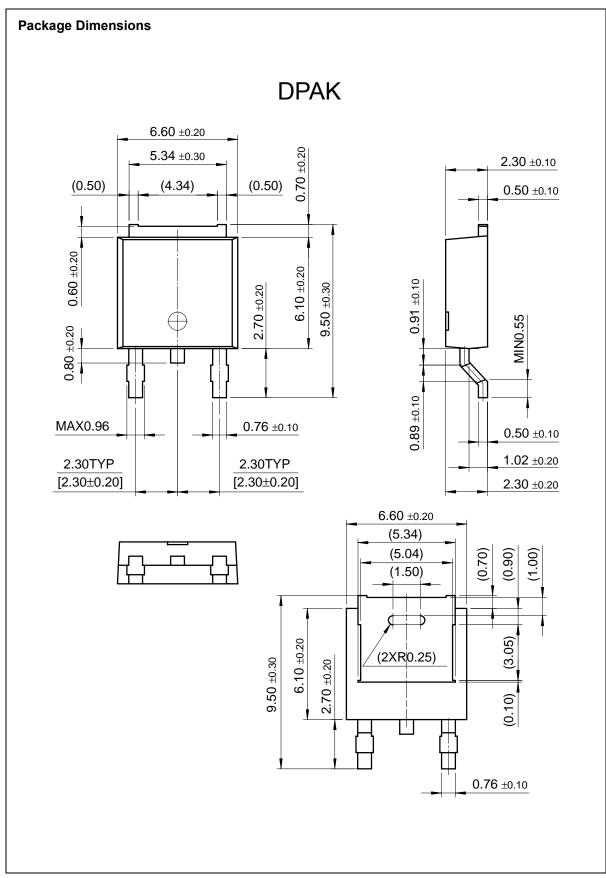






Body Diode Reverse Current









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