
3-wire Serial EEPROM
1K (128 x 8 or 64 x 16)

DATASHEET

Features

- Low-voltage Operation
 - $V_{CC} = 1.8V$ to $5.5V$
- User-selectable Internal Organization
 - 1K: 128 x 8 or 64 x 16
- 3-wire Serial Interface
- 2MHz Clock Rate (5V)
- Self-timed Write Cycle (5ms Max)
- High Reliability
 - Endurance: 1,000,000 Write Cycles
 - Data Retention: 100 Years
- 8-lead JEDEC SOIC, 8-lead TSSOP, 8-pad UDFN, 8-lead PDIP, and 8-ball VFBGA Packages

Description

The Atmel® AT93C46D provides 1,024 bits of Serial Electrically Erasable Programmable Read-Only Memory (EEPROM) organized as 64 words of 16 bits each (when the ORG pin is connected to V_{CC}) and 128 words of 8 bits each (when the ORG pin is tied to ground). The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operations are essential. The AT93C46D is available in space-saving 8-lead JEDEC SOIC, 8-lead TSSOP, 8-pad UDFN, 8-lead PDIP, and 8-ball VFBGA packages.

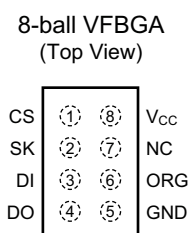
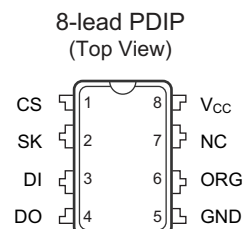
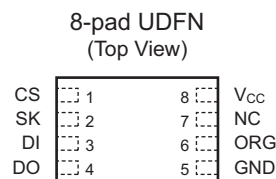
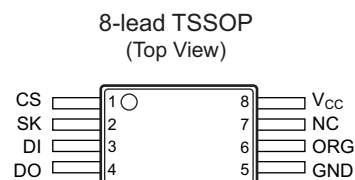
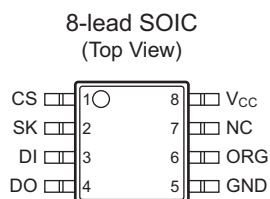
The AT93C46D is enabled through the Chip Select pin (CS) and accessed via a 3-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a Read instruction at DI, the address is decoded, and the data is clocked out serially on the DO pin. The write cycle is completely self-timed, and no separate erase cycle is required before Write. The write cycle is only enabled when the part is in the Erase/Write Enable state. When CS is brought high following the initiation of a write cycle, the DO pin outputs the Ready/Busy status of the part.

The AT93C46D operates from 1.8V to 5.5V.

1. Pin Configurations and Pinouts

Table 1-1. Pin Configurations

Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V _{CC}	Power Supply
ORG	Internal Organization
NC	No Connect



Note: Drawings are not to scale.

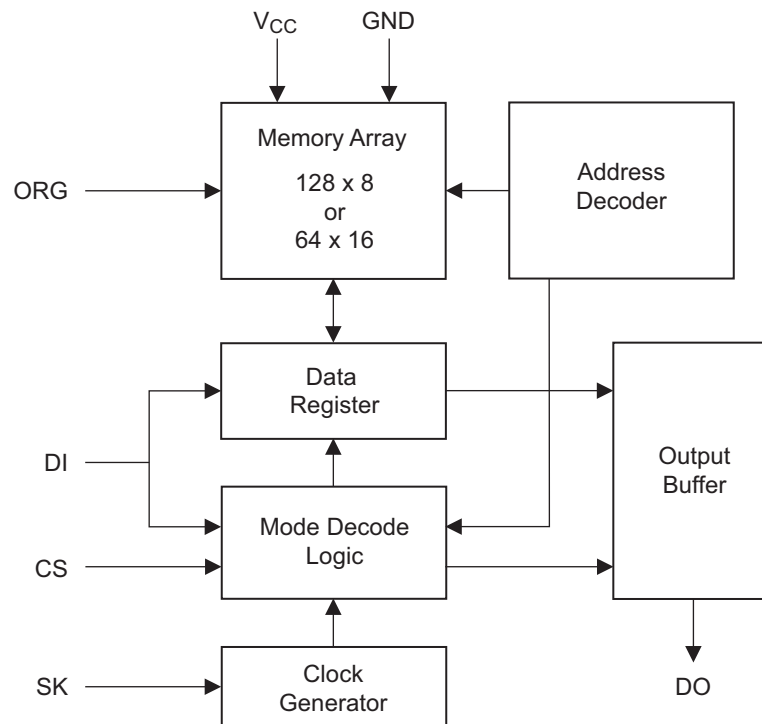
2. Absolute Maximum Ratings*

Operating Temperature -55°C to +125°C
Storage Temperature -65°C to +150°C
Voltage on any pin
with respect to ground -1.0V to +7.0V
Maximum Operating Voltage 6.25V
DC Output Current 5.0mA

*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3. Block Diagram

Figure 3-1. Block Diagram



- Notes:
1. When the ORG pin is connected to V_{CC} , the x16 organization is selected. When it is connected to ground, the x8 organization is selected. If the ORG pin is left unconnected and the application does not load the input beyond the capability of the internal $1M\Omega$ pull-up resistor, then the x16 organization is selected.
 2. If the x16 organization is the mode of choice and pin 6 (ORG) is left unconnected, Atmel recommends using AT93C46E device. For more details, see the AT93C46E datasheet.

4. Memory Organization

4.1 Pin Capacitance

Table 4-1. Pin Capacitance⁽¹⁾

Applicable over recommended operating range from $T_A = 25^\circ\text{C}$, $f = 1.0\text{MHz}$, $V_{CC} = 1.8\text{V}$ (unless otherwise noted).

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	$V_{OUT} = 0\text{V}$
C_{IN}	Input Capacitance (CS, SK, DI)	5	pF	$V_{IN} = 0\text{V}$

Note: 1. This parameter is characterized, and is not 100% tested.

4.2 DC Characteristics

Table 4-2. DC Characteristics

Applicable over recommended operating range from $T_{AI} = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 1.8\text{V}$ to 5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
V_{CC1}	Supply Voltage			1.8		5.5	V
V_{CC2}	Supply Voltage			2.7		5.5	V
V_{CC3}	Supply Voltage			4.5		5.5	V
I_{CC}	Supply Current	$V_{CC} = 5.0\text{V}$	Read at 1.0MHz		0.5	2.0	mA
			Write at 1.0MHz		0.5	2.0	mA
I_{SB1}	Standby Current	$V_{CC} = 1.8\text{V}$	CS = 0V		0.4	1.0	μA
I_{SB2}	Standby Current	$V_{CC} = 2.7\text{V}$	CS = 0V		6.0	10.0	μA
I_{SB3}	Standby Current	$V_{CC} = 5.0\text{V}$	CS = 0V		10.0	15.0	μA
I_{IL}	Input Leakage	$V_{IN} = 0\text{V}$ to V_{CC}			0.1	1.0	μA
I_{OL}	Output Leakage	$V_{IN} = 0\text{V}$ to V_{CC}			0.1	1.0	μA
$V_{IL1}^{(1)}$	Input Low Voltage	$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$		-0.6		0.8	V
$V_{IH1}^{(1)}$	Input High Voltage	$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$		2.0		$V_{CC} + 1$	V
$V_{IL2}^{(1)}$	Input Low Voltage	$1.8\text{V} \leq V_{CC} \leq 2.7\text{V}$		-0.6		$V_{CC} \times 0.3$	V
$V_{IH2}^{(1)}$	Input High Voltage	$1.8\text{V} \leq V_{CC} \leq 2.7\text{V}$		$V_{CC} \times 0.7$		$V_{CC} + 1$	V
V_{OL1}	Output Low Voltage	$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	$I_{OL} = 2.1\text{mA}$			0.4	V
V_{OH1}	Output High Voltage	$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	$I_{OH} = -0.4\text{mA}$	2.4			V
V_{OL2}	Output Low Voltage	$1.8\text{V} \leq V_{CC} \leq 2.7\text{V}$	$I_{OL} = 0.15\text{mA}$			0.2	V
V_{OH2}	Output High Voltage	$1.8\text{V} \leq V_{CC} \leq 2.7\text{V}$	$I_{OH} = -100\mu\text{A}$	$V_{CC} - 0.2$			V

Note: 1. V_{IL} min and V_{IH} max are reference only, and are not tested.

4.3 AC Characteristics

Table 4-3. AC Characteristics

Applicable over recommended operating range from $T_{AI} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} =$ as specified, $CL = 1$ TTL gate and 100pF (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
f_{SK}	SK Clock Frequency	$4.5V \leq V_{CC} \leq 5.5V$	0		2	MHz
		$2.7V \leq V_{CC} \leq 5.5V$	0		1	MHz
		$1.8V \leq V_{CC} \leq 5.5V$	0		250	kHz
t_{SKH}	SK High Time	$4.5V \leq V_{CC} \leq 5.5V$	250			ns
		$2.7V \leq V_{CC} \leq 5.5V$	250			ns
		$1.8V \leq V_{CC} \leq 5.5V$	1000			ns
t_{SKL}	SK Low Time	$4.5V \leq V_{CC} \leq 5.5V$	250			ns
		$2.7V \leq V_{CC} \leq 5.5V$	250			ns
		$1.8V \leq V_{CC} \leq 5.5V$	1000			ns
t_{CS}	Minimum CS Low Time	$4.5V \leq V_{CC} \leq 5.5V$	250			ns
		$2.7V \leq V_{CC} \leq 5.5V$	250			ns
		$1.8V \leq V_{CC} \leq 5.5V$	1000			ns
t_{CSS}	CS Setup Time	Relative to SK	$4.5V \leq V_{CC} \leq 5.5V$	50		ns
			$2.7V \leq V_{CC} \leq 5.5V$	50		ns
			$1.8V \leq V_{CC} \leq 5.5V$	200		ns
t_{DIS}	DI Setup Time	Relative to SK	$4.5V \leq V_{CC} \leq 5.5V$	100		ns
			$2.7V \leq V_{CC} \leq 5.5V$	100		ns
			$1.8V \leq V_{CC} \leq 5.5V$	400		ns
t_{CSH}	CS Hold Time	Relative to SK		0		ns
t_{DIH}	DI Hold Time	Relative to SK	$4.5V \leq V_{CC} \leq 5.5V$	100		ns
			$2.7V \leq V_{CC} \leq 5.5V$	400		ns
			$1.8V \leq V_{CC} \leq 5.5V$			ns
t_{PD1}	Output Delay to 1	AC Test	$4.5V \leq V_{CC} \leq 5.5V$		250	ns
			$2.7V \leq V_{CC} \leq 5.5V$		250	ns
			$1.8V \leq V_{CC} \leq 5.5V$		1000	ns
t_{PD0}	Output Delay to 0	AC Test	$4.5V \leq V_{CC} \leq 5.5V$		250	ns
			$2.7V \leq V_{CC} \leq 5.5V$		250	ns
			$1.8V \leq V_{CC} \leq 5.5V$		1000	ns
t_{SV}	CS to Status Valid	AC Test	$4.5V \leq V_{CC} \leq 5.5V$		250	ns
			$2.7V \leq V_{CC} \leq 5.5V$		250	ns
			$1.8V \leq V_{CC} \leq 5.5V$		1000	ns
t_{DF}	CS to DO in High-impedance	AC Test CS = V_{IL}	$4.5V \leq V_{CC} \leq 5.5V$		100	ns
			$2.7V \leq V_{CC} \leq 5.5V$		250	ns
			$1.8V \leq V_{CC} \leq 5.5V$		400	ns
t_{WP}	Write Cycle Time	$1.8V \leq V_{CC} \leq 5.5V$	0.1	3	5	ms
Endurance ⁽¹⁾	5.0V, 25°C			1,000,000		Write Cycles

Note: 1. This parameter is characterized, and is not 100% tested.

5. Functional Description

The AT93C46D is accessed via a simple and versatile 3-wire serial communication interface. Device operation is controlled by seven instructions issued by the Host processor. A valid instruction starts with a rising edge of CS and consists of a Start bit (Logic 1), followed by the appropriate opcode, and the desired memory address location.

Table 5-1. AT93C46D Instruction Set

Instruction	SB	Opcode	Address		Data		Comments
			x8 ⁽¹⁾	x16 ⁽¹⁾	x8	x16	
READ	1	10	A ₆ – A ₀	A ₅ – A ₀			Reads data stored in memory at specified address.
EWEN	1	00	11XXXXXXX	11XXXXXX			Write Enable must precede all programming modes.
ERASE	1	11	A ₆ – A ₀	A ₅ – A ₀			Erases memory location A _N – A ₀ .
WRITE	1	01	A ₆ – A ₀	A ₅ – A ₀	D ₇ – D ₀	D ₁₅ – D ₀	Writes memory location A _N – A ₀ .
ERAL	1	00	10XXXXXXX	10XXXXXX			Erases all memory locations. Valid only at V _{CC3} (Section 4.2, “DC Characteristics” on page 4).
WRAL	1	00	01XXXXXXX	01XXXXXX	D ₇ – D ₀	D ₁₅ – D ₀	Writes all memory locations. Valid only at V _{CC3} (Section 4.2).
EWDS	1	00	00XXXXXXX	00XXXXXX			Disables all programming instructions.

Note: 1. The ‘X’ in the address field represent don’t care values, and must be clocked.

READ: The READ instruction contains the address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the Serial Output pin, DO. Output data changes are synchronized with the rising edges of the Serial Clock pin, SK. It should be noted that a dummy bit (Logic 0) precedes the 8-bit or 16-bit data output string.

Erase/Write Enable (EWEN): To ensure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out.

Note: Once in the EWEN state, programming remains enabled until an EWDS instruction is executed, or V_{CC} power is removed from the part.

ERASE: The ERASE instruction programs all bits in the specified memory location to the Logic 1 state. The self-timed erase cycle starts once the ERASE instruction and address are decoded. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of t_{CS}. A Logic 1 at the DO pin indicates that the selected memory location has been erased, and the part is ready for another instruction.

WRITE: The WRITE instruction contains the 8-bits or 16-bits of data to be written into the specified memory location. The self-timed programming cycle, t_{WP} , starts after the last bit of data is received at Serial Data Input pin DI. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of t_{CS} . A Logic 0 at DO indicates that programming is still in progress. A Logic 1 indicates that the memory location at the specified address has been written with the data pattern contained in the instruction, and the part is ready for further instructions. A Ready/Busy status cannot be obtained if CS is brought high after the end of the self-timed programming cycle, t_{WP} .

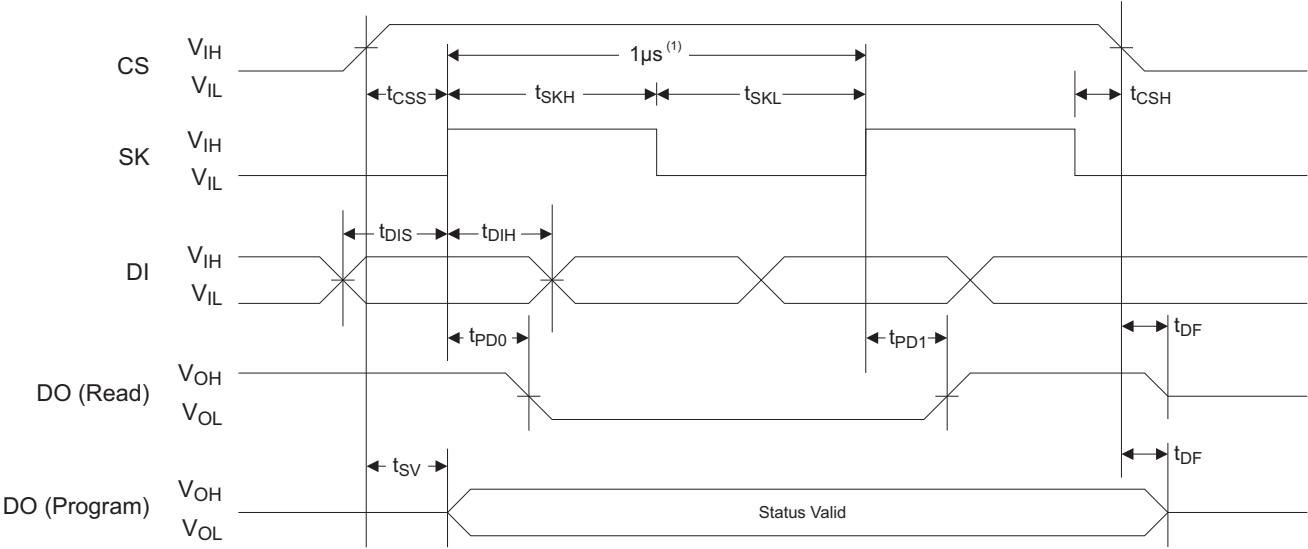
Erase All (ERAL): The Erase All (ERAL) instruction programs every bit in the Memory Array to the Logic 1 state and is primarily used for testing purposes. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of t_{CS} . The ERAL instruction is valid only at $V_{CC} = 5.0V \pm 10\%$ ([Section 4.2](#), “DC Characteristics” on page 4).

Write All (WRAL): The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of t_{CS} . The WRAL instruction is valid only at $V_{CC} = 5.0V \pm 10\%$ ([Section 4.2](#)).

Erase/Write Disable (EWDS): To protect against accidental data disturbance, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the Read instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

6. Timing Diagrams

Figure 6-1. Synchronous Data Timing



Note: 1. This is the minimum SK period.

Table 6-1. Organization Key for Timing Diagrams

I/O	AT93C46D (1K)	
	x8	x16
A _N	A ₆	A ₅
D _N	D ₇	D ₁₅

Figure 6-2. READ Timing

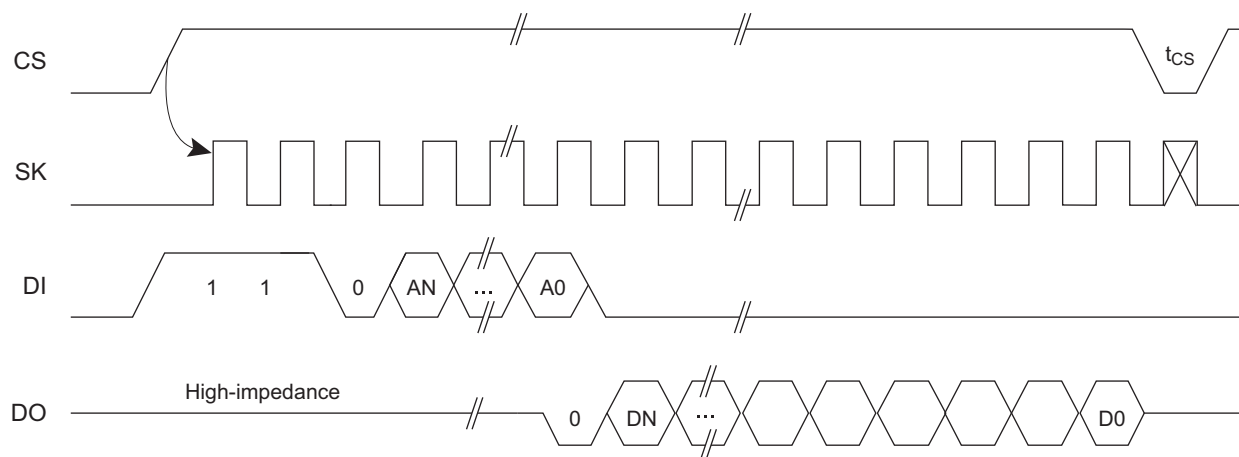


Figure 6-3. EWEN Timing

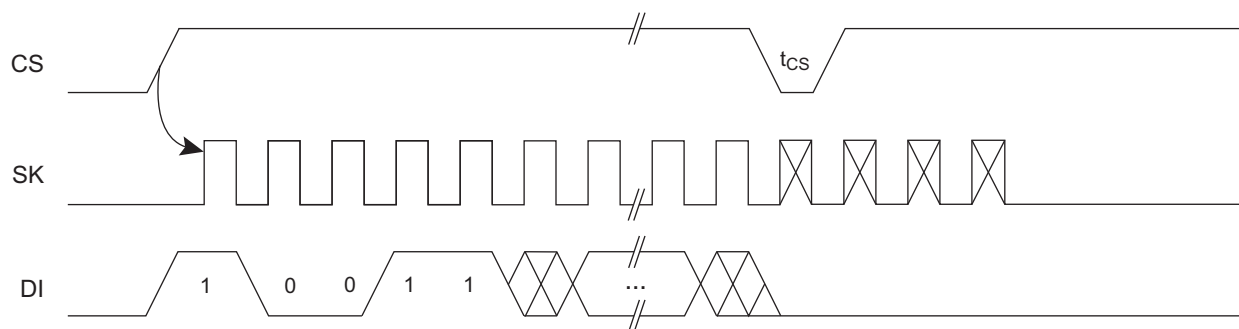


Figure 6-4. EWDS Timing

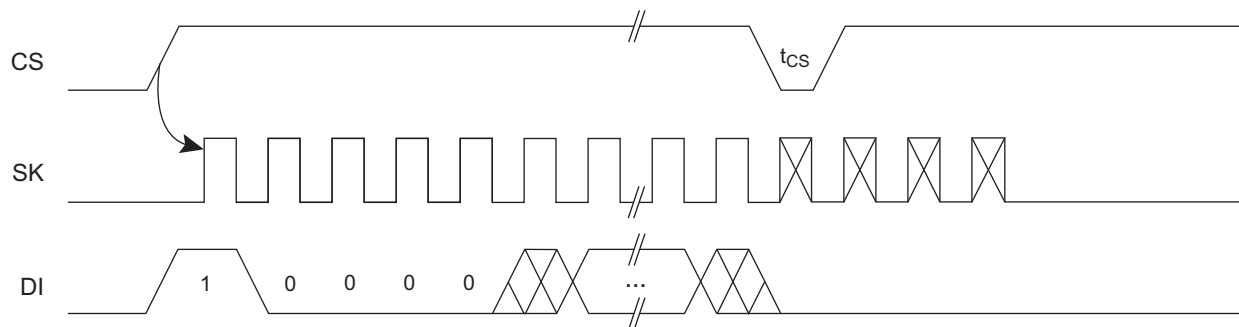


Figure 6-5. WRITE Timing

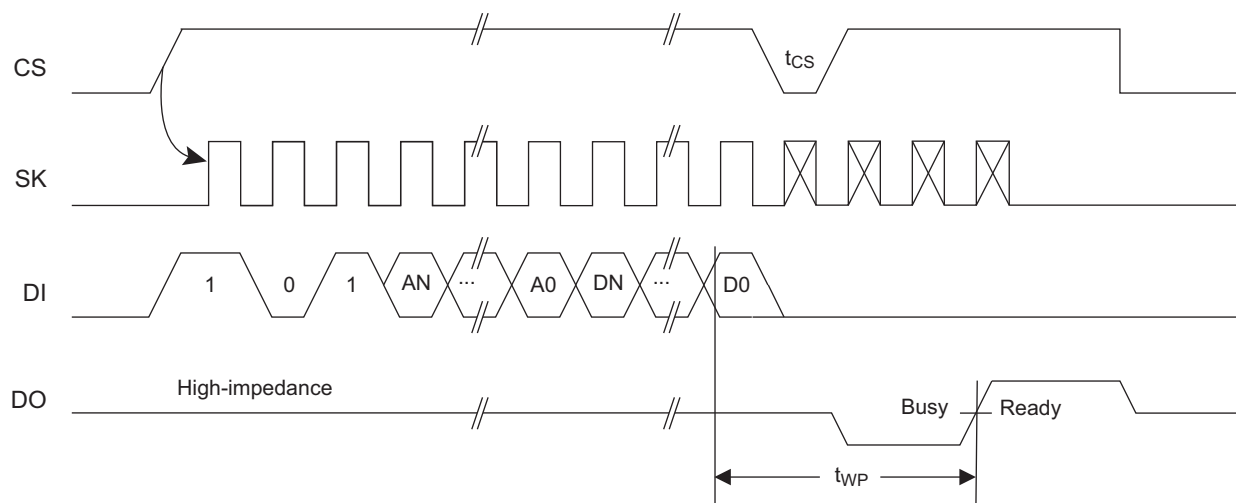
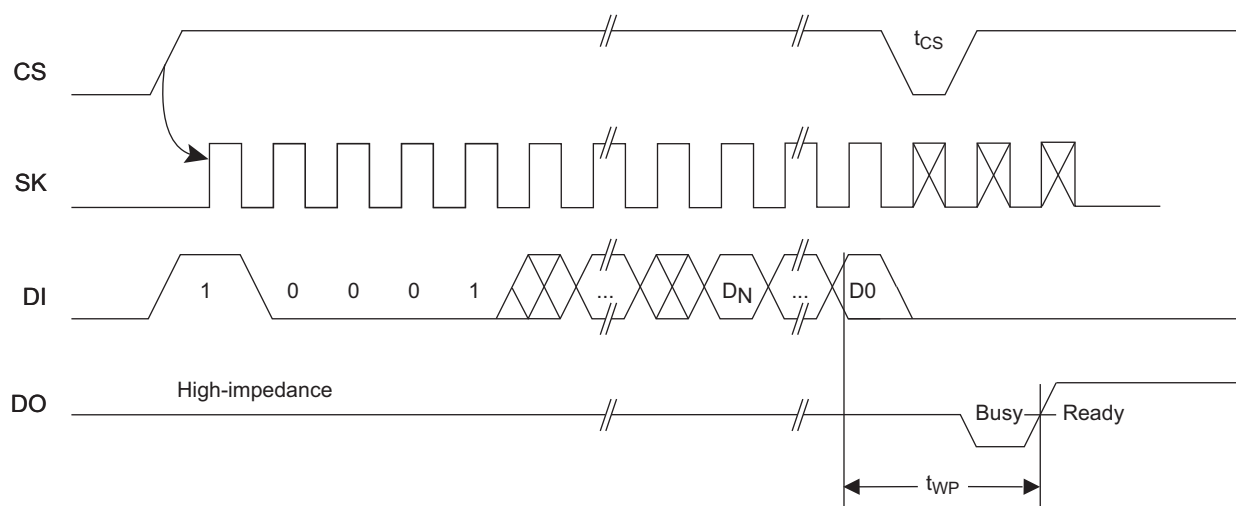


Figure 6-6. WRAL Timing⁽¹⁾



Note: 1. Valid only at V_{CC3} (Section 4.2, "DC Characteristics" on page 4).

Figure 6-7. ERASE Timing

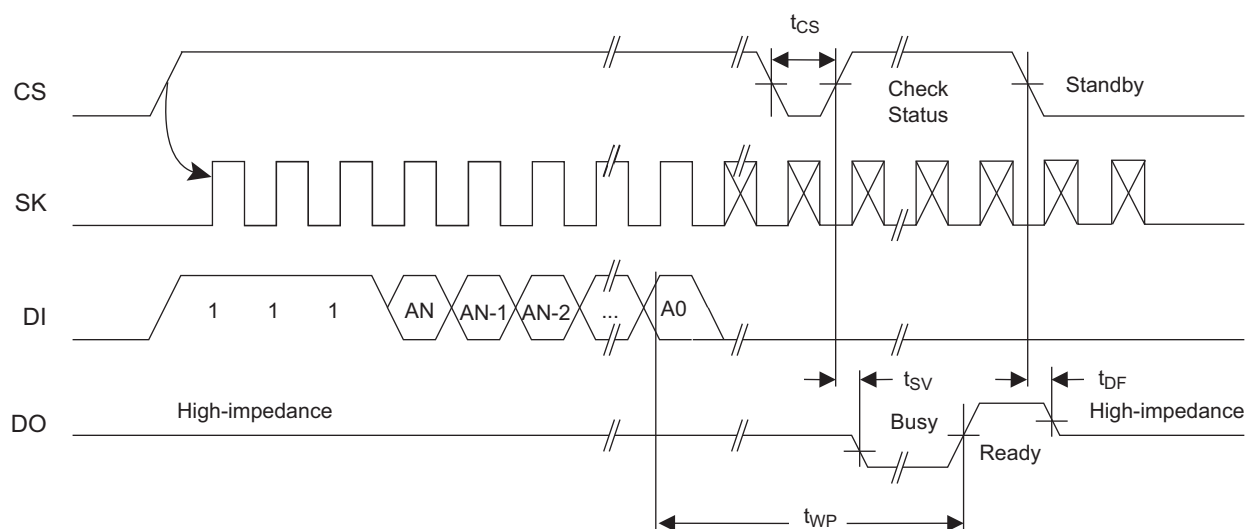
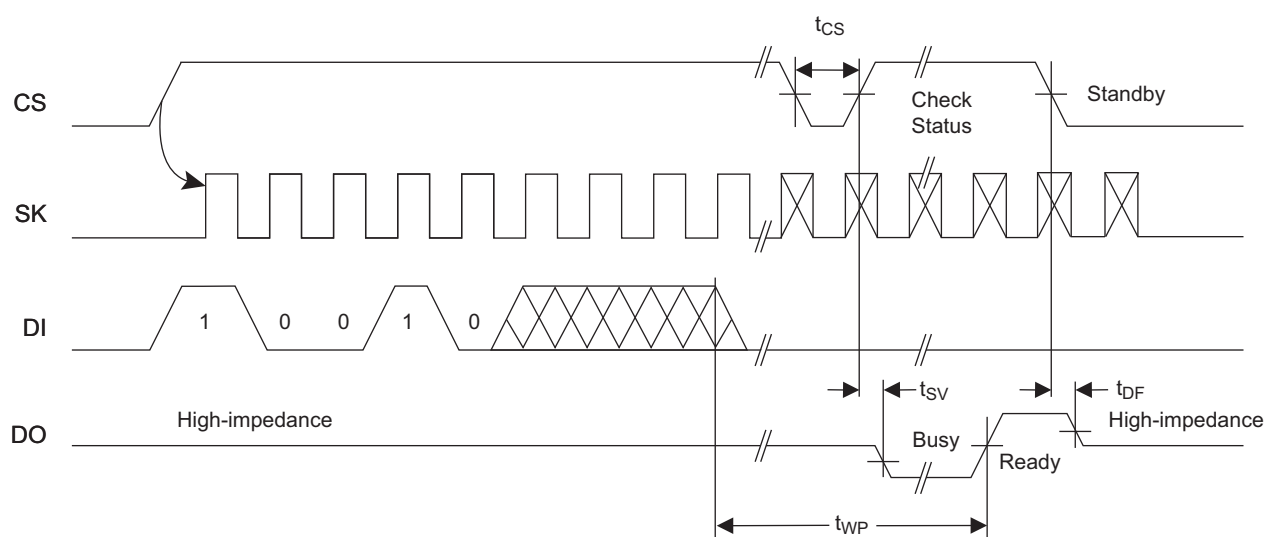
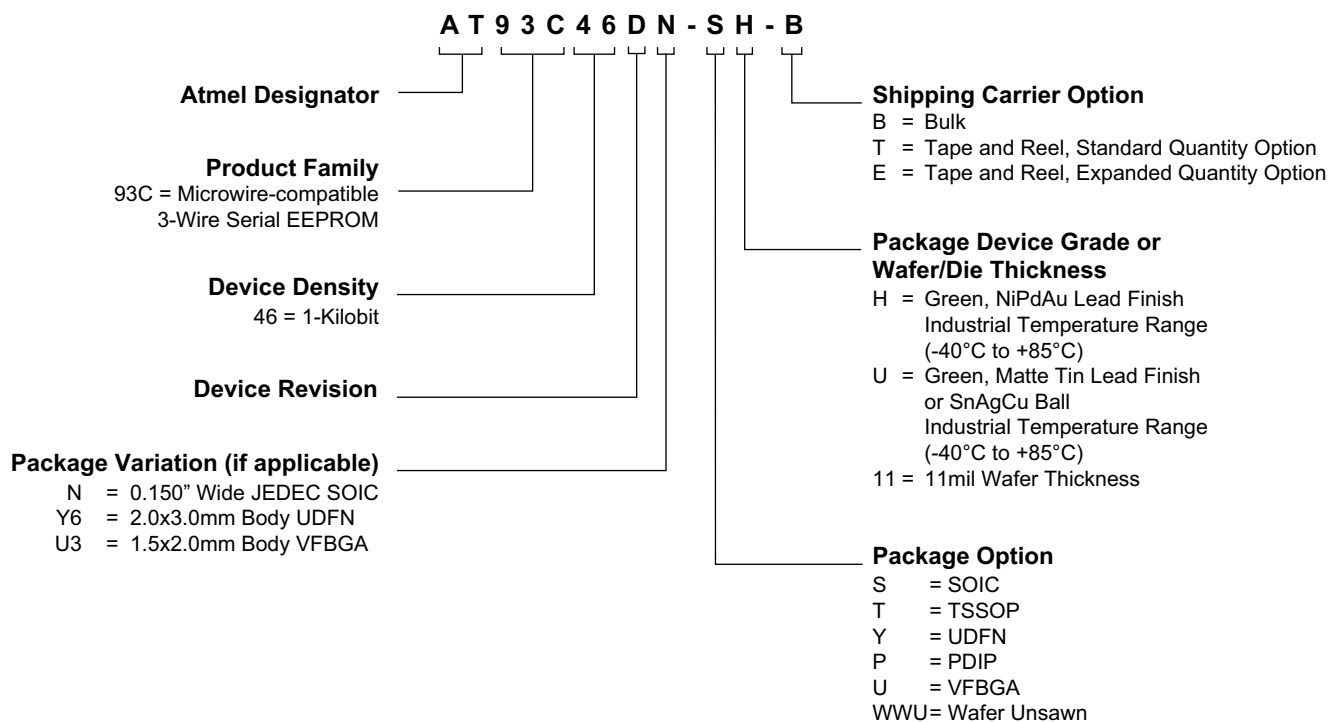


Figure 6-8. ERAL Timing⁽¹⁾



Note: 1. Valid only at V_{CC3} (Section 4.2, "DC Characteristics" on page 4).

7. Ordering Code Detail



8. Ordering Information

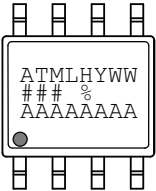
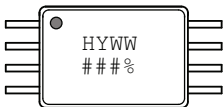
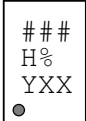
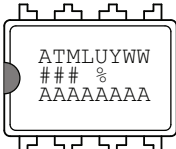
Atmel Ordering Code	Lead Finish	Package	Delivery Information		Operation Range
			Form	Quantity	
AT93C46DN-SH-B	NiPdAu (Lead-free/Halogen-free)	8S1	Bulk (Tubes)	100 per Tube	Industrial Temperature (-40°C to 85°C)
AT93C46DN-SH-T			Tape and Reel	4,000 per Reel	
AT93C46D-TH-B		8X	Bulk (Tubes)	100 per Tube	
AT93C46D-TH-T			Tape and Reel	5,000 per Reel	
AT93C46DY6-YH-T		8MA2	Tape and Reel	5,000 per Reel	
AT93C46DY6-YH-E			Tape and Reel	15,000 per Reel	
AT93C46D-PU	Matte Tin (Lead-free/Halogen free)	8P3	Bulk (Tubes)	50 per Tube	
AT93C46DU3-UU-T	SnAgCu (Lead-free/Halogen-free)	8U3-1	Tape and Reel	5,000 per Reel	
AT93C46D-W-11 ⁽¹⁾	N/A	Wafer Sale	Note 1		

Note: 1. For wafer sales, please contact Atmel sales. Bumped die available upon request.

Package Type	
8S1	8-lead, 0.150" wide, Plastic Gull Wing, Small Outline (JEDEC SOIC)
8X	8-lead, 0.170" wide, Thin Shrink Small Outline (TSSOP)
8MA2	8-pad, 2.00mm x 3.00mm body, 0.50mm pitch, Ultra Thin Dual No Lead (UDFN)
8P3	8-lead, 0.300" wide body, Plastic Dual In-line Package (PDIP)
8U3-1	8-ball, 1.50mm x 2.00mm body, 0.50mm pitch, Small Die Ball Grid Array (VFBGA)

9. Part Markings

AT93C46D: Package Marking Information

8-lead SOIC 	8-lead TSSOP  <i>Note: Lot Number and location of assembly and on the bottom side of the package.</i>	8-pad UDFN 2.0 x 3.0 mm Body 
8-lead PDIP 	8-ball VFBGA 1.5 x 2.0 mm Body 	

Note 1: ● designates pin 1

Note 2: Package drawings are not to scale

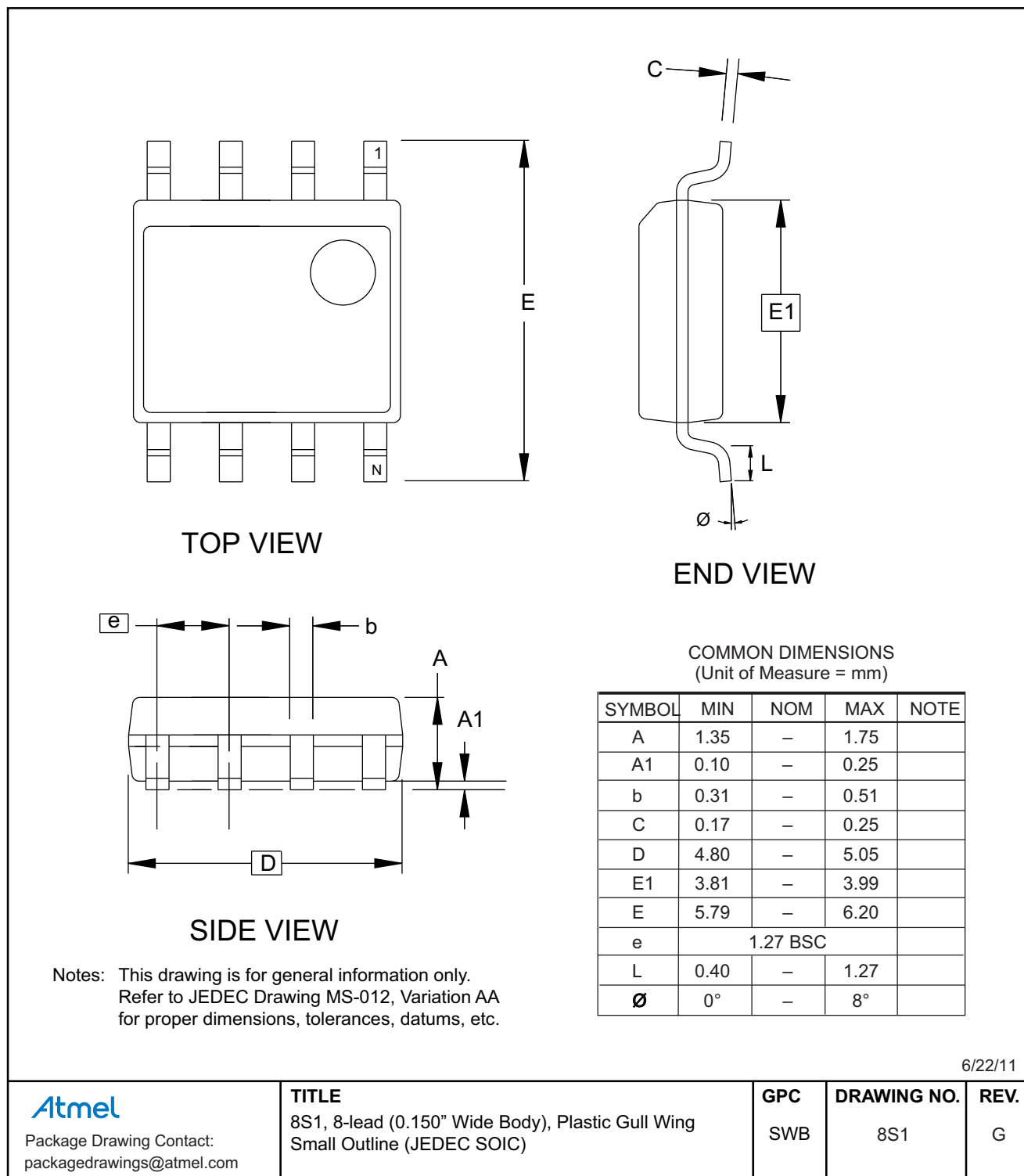
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AT93C46D		Truncation Code ###: 46D		
Date Codes			Voltages	
Y = Year		M = Month	WW = Work Week of Assembly	% = Minimum Voltage
4: 2014	8: 2018	A: January	02: Week 2	1: 1.8V min
5: 2015	9: 2019	B: February	04: Week 4	
6: 2016	0: 2020	...	...	
7: 2017	1: 2021	L: December	52: Week 52	
Country of Assembly		Lot Number		Grade/Lead Finish Material
@ = Country of Assembly		AAA...A = Atmel Wafer Lot Number		H: Industrial/NiPdAu U: Industrial/Matte Tin/SnAgCu
Trace Code				Atmel Truncation
XX = Trace Code (Atmel Lot Numbers Correspond to Code) Example: AA, AB.... YZ, ZZ				AT: Atmel ATM: Atmel ATML: Atmel

6/11/14

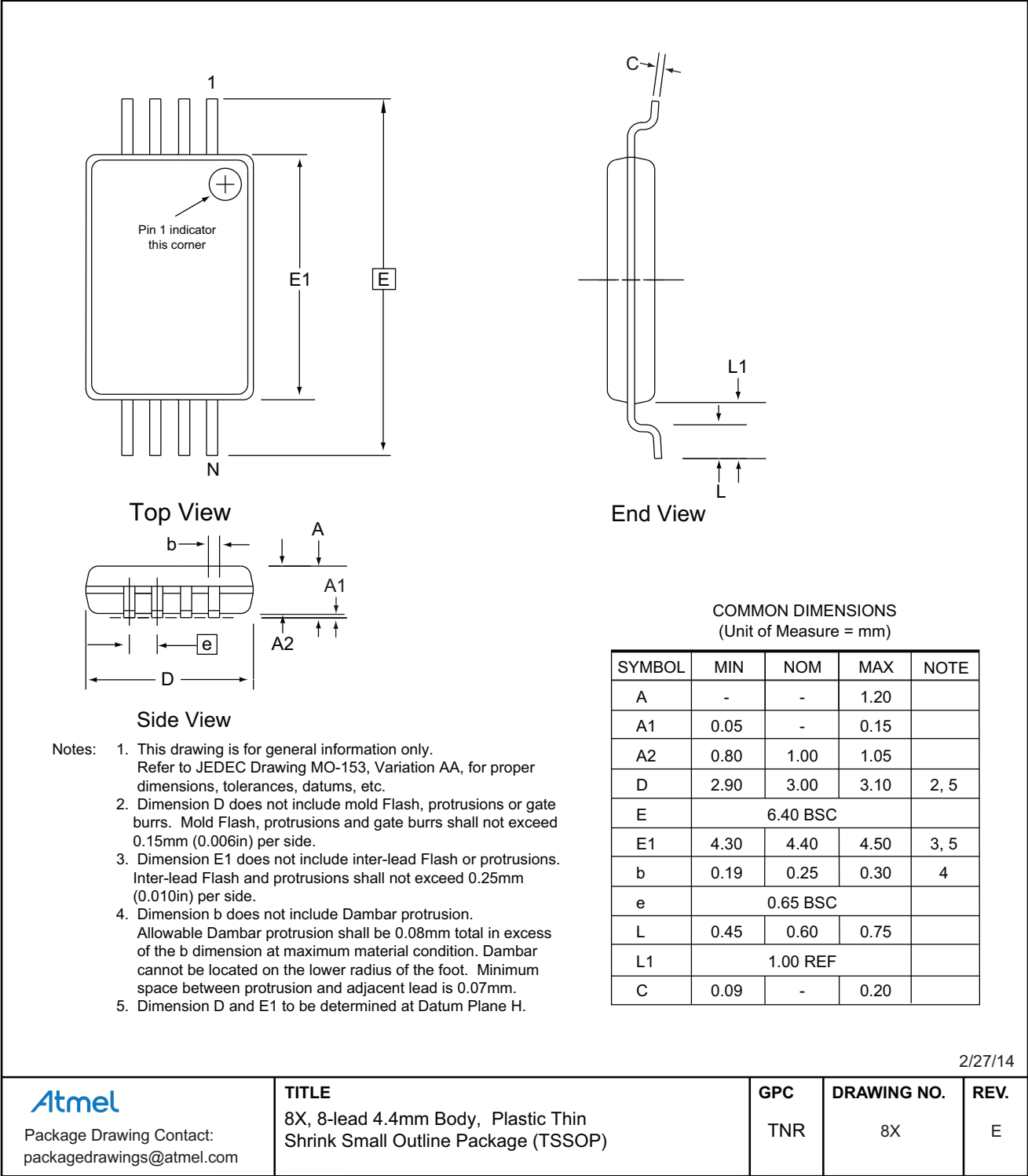
 Package Mark Contact: DL-CSO-Assy_eng@atmel.com	TITLE 93C46DSM, AT93C46D Package Marking Information	DRAWING NO. 93C46DSM	REV. A
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10. Packaging Information

10.1 8S1 — 8-lead JEDEC SOIC



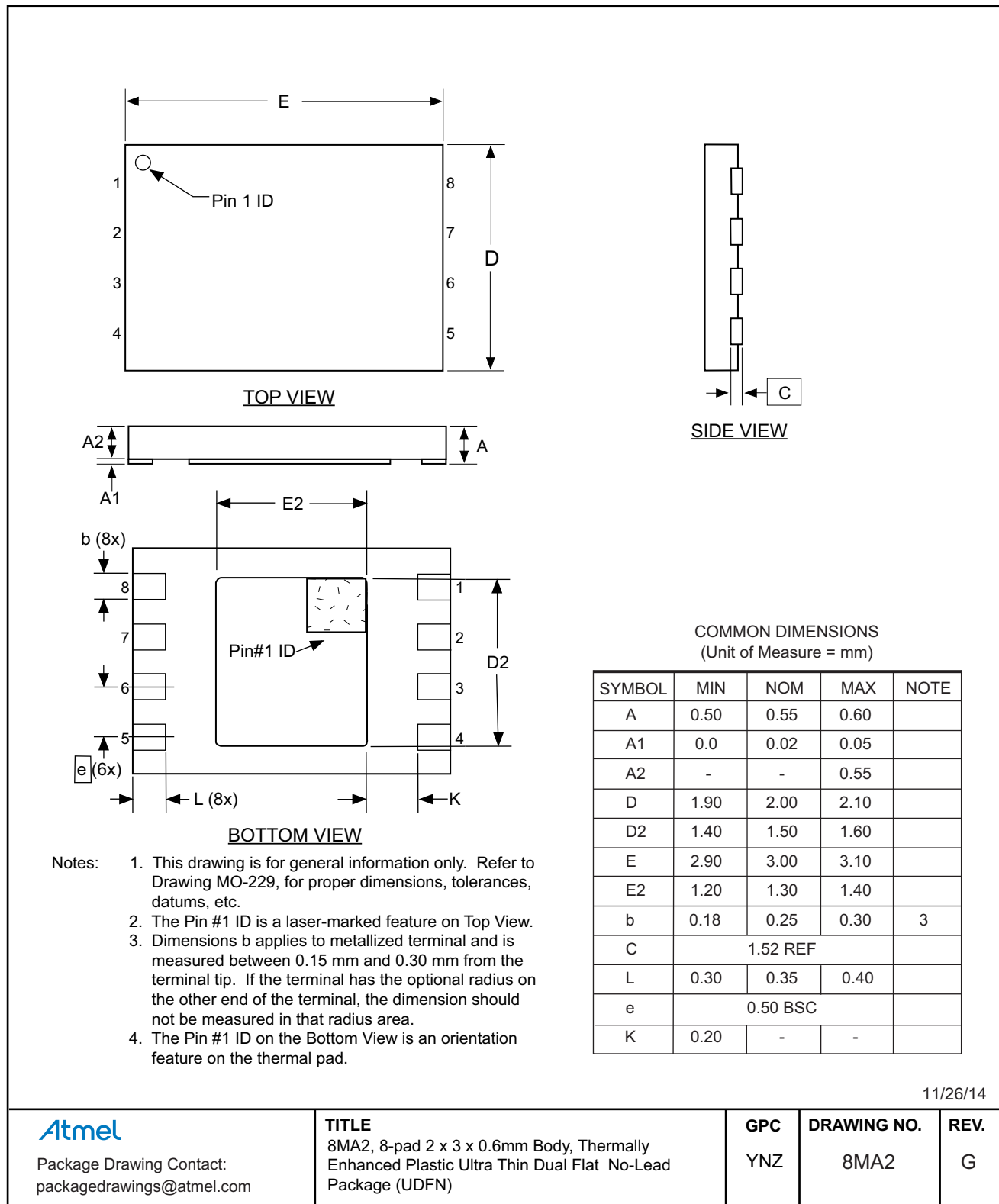
10.2 8X — 8-lead TSSOP



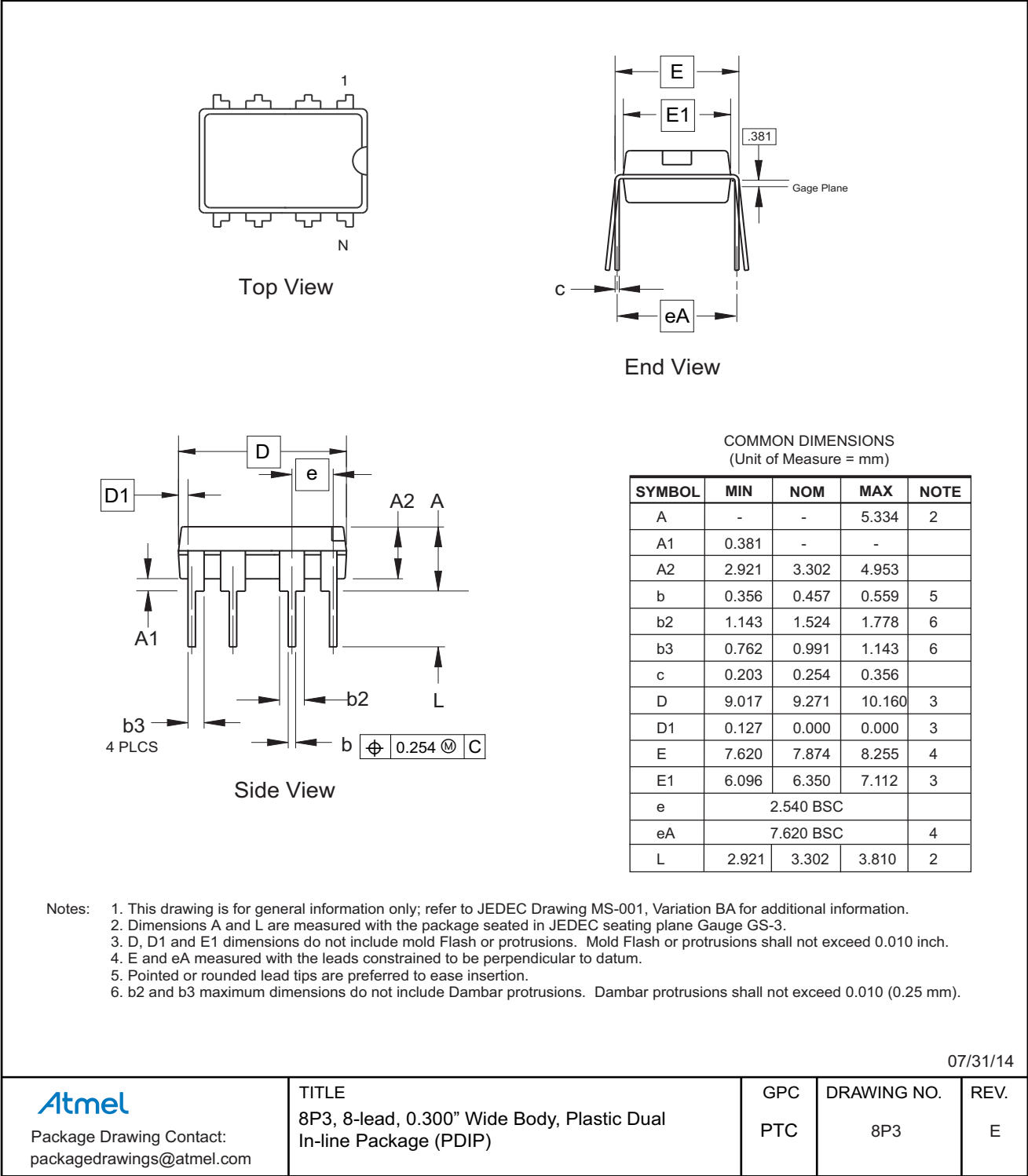
2/27/14

 Package Drawing Contact: packagedrawings@atmel.com	TITLE 8X, 8-lead 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	GPC TNR	DRAWING NO. 8X	REV. E
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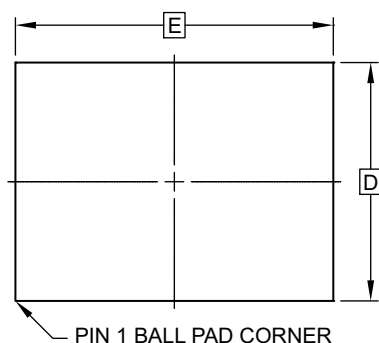
10.3 8MA2 — 8-pad UDFN



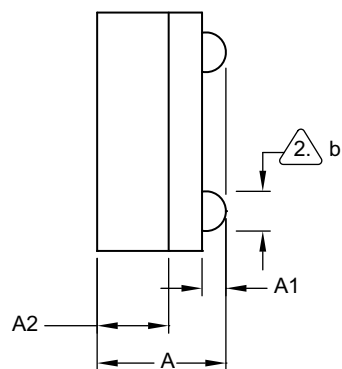
10.4 8P3 — 8-lead PDIP



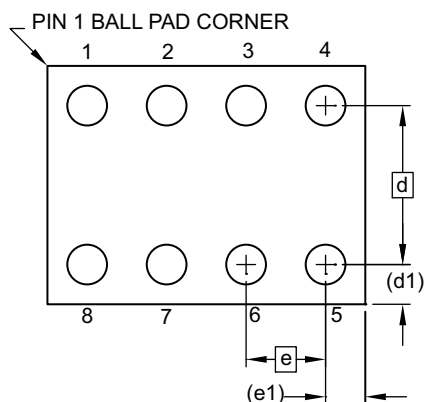
10.5 8U3-1 — 8-ball VFBGA



TOP VIEW



SIDE VIEW



BOTTOM VIEW
8 SOLDER BALLS

Notes:

1. This drawing is for general information only.
2. Dimension 'b' is measured at maximum solder ball diameter.
3. Solder ball composition shall be 95.5Sn-4.0Ag-.5Cu.

COMMON DIMENSIONS
(Unit of Measure - mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.73	0.79	0.85	
A1	0.09	0.14	0.19	
A2	0.40	0.45	0.50	
b	0.20	0.25	0.30	2
D	1.50 BSC			
E	2.0 BSC			
e	0.50 BSC			
e1	0.25 REF			
d	1.00 BSC			
d1	0.25 REF			

6/11/13



Package Drawing Contact:
packagedrawings@atmel.com

TITLE
8U3-1, 8-ball, 1.50mm x 2.00mm body, 0.50mm pitch,
Very Thin, Fine-Pitch Ball Grid Array Package (VFBGA)

GPC
GXU

DRAWING NO.
8U3-1

REV.
F

11. Revision History

Revision No.	Date	Comments
5193H	01/2015	Added the UDFN expanded quantity option and the ordering information section. Updated the 8MA2 and 8P3 package drawings.
5193G	08/2014	Updated package drawings, template, logos, and disclaimer page.
5193F	01/2008	Removed the 'preliminary' status.
5193E	11/2007	Modified the 'max' value in AC Characteristics table.
5193D	08/2007	Moved Pinout figure. Added new feature for Die Sales. Modified Ordering Information table layout. Modified Park Marking Schemes.
5193C	06/2007	Updated to new template. Added Product Markup Scheme. Added Technical email contact. Corrected Figures 4 and 5.
5193B	02/2007	Added 'Ultra Thin' description to 8-lead Mini-MAP package.
5193A	01/2007	Initial document release.

