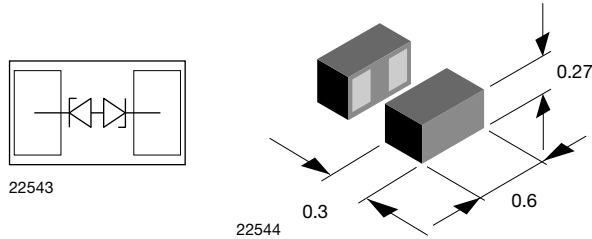




Bidirectional Symmetrical (BiSy) Single Line ESD Protection Diode in Silicon Package



FEATURES

- Ultra compact CLP0603 package
- Low package height < 0.3 mm
- 1-line ESD protection
- AEC-Q101 qualified available
- Working range ± 5.5 V
- Low leakage current < 0.1 μ A
- Low load capacitance $C_D < 14$ pF
- ESD immunity acc. IEC 61000-4-2 ± 30 kV contact discharge ± 30 kV air discharge
- Lead plating: Au (e4)
- Lead material: Ni
- Topside coating
- e4 - precious metal (e.g. Ag, Au, NiPd, NiPdAu) (no Sn)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



MARKING (example only)



1 = year code
 Open circle = month code and pin 1
 XY = type code

DESIGN SUPPORT TOOLS click logo to get started



| ORDERING INFORMATION | | | | | |
|-----------------------|--------------------------------|--|-------------|---|-------------------------|
| PART NUMBER (EXAMPLE) | ENVIRONMENTAL AND QUALITY CODE | | | PACKAGING CODE | ORDERING CODE (EXAMPLE) |
| | AEC-Q101 QUALIFIED | RoHS-COMPLIANT + LEAD (Pb)-FREE TERMINATIONS GREEN | GOLD PLATED | 15K PER 7" REEL (8 mm TAPE) 15K/BOX = MOQ | |
| VCUT05E1-SD0 | - | G | 4 | -08 | VCUT05E1-SD0-G4-08 |
| VCUT05E1-SD0 | H | G | 4 | -08 | VCUT05E1-SD0HG4-08 |

| PACKAGE DATA | | | | |
|--------------|--------------|-----------|---------|---|
| DEVICE NAME | PACKAGE NAME | TYPE CODE | WEIGHT | SOLDERING CONDITIONS |
| VCUT05E1-SD0 | CLP0603-2L | 5D | 0.12 mg | 260 °C/10 s at terminals Reflow soldering according JEDEC® STD-020 |

| ABSOLUTE MAXIMUM RATINGS | | | | |
|--------------------------|---|-----------|-------------|------|
| PARAMETER | TEST CONDITIONS | SYMBOL | VALUE | UNIT |
| Peak pulse current | acc. IEC 61000-4-5, 8/20 μ s/single shot | I_{PPM} | 6 | A |
| Peak pulse power | Pin 1 to pin 2 acc. IEC 61000-4-5; $t_p = 8/20$ μ s; single shot | P_{PP} | 78 | W |
| ESD immunity | Contact discharge acc. IEC 61000-4-2; 10 pulses | V_{ESD} | ± 30 | kV |
| | Air discharge acc. IEC 61000-4-2; 10 pulses | | ± 30 | |
| Operating temperature | Junction temperature | T_J | -55 to +150 | °C |
| Storage temperature | | T_{stg} | -55 to +150 | °C |



CUT THE SPIKES WITH VCUT05E1-SD0

The VCUT05E1-SD0 is a Bidirectional and Symmetrical (BiSy) ESD protection device which clamps positive and negative overvoltage transients to ground. Connected between the signal or data line and the ground the VCUT05E1-SD0 offers a high isolation (low leakage current, low capacitance) within the specified working range. Due to the short leads and small package size of the tiny CLP0603 package the line inductance is very low, so that fast transients like and ESD strike can be clamped with minimal over- or undershoots.

| ELECTRICAL CHARACTERISTICS (T _{amb} = 25 °C, unless otherwise specified) | | | | | | |
|---|---|----------------------|------|------|------|-------|
| PARAMETER | TEST CONDITIONS/REMARKS | SYMBOL | MIN. | TYP. | MAX. | UNIT |
| Protection paths | Number of lines which can be protected | N _{channel} | - | - | 1 | lines |
| Reverse stand-off voltage | Max. reverse working voltage | V _{RWM} | - | - | 5.5 | V |
| Reverse voltage | at I _R = 0.1 μA | V _R | 5.5 | - | - | V |
| Reverse current | at V _{RWM} = 5.5 V | I _R | - | - | 0.1 | μA |
| Reverse breakdown voltage | at I _R = 1 mA | V _{BR} | 6.5 | 8 | 9 | V |
| Reverse clamping voltage | at I _{PP} = 1 A | V _C | - | 8.8 | 10 | V |
| | at I _{PP} = I _{PPM} = 6 A | V _C | - | 11 | 13 | V |
| Capacitance | at V _R = 0 V; f = 1 MHz | C _D | - | 13 | 14 | pF |
| | at V _R = 2.5 V; f = 1 MHz | C _D | - | 11 | - | pF |
| Clamping voltage | Transmission Line Pulse (TLP); t _p = 100 ns I _{TLP} = 8 A | V _{C-TLP} | - | 9.8 | - | V |
| Clamping voltage | Transmission Line Pulse (TLP); t _p = 100 ns I _{TLP} = 16 A | V _{C-TLP} | - | 11 | - | V |
| Dynamic resistance | Transmission Line Pulse (TLP); t _p = 100 ns | R _{DYN} | - | 0.15 | - | Ω |

TYPICAL CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

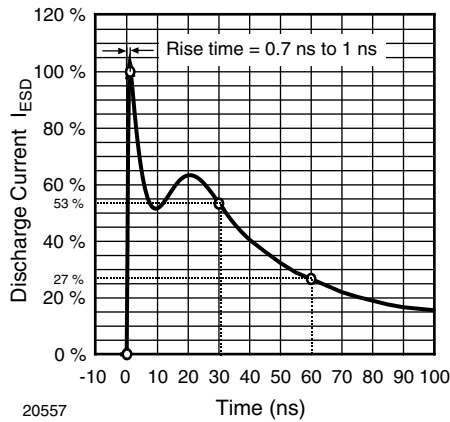


Fig. 1 - ESD Discharge Current Wave Form acc. IEC 61000-4-2 (330 Ω/150 pF)

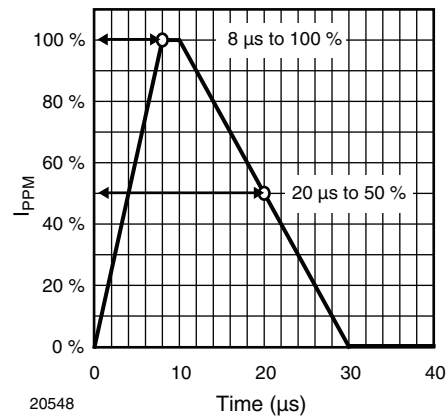


Fig. 2 - 8/20 μs Peak Pulse Current Wave Form acc. IEC 61000-4-5

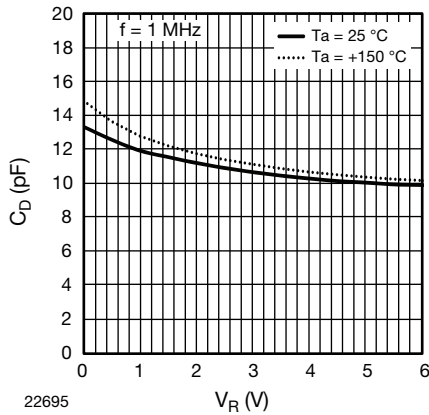


Fig. 3 - Typical Capacitance C_D vs. Reverse Voltage V_R

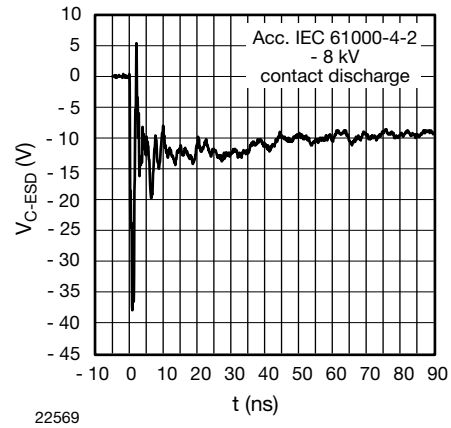


Fig. 6 - Typical Clamping Performance at 8 kV Contact Discharge acc. IEC 61000-4-2

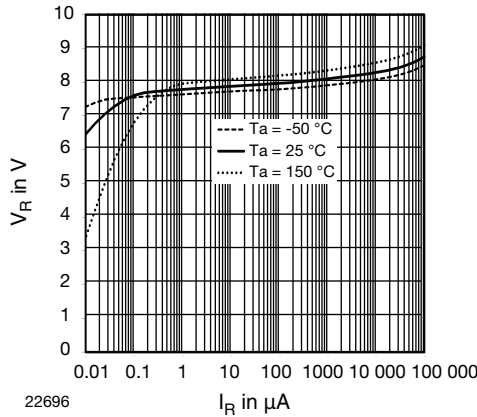


Fig. 4 - Typical Reverse Voltage V_R vs. Reverse Current I_R

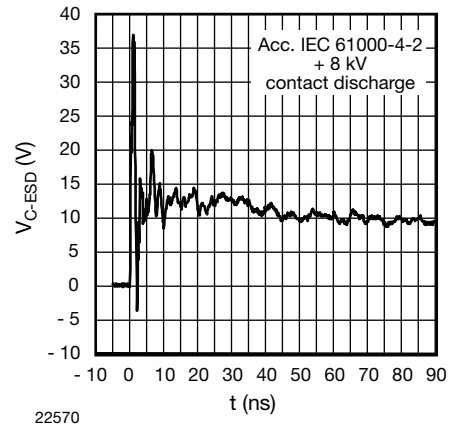


Fig. 7 - Typical Clamping Performance at 8 kV Contact Discharge acc. IEC 61000-4-2

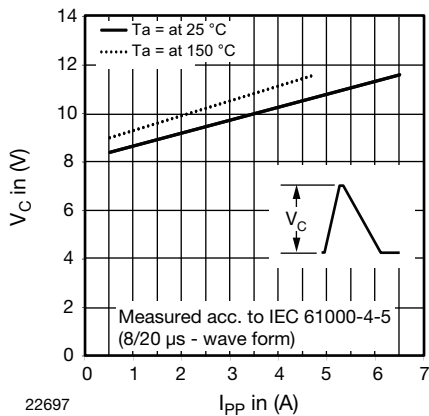


Fig. 5 - Typical Peak Clamping Voltage V_C vs. Peak Pulse Current I_{PP}

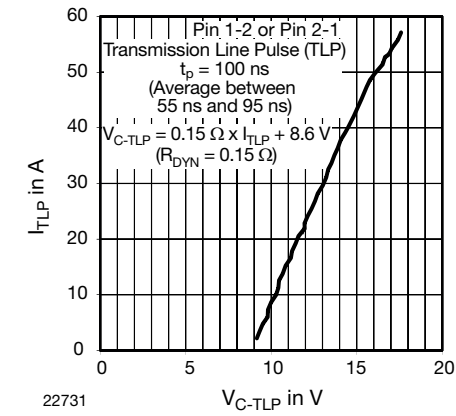
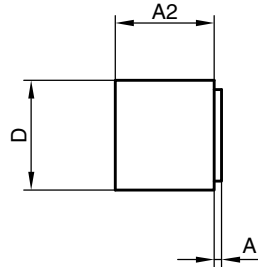
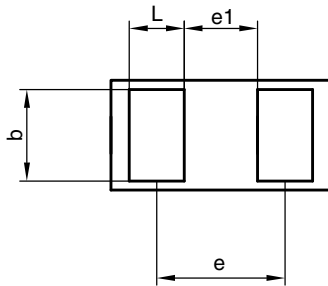


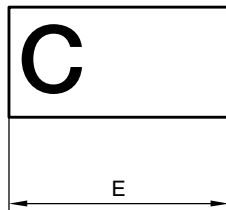
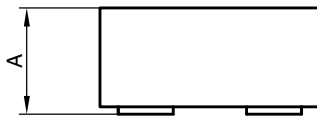
Fig. 8 - Typical Clamping Voltage at 100 ns Transmission Line Pulse (TLP)



PACKAGE DIMENSIONS in millimeters (mils): **CLP0603-2L**



Package = chip dimensions in mm [mils]



| | Millimeters | | | mils | | |
|----|-------------|------|------|-------|-------|-------|
| | min. | nom. | max. | min. | nom. | max. |
| A | 0.25 | 0.28 | 0.30 | 9.84 | 11.02 | 11.81 |
| A1 | 0.01 | 0.01 | 0.02 | 0.39 | 0.39 | 0.79 |
| A2 | 0.24 | 0.27 | 0.28 | 9.45 | 10.63 | 11.02 |
| b | 0.22 | 0.25 | 0.28 | 8.66 | 9.84 | 11.02 |
| D | 0.27 | 0.30 | 0.33 | 10.62 | 11.81 | 12.99 |
| E | 0.57 | 0.60 | 0.63 | 22.44 | 23.62 | 24.80 |
| e | | 0.40 | | | 15.75 | |
| e1 | | 0.25 | | | 9.84 | |
| L | 0.12 | 0.15 | 0.18 | 4.72 | 5.91 | 7.09 |

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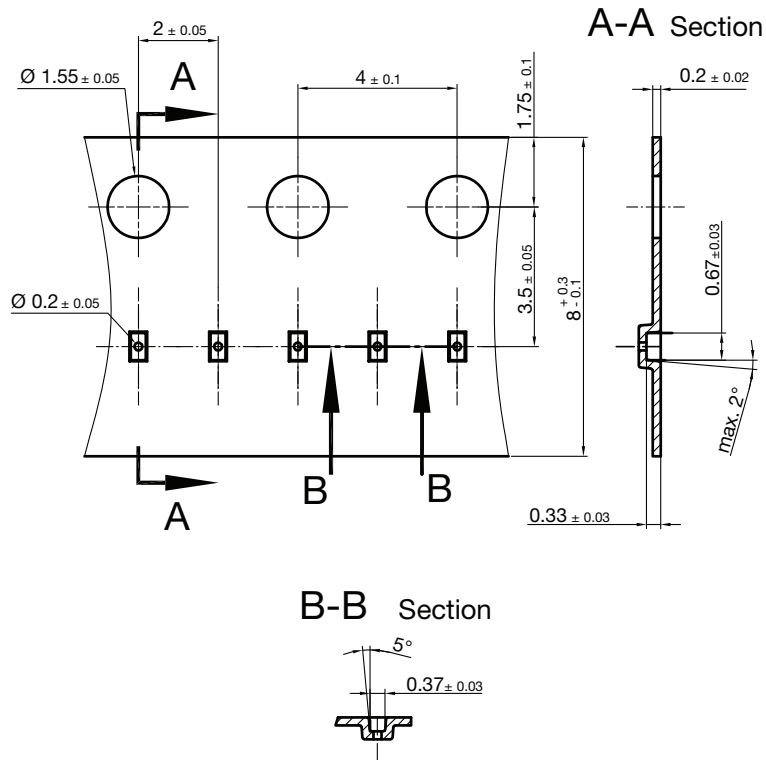
2 terminal leadless package (CLP)
Document no.: S8-V-3906.04-023 (4)
Created - Date: 22. Nov. 2010
Rev.8 - Date: 11. Nov. 2016

Footprint and soldering recommendation:

please see Application Note: www.vishay.com/doc?85917



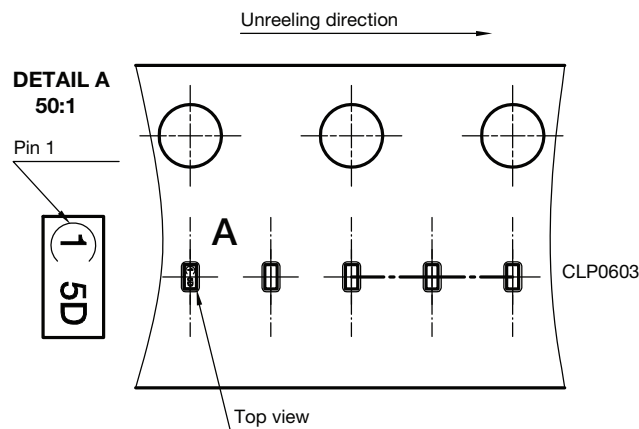
CARRIER TAPE in millimeters: **CLP0603-2L**



Cummulative tolerances of 10 sprocket holes is +/-0.2mm

22591
Document no. S8-V-3906.04-0025 (4)
Created - Date: 22. Nov. 2010

ORIENTATION IN CARRIER CLP0603-2L



Orientation in Carrier Tape (CLP0603)
S8-V-3906.04-026 (4)
22.10.2010
22936



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