



MLX83100 Automotive DC Pre-Driver

EVB83100 for Brushed DC Applications with MLX83100

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JULY 17, 2017

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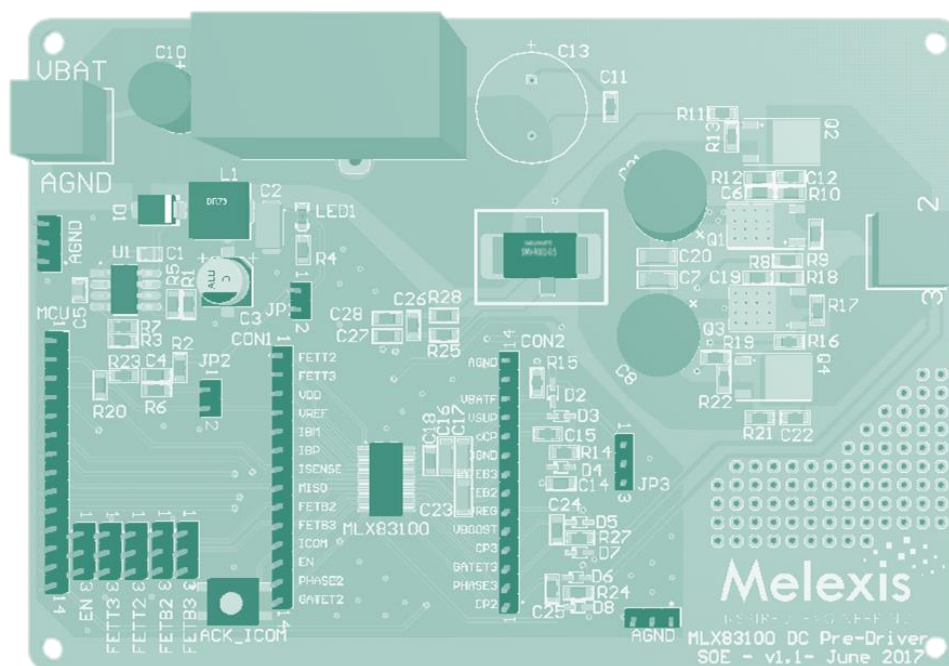
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1. Scope

This application note is to be used in combination with the pre-driver MLX83100 datasheet.

This application note describes the Melexis pre-driver evaluation board. It should help the user to make the system setup and get the motor running with the Melexis pre-driver to get familiar with all the features.

Further it describes all different sections: supply system, driver stage, current sensing, and auxiliary parts. The application note also gives some recommendations to customers who will be developing their own application board regarding to the schematic, components and layout.



2. Description

The MLX83100 is a full-bridge pre-driver (also called ‘bridge’ or ‘gate’ driver) IC with integrated current sense amplifier. This device is used to drive brushed DC motors in combination with a microcontroller and four discrete power N-FETs.

The evaluation board “EVB83100” described in this document allows customer to evaluate the pre-driver for applications in the typical range of 12V-30A. The absolute maximum operating voltage is limited by the external N-FETs to 40V, all auxiliary components on the board can also support 40V or higher. This means the evaluation board can be used to evaluate the pre-driver for 24V applications as well.

The pre-driver IC is supplied from the battery via a reverse polarity diode, whereas the half-bridges are supplied via a CLC-filter. Supply for the pre-drivers’ digital IO’s and current sense amplifier is realized by a linear regulator on the board. This VDD supply is routed to the microcontroller connector in order to supply the microcontroller from the same supply.

The device is able to control four external N-FETs in the supply range from 4.5V to 28V, by means of the integrated charge pump. The high side gate drivers are supplied via bootstrap circuits on the PCB. The trickle charge pump allows 100% PWM operation despite the use of bootstrap capacitors. The bootstrap voltage regulator is optimized for gate charges up to 500nC per FET at 20 kHz PWM.

The device comprises various monitoring and protection functions, including under voltage and over voltage detection at multiple internal voltage nodes, over temperature detection, drain-source and gate-source voltage monitoring of the external N-FETs and over current detection. The ICOM diagnostics interface is routed to the microcontroller connector to inform the microcontroller of any fault condition.

An integrated fast, high-bandwidth, low offset current sense amplifier measures and amplifies voltage sensed over the shunt resistor. Via a resistive divider from VDD a bias voltage is applied on the output of the current sense amplifier through VREF, allowing to measure negative currents as well.

The MLX83100 provides an EEPROM for configurability, avoiding the need for a high pin-count package and/or external components for configuration. The configuration allows the customer to optimize the pre-driver’s operation for different applications through the custom SPI interface with the microcontroller.

3. Application Setup – Start Guide

The MLX83100 is a full-bridge pre-driver (also called 'bridge' or 'gate' driver) IC used to drive brushed DC motors in combination with a microcontroller and 4 discrete power N-FETs in the supply range from 4.5V to 28V.

3.1. Supply Connection

The board power supply is connected to the battery connector VBAT at the top left corner.

Via jumper JP3 the charge pump mode can be selected. In position 1-2 the pre-driver will regulate the boosted voltage relative to VSUP, in position 2-3 the boosted voltage is regulated relative to GND.

A linear regulator provides the digital supply for the pre-driver and the microcontroller, when the pins of JP1 are shorted. In order to put the pre-driver in sleep mode the digital supply has to be disabled, by removing JP1.

3.2. Motor Connection

The brushed DC motor is connected via the MOTOR-connector on the right side of the board.

3.3. Microcontroller Connection

The evaluation board is delivered without microcontroller as the focus off Melexis is on the analog performance of the motor driver system, being the pre-driver, rather than on the motor control algorithm in software.

However the evaluation board does provide the option to connect the microcontroller via a dedicated pin header on the left of the board. This pin header provides the necessary supply voltages and all necessary signals to interface with the pre-driver and control the motor.

The evaluation board can also be used without microcontroller for brushed DC applications, via the jumpers on the bottom left corner.

- All errors on ICOM should be acknowledged by pressing the ACK_ICOM button
- The enable input EN should be pulled high to VDD (short JP_EN pins 1-2)
- For brushed DC applications it is necessary to control four external N-FETs
 - The 1st motor phase can be shorted to GND by pulling FETBx low (short pins 2-3) and FETTx low (short pins 2-3)
 - The 2nd motor phase should be a PWM-signal in for speed control. This can be done by applying the signal from a function generator on FETBy (pin 2) and pulling FETTy high (short pins 1-2), which will cause high-side and low-side N-FET to switch complementary.
- Diagnostics information is available on ICOM, current information on ISENSE



4. Functional Description

4.1. Supply System

The evaluation board is supplied via the battery connector VBAT-AGND. The pre-driver is supplied via pins VSUP and VDD. VSUP supplies the internal operation, whereas the VDD supply is used for the digital IO's and the current sense amplifier.

4.1.1. Power Supply V_{SUP}

V_{SUP} supplies the internal operation and charge pump. The charge pump guarantees functional operation even at low battery voltage. This charge pump needs to be configured with two external silicon diodes, a charge pump capacitor and a boost capacitor. See Figure 4-1 for more details.

The charge pump can regulate the boost voltage, V_{BOOST} , in two modes. The standard mode of operation is when the boost voltage is regulated to ground, in which case the boost capacitor is connected to ground. Alternatively the charge pump can regulate the boost voltage relative to the power supply. In this case the boost capacitor should be connected to the power supply. This mode is used to drive a high side reverse polarity Nfet. The mode of operation is determined by a bit in EEPROM and the boost capacitor connection can be changed with the position of jumper JP3.

The minimum charge pump capacitor is calculated from the supply voltage, the maximum load current and charge pump frequency as specified in the datasheet. In the standard application where 12V supply is used, this means the charge pump capacitor needs to be $>25nF$. On the evaluation board a 33nF capacitor is used.

If the charge pump is only configured with a 33nF capacitor, the charge pump will generate large current spikes, and will thus have bad EMC performance. Therefore a series resistance is added to slow down the switching of the charge pump. Based on the charge pump frequency and the 33nF capacitor, a 22 Ω resistor is selected. To further improve the EMC behaviour a 2.2uF capacitor is put in parallel with the 100nF minimum capacitance on V_{SUP} .

The boost capacitor should be at least an order of magnitude larger than the charge pump capacitor. A 1uF capacitor is selected after consideration of the number of charge pump cycles needed to recharge the boost voltage and the time between two charge pump events.

The pre-driver is protected against reverse polarity via diode D7 in Figure 4-1.

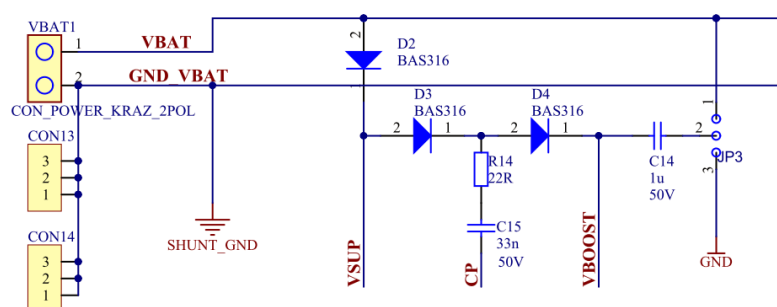


Figure 4-1 Power Supply V_{SUP}

4.1.2. Motor Supply V_{BRIDGE}

V_{BRIDGE} is used as supply for the external high side MOSFETs in the driver stage. This voltage is connected to V_{BATF} , to monitor drain-source voltages of the high side MOSFETs, via a 470 Ohm resistor to limit the negative input current in case of reverse polarity voltage.

A CLC filter is implemented to reduce the power supply noise. All capacitors are 50V rated for the case load dump can be applied.

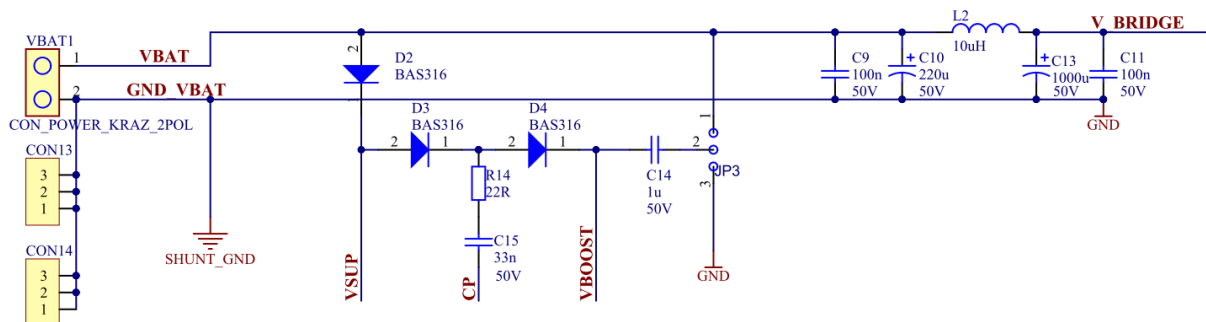


Figure 4-2 Motor Supply V_{BRIDGE}

4.1.3. Digital Supply V_{DD}^1

The pre-driver is supplied from V_{SUP} and V_{DD} . V_{DD} is used to supply the digital IO's and the current sense amplifier. To supply V_{DD} , a linear regulator is used, see Figure 4-3. By default the linear regulator is configured for 3.3V operation. By replacing resistor R3 from 22kOhm to 40kOhm the linear regulator will regulate 5V on the output.

This 3.3V or 5V is supplied to the pre-driver V_{DD} via jumper JP1. By removing jumper JP1, and pulling VDD to ground it is possible to put the pre-driver in sleep mode. Shorting jumper JP1 will wake the MLX83100.

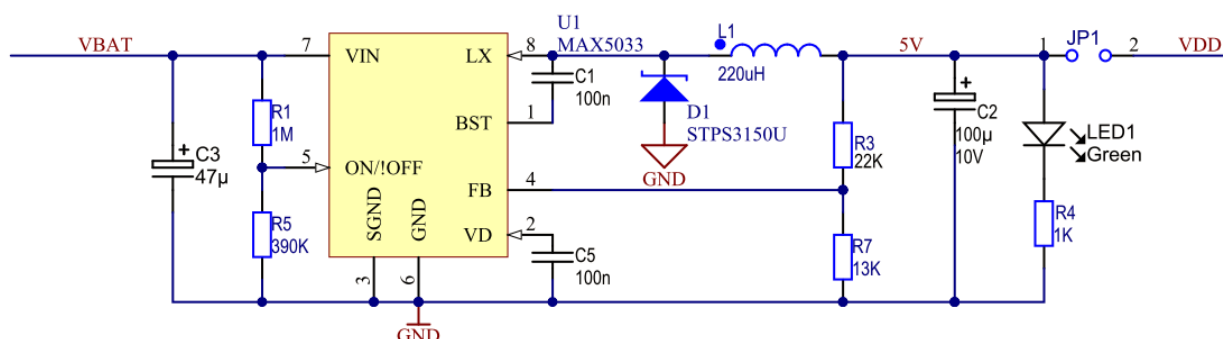


Figure 4-3 Digital Supply V_{DD}

¹ On EVB83100 v1 the linear regulator is not supplied from VBAT. An external V_{DD} is to be applied.

4.2. Pre-Driver

The MLX83100 in TSSOP28-EP package is soldered directly on the evaluation board.

Pin-headers next to the IC allow easy access to measure all the different signals of the pre-driver. For practical use the pin-header pins are labelled conform the pre-driver IC pin names.



Figure 4-4 MLX83100 Connection

4.3. 2x Half-Bridges

The evaluation board is designed for full-bridge control of brushed DC applications, thus 2 half bridges are present on the evaluation board. Each of the half bridges consists of a high side N-FET and a low side N-FET. Bootstrap circuits are used for driving the high side gates. To reduce the switching noise, decouple capacitors are present and footprint for snubber circuits are provided. See Figure 4-5 for the schematic of the driver stage.

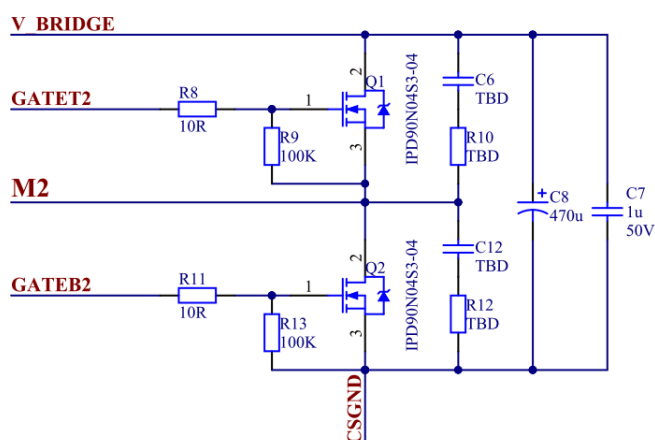


Figure 4-5 2x Half-bridges

The MOSFETs on the evaluation board are IPD90N04S3-04. These automotive N-FETs have a break down voltage of 40V, can conduct 90A and have a typical total gate charge of 80nC.

In order to control the slope of the output phases, external gate resistors are used for both high side and low side N-FET gates. These resistors decrease the switching speed and reduce the resulting voltage spikes. In case the standard EEPROM configuration is used, the dead time is set to 1μs. Based on the total gate charge of the MOSFETs the resistor values are set to 10Ω. To further reduce the switching noise decouple capacitors of 470μF//1μF are present and footprints are provided for snubber circuits.

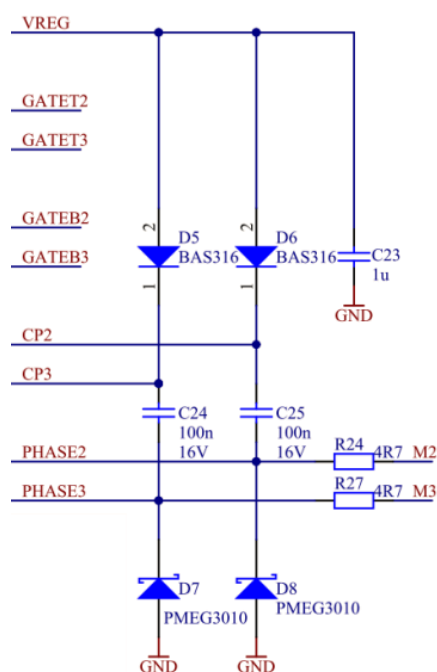
When the high side N-FET is switched on, the phase voltage is pulled high. The intrinsic Cgd and Cgs capacitors of the low-side N-FET create a capacitive voltage divider between the phase voltage and low side gate voltage. This can result in parasitic turn-on of the low side N-FET. In order to eliminate this effect, 100kΩ pull-down resistors are placed between gate and source of all low-side and high-side N-FETs.

4.4. Bootstrap Circuit

4.4.1. Voltage Regulator

The pre-driver has an integrated 12V voltage regulator. The V_{REG} output is used for the bootstrap circuits and can supply currents $< 40\text{mA}$.

4.4.2. Bootstrap Circuit



In order to switch on the high side N-FETs it is necessary to pull the gate voltage $\sim 12\text{V}$ above the phase voltage. This means the gate voltage should be pulled $\sim 12\text{V}$ above battery level. Therefore external bootstrap circuits are used, see Figure 4-6.

The overdrive gate voltage for the high side N-FET is provided by the bootstrap capacitor. This capacitor is charged by the V_{REG} voltage through the bootstrap diode during the time when the device is off (assuming that the source of the N-FET swings to ground during that off-time). The bootstrap capacitor is discharged only when the high side gate is switched on.

If the bootstrap capacitor is too high, charging of the capacitor will limit the PWM frequency and duty cycle. If the capacitance is too low, there can be a large voltage drop at the time the charge is transferred from the bootstrap capacitor to the N-FET gate.

The value of the bootstrap capacitor is chosen to be 100nF , such that it is one order of magnitude larger than the N-FET gate capacitance. The V_{REG} tank capacitor in turn is one order of magnitude bigger than the bootstrap capacitor and is thus set to $2.2\mu\text{F}$.

Figure 4-6 Bootstrap Circuits

Due to the motor inductance and the diode reverse recovery effect, it is possible that the phase voltages are pulled below ground. To protect the pre-driver IC against negative voltages on the phase pins, diodes and phase resistors are used to clamp the negative voltages, see Figure 4-6.

4.5. Current Sense Amplifier

The pre-driver has an integrated current sense amplifier. The current sense amplifier is supplied from the digital supply V_{DD} . It senses the voltage over the low-side shunt via input pins IBP-IBM, amplifies it with the gain programmed in EEPROM and adds the offset provided on V_{REF} . The output of the amplifier is available on ISENSE.

A single, common shunt of 2 m Ω is used. The positive and negative signals of the shunt are filtered via 10 Ω series resistors and 10nF capacitors, complemented with an additional 22nF differential capacitor.

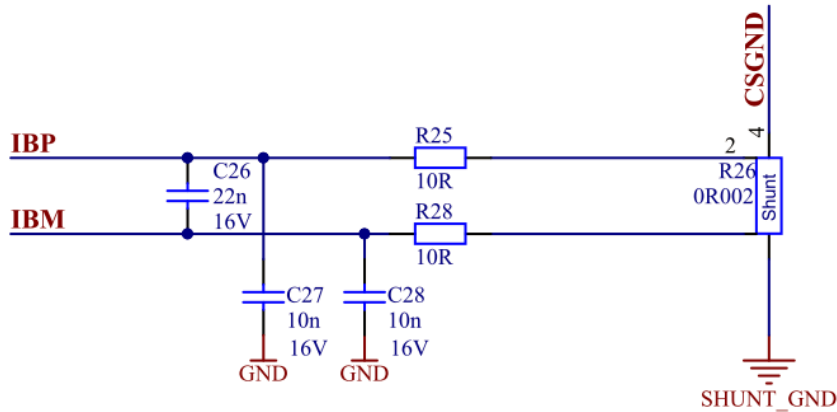


Figure 4-7. Current Sense Input Filter

An offset voltage V_{REF} can be applied on the current sense output via a resistive divider available on jumper JP2.

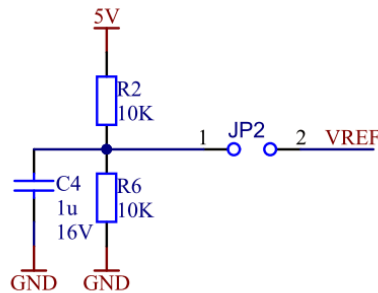


Figure 4-8. Current Sense Output Bias Voltage

4.6. Microcontroller Connection

The pre-driver is controlled by a microcontroller (not provided with the evaluation board). A pin-header is provided on the evaluation board to connect a microcontroller.

All necessary pins to control the pre-driver/motor are routed to this microcontroller connector:

- Microcontroller supply
 - **VSUP-GND:** Power supply and ground
 - **VDD-GND:** Digital supply and ground from the linear regulator
- Control of the pre-driver/motor
 - **EN:** pre-driver input to enable/disable the gate driver outputs
 - **ICOM:** bidirectional, serial interface for diagnostics communication and used as CS for the custom SPI interface to read/program pre-drivers' EEPROM
 - **FETT_x:** pre-driver input signals to control the high-side N-FETs
 - **FETB_x:** pre-driver input signals to control the low-side N-FETs and used for the custom SPI interface to read/program the pre-drivers' EEPROM
- Motor control
 - **ISENSE_s-GND:** output of the current sense amplifier, after a resistive divider to scale the voltage in case of a lower voltage ADC input in the external MCU

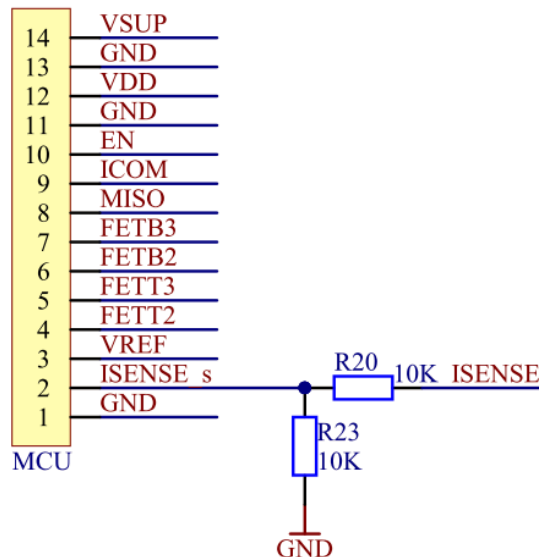


Figure 4-9 Microcontroller Connection

5. General Guidelines for Components Placement

- For reliable operation both AGND-DGND should be shorted as close as possible to the pre-driver IC.
- All supply decouple capacitors are to be placed as close as possible to the IC.
- All current sense filter components are to be placed as close as possible to the IC.
- All bootstrap components are to be placed as close as possible to the IC.
- The VBATF series resistor is to be placed next to the IC.
- Each of the 2 bulk and ceramic capacitors are to be placed close to the corresponding half-bridge.
- The components within one half bridge should be placed as close as possible to each other. High side MOSFET, low side MOSFET, bulk capacitor CB and ceramic capacitor CC (CB and CC are in parallel) and the shunt resistor form a loop that should be as small and tight as possible. The traces should be short and wide.

6. General Layout Recommendations

- Divide the PCB in two parts. One part for the low power traces and components, the other part for the high power circuits. Place all half bridges and related components on the high power side. The pre-driver IC, and all components related to it, should be placed on the low power side.
- Consider a star point for the ground and the supply, to guarantee that the high currents will never flow through or across the low power side.
- Apply a ground plane. Especially on the bottom layer below the pre-driver IC, the MCU and all paths in between.
- Short the AGND and DGND pre-driver IC pins together, close to the IC.
- Connect the exposed pad to the ground plane.
- All connections between the pre-driver and the half bridges should be as short as possible and symmetrical. Use the same trace width and aim for equal trace lengths for all these nets. These rules also apply for the IBP and IBM paths.
- For the best performance the PCB needs to be optimized. The focus should be on design quality rather than flexibility. This means any optional components/features should be avoided if they are not required.

Note:

The EVB83100 should not be considered as an overall reference layout. The focus of this board is on flexibility in order to allow the user the opportunity to use all functionalities and to get familiar with the Melexis pre-driver.

7. Revision History

Revision	Date	Description
1.0	14-07-17	First release
1.1	04-12-17	3.3 Microcontroller Connection updated

Table 7-1 Revision history

8. Disclaimer

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