MIC4600

28V Half Bridge MOSFET Driver

Revision 1.0

General Description

The Micrel MIC4600 is a 28V half bridge MOSFET driver targeted for cost sensitive applications requiring high performance such as set-top boxes, gateways, routers, computing peripherals, telecom and networking equipment.

The MIC4600 operates over a supply range of 4.5V to 28V. It has an internal linear regulator which provides a regulated 5V to power the MOSFET gate drive and operates up to 1.5MHz switching frequency.

The MIC4600 uses an adjustable dead time circuit to prevent shoot-through in the external high and low-side MOSFETs.

The MIC4600 is available in a small 3mm × 3mm QFN package with a junction temperature range of –40°C to 125°C

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

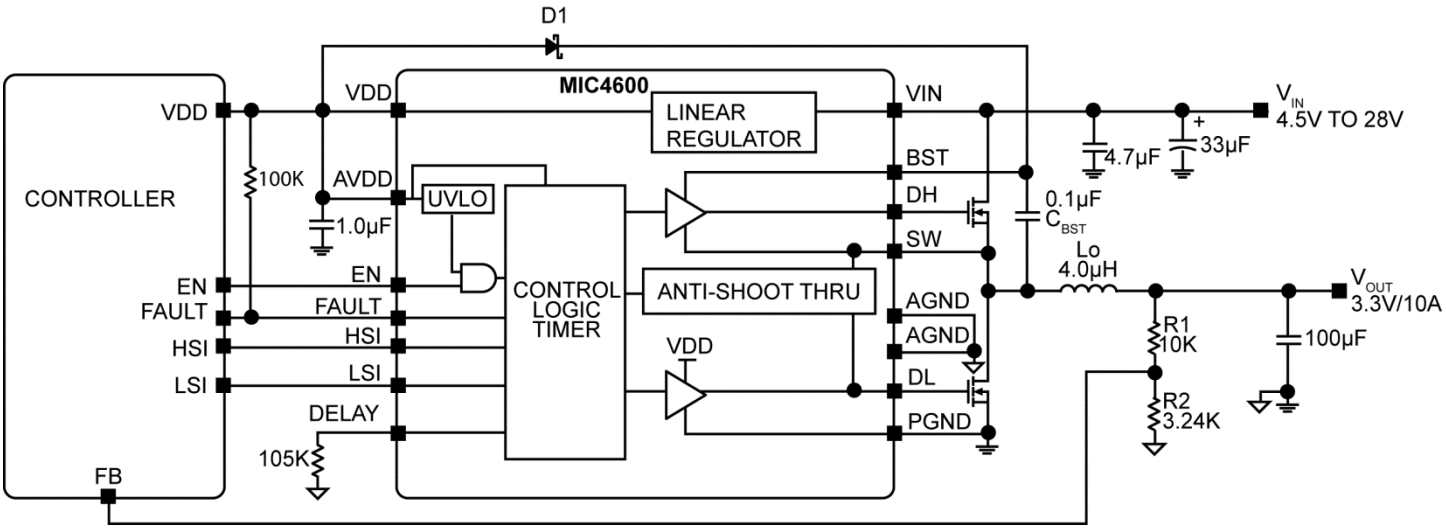
Features

- Adjustable dead time circuitry
- Anti-shoot-through protection
- Internal LDO for Single Supply Operation
- Input voltage range: 4.5V to 28V
- Fast propagation delay – 20ns
- Up to 1.5 MHz operation
- Low voltage logic level inputs for µC or FPGA driven power solutions
- Independent inputs for low and high side drivers
- 2Ω gate drive capable of driving 3000pF load with 15ns rise and fall times
- Low 450uA typical quiescent current
- 3mm × 3mm QFN package
- –40°C to +125°C junction temperature range

Applications

- Distributed power systems
- Communications/networking infrastructure
- Set-top box, gateways and routers
- Printers and scanners
- µP and FPGA controlled DC-DC regulator

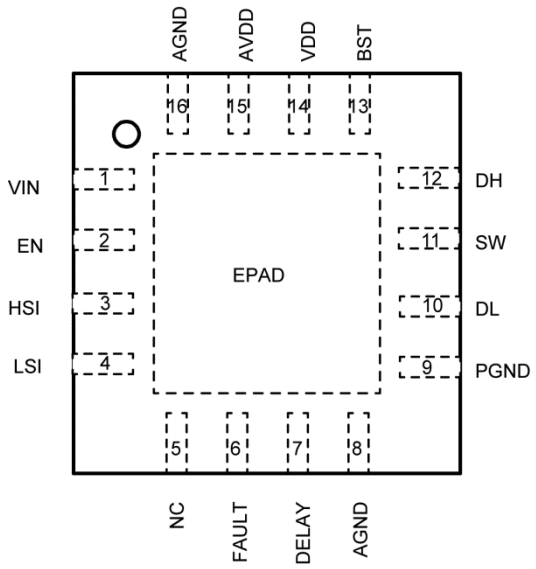
Typical Application



Ordering Information

Part Number	Junction Temp. Range	Package	Lead Finish
MIC4600YML	–40°C to +125°C	16 lead 3mm × 3mm QFN	Pb-Free

Pin Configuration



16-lead 3mm × 3mm QFN (ML)
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	VIN	VIN Supply (Input): Input supply to the internal LDO. The VIN operating voltage range is from 4.5V to 28V. Connect a decoupling capacitor between this pin and PGND.
2	EN	Enable (Input): A logic level high allows normal operation. A logic level low on this pin shuts down the drive in a low quiescent current state. The EN pin must not be left floating.
3	HSI	High side input (input): A logic level input that controls the high side gate drive.
4	LSI	Low side input (input): A logic level input that controls the low side gate drive.
5	NC	No Connect. Not internally connected.
6	FAULT	FAULT (Output). The active low, open drain output pulls low during an over-temperature fault. A resistor to VDD is needed to pull this signal high.
7	DELAY	Delay (Output). Connect a resistor from this pin to ground to adjust the dead time (break before make) .
8, 16	AGND	Analog ground. AGND must be connected directly to the ground planes. Do not route the AGND pin to the PGND Pad on the top layer. Refer to the PCB layout guidelines for details.
9	PGND	Power Ground. PGND is the ground path for the MIC4600 output drivers. The PGND pin should be connected to the source of low-side N-Channel MOSFET and the negative terminals of decoupling capacitors.
10	DL	Drive Low (Output). Low side MOSFET gate driver.
11	SW	Switch Node (Output): Internal connection for the high-side MOSFET source and low-side MOSFET drain. Due to the high speed switching on this pin, the SW pin should be routed away from sensitive nodes.

Pin Description (Continued)

Pin Number	Pin Name	Pin Function
12	DH	Drive High (Output). High side MOSFET gate driver.
13	BST	Boost (output): Bootstrapped voltage to the high-side N-channel MOSFET driver. Connect a Schottky diode between the VDD pin and the BST pin. Connect a boost capacitor between the BST pin and the SW pin.
14	VDD	5V Internal Linear Regulator (Output): VDD supplies the power MOSFET gate drive supply voltage. VDD is created by internal LDO from VIN. When VIN < +5.5V, VDD should be tied to VIN pin. A 2.2µF ceramic capacitor from the VDD pin to ground plane on PCB is required for stability.
15	AVDD	5V Analog Input (Input): AVDD is the supply for the internal driver logic and control circuitry. Connect the VDD output to the AVDD pin.
EPAD	EPAD	Exposed thermal pad. Connect to the ground plane for optimum thermal performance.

Absolute Maximum Ratings[1]

V_{IN} to PGND ..... -0.3V to +29V
V_{DD} to PGND ..... -0.3V to +6V
V_{SW} to PGND ..... -0.3V to (V_{IN} +0.3V)
V_{BST} to V_{SW} ..... -0.3V to 6V
V_{BST} to PGND ..... -0.3V to 34V
V_{HSI}, V_{LSI} to PGND ..... -0.3V to (V_{DD} + 0.3V)
V_{FAULT} to AGND ..... -0.3V to 6V
V_{EN} to PGND ..... -0.3V to (V_{IN} +0.3V)
PGND to AGND ..... -0.3V to +0.3V
Junction Temperature ..... +150°C
Storage Temperature (T_S) ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... 260°C
ESD Ratings
HBM 2kV
MM 200V

Operating Ratings[2]

Supply Voltage (V_{IN}) ..... 4.5V to 28V
VDD Supply Voltage (V_{DD}) ..... 4.5V to 5.5V
Enable Input (V_{EN}) ..... 0V to V_{IN}
Junction Temperature (T_J) ..... -40°C to +125°C
Maximum Power Dissipation ..... Note 4
Package Thermal Resistance[3]
3mm × 3mm QFN (θ_{JA}) ..... 59°C/W

Electrical Characteristics[4]

V_{IN} = V_{EN} = 12V, V_{BST} – V_{SW} = 5V; T_A = 25°C, C_{VIN}=C_{VDD}= 1µF unless noted. **Bold** values indicate -40°C ≤ T_J ≤ +125°C.

Parameter	Condition	Min.	Typ.	Max.	Units
Power Supply Input					
Input Voltage Range (V_{IN})		**4.5**		**28**	V
Quiescent Supply Current	HSI=V_{DD}, LSI=0V, R_{DELAY}=124kΩ, non-switching		450	**750**	µA
Shutdown Supply Current	V_{EN} = 0V		9	**20**	µA
V_{DD} Supply Voltage					
V_{DD} Output Voltage	V_{IN} = 7V to 26V, I_{DD} = 25mA	**4.8**	5	**5.4**	V
V_{DD} UVLO Threshold	V_{DD} Rising	**3.6**	4.2	**4.3**	V
V_{DD} UVLO Hysteresis			400		mV
Dropout Voltage (V_{IN} – V_{DD})	I_{DD} = 25mA, V_{IN}= 5V		380		mV
V_{DD} load regulation	I_{DD} = 0 to 25mA		1.23		%
Enable Control					
EN Logic Threshold	Rising	**0.65**	1.25	**1.4**	V
EN Hysteresis			69		mV
EN Input Bias Current	V_{EN} = 12V			**2**	µA

Notes:

1. Exceeding the absolute maximum ratings may damage the device.
2. The device is not guaranteed to function outside its operating ratings.
3. $PD_{(MAX)}$ = ($T_{J(MAX)}$ – T_A)/ θ_{JA}, where θ_{JA} depends upon the printed circuit layout. See “Applications Information.”
4. Specification for packaged product only.

Electrical Characteristics[4] (Continued)

Fault					
Fault Over temperature	T_J Rising		150		°C
Over Temperature Hysteresis			23		°C
FAULT Logic Level Low	I_{FAULT}=5mA		0.05	**0.2**	V
FAULT pin leakage current	V_{FAULT}=5.5V		0.01	**0.1**	µA
Input Control					
HSI Logic Level High		**1.4**			V
HSI Logic Level Low				**0.65**	V
HSI Bias Current	V_{HSI} = 5V		0.01	**0.1**	µA
LSI Logic Level High		**1.4**			V
LSI Logic Level Low				**0.65**	V
LSI Bias Current	V_{LSI} = 5V		0.01	**0.1**	µA
Timing					
Dead Time	R_{DELAY}=105kΩ		18.7		ns
Switching Frequency Range				**1.5**	MHz
Minimum Allowable Pulse Width			32		ns
Rise Time (DH, DL)	C_{LOAD}=3nF, 10%V_{DD} to 90%V_{DD}		15		ns
Fall Time (DH,DL)	C_{LOAD}=3nF, 90%V_{DD} to 10%V_{DD}		13.5		ns
Propagation Delay, Rising HSI to DH	GND to 10%xV_{DD}		26		ns
Propagation Delay, Rising LSI to DL	GND to 10%xV_{DD}		18		ns
Propagation Delay, Falling HSI to DH	V_{DD} to 90%xV_{DD}		55		ns
Propagation Delay, Falling LSI to DL	V_{DD} to 90%xV_{DD}		14		ns
MOSFET Drivers					
DH $R_{DS(ON)}$, High	I_{DH} = 20mA		2	**3**	Ω
DH $R_{DS(ON)}$, Low	I_{DH} = -20mA		1.5	**3**	Ω
DL $R_{DS(ON)}$, High	I_{DL} = 20mA		2	**3**	Ω
DL $R_{DS(ON)}$, Low	I_{DL} = -20mA		1	**2**	Ω

Timing Diagrams

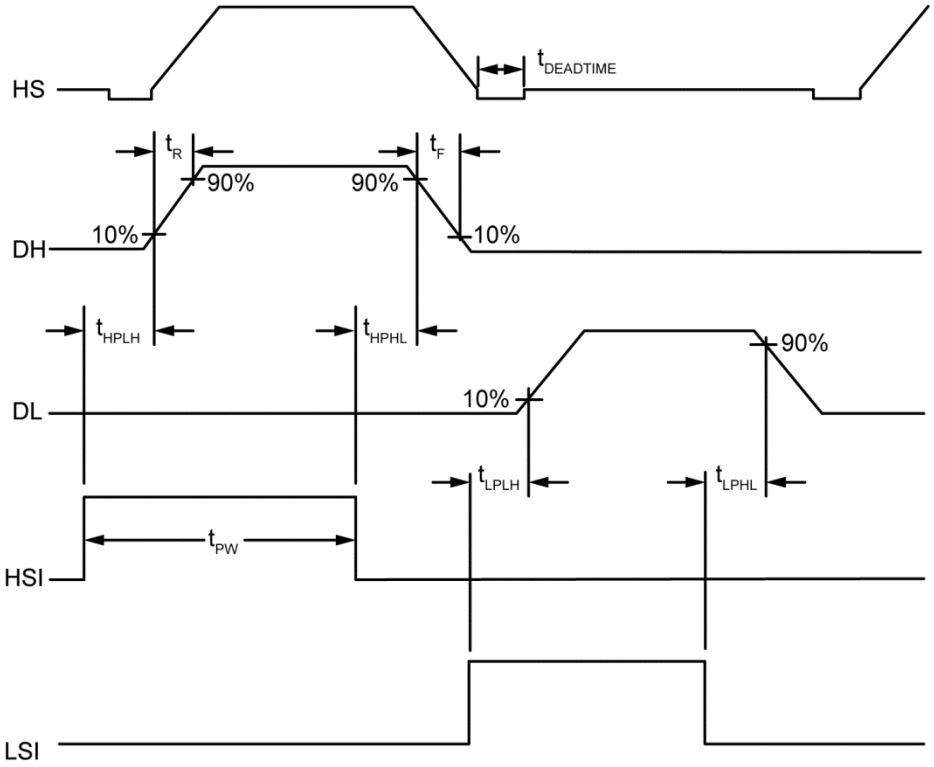
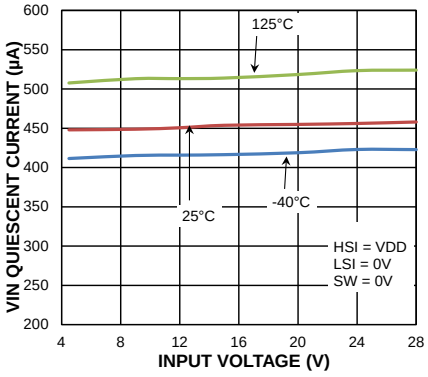


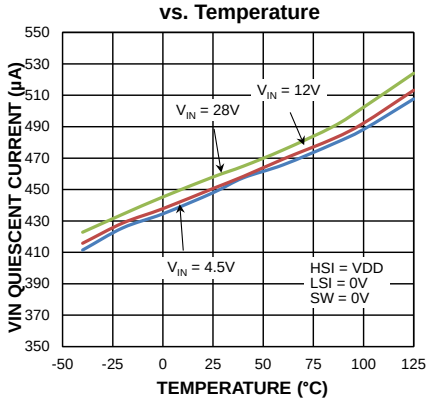
Figure 1. MIC4600 Timing Waveforms

Typical Characteristics (V_{IN}=12V unless noted)

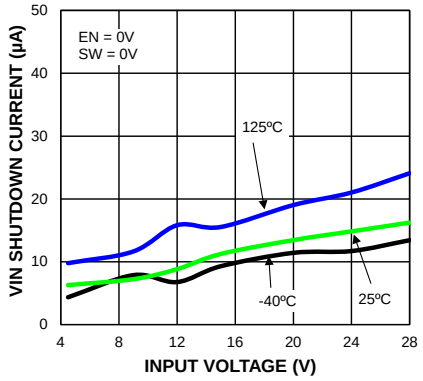
VIN Quiescent Current vs. Input Voltage



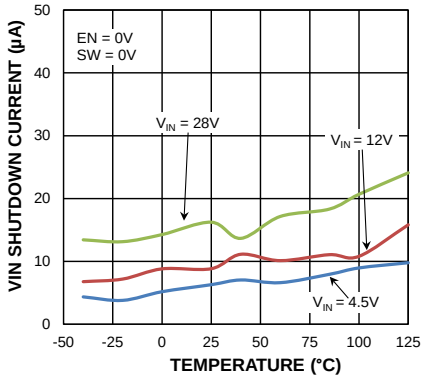
VIN Quiescent Current vs. Temperature



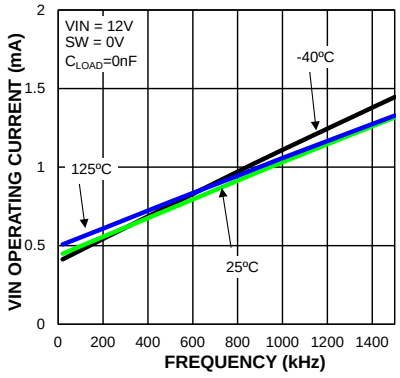
VIN Shutdown Current vs. Input Voltage



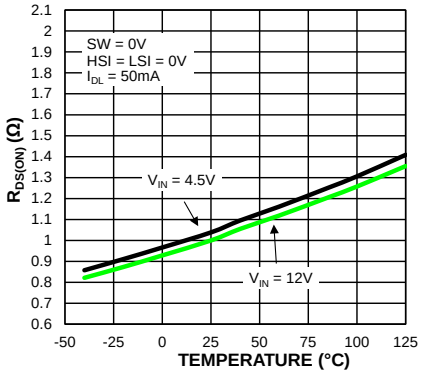
VIN Shutdown Current vs. Temperature



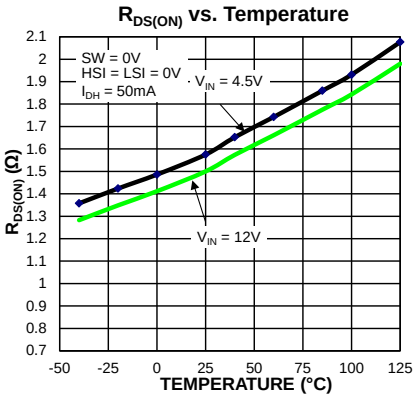
VIN Operating Current vs. Frequency



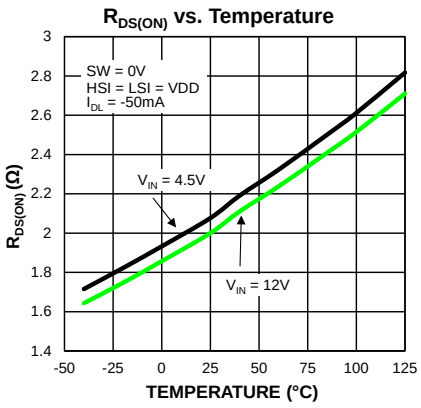
$R_{DS(ON)}$ vs. Temperature



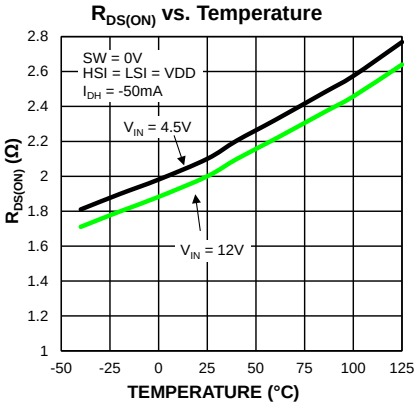
$R_{DS(ON)}$ vs. Temperature



$R_{DS(ON)}$ vs. Temperature

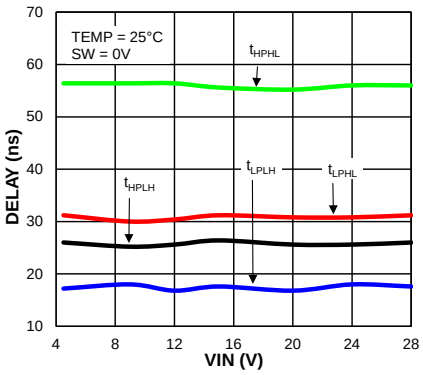


$R_{DS(ON)}$ vs. Temperature

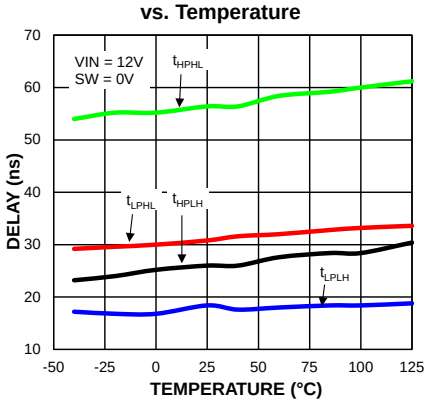


Typical Characteristics (Continued)

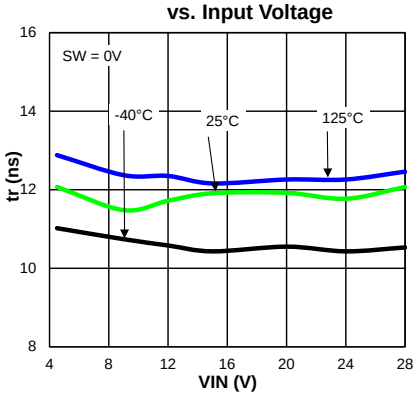
Propagation Delay vs. Input Voltage



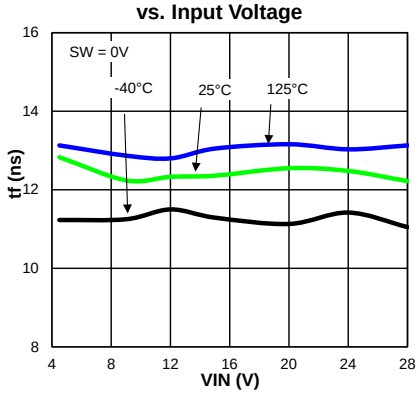
Propagation Delay vs. Temperature



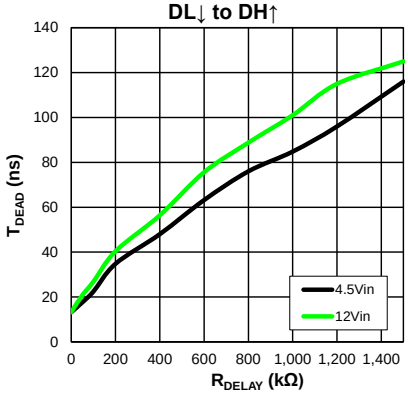
DH Rise Time vs. Input Voltage



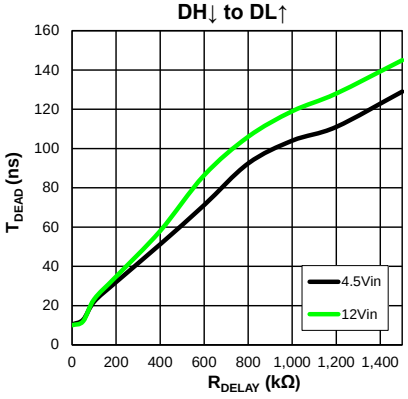
DH Fall Time vs. Input Voltage



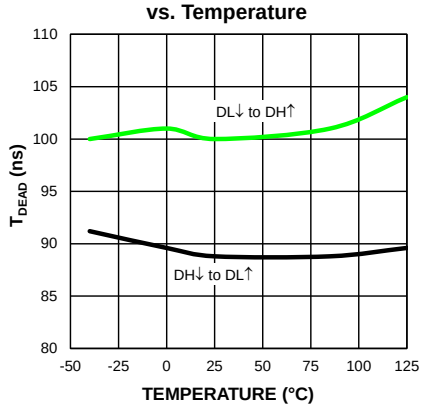
Deadtime vs. R_{DELAY} for DL↓ to DH↑



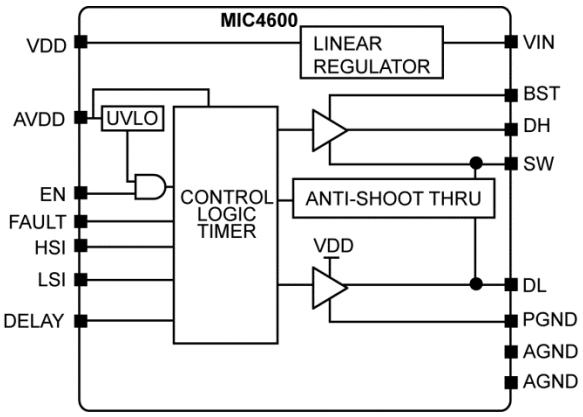
Deadtime vs. R_{DELAY} for DH↓ to DL↑



Deadtime Delay vs. Temperature



Functional Diagram



Functional Description

The MIC4600 is a 28V half-bridge MOSFET driver with integrated LDO. It is designed to independently drive both high-side and low-side N-Channel MOSFETs. The LDO eliminates the need for a second VDD supply voltage by generating the gate drive voltage from the input supply. The MIC4600 offers a wide 4.5V to 28V operating supply range. Refer to the MIC4600 Block Diagram above.

The high and low-side drivers contain an input buffer with hysteresis and an output buffer. The high-side output buffer includes a high-speed level-shifting circuit that is referenced to the HS pin. An external diode is used to supply V_{DD} to the bootstrap circuit that provides the drive voltage for the high-side output.

Startup and UVLO

The UVLO circuit monitors V_{DD} and inhibits both drivers in a low state when the supply voltage is below the UVLO threshold. Hysteresis in the UVLO circuit prevents noise and circuit impedance from causing chatter during turn-on.

Enable Input

A logic high on the enable pin (EN) allows normal operation to occur. Conversely, when a logic low is applied on the enable pin, the high and low-side driver outputs turn-off and the driver enters a low supply current shutdown mode. Do not leave floaing.

Dead-Time Delay

Shoot-through occurs in a half-bridge or synchronous buck topology when both the high and low side MOSFETs conduct at the same time. This condition is caused by driver propagation delay variation and MOSFET turn on/off times. Shoot-through causes an increase in MOSFET power dissipation, circuit noise and interference with power circuit operation. A resistor on the DELAY pin sets the break-before-make delay time between the high and low-side MOSFETs . See the Applications section for additional information.

Input Stage

Both the HSI and LSI pins are referenced to the AGND pin. The voltage state of the input signal does not change the quiescent current draw of the driver.

The MIC4600 has a TTL-compatible input range and can be used with input signals with amplitude less than or equal to the V_{DD} voltage. A small amount of hysteresis improves the noise immunity of the driver inputs.

Low-Side Driver

Figure 2 shows a block diagram of the low-side driver. The low-side driver is designed to drive a ground (PGND pin) referenced N-channel MOSFET. The low-side gate drive voltage equals V_{DD}, which is typically 5V.

A low driver impedance allows the external MOSFET to be turned on and off quickly. The rail-to-rail drive capability of the output ensures a low R_{DSON} from the external MOSFET.

A high level applied to LSI pin causes the upper driver MOSFET to turn on and VDD voltage is applied to the gate of the external MOSFET. A low level on the LSI pin turns off the upper driver and turns on the low side driver to ground the gate of the external MOSFET.

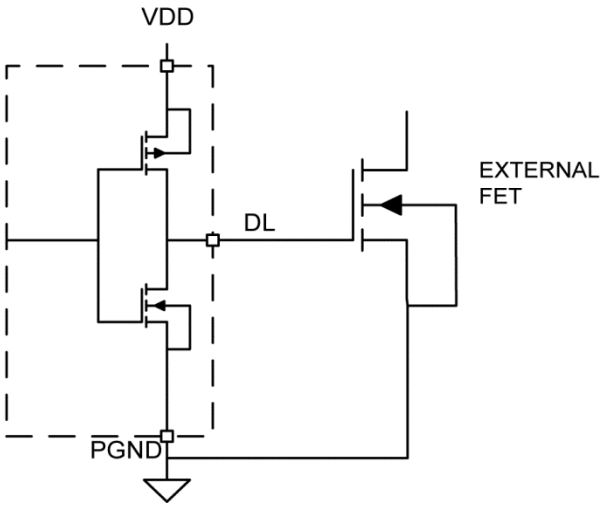


Figure 2. Low-Side Driver Circuit

High-Side Driver and Bootstrap Circuit

A block diagram of the high-side driver and bootstrap circuit is shown in Figure 3. This driver is designed to drive a floating N-channel MOSFET, whose source terminal is referenced to the SW pin. The output voltage of the DH pin equals VDD minus the external bootstrap diode forward voltage drop. The high-side gate drive voltage is typically 4.5V.

A low-power, high-speed, level-shifting circuit isolates the low side (AGND pin) referenced circuitry from the high-side (SW pin) referenced driver. Power to the high-side driver is supplied by the bootstrap circuit.

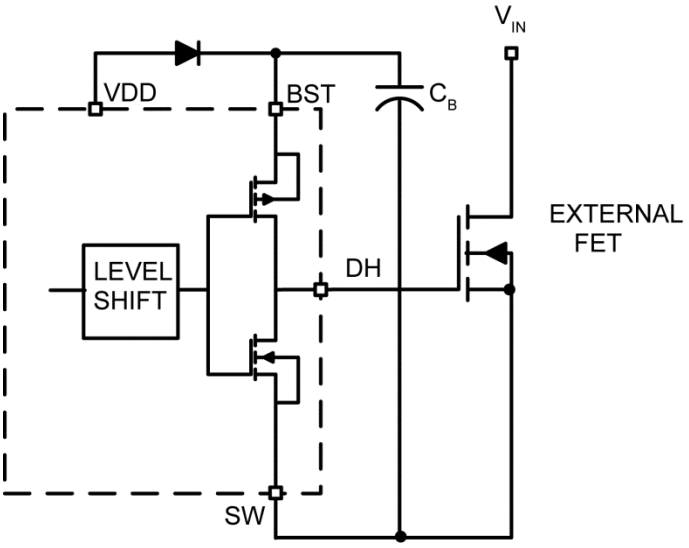


Figure 3. High-Side Driver and Bootstrap Circuit

The bootstrap circuit consists of an external diode and external capacitor, C_B. In a typical application, such as the synchronous buck converter shown in Figure 4, the SW pin is at ground potential while the low-side MOSFET is on. During this time, the diode allows capacitor C_B to charge up to V_{DD}-V_F (where V_F is the forward voltage drop of the diode). After the low-side MOSFET is turned off and the DH pin goes high, the voltage across capacitor C_B is applied to the gate of the upper external MOSFET. As the upper MOSFET turns on, voltage on the SW pin rises with the source of the high-side MOSFET until it reaches V_{IN}. As the SW and BST pins rise, the diode is reverse biased preventing capacitor C_B from discharging.

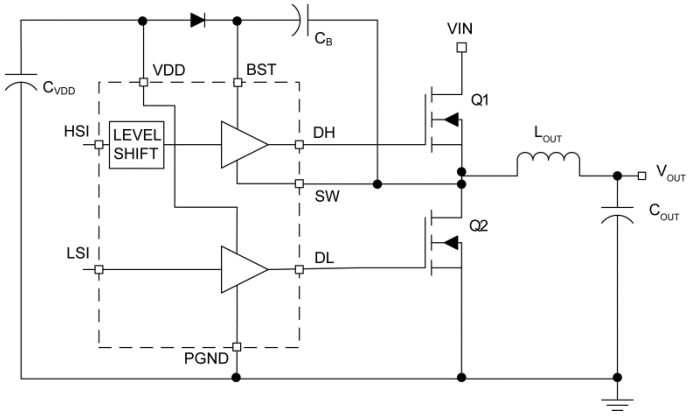


Figure 4. MIC4600 Driving a Synchronous Buck Converter

Thermal Shutdown

Thermal shutdown protects the driver from damage due to excessive die temperature. If the die exceeds the high temperature threshold, the output drive is inhibited and the FAULT pin is asserted low. The driver automatically resumes operation, and the FAULT pin is de-asserted, when the die temperature cools below the lower threshold, set by the circuit's hysteresis. If resumed operation results in reheating of the die above the high threshold, another shutdown cycle occurs. The switch continues thermal cycling until the condition has been resolved.

Fault Pin

The FAULT signal is an N-channel open drain output, which is asserted low when the MIC4600 enters thermal shutdown.

Application Information

Adjustable Dead Time

Dead-time control prevents shoot-through current from flowing through the external power MOSFETs during switching transitions. The delay allows enough time for the high-side driver to turn off before the low-side driver turns on. It also prevents the high-side driver from turning on before the low-side driver has turned off.

The dead-time between the high and low-side MOSFETs can be adjusted with a resistor on the DELAY pin. The dead-time can be approximated with the formula below. See the Typical Characteristic graphs for a more precise determination of R_{DELAY} vs. T_{DEAD}.

$$T_{DEAD} = 12 \times 10^{-9} + R_{DELAY} \times 0.9 \times 10^{-10} \quad \textbf{Eq. 1}$$

Where:

T_{DEAD} is the break-before-make delay between the high-side and low-side gate drive signals

R_{DELAY} is the DELAY pin resistance in kΩ.

Other Timing Considerations

Make sure the input signal pulse width is greater than the minimum specified pulse width. An input signal that is less than the minimum pulse width may result in no output pulse or an output pulse whose width is significantly less than the input.

The maximum duty cycle (ratio of high side on-time to switching period) is controlled by the minimum pulse width of the low side and by the time required for the C_B capacitor to charge during the off-time. Adequate time must be allowed for the C_B capacitor to charge up before the high-side driver is turned on.

Single Input Operation

Both outputs can be controlled from a single input signal by pulling the LSI input high to VDD and applying the input signal to the HSI pin. In this configuration, the dead-time between the DH and DL transitions is set by the resistor value connected to the DELAY pin.

When the HSI pin goes from a low to a high, the DL pin goes low and the DH pin goes high after the dead time delay. When the HSI pin changes from a high to a low, the DH pin goes lowAfter the delay time, the DL pin goes high.

Bootstrap Diode and Capacitor

The gate drive voltage of the high-side driver equals the V_{DD} voltage minus the voltage drop across the bootstrap diode. A Schottky diode is recommended due to the lower forward voltage drop.

Power dissipation in the bootstrap diode can be calculated using the following equations. The average current drawn by repeated charging of the high-side MOSFET is calculated by:

$$I_{F(AVE)} = Q_{gate} \times f_S \quad \textbf{Eq. 2}$$

where;
Q_{gate} = total gate charge at V_{DD}
f_s = gate drive switching frequency

The average power dissipated by the forward voltage drop of the diode equals:

$$Pdiode_{fwd} = I_{F(AVE)} \times V_F \quad \textbf{Eq. 3}$$

where; V_F = diode forward voltage drop

The value of V_F should be taken at the peak current through the diode; however, this current is difficult to calculate because of differences in source impedances. The peak current can either be measured or the value of V_F at the average current can be used, which will yield a good approximation of diode power dissipation.

The voltage on the bootstrap capacitor drops each time it delivers charge to turn on the MOSFET. The voltage drop depends on the gate charge required by the MOSFET. Most MOSFET specifications specify gate charge versus V_{GS} voltage. Based on this information and a suggested capacitor voltage drop of less than 0.1V, the minimum value of bootstrap capacitance is:

$$C_B \geq \frac{Q_{GATE}}{\Delta V_{BST}} \quad \textbf{Eq. 4}$$

Where:

Q_{GATE} = Total gate charge at V_{DD}

ΔV_{BST} = Voltage drop at the BST pin

Power Dissipation Considerations

Power dissipation in the driver can be separated into two areas:

- Quiescent current dissipation
- Internal driver dissipation

Quiescent Current Power Dissipation

Power is dissipated in the MIC4600 even if nothing is being driven. The quiescent current is drawn by the bias for the internal circuitry and the level shifting circuitry. The quiescent current is proportional to operating frequency.

The typical characteristic graphs show how quiescent current varies with switching frequency.

The power dissipated due to quiescent current is calculated in

$$P_{DISS\_IQ} = V_{DD} \times I_{DD}$$ **Eq.** 5

Gate Driver Power Dissipation

Power dissipation in the output driver stage is mainly caused by charging and discharging the gate to source and gate to drain capacitance of the external MOSFET. Figure 5 shows a simplified equivalent circuit of the MIC4600 driving an external high-side MOSFET.

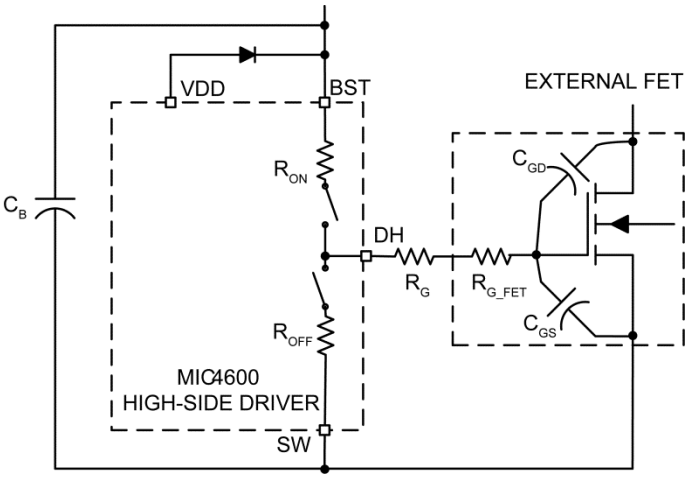


Figure 5. MIC4600 Driving an External MOSFET

Dissipation during the External MOSFET Turn-On

Energy from capacitor C_B is used to charge up the input capacitance of the MOSFET (C_{GD} and C_{GS}). The energy delivered to the MOSFET is dissipated in the three resistive components, R_{ON}, R_G and R_{G_FET}. R_{ON} is the on resistance of the upper driver MOSFET in the MIC4600. R_G is the series resistor (if any) between the driver IC and the MOSFET. R_{G_FET} is the gate resistance of the MOSFET. R_{G_FET} is usually listed in the power MOSFET's specifications. The ESR of capacitor C_B and the resistance of the connecting etch can be ignored since they are much less than R_{ON} and R_{G_FET}.

The effective capacitances of C_{GD} and C_{GS} are difficult to calculate because they vary non-linearly with Id, V_{GS}, and V_{DS}. Fortunately, most power MOSFET specifications include a typical graph of total gate charge vs. V_{GS}. Figure 6 is a typical gate charge curve for a power MOSFET. This chart shows that for a gate voltage of 4.5V, the MOSFET gate is charged up to 25nC of total gate charge. The energy dissipated by the resistive components of the gate drive circuit during turn-on is calculated as noted in

$$E = \frac{1}{2} \times C_{ISS} \times V_{GS}^{2},$$

but

$$Q = C \times V,$$

so

$$E = \frac{1}{2} \times Q_G \times V_{GS}$$ **Eq. 6**

Where:
C_{ISS} = Total gate capacitance of the MOSFET

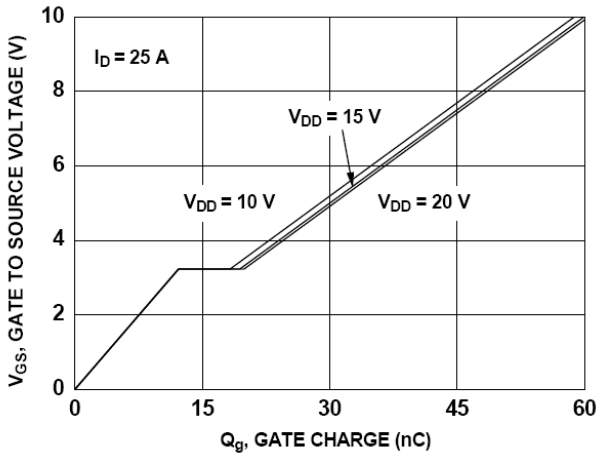


Figure 6. Typical Gate Charge vs. V_{GS}

The same energy is dissipated by R_{OFF}, R_G, and R_{G_FET} when the driver IC turns the MOSFET off. Assuming Ron is approximately equal to R_{OFF}, the total energy and power dissipated by the resistive drive elements is illustrated in Equation 7:

$$E_{DRIVER} = Q_G \times V_{GS}$$
and
$$P_{DRIVER} = Q_G \times V_{GS} \times f_S$$ **Eq. 7**

Where:

E_{DRIVER} = Energy dissipated per switching cycle

P_{DRIVER} = Power dissipated per switching cycle

Q_G = Total gate charge at V_{GS}

V_{GS} = Gate to source voltage on the MOSFET

f_S = Switching frequency of the gate drive circuit

The power dissipated inside the driver is equal to the ratio of R_{ON} and R_{OFF} to the external resistive losses in R_G and R_{G_FET}. Letting $R_{ON} = R_{OFF}$, the power dissipated in the MIC4600 due to driving the external MOSFET is illustrated in Equation 8:

$$P_{DISS_{DRIVER}} = P_{DRIVER} \frac{R_{ON}}{R_{ON} + R_G + R_{G\_FET}} \quad \textbf{Eq. 8}$$

Total Power Dissipation and Thermal Considerations

Total power dissipation in the MIC4600 is equal to the power dissipation caused by driving the external MOSFETs and the Quiescent current.

$$P_{DISS\,TOTAL} = P_{DISS\,IQ} + P_{DISS\,DRIVE} \quad \textbf{Eq. 9}$$

The die temperature can be calculated after the total power dissipation is known, as in Equation 10:

$$T_J = T_A + P_{DISS_{TOTAL}} \times \theta_{JA} \quad \textbf{Eq. 10}$$

Where:

T_A = Maximum ambient temperature

T_J = Junction temperature (°C)

$P_{DISS_{TOTAL}}$ = Power dissipation of the MIC4600

θ_{JA} = Thermal resistance from junction to ambient air

Decoupling and Bootstrap Capacitor Selection

Decoupling capacitors are required for both the low side (VDD) and high side (BST) supply pins. These capacitors supply the charge necessary to drive the external MOSFETs and also minimize the voltage ripple on these pins. The capacitor from BST to SW has two functions: it provides decoupling for the high-side driver and is the supply voltage to the high-side circuit while the external MOSFET is on. Ceramic capacitors are recommended because of their low impedance and small size. Z5U type ceramic capacitor dielectrics are not recommended because of the large change in capacitance over temperature and voltage. A minimum value of 0.1µF is required for each of the capacitors, regardless of the MOSFETs being driven. Larger MOSFETs may require larger capacitance values for proper operation.

Placement of the decoupling capacitors is critical. The bypass capacitor for VDD should be placed as close as possible between the VDD and PGND pins. The bypass capacitor (C_B) for the BST supply pin must be located as close as possible between the BST and SW pins. The etch connections must be short, wide, and direct. The use of a ground plane to minimize connection impedance is recommended (refer to the Grounding, Component Placement, and Circuit Layout section for more information).

Grounding, Component Placement, and Circuit Layout

Nanosecond switching speeds and ampere peak currents in and around the MIC4600 drivers require proper placement and trace routing of all components. Improper placement may cause degraded noise immunity, false switching, excessive ringing, or circuit latch-up.

Figure 7 shows the critical current paths when the driver outputs go high and turn on the external MOSFETs. It also helps demonstrate the need for a low impedance ground plane. Charge needed to turn-on the MOSFET gates comes from the decoupling capacitors C_{VDD} and C_B. Current in the low-side gate driver flows from C_{VDD} through the internal driver, into the MOSFET gate, and out the source. The return connection back to the decoupling capacitor is made through the ground plane. Any inductance or resistance in the ground return path causes a voltage spike or ringing to appear on the source of the MOSFET. This voltage works against the gate drive voltage and can either slow down or turn off the MOSFET during the period when it should be turned on.

Current in the high-side driver is sourced from capacitor C_B and flows into the BST pin and out the DH pin, into the gate of the high side MOSFET. The return path for the current is from the source of the MOSFET and back to capacitor C_B. The high-side circuit return path usually does not have a low-impedance ground plane so the etch connections in this critical path should be short and wide to minimize parasitic inductance. As with the low-side circuit, impedance between the MOSFET source and the decoupling capacitor causes negative voltage feedback that fights the turn-on of the MOSFET.

It is important to note that capacitor C_B must be placed close to the BST and SW pins. This capacitor not only provides all the energy for turn-on but it must also keep HB pin noise and ripple low for proper operation of the high-side drive circuitry.

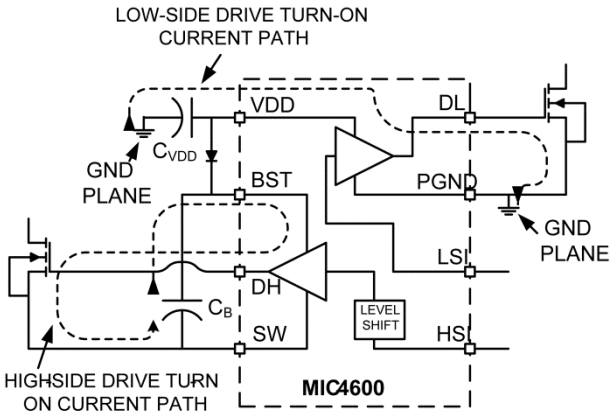


Figure 7. Turn-On Current Paths

Figure 8 shows the critical current paths when the driver outputs go low and turn off the external MOSFETs. Short, low-impedance connections are important during turn-off for the same reasons given in the turn-on explanation. Current flowing through the internal diode replenishes charge in the bootstrap capacitor, C_{BST}

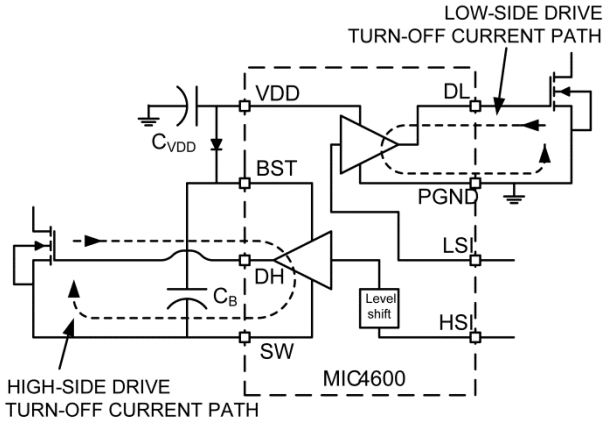
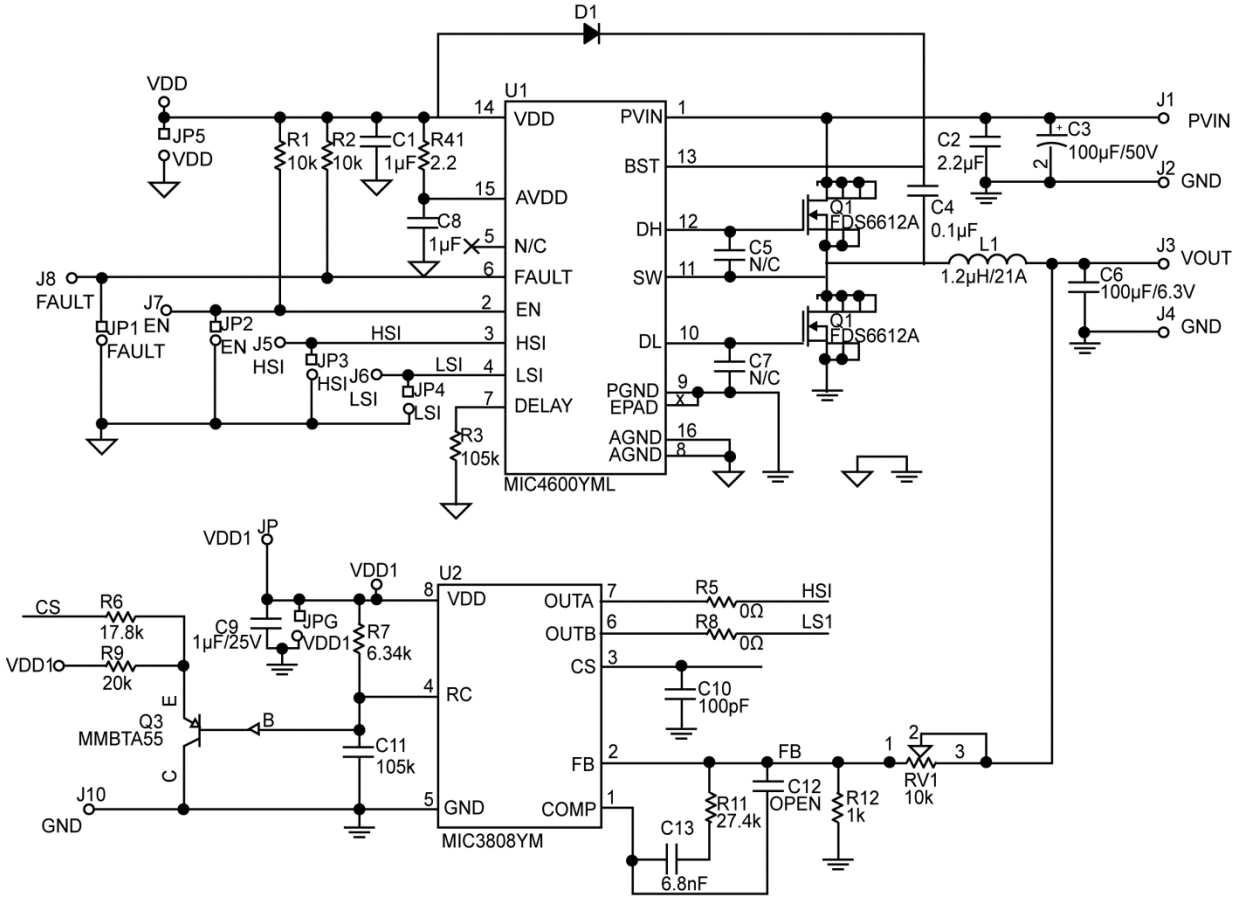


Figure 8. Turn-Off Current Paths

Use a ground plane to minimize parasitic inductance and impedance of the return paths. The MIC4600 is capable of greater than 1A peak currents and any impedance between the MIC4600, the decoupling capacitors, and the external MOSFET will degrade the performance of the driver.

Typical Application Schematic



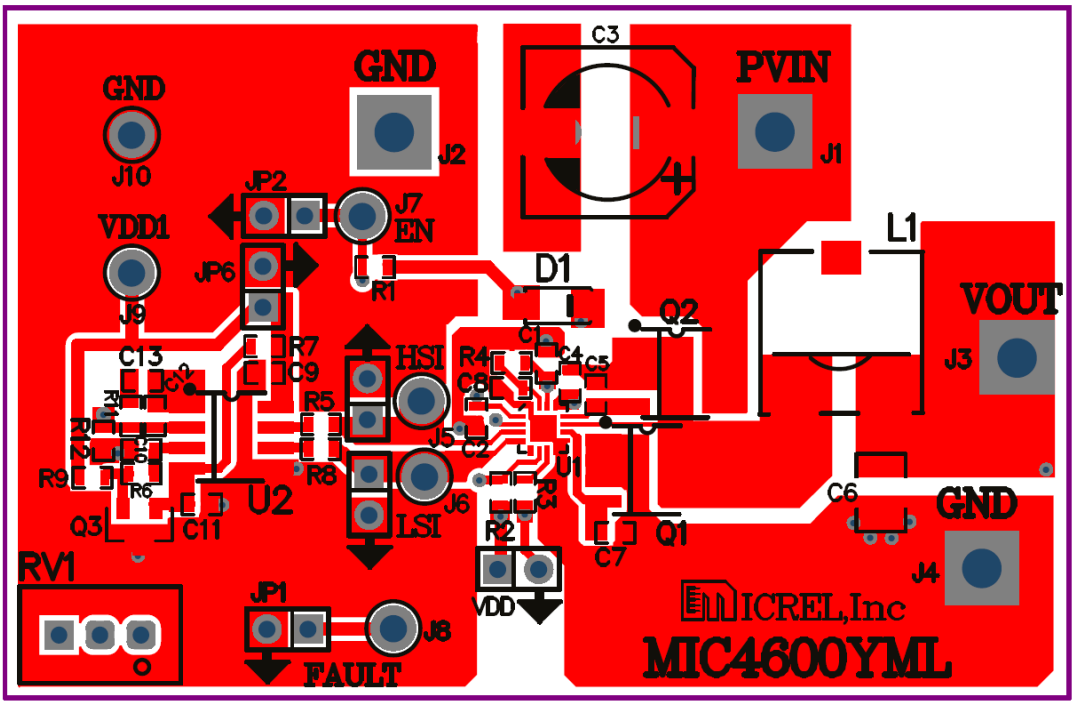
Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1, C8	06036D105MAT2A	AVX[5]	1µF, 6.3V, X5R, Ceramic Capacitor	2
C2	C1608X5R1V225M080AC	TDK[6]	2.2µF, 50V, X5R, Ceramic capacitor	1
C3	EEU-FM1H101B	Panasonic[7]	100µf, 50V, Al. El.	1
C4	06033D107MAT2A	AVX	0.1uF, 25V, X5R, ceramic capacitor	1
C5, C7, C12			0603 size capacitor, not fitted	0
C6	C3216X5R0J107M160AB	TDK	100µF, 6.3V, x5R, ceramic	1
C9	C1608X5R1E105M080AC	TDK	1µF, 25V, X5R, ceramic	1
C10	06033A101JAT2A	AVX	100pF, 25V, NPO, ceramic	1
C11	06033A221JAT2A	AVX	220pF, 25V, NPO, ceramic	1
C13	06033C682MAT2A	AVX	6.8nF, 25V, X7R ceramic	1
R1, R2	CRCW06031002FRT1	Vishay Dale[8]	10kΩ (0603 size), 1%	2
R3	CRCW06031053FRT1	Vishay Dale	105kΩ (0603 size), 1%	1
R4	CRCW06032R20JNEA	Vishay Dale	2.2Ω (0603 size), 5%	1
R5, R8	CRCW0600000FRT1	Vishay Dale	0Ω (0603 size)	2
R6	CRCW06031782FRT1	Vishay Dale	17.8kΩ (0603 size), 1%	1
R7	CRCW06036341FRT1	Vishay Dale	6.34kΩ (0603 size), 1%	1
R9	CRCW06032002FRT1	Vishay Dale	20kΩ (0603 size), 1%	1
R11	CRCW06032742FRT1	Vishay Dale	27.4kΩ (0603 size), 1%	1
R12	CRCW06031001FRT1	Vishay Dale	1kΩ (0603 size), 1%	1
D1	RB500V-40-TP	MCC[10]	40V, 0.1A, schottky, SOD323	1
Q1, Q2	FDS6612A	Fairchild[9]	MOSFET	2
Q3	MBTA55-TP	MCC	60V, 500mA, NPN, SOT-23	1
RV1	67YR10KLF	TT Electronics[11]	10kΩ, 10 turn trim pot	1
L1	CDEP105MENP-1R2PC	Sumida[12]	1.2ΩH, 21A, inductor	1
U1	**MIC4600YML**	**Micrel[13]**	**28V Half-Bridge MOSFET Driver**	**1**
U2	**MIC3808YM**	**Micrel**	**PWM Controller**	**1**

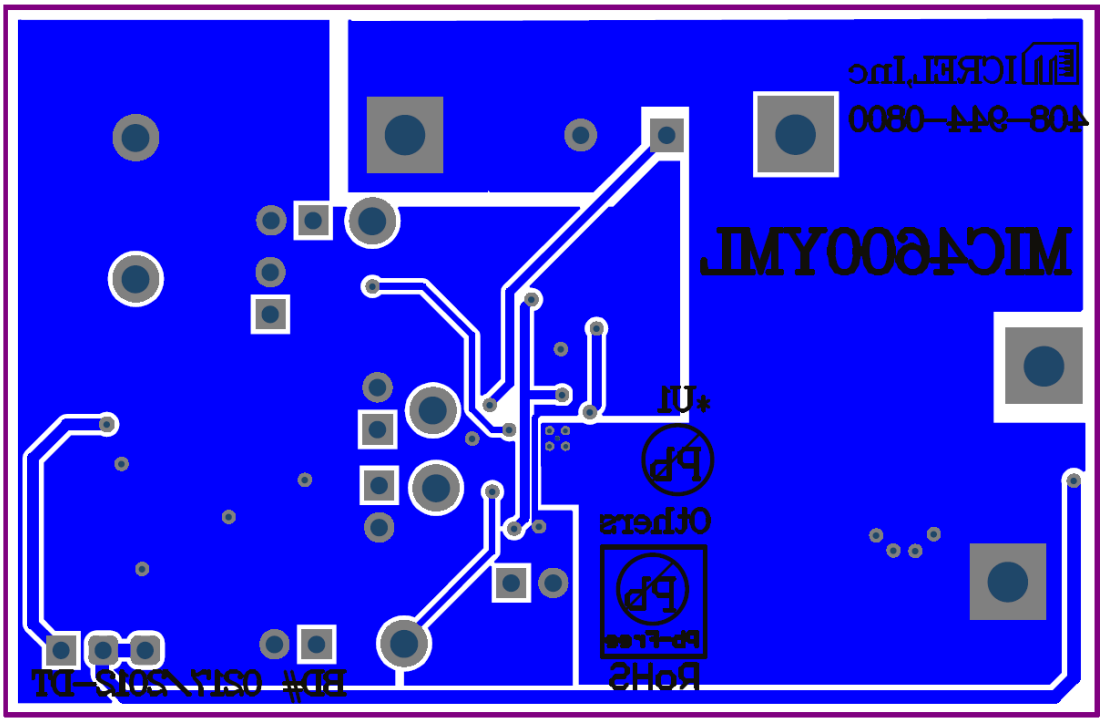
Notes:

5. AVX: www.avx.com.
6. TDK: www.tdk.com.
7. Panasonic: www.panasonic.com.
8. Vishay: www.vishay.com.
9. Fairchild: www.fairchild.com.
10. MCC: www.mccsemi.com.
11. TT Electronics: www.bitechnologies.com.
12. Sumida: www.sumida.com.
13. **Micrel, Inc.: www.micrel.com.**

PCB Layout Recommendations

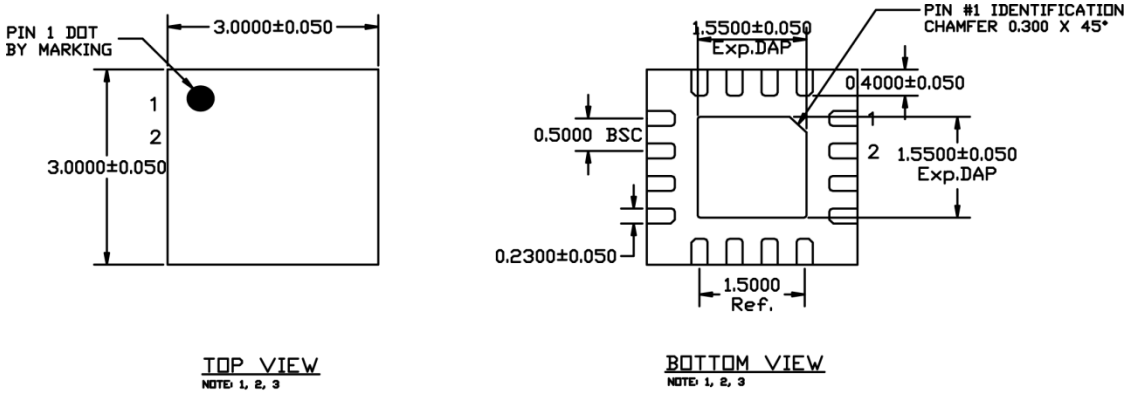


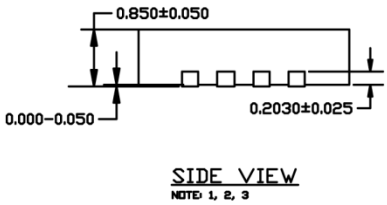
Top Layer



Bottom Layer

Package Information[11]





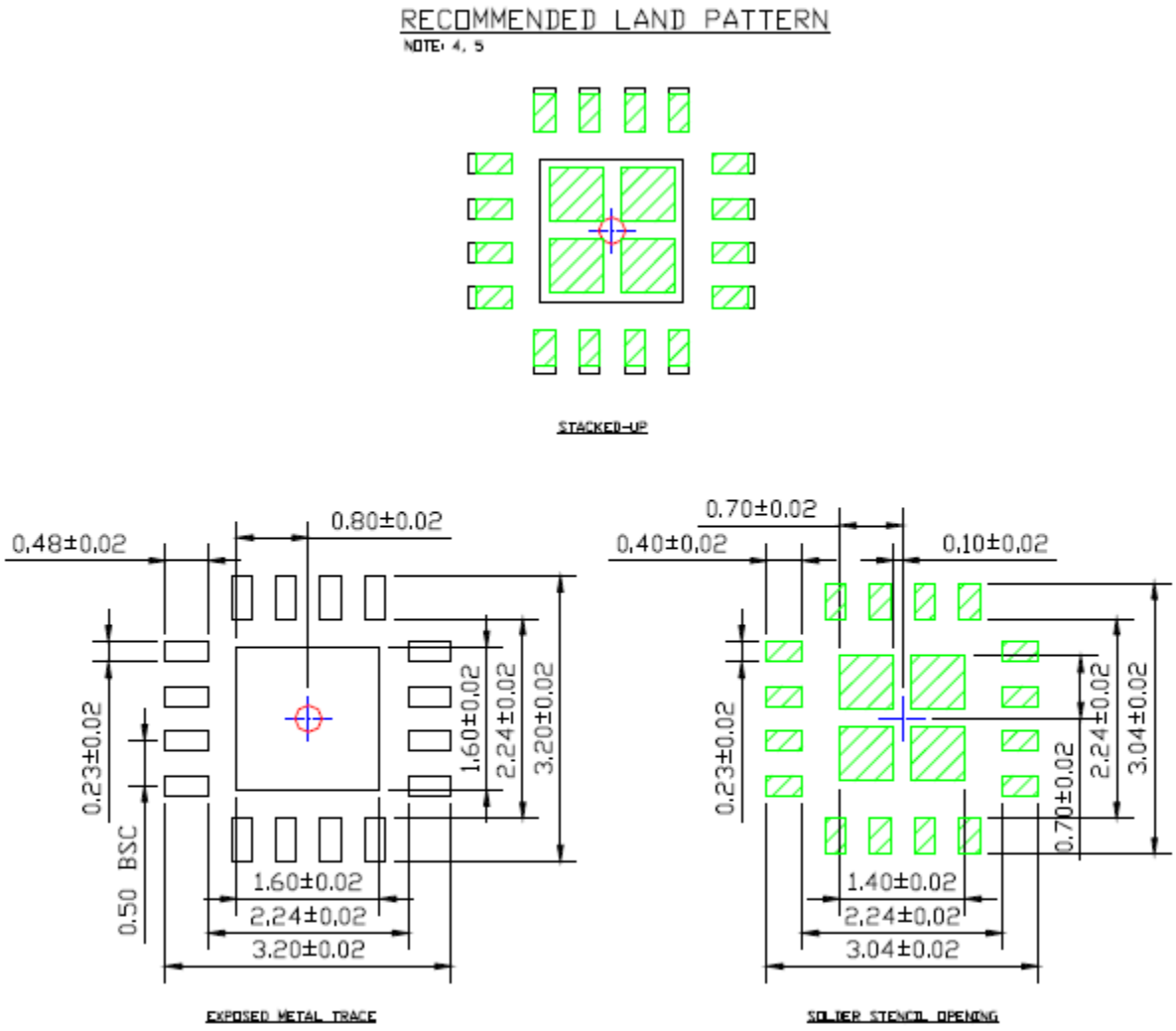
NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076 MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.35 MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) Indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.60x0.60 MM IN SIZE, 0.20 MM SPACING.

3mm × 3mm QFN 16-Pin Package (ML)

Note:

14. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

Recommended Landing Pattern



MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com

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