Low Power, 18 MHz Variable Gain Amplifier

Data Sheet **AD8338**

FEATURES

Voltage controlled gain range of 0 dB to 80 dB
3 mA supply current at gain of 40 dB
Low frequency (LF) to 18 MHz operation
Supply range: 3.0 V to 5.0 V
Adjustable gain range
Low noise: 4.5 nV/√Hz
Fully differential signal path
Offset correction (offset null) feature
Adjustable bandwidth
Internal 1.5 V reference
16-lead LFCSP
Automatic gain control feature
Wide gain range for high dynamic range signals

APPLICATIONS

Front end for inductive telemetry systems
Ultrasonic signal receivers
RF baseband signal conditioning

GENERAL DESCRIPTION

The AD8338 is a variable gain amplifier (VGA) for applications that require a fully differential signal path, low power, low noise, and a well-defined gain over frequencies from LF to 18 MHz. The device can also operate using single-ended sources if required.

The basic gain function is linear-in-dB with a nominal gain range of 0 dB to 80 dB; the nominal gain range corresponds to a control voltage on the GAIN pin of 0.1 V to 1.1 V. The gain range can be adjusted up or down via direct access to the internal summing nodes at the INPD and INMD pins. For example, if a 47 Ω resistor is applied to the INPD and INMD pins, a gain range of 20 dB to 100 dB is set with an input referred noise level of 1.5 nV√Hz.

The AD8338 includes additional circuits to enable offset correction and automatic gain control (AGC). DC offset voltages are removed by the offset correction circuit, which behaves like a high-pass filter. The high-pass filter corner frequency is set using an external capacitor. The AGC function varies the gain of the AD8338 to maintain a constant rms output voltage. A user supplied voltage controls the target output rms voltage. A user supplied capacitor to ground at the DETO pin controls the response time of the AGC circuit.

FUNCTIONAL BLOCK DIAGRAM

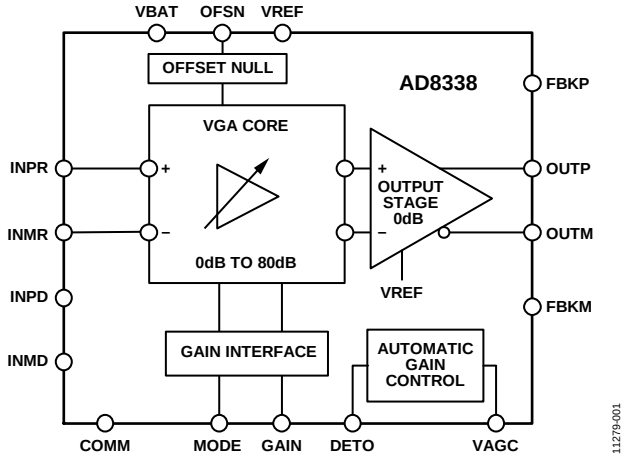

Figure 1.

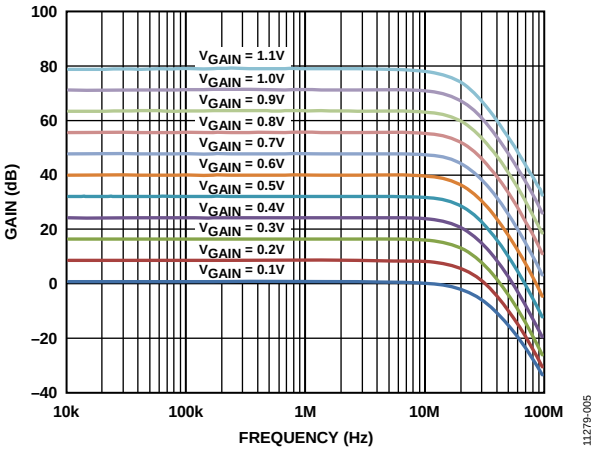

Figure 2. Gain vs. Frequency

The AD8338 offers additional versatility by allowing user access to the internal summing nodes. With a few discrete components, users can customize the gain, bandwidth, input impedance, and noise profile of the part to fit their application.

The AD8338 uses a single supply voltage of 3.0 V to 5.0 V and is very power efficient, consuming as little as 3 mA quiescent current. The AD8338 is available in a 3 mm × 3 mm, RoHS compliant, 16-lead LFCSP. It is specified over the industrial temperature range of −40°C to +85°C.

Rev. 0 **Document Feedback**

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REVISION HISTORY

4/13—Revision 0: Initial Version

SPECIFICATIONS

AC SPECIFICATIONS

VBAT = 3.0 V, T_A = 25°C, C_L = 2 pF on OUTP and OUTM, R_L = ∞, MODE pin high, R_{IN} = 2 × 500 Ω, V_{GAIN} = 0.6 V, differential operation, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT INTERFACE					
Gain Range	Standard configuration using the INPR and INMR inputs	0		80	dB
Gain Span			80		dB
Input Voltage Range			3		V p-p
Input 1 dB Compression	Differential input, V_{CM} = 1.5 V, gain = 0.1 V/0 dB				
	f = 400 kHz		2.2		V p-p
	f = 1 MHz		2		V p-p
	f = 4 MHz		1.6		V p-p
	f = 10 MHz		0.75		V p-p
−3 dB Bandwidth			18		MHz
Gain Accuracy	Standard configuration using the INPR and INMR inputs; 0.1 V < V_{GAIN} < 1.1 V	−2	+0.5	+2	dB
Input Resistance	Standard configuration using the INPR and INMR inputs	0.8	1	1.2	kΩ
Input Capacitance			2		pF
OUTPUT INTERFACE	OUTP and OUTM pins				
Small Signal Bandwidth	V_{GAIN} = 0.6 V		18		MHz
Peak Slew Rate	V_{GAIN} = 0.6 V		50		V/µs
Peak-to-Peak Output Swing	Differential output		2.8		V p-p
Common-Mode Voltage			1.5		V
Input-Referred Noise Voltage	Standard configuration using the INPR and INMR inputs		4.5		nV/√Hz
	Driving external 47 Ω input resistors connected to INPD and INMD		1.5		nV/√Hz
Offset Voltage	RTO, V_{GAIN} = 0.1 V, offset null on	−10		+10	mV
	RTO, V_{GAIN} = 0.6 V, offset null on	−10		+10	mV
	RTO, V_{GAIN} = 0.1 V, offset null off	−50		+50	mV
	RTO, V_{GAIN} = 0.6 V, offset null off	−200		+200	mV
POWER SUPPLY					
VBAT		3.0		5.0	V
I_{VBAT}	Min gain, V_{GAIN} = 0.1 V		6.0	8.0	mA
	Mid gain, V_{GAIN} = 0.6 V		3.0	3.8	mA
	Max gain, V_{GAIN} = 1.1 V		4.5	6.0	mA
GAIN CONTROL					
Gain Voltage		0.1		1.1	V
Gain Slope		77	80	83	dB/V
			12.5		mV/dB
VREF ACCURACY	VREF = 1.5 V		2		%
DETO OUTPUT CURRENT			±10		µA
AGC CONTROL	MODE = 0 V				
Maximum Target Amplitude	Expected rms output value for target = VAGC − VREF = 1.0 V		1.0		V rms

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VBAT to COMM	−0.3 V to +5.5 V
INPR, INPD, INMD, INMR, MODE, GAIN, FBKM, FBKP, OUTM, OUTP, VAGC, VREF, OFSN	COMM to VBAT
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
16-Lead LFCSP	48.75	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

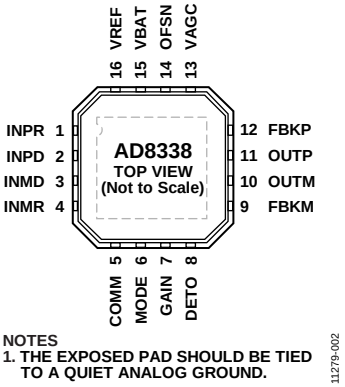


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
0	EPAD	Exposed Pad. The exposed pad should be tied to a quiet analog ground.
1	INPR	Positive 500 Ω Resistor Input for Voltage Input Applications.
2	INPD	Positive Input for Current Input Applications.
3	INMD	Negative Input for Current Input Applications.
4	INMR	Negative 500 Ω Resistor Input for Voltage Input Applications.
5	COMM	Ground.
6	MODE	Gain Mode. This pin selects positive or negative gain slope for gain control. When this pin is tied to VBAT, the gain of the AD8338 increases proportionally with an increase of the voltage on the GAIN pin. When this pin is tied to COMM, the gain decreases with an increase of the voltage on the GAIN pin.
7	GAIN	Gain Control Input, 12.5 mV/dB or 80 dB/V.
8	DETO	Detector Output Terminal, ±10 µA. If the AGC feature is not used, tie this pin to COMM.
9	FBKM	Negative Feedback Node. For more information, see the Adjusting the Output Common-Mode Voltage section.
10	OUTM	Negative Output.
11	OUTP	Positive Output.
12	FBKP	Positive Feedback Node. For more information, see the Adjusting the Output Common-Mode Voltage section.
13	VAGC	Voltage for Automatic Gain Control Circuit. This pin controls the target rms output voltage for the AGC circuit. For more information, see the AGC Circuit section.
14	OFSN	Offset Null Terminal. For more information, see the Offset Correction Circuit section.
15	VBAT	Positive Supply Voltage.
16	VREF	Internal 1.5 V Voltage Reference.

TYPICAL PERFORMANCE CHARACTERISTICS

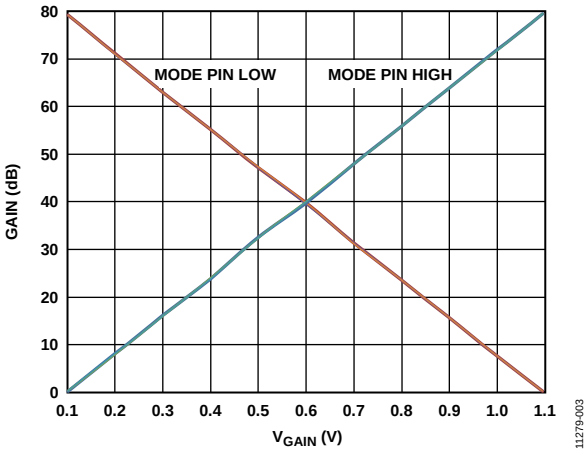


Figure 4. Gain vs. V_{GAIN}

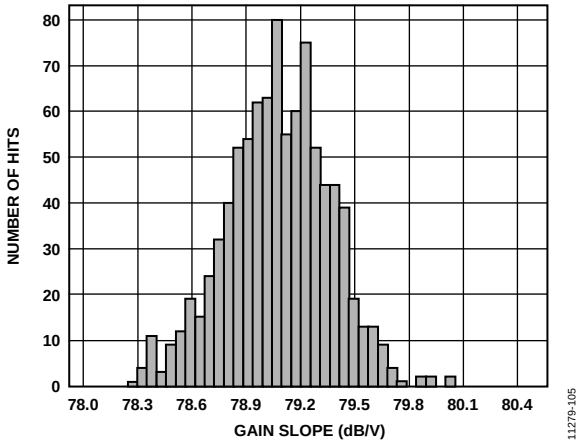


Figure 5. Gain Slope Histogram

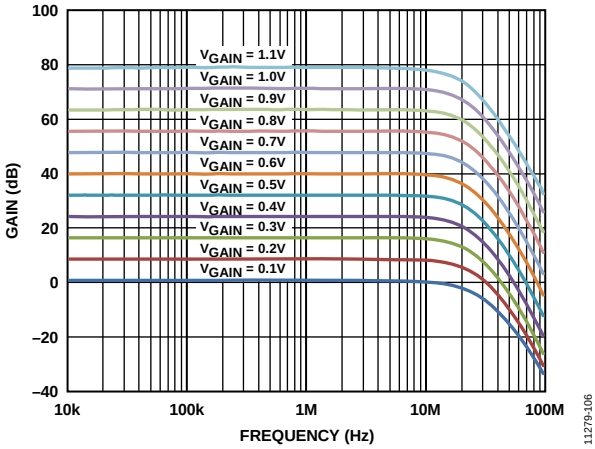


Figure 6. Gain vs. Frequency

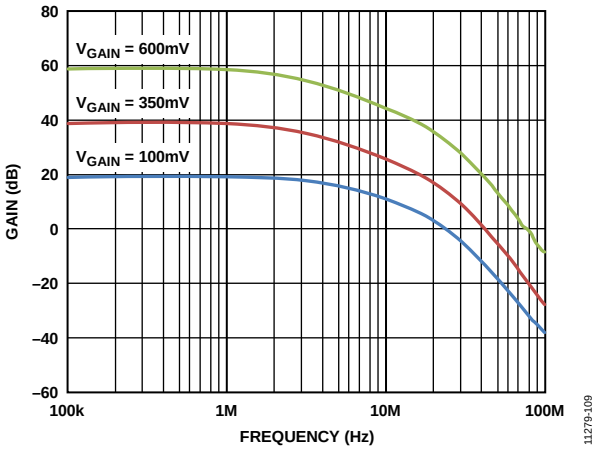


Figure 7. Gain vs. Frequency, R_{IN} = 50 Ω

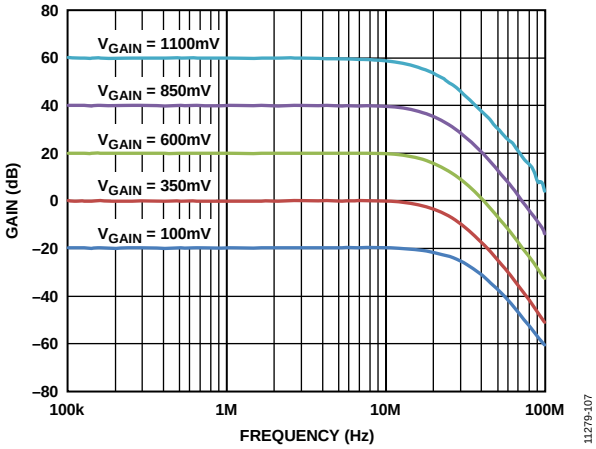
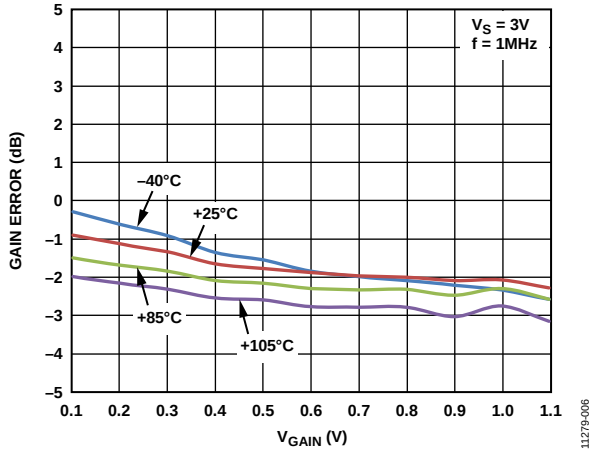


Figure 8. Gain vs. Frequency, R_{IN} = 5 kΩ



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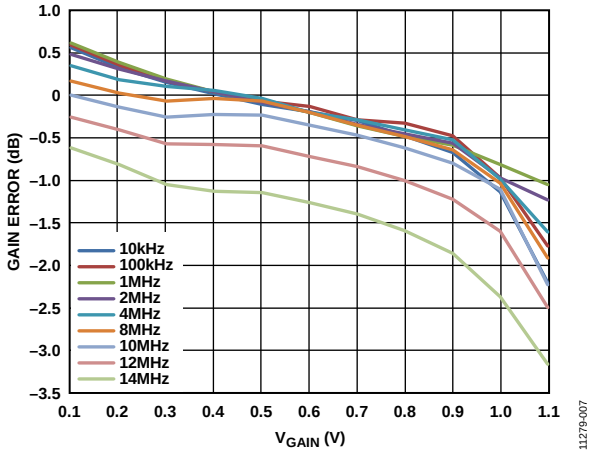


Figure 10. Gain Error vs. V_{GAIN} over Frequency

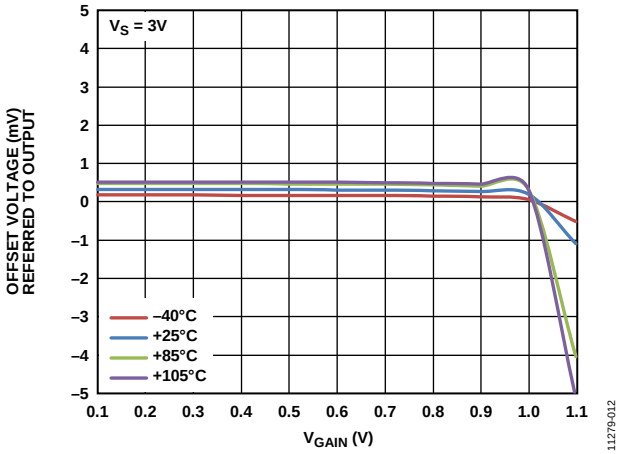


Figure 13. Differential Offset Voltage vs. V_{GAIN}, Offset Null On

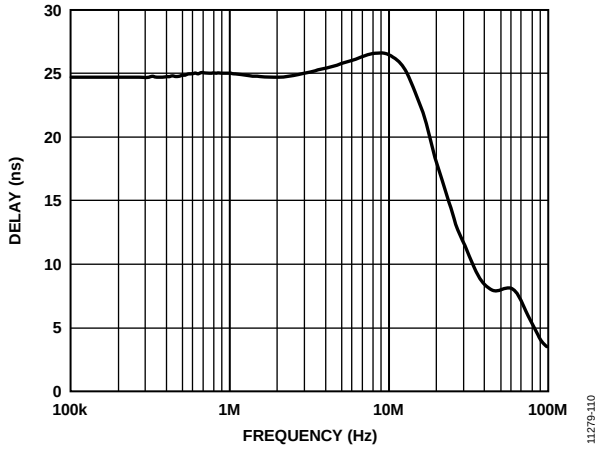


Figure 11. Group Delay vs. Frequency

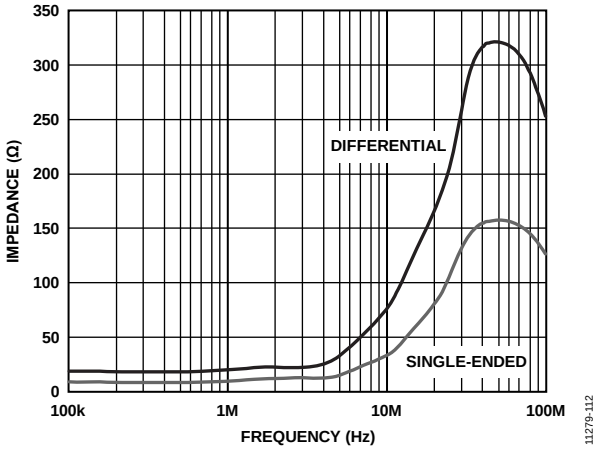


Figure 14. Output Impedance vs. Frequency

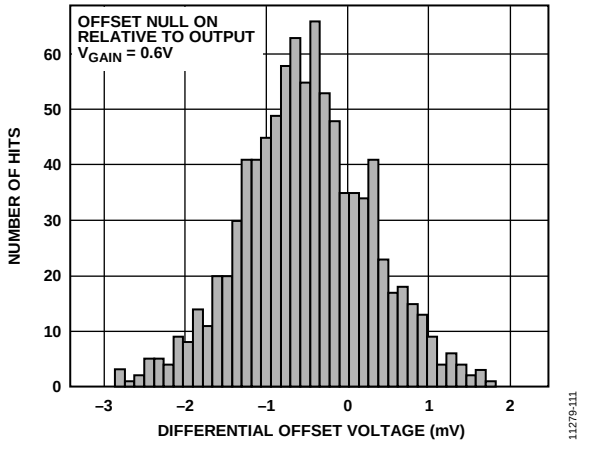
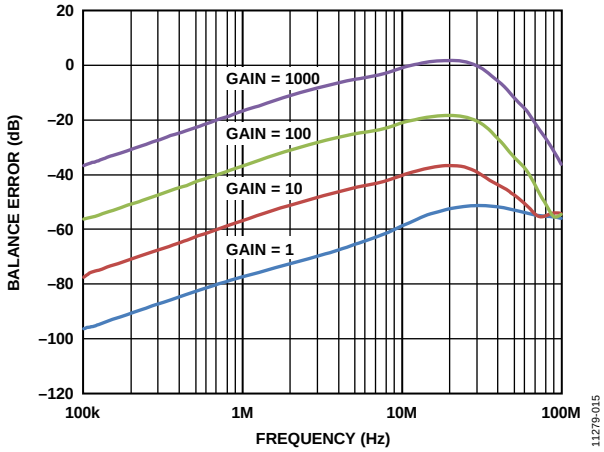


Figure 12. Differential Offset Voltage Histogram



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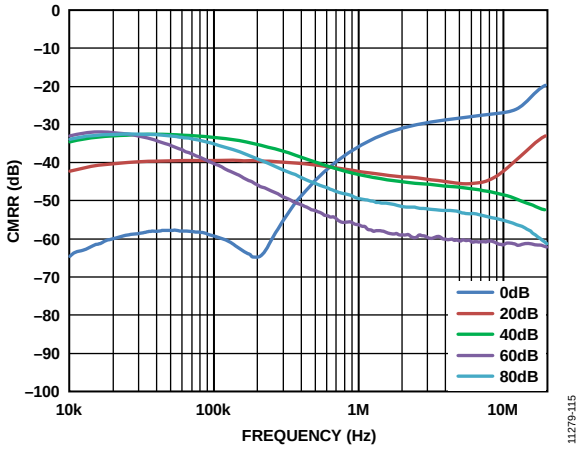


Figure 16. CMRR vs. Frequency over Gain, Offset Null On, Referred to Input

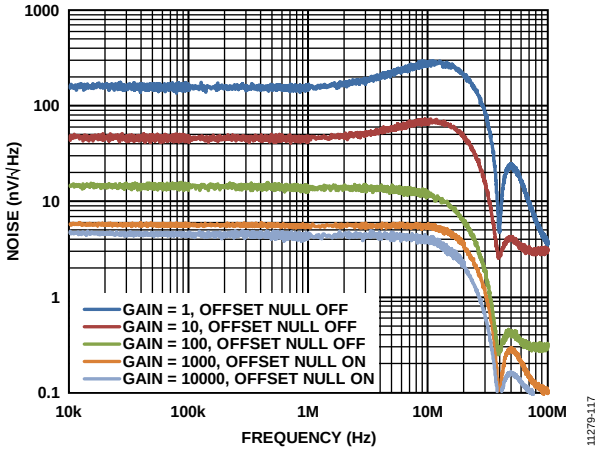


Figure 19. Input Referred Noise vs. Frequency, VBAT = 3 V

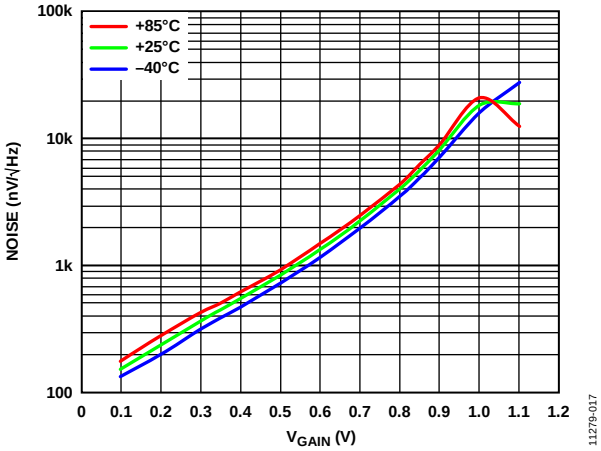


Figure 17. Output Referred Noise vs. V_{GAIN}

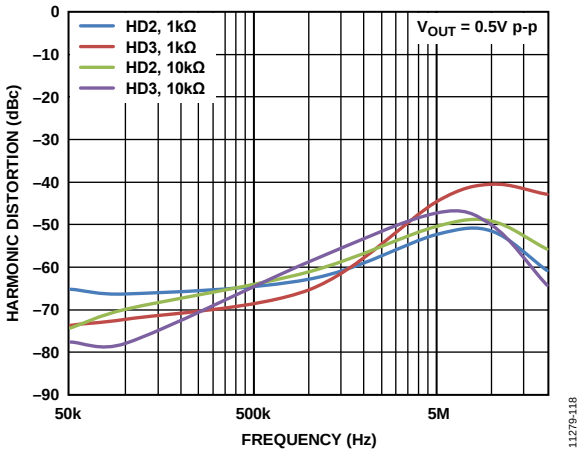


Figure 20. Harmonic Distortion vs. Frequency

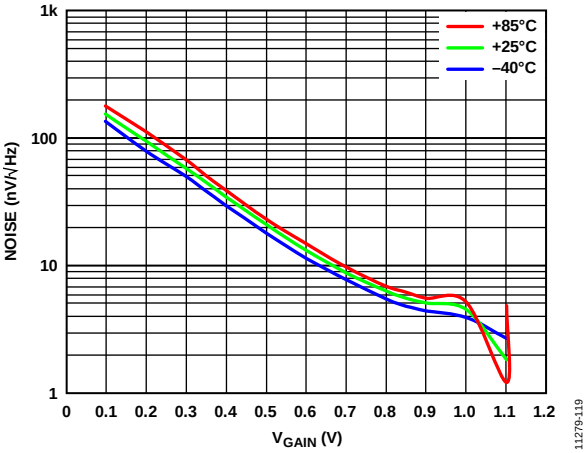


Figure 18. Input Referred Noise vs. V_{GAIN}

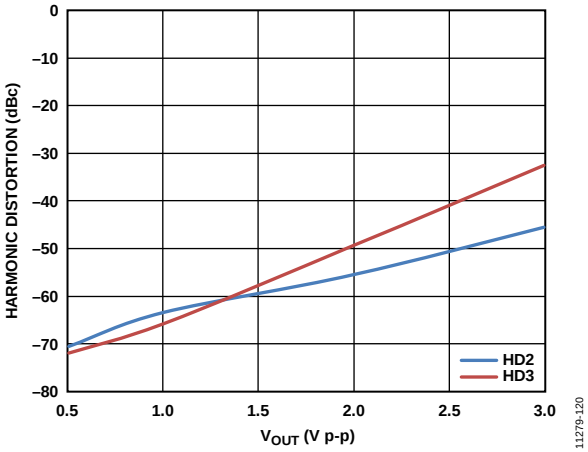


Figure 21. Harmonic Distortion vs. Output Amplitude

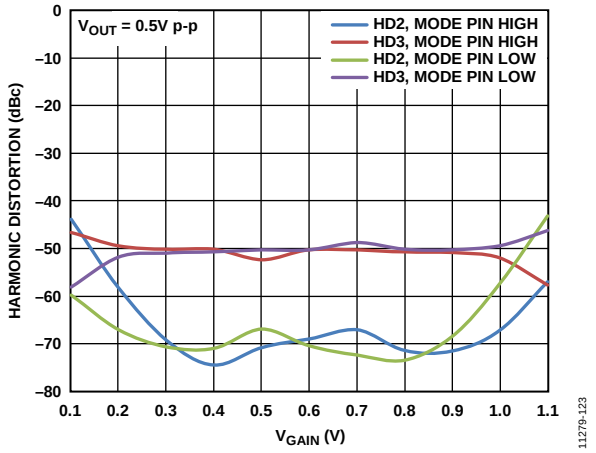


Figure 22. Harmonic Distortion vs. V_{GAIN}

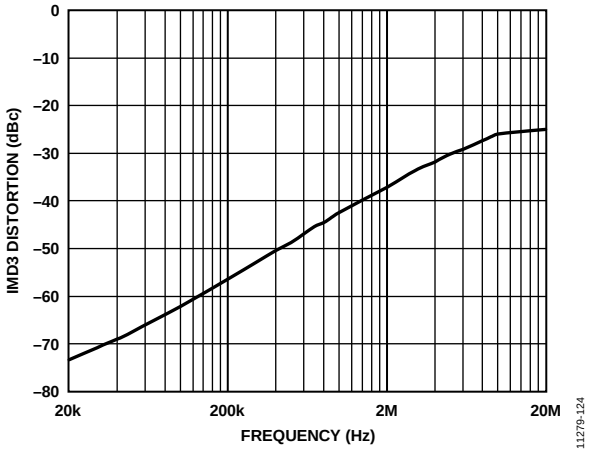


Figure 25. IMD3 Distortion vs. Frequency

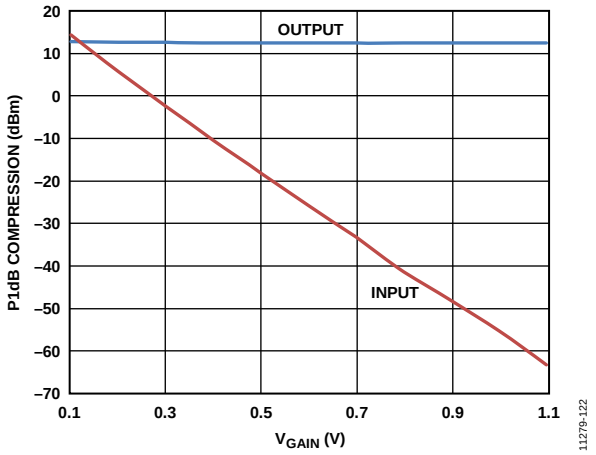


Figure 23. Input and Output 1 dB Compression vs. V_{GAIN}

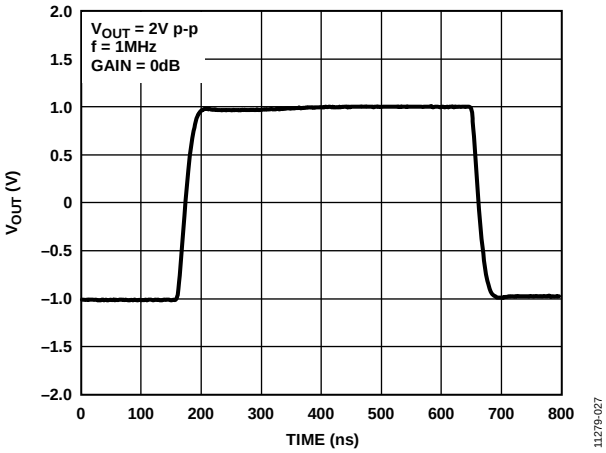


Figure 26. Large Signal Pulse Response vs. Time, V_{GAIN} = 0 V

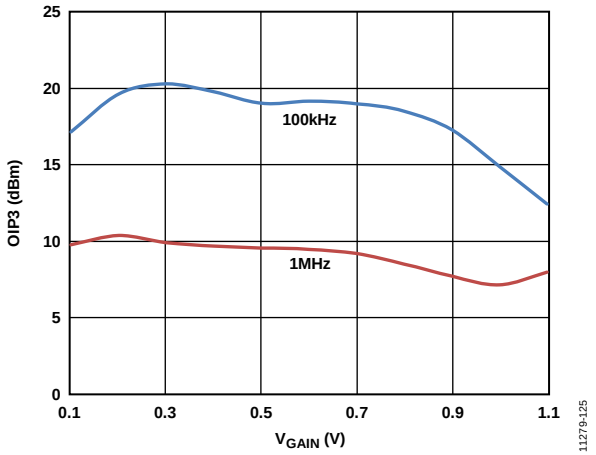


Figure 24. OIP3 vs. V_{GAIN}

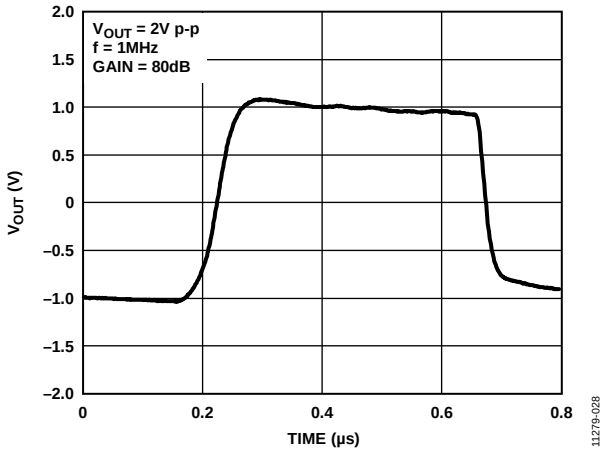


Figure 27. Large Signal Pulse Response vs. Time, V_{GAIN} = 1.0 V

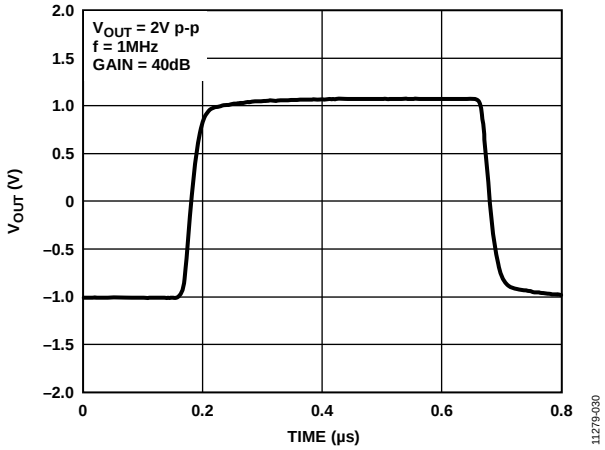


Figure 28. Large Signal Pulse Response vs. Time, V_{GAIN} = 0.6 V

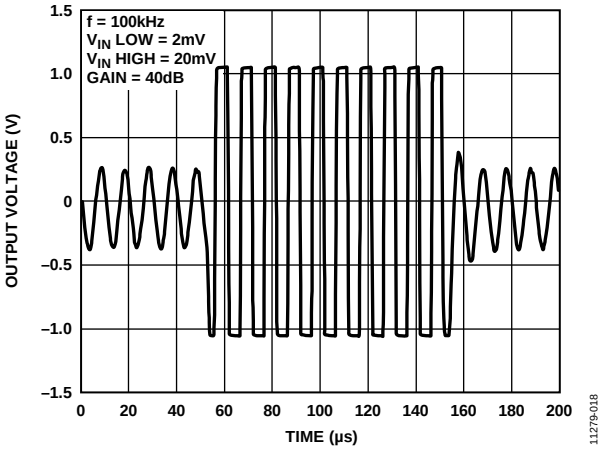


Figure 31. Overdrive Recovery vs. Time

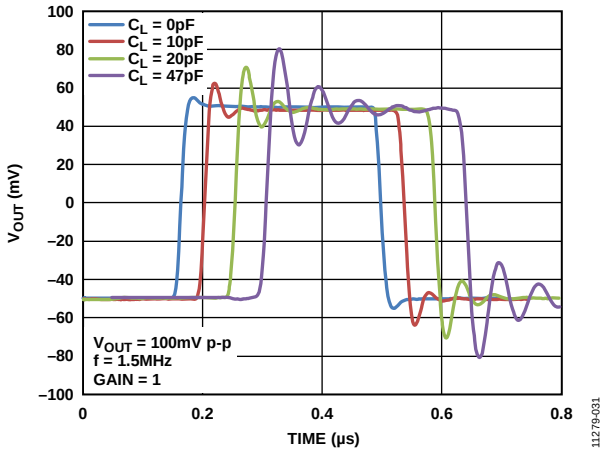


Figure 29. Small Signal Pulse Response vs. Time (Varying Capacitive Loads)

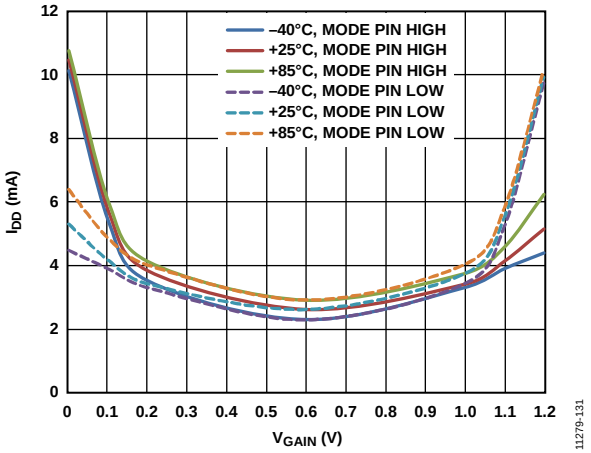


Figure 32. Supply Current vs. V_{GAIN}

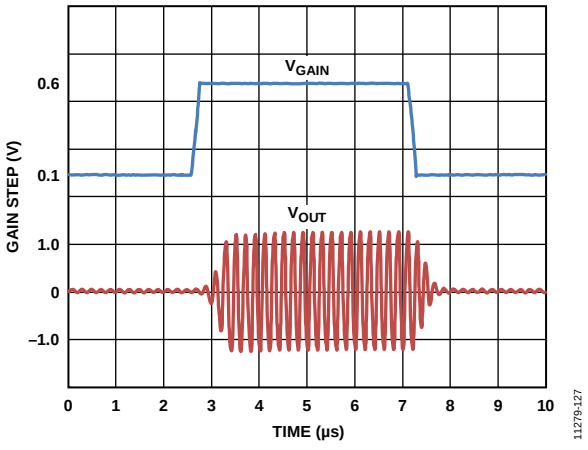
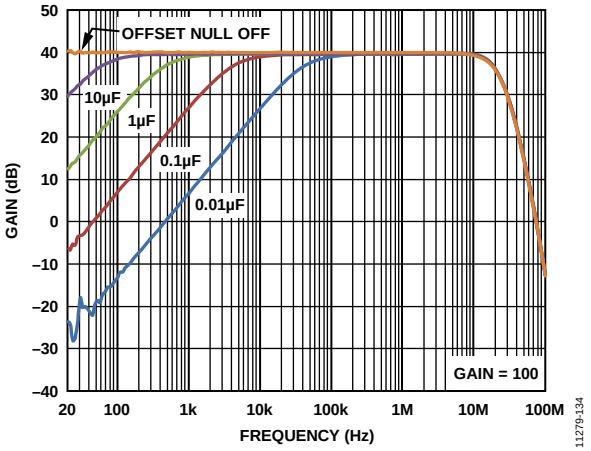


Figure 30. Gain Step Response vs. Time



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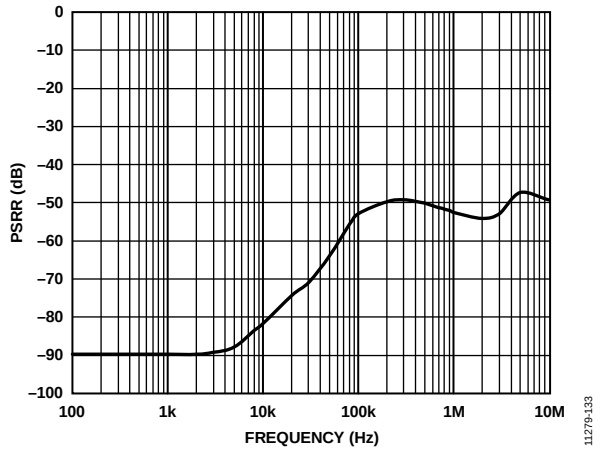

Figure 34. PSRR vs. Frequency

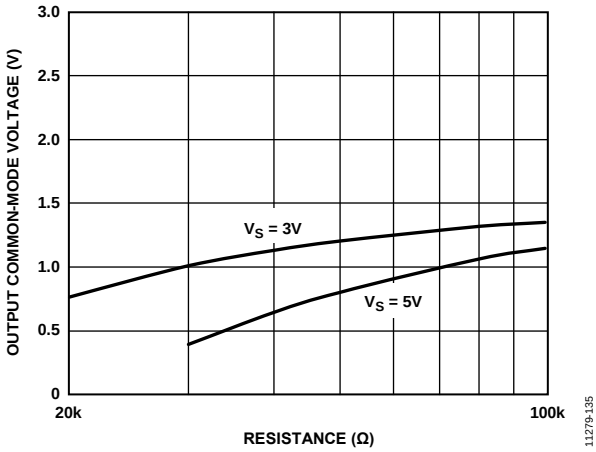

Figure 37. Output Common-Mode Voltage vs. R_{CM} to VBAT

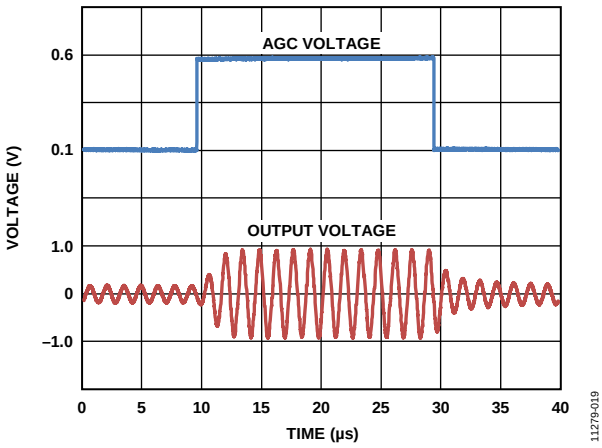

Figure 35. AGC Response vs. Time, No Load

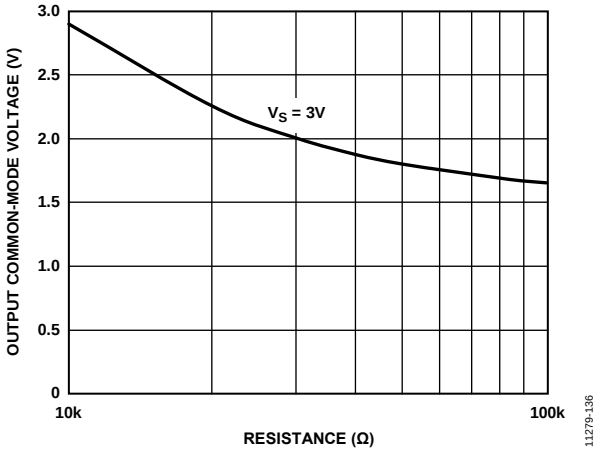

Figure 38. Output Common-Mode Voltage vs. R_{CM} to COMM

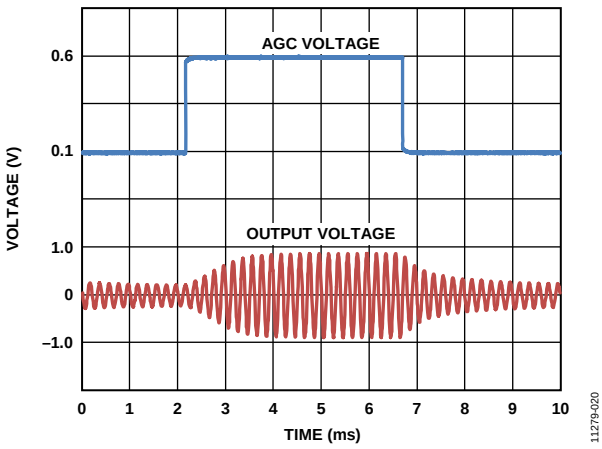

Figure 36. AGC Response vs. Time, C_L = 0.01 µF

THEORY OF OPERATION

GETTING STARTED WITH THE AD8338

The AD8338 is a variable gain amplifier (VGA) that provides a variable gain range of 80 dB. With a constant −3 dB bandwidth of 18 MHz across all gains, a gain bandwidth product of 180 GHz is achieved at the highest gain using only 4.5 mA of supply current. The differential output allows the AD8338 to directly drive an ADC input, simplifying board design and saving space and power.

In addition to its gain, bandwidth, and power performance, the AD8338 includes a range of features that increase its versatility.

- Single-supply operation ranging from 3.0 V to 5.0 V
- Built-in offset correction circuit to cancel out dc offsets
- Automatic gain control (AGC) circuit to control the gain and keep the output at a steady rms level

Access to internal nodes at both the input and output allows the user to adjust the gain range, adjust the output common-mode voltage, and tune the bandwidth.

INPR and INMR Pins in the Standard Configuration

The gain is controlled by a user supplied voltage input applied to the GAIN pin. The gain can be varied from 0 dB to 80 dB when the default internal resistors are used; the voltage at the GAIN pin can be varied from 0.1 V to 1.1 V. The default internal resistors are used by applying the input voltage to the INPR and INMR pins (Pin 1 and Pin 4; see Figure 39).

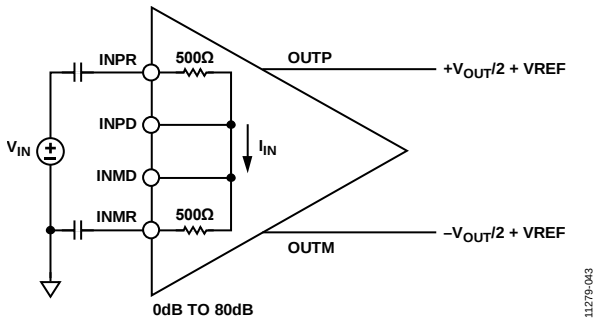

Figure 39. Input Voltage Applied to the INPR and INMR Pins

In the standard configuration, a differential input voltage applied across INPR and INMR is amplified, with the output voltage appearing differentially across OUTP and OUTM. The outputs have a default common-mode voltage of VREF, which is equal to 1.5 V.

GAIN and MODE Pins

The gain of the AD8338 is controlled by the GAIN and MODE pins. Adjusting the voltage at the GAIN pin from 0.1 V to 1.1 V adjusts the gain from its lowest to highest value.

The MODE pin controls the polarity of the gain adjustment. When MODE is tied to VBAT, the gain of the AD8338 increases proportionally with an increase of the voltage on the GAIN pin. When MODE is tied to COMM, the gain decreases with an increase of the voltage on the GAIN pin.

OFFSET CORRECTION CIRCUIT

The AD8338 provides an offset correction circuit to cancel out any dc offsets that may be present. Connecting a 0.2 µF capacitor from the OFSN pin to VREF allows frequencies above 400 Hz to pass through, but eliminates dc offsets. For dc-coupled operation, disable the offset correction circuit by connecting the OFSN pin directly to the COMM pin. When the part is operated without offset correction, exercise caution with large gains because any offsets present large errors on the outputs.

Unlike a high-pass filter, the offset correction circuit allows signals below the corner frequency to pass through with high levels of crossover distortion. If a frequency below the band of interest may present itself to the inputs, apply a filter in front of the VGA for best performance.

For lower frequency operation, a larger value of C_{OFSN} gives unpredictable results. If the part is operated at frequencies below 400 Hz, disable the offset correction circuit and compensate the offset externally.

The corner frequency can be approximately calculated as follows:

$$f_C = \frac{1}{2\pi \times 600 \times C_{OFSN}} \quad (1)$$

EXPLANATION OF THE GAIN FUNCTION

From a designer's standpoint, the gain of the AD8338 can be modeled as three cascaded gain stages. The first stage can be thought of as a differential input transconductance stage, where the input current is proportional to the differential input voltage that is applied to the input resistors, as follows:

$$I_{IN} = \frac{INPx - INMx}{R_P + R_N} \quad (2)$$

This current is then fed into the conceptual second stage, a current input-current output VGA, which has a gain range of −26 dB to +54 dB. The conceptual output current is given by Equation 3.

$$I_{OUT\_VGA} = I_{IN} \times 10^{-26 + 80 \times ((V_{GAIN} - 0.1)/20)} \quad (3)$$

When V_{GAIN} = 0.1 V, the output current is −26 dB less than the input current; when V_{GAIN} = 1.1 V, the output current is +54 dB greater than the input current.

The third and final stage can be modeled as a transimpedance stage, expressed as follows:

$$V_{OP} = I_{OUT\_VGA} \times R_{FEEDBACK} \quad (4a)$$

$$V_{ON} = -I_{OUT\_VGA} \times R_{FEEDBACK} \quad (4b)$$

$$V_{OUT} = V_{OP} - V_{ON} = 2 \times I_{OUT\_VGA} \times R_{FEEDBACK} \quad (4c)$$

For example, if the 500 Ω input resistors and 9.5 kΩ feedback resistors are used and a 1 V p-p signal is applied with V_{GAIN} set to 0.1 V, the output value is as follows:

$$I_{IN} = 1/(500 + 500) = 1 \text{ mA} \quad (5a)$$

$$I_{OUT\_VGA} = 1 \text{ mA} \times 10^{-26/20} = 50 \text{ μA} \quad (5b)$$

$$V_{OUT} = 2 \times 50 \text{ μA} \times 9.5 \text{ kΩ} = 0.95 \text{ V p-p} \quad (5c)$$

The calculation in Equation 5 results in a total gain of approximately −0.4 dB under the specified conditions. Compressing Equation 2 through Equation 4 produces the following simplified gain equation:

$$Gain \text{ (dB)} = (V_{GAIN} - 0.1) \times 80 + 20\log(R_{FEEDBACK}/R_{IN}) - 26 \quad (6)$$

where $R_{FEEDBACK}$ and R_{IN} are the resistor values from a single input to a single output.

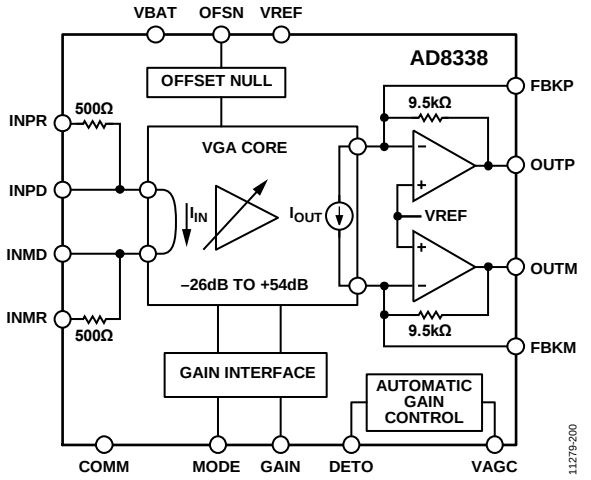

Figure 40. Functional Block Diagram

For example, if a design requires a minimum gain of 20 dB using a few additional components, Equation 6 shows that applying a 47 Ω resistor to both the INPD and INMD pins (overriding the value of R_{IN}) sets a gain range of 20 dB to 100 dB (see Figure 41).

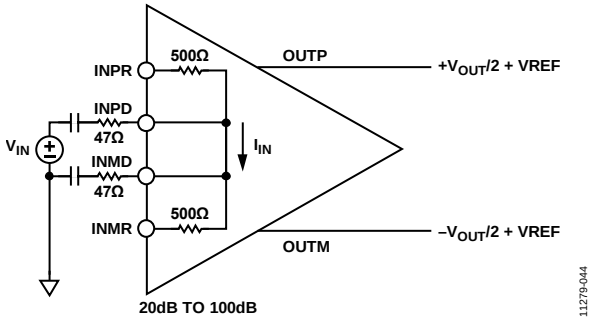

Figure 41. Using External Resistors at the INPD and INMD Pins

Similarly, if the user requires a minimum gain of −10 dB, applying a 1.5 kΩ resistor to both the INPD and INMD pins sets a gain range of −10 dB to +70 dB.

Effects of Using External Resistors

When the gain is modified through the use of external resistors, several trade-offs must be considered. For example, with the application of 47 Ω resistors at the inputs, the input noise decreases to approximately 1.5 nV/√Hz, less than the 4.5 nV/√Hz obtained when using the internal 500 Ω resistors. However, the −3 dB bandwidth is reduced from 18 MHz to approximately 3 MHz.

AGC CIRCUIT

The automatic gain control (AGC) circuit compares the rms output of the part with the desired rms output at the VAGC pin. Based on this comparison, the DETO pin either sources or sinks current. By connecting the DETO and GAIN pins together and by connecting the MODE pin to ground, the AGC circuit can be used to keep the output rms voltage constant.

To ensure that the AGC circuit reacts fast enough to adjust the gain, but slow enough to allow signals through, place a capacitor from DETO to ground. For example, in an on-off keying (OOK) application with a carrier frequency of 6.795 MHz and a bit rate of 10 kb/sec, a capacitor value of 0.01 μF is recommended. This value ensures that the gain reacts to the bit energy but does not react to the carrier signal.

To set the target rms output voltage, apply a voltage to VAGC. The target output voltage is lowest when VAGC is set to 1.5 V and increases when the applied voltage diverges from the 1.5 V reference voltage. To enable an increasing voltage at the VAGC pin to increase the rms output voltage, use Equation 7.

$$V_{ORMS} = 1.7 \times VAGC - 2.264 \quad (7)$$

To enable a decreasing voltage at the VAGC pin to increase the rms output voltage, use Equation 8.

$$V_{ORMS} = -1.7 \times VAGC + 2.864 \quad (8)$$

If the AGC feature is not used, tie the DETO pin to COMM.

ADJUSTING THE OUTPUT COMMON-MODE VOLTAGE

As with any differential output, the output of the AD8338 is a differential voltage that is centered about a common-mode voltage. The output common-mode voltage (V_{OCM}) of the AD8338 is nominally set to 1.5 V using an internal reference (see Figure 42).

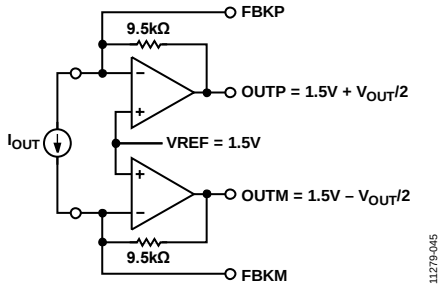

Figure 42. Output Common-Mode Voltage Set to 1.5 V (Default Setting)

The output common-mode voltage of the AD8338 can be adjusted to directly drive ADCs with various input common-mode requirements. To adjust the output common-mode voltage, add a resistor from each feedback node (FBKP and FBKM) to either COMM or VBAT. Adding a resistor from each feedback node to VBAT decreases the output common-mode voltage; adding a resistor from each feedback node to COMM increases the output common-mode voltage (see Figure 43 and Figure 44).

Table 5 and Table 6 provide examples of resistor values for decreasing or increasing the output common-mode voltage.

Table 5. Resistor Values for Decreasing the Output Common-Mode Voltage (Resistor Tied to VBAT)

VBAT (V)	Target V_{OCM} (V)	Resistor Value (Ω)	Tied to
5.0	0.9	55,417	VBAT
3.3	0.9	28,500	VBAT
3.0	0.9	23,750	VBAT

Table 6. Resistor Values for Increasing the Output Common-Mode Voltage (Resistor Tied to COMM)

VBAT (V)	Target V_{OCM} (V)	Resistor Value (Ω)	Tied to
Any	1.8	47,500	COMM
Any	2.0	28,500	COMM
Any	2.5	14,250	COMM

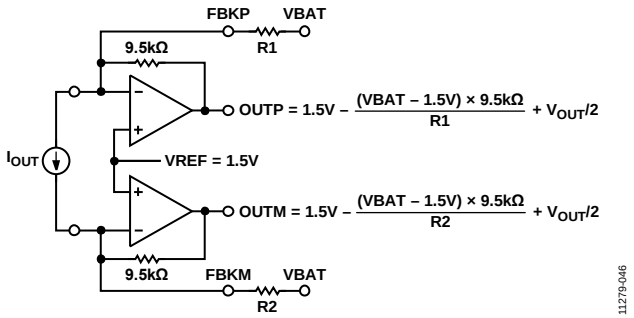

Figure 43. Decreasing the Output Common-Mode Voltage (Resistors Connected Between the FBKP and FBKM Pins to the VBAT Pin)

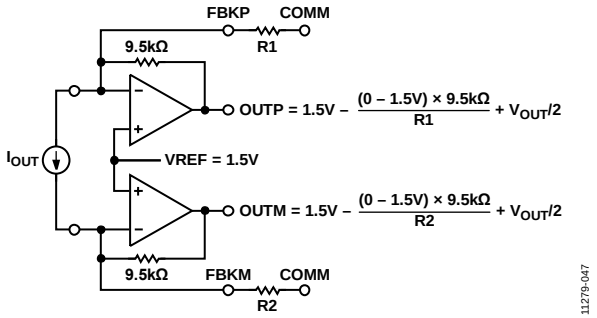

Figure 44. Increasing the Output Common-Mode Voltage (Resistors Connected Between the FBKP and FBKM Pins to the COMM Pin)

The AD8338 uses its internal reference for all signal processing. Therefore, although the output common-mode voltage can be changed through the application of external resistors, the VREF signal cannot be changed. For applications that require dc coupling to an ADC, a differential amplifier must be used.

APPLICATIONS INFORMATION

The excellent performance of the AD8338 results in a flat response over various gains with rail-to-rail output signal swing, high drive capability, and a very high dynamic range at a low 12 mW. These features make the AD8338 an exceptional choice for use in battery-operated equipment, low frequency and baseband applications, and many other applications.

SIMPLE ON-OFF KEYED (OOK) RECEIVER

For low complexity, low power data communications, a simple link built using a modulating carrier tone in an on/off state provides a fast and cost-effective solution to the designer. Such designs are used in a variety of applications, including near-field communications among noninterference mechanical systems, low data rate sensors, RFID tags, and so on.

The schematic shown in Figure 45 demonstrates a complete inductive telemetry on-off keyed (OOK) front end. The crystal is cut for the target receive frequency of interest, creating a very narrow-band filter, typically around the 6.78 MHz ISM band.

The AD8338 amplifies the signal (the gain is set by an external controller) and drives a full-wave rectifier bridge. The output of this bridge is then low-pass filtered into 100 Ω terminations. This design provides excellent rejection of RF and excellent baseband information recovery for the decision stage that follows.

The reactive filter components—Capacitors C1 through C4 and Inductors L1 and L2—set the baseband recovery performance. A design trade-off exchanges baseband response for RF attenuation.

Table 7 provides typical values for these components at two data rates. Note that Capacitors C1 through C4 are all of equal value, and Inductor L2 has the same value as L1.

Table 7. Typical Values for Components in Reactive Filter

Data Rate	C1 to C4	L1 and L2	Carrier Attenuation, f = 6.78 MHz
19,200 bps	12 nF	240 µH	−101 dB
57,600 bps	3.9 nF	82 µH	−73 dB

INTERFACING THE AD8338 TO AN ADC

The AD8338 is well suited to drive a high speed analog-to-digital converter (ADC) and is compatible with many ADCs from Analog Devices, Inc. This example illustrates the interfacing of the AD8338 to the AD7451. The AD7451 is a low power, 3.0 V ADC, which is also competitively priced for a low cost total solution.

Figure 46 shows the basic connections between the AD8338 and the AD7451. The common-mode voltage provided by the AD8338 is within the specifications of the AD7451.

The AD8338 can be coupled directly to the AD7451 for full dc-to-18 MHz operation at the highest level of performance with low operating power (160 mW typical). The glueless interface enables a physically small, high performance data acquisition system that is ideal for many field instruments. A filter before the VGA provides the antialiasing function and noise limiting.

In applications where the modulated information is not encoded in the signal amplitude, use the AGC feature of the AD8338 to reduce any bit errors in the sampled signal.

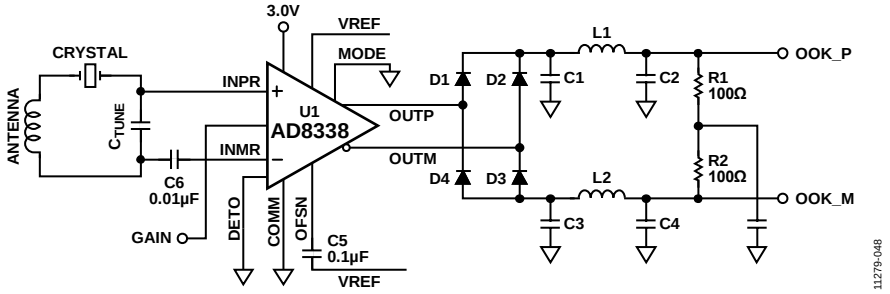

Figure 45. Complete, Low Power OOK Receiver

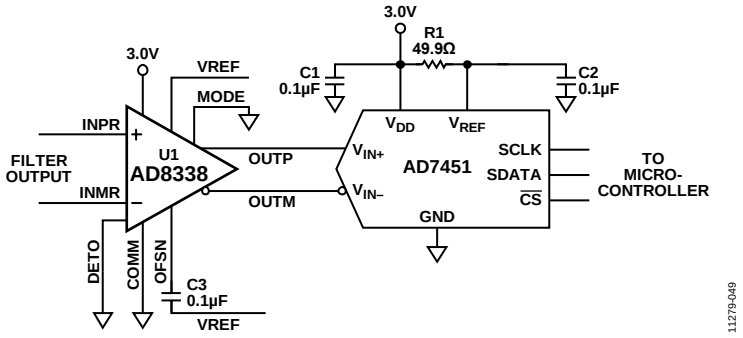

Figure 46. Basic Connections to the AD7451 ADC

OUTLINE DIMENSIONS

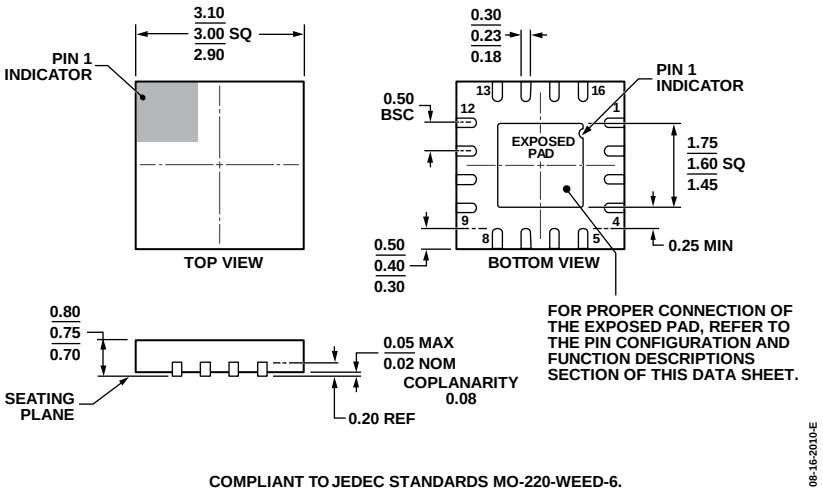

Figure 47. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
3 mm × 3 mm Body, Very Very Thin Quad
(CP-16-22)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD8338ACPZ-R7	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-22	Y4K
AD8338ACPZ-RL	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-22	Y4K

[1] Z = RoHS Compliant Part.

D11279-0-4/13(0)