

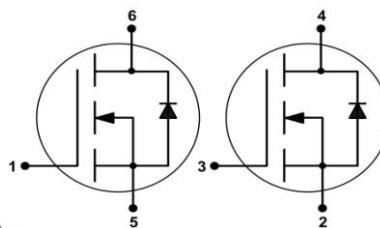
## OptiMOS™ 2 Small-Signal-Transistor

### Features

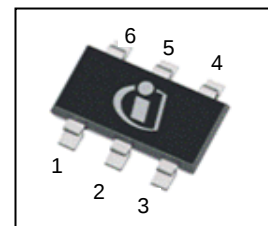
- Dual N-channel
- Enhancement mode
- Ultra Logic level (1.8V rated)
- Avalanche rated
- Qualified according to AEC Q101
- 100% lead-free; RoHS compliant
- Halogen free according to IEC61249-2-21



Halogen-Free



PG-TSOP6



| Type    | Package  | Tape and Reel Information | Marking | Lead Free | Packing |
|---------|----------|---------------------------|---------|-----------|---------|
| BSL806N | PG-TSOP6 | H6327: 3000 pcs/ reel     | sPO     | Yes       | Non dry |

Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified

| Parameter <sup>(1)</sup>            | Symbol            | Conditions                                                                                                     | Value       | Unit              |
|-------------------------------------|-------------------|----------------------------------------------------------------------------------------------------------------|-------------|-------------------|
| Continuous drain current            | $I_D$             | $T_A=25\text{ °C}$                                                                                             | 2.3         | A                 |
|                                     |                   | $T_A=70\text{ °C}$                                                                                             | 1.9         |                   |
| Pulsed drain current                | $I_{D,pulse}$     | $T_A=25\text{ °C}$                                                                                             | 9.3         |                   |
| Avalanche energy, single pulse      | $E_{AS}$          | $I_D=2.3\text{ A}$ , $R_{GS}=25\text{ }\Omega$                                                                 | 10.8        | mJ                |
| Reverse diode $dv/dt$               | $dv/dt$           | $I_D=2.3\text{ A}$ , $V_{DS}=16\text{ V}$ ,<br>$di/dt=200\text{ A}/\mu\text{s}$ ,<br>$T_{j,max}=150\text{ °C}$ | 6           | kV/ $\mu\text{s}$ |
| Gate source voltage                 | $V_{GS}$          |                                                                                                                | $\pm 8$     | V                 |
| Power dissipation <sup>1)</sup>     | $P_{tot}$         | $T_A=25\text{ °C}$                                                                                             | 0.5         | W                 |
| Operating and storage temperature   | $T_j$ , $T_{stg}$ |                                                                                                                | -55 ... 150 | °C                |
| ESD Class                           |                   | JESD22-A114 -HBM                                                                                               | 0 (<250V)   |                   |
| Soldering Temperature               |                   |                                                                                                                | 260 °C      |                   |
| IEC climatic category; DIN IEC 68-1 |                   |                                                                                                                | 55/150/56   |                   |

<sup>1)</sup> Remark: one of both transistors active

| Parameter | Symbol | Conditions | Values |      |      | Unit |
|-----------|--------|------------|--------|------|------|------|
|           |        |            | min.   | typ. | max. |      |

**Thermal characteristics**

|                                           |            |                                 |   |   |     |     |
|-------------------------------------------|------------|---------------------------------|---|---|-----|-----|
| Thermal resistance,<br>junction - ambient | $R_{thJA}$ | minimal footprint <sup>2)</sup> | - | - | 250 | K/W |
|-------------------------------------------|------------|---------------------------------|---|---|-----|-----|

**Electrical characteristics, at  $T_j=25\text{ °C}$ , unless otherwise specified**
**Static characteristics**

|                                  |               |                                                            |     |      |      |                  |
|----------------------------------|---------------|------------------------------------------------------------|-----|------|------|------------------|
| Drain-source breakdown voltage   | $V_{(BR)DSS}$ | $V_{GS}=0\text{ V}, I_D=250\text{ }\mu\text{A}$            | 20  | -    | -    | V                |
| Gate threshold voltage           | $V_{GS(th)}$  | $V_{DS}=V_{GS}, I_D=11\text{ }\mu\text{A}$                 | 0.3 | 0.55 | 0.75 |                  |
| Drain-source leakage current     | $I_{DSS}$     | $V_{DS}=20\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$  | -   | -    | 1    | $\mu\text{A}$    |
|                                  |               | $V_{DS}=20\text{ V}, V_{GS}=0\text{ V}, T_j=150\text{ °C}$ | -   | -    | 100  |                  |
| Gate-source leakage current      | $I_{GSS}$     | $V_{GS}=8\text{ V}, V_{DS}=0\text{ V}$                     | -   | -    | 100  | nA               |
| Drain-source on-state resistance | $R_{DS(on)}$  | $V_{GS}=1.8\text{ V}, I_D=1.3\text{ A}$                    | -   | 55   | 82   | $\text{m}\Omega$ |
|                                  |               | $V_{GS}=2.5\text{ V}, I_D=2.3\text{ A}$                    | -   | 40   | 57   |                  |
| Transconductance                 | $g_{fs}$      | $ V_{DS} >2 I_D R_{DS(on)max}, I_D=1.9\text{ A}$           |     | 9    | -    | S                |

<sup>2)</sup> Performed on 40mm<sup>2</sup> FR4 PCB. The traces are 1mm wide, 70 $\mu\text{m}$  thick and 20mm long; they are present on both sides of the PCB.

| Parameter | Symbol | Conditions | Values |      |      | Unit |
|-----------|--------|------------|--------|------|------|------|
|           |        |            | min.   | typ. | max. |      |

#### Dynamic characteristics

|                              |              |                                                                                       |   |     |      |    |
|------------------------------|--------------|---------------------------------------------------------------------------------------|---|-----|------|----|
| Input capacitance            | $C_{iss}$    | $V_{GS}=0\text{ V}, V_{DS}=10\text{ V},$<br>$f=1\text{ MHz}$                          | - | 370 | 259  | pF |
| Output capacitance           | $C_{oss}$    |                                                                                       | - | 118 | 169  |    |
| Reverse transfer capacitance | $C_{rss}$    |                                                                                       | - | 20  | 28.6 |    |
| Turn-on delay time           | $t_{d(on)}$  | $V_{DD}=10\text{ V}, V_{GS}=2.5\text{ V},$<br>$I_D=2.3\text{ A}, R_{G,ext}=6\ \Omega$ | - | 7.5 | -    | ns |
| Rise time                    | $t_r$        |                                                                                       | - | 9.9 | -    |    |
| Turn-off delay time          | $t_{d(off)}$ |                                                                                       | - | 12  | -    |    |
| Fall time                    | $t_f$        |                                                                                       | - | 3.7 | -    |    |

#### Gate Charge Characteristics

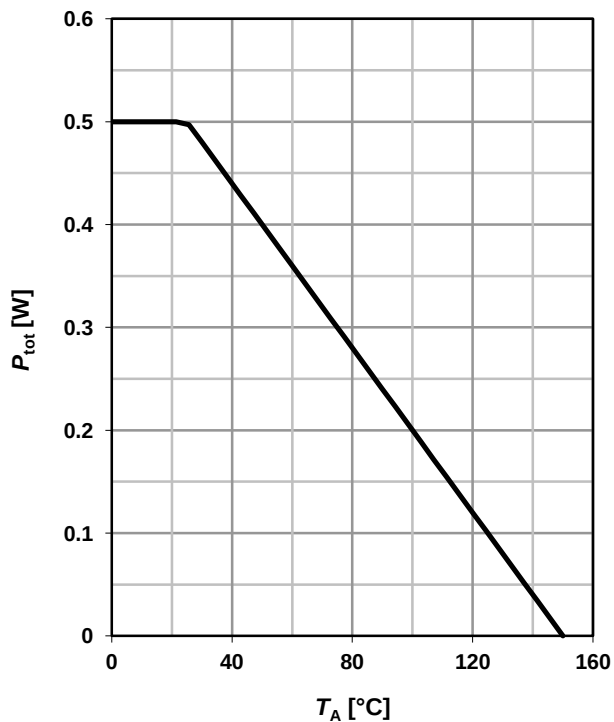
|                       |               |                                                                              |   |      |   |    |
|-----------------------|---------------|------------------------------------------------------------------------------|---|------|---|----|
| Gate to source charge | $Q_{gs}$      | $V_{DD}=10\text{ V}, I_D=2.3\text{ A},$<br>$V_{GS}=0\text{ to }2.5\text{ V}$ | - | 0.55 | - | nC |
| Gate to drain charge  | $Q_{gd}$      |                                                                              | - | 0.58 | - |    |
| Gate charge total     | $Q_g$         |                                                                              | - | 1.7  | - |    |
| Gate plateau voltage  | $V_{plateau}$ |                                                                              | - | 1.5  | - | V  |

#### Reverse Diode

|                                  |               |                                                                            |   |      |     |    |
|----------------------------------|---------------|----------------------------------------------------------------------------|---|------|-----|----|
| Diode continuous forward current | $I_S$         | $T_A=25\text{ °C}$                                                         | - | -    | 0.5 | A  |
| Diode pulse current              | $I_{S,pulse}$ |                                                                            | - | -    | 9.3 |    |
| Diode forward voltage            | $V_{SD}$      | $V_{GS}=0\text{ V}, I_F=2.3\text{ A},$<br>$T_j=25\text{ °C}$               | - | 0.82 | 1.1 | V  |
| Reverse recovery time            | $t_{rr}$      | $V_R=10\text{ V}, I_F=2.3\text{ A},$<br>$di_F/dt=100\text{ A}/\mu\text{s}$ | - | 11   | -   | ns |
| Reverse recovery charge          | $Q_{rr}$      |                                                                            | - | 3.3  | -   | nC |

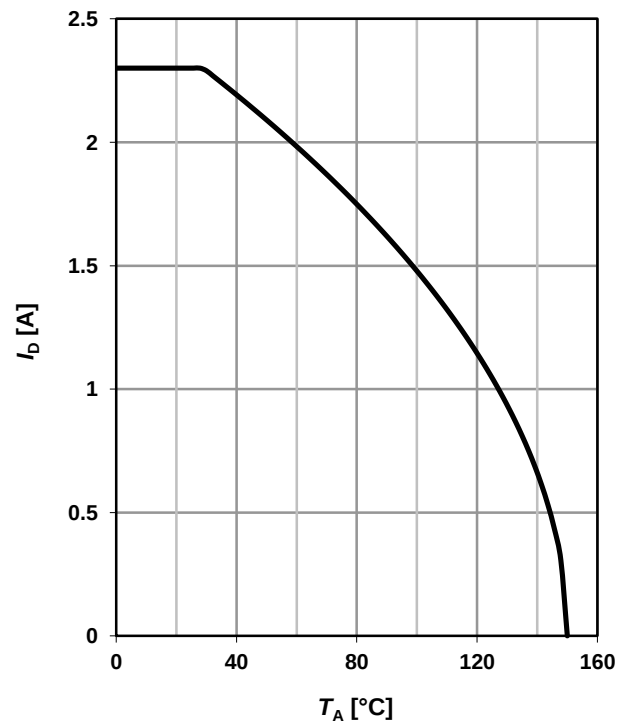
## 1 Power dissipation

$$P_{\text{tot}} = f(T_A)$$



## 2 Drain current

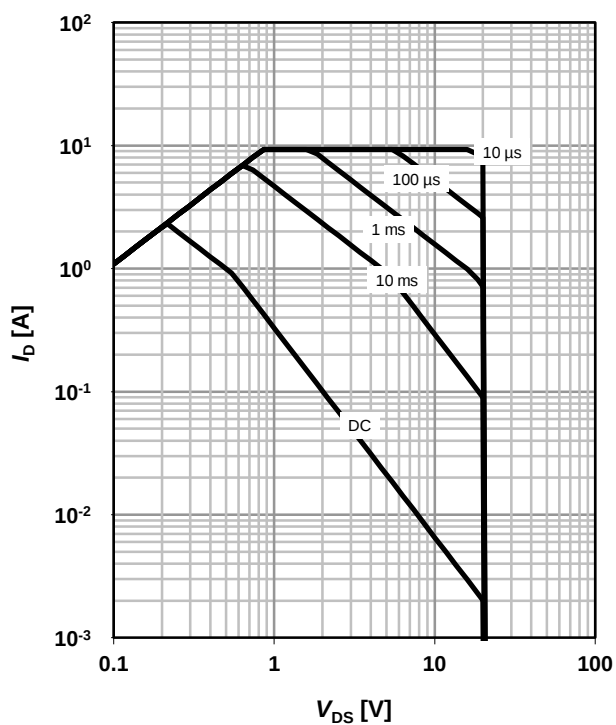
$$I_D = f(T_A); V_{GS} \geq 2.5 \text{ V}$$



## 3 Safe operating area

$$I_D = f(V_{DS}); T_A = 25 \text{ °C}; D = 0$$

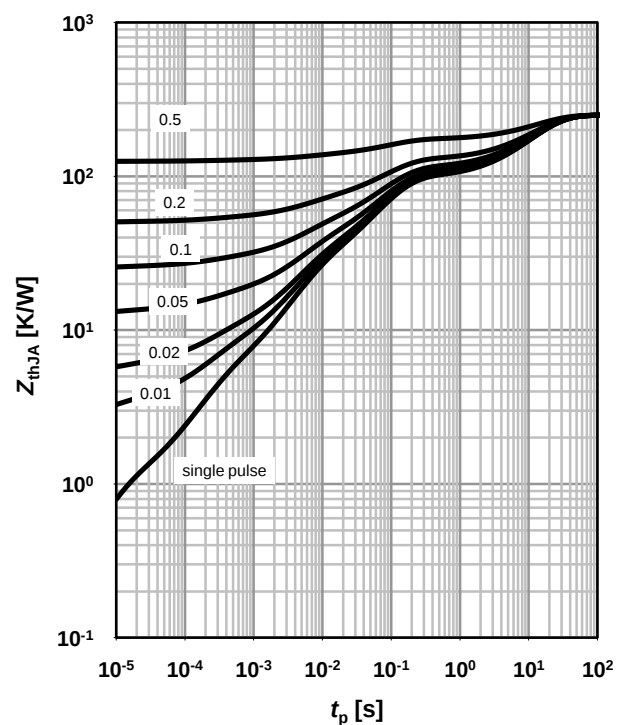
parameter:  $t_p$



## 4 Max. transient thermal impedance

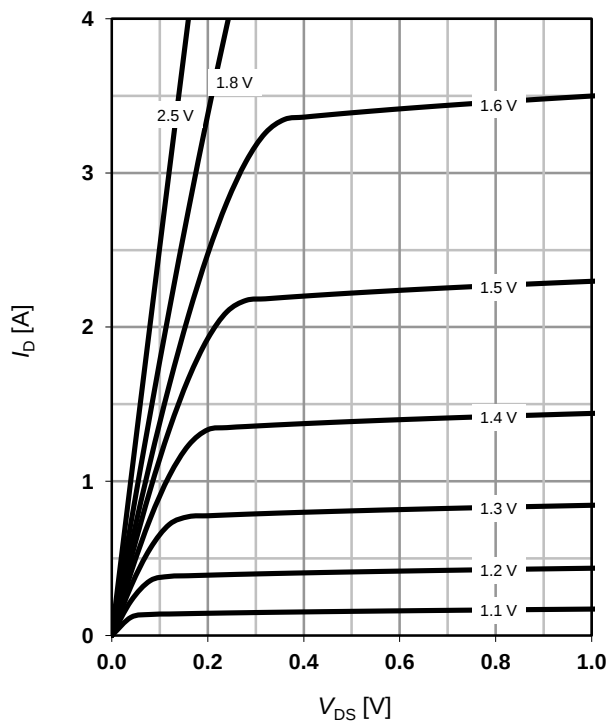
$$Z_{thJA} = f(t_p)$$

parameter:  $D = t_p/T$



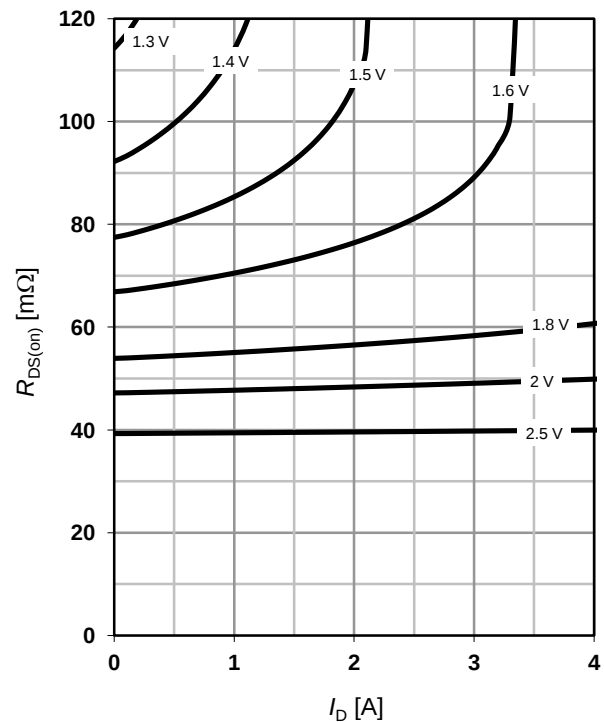
### 5 Typ. output characteristics

 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}$ 

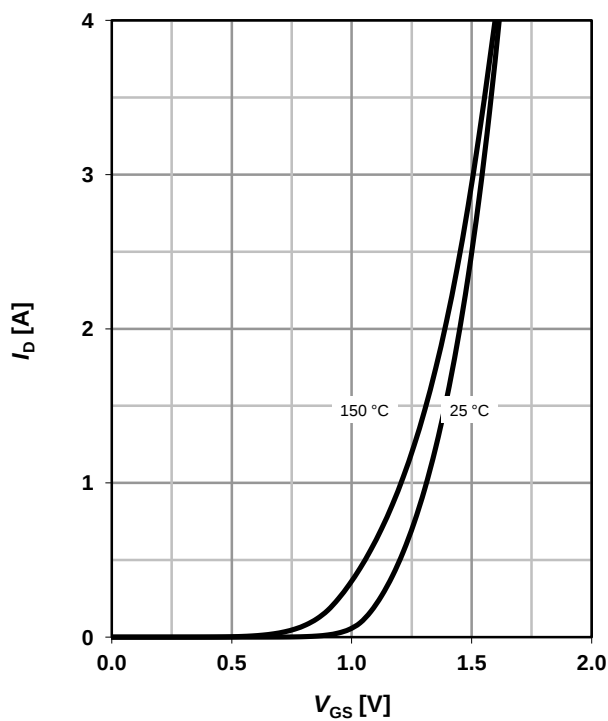
parameter:  $V_{GS}$ 


### 6 Typ. drain-source on resistance

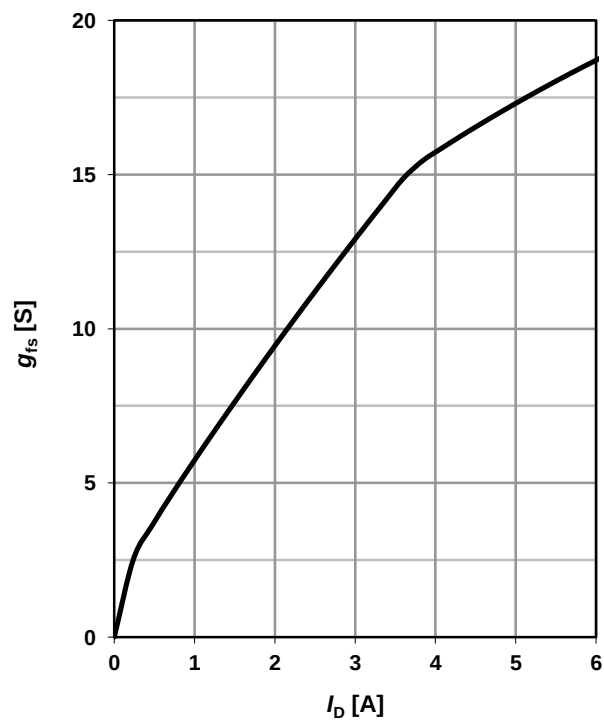
 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$ 

parameter:  $V_{GS}$ 


### 7 Typ. transfer characteristics

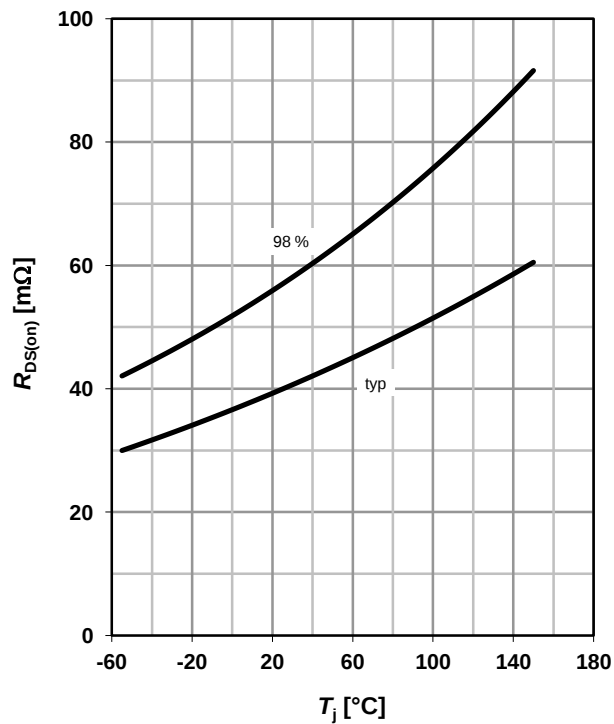
 $I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$ 


### 8 Typ. forward transconductance

 $g_{fs} = f(I_D); T_j = 25^\circ\text{C}$ 


## 9 Drain-source on-state resistance

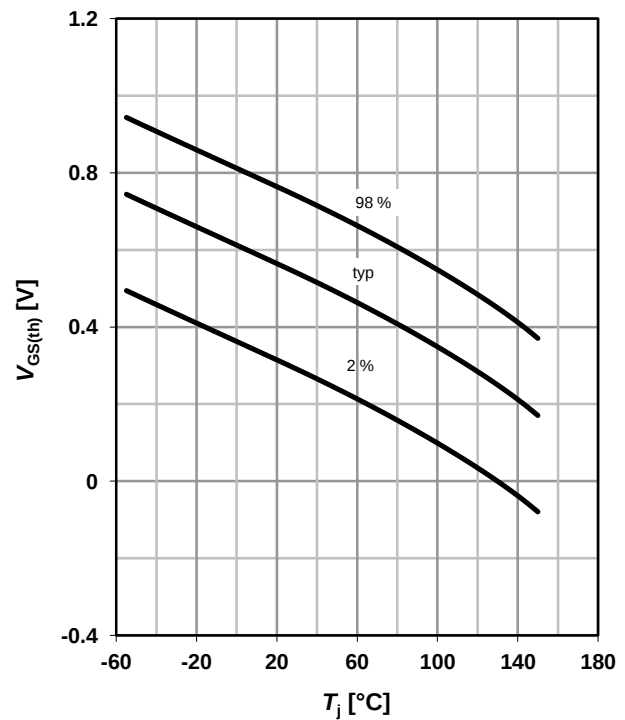
$$R_{DS(on)} = f(T_j); I_D = 2.3 \text{ A}; V_{GS} = 2.5 \text{ V}$$



## 10 Typ. gate threshold voltage

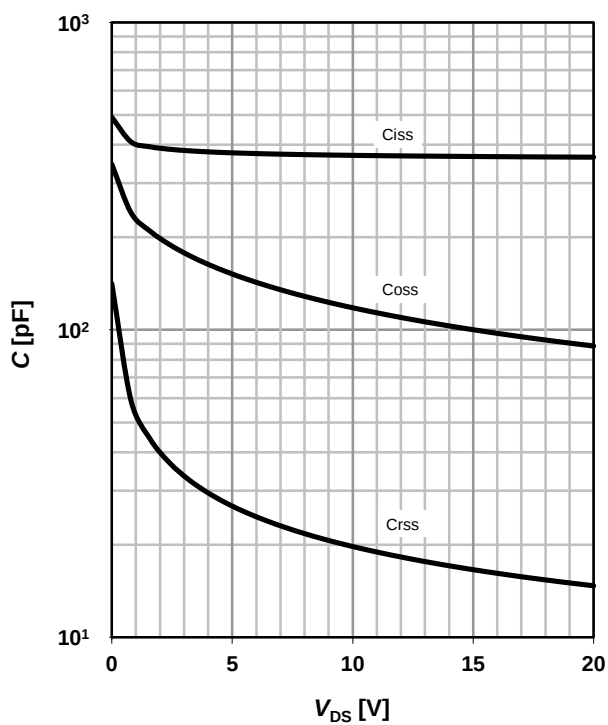
$$V_{GS(th)} = f(T_j); V_{DS} = V_{GS}; I_D = 11 \mu\text{A}$$

parameter:  $I_D$



## 11 Typ. capacitances

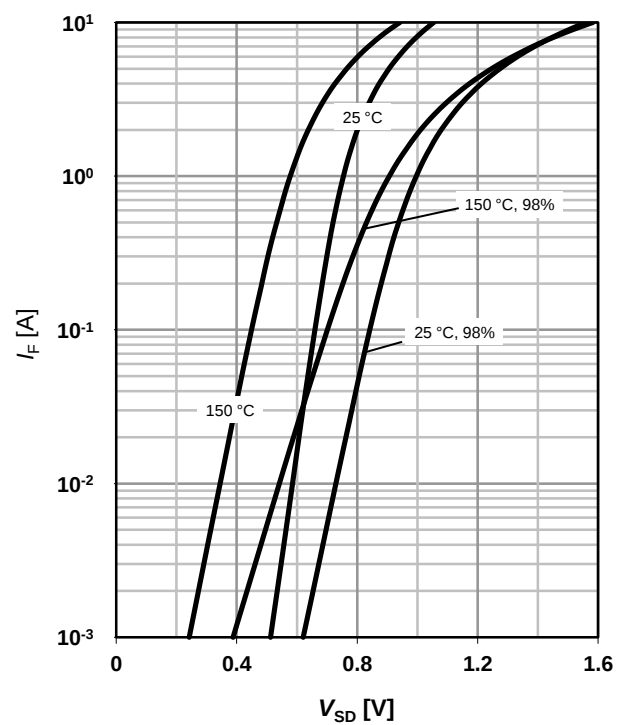
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25^\circ\text{C}$$



## 12 Forward characteristics of reverse diode

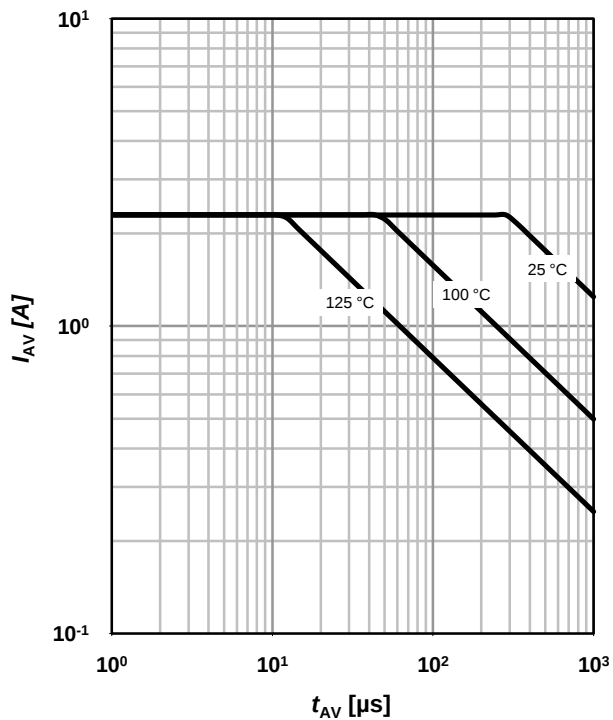
$$I_F = f(V_{SD})$$

parameter:  $T_j$



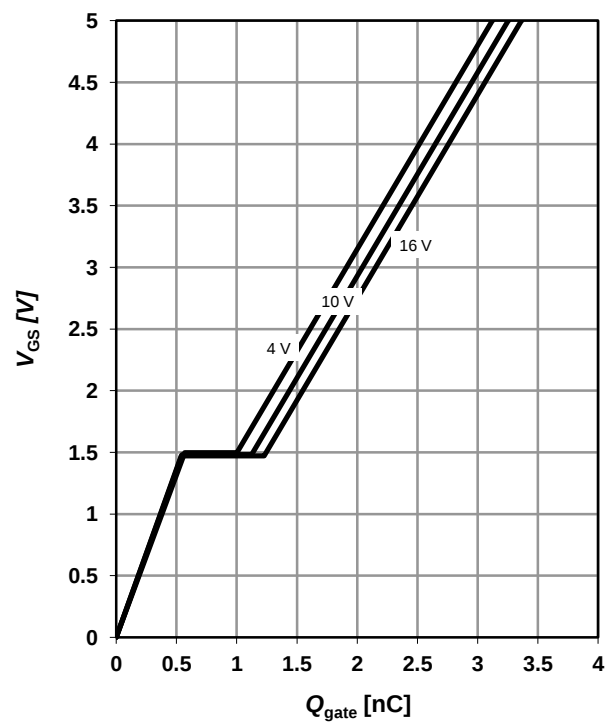
### 13 Avalanche characteristics

 $I_{AS}=f(t_{AV}); R_{GS}=25\ \Omega$ 

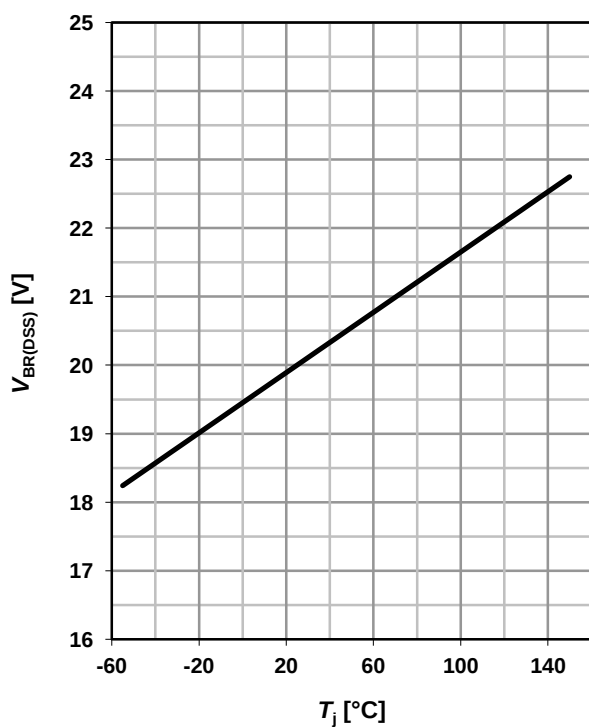
parameter:  $T_{j(\text{start})}$ 


### 14 Typ. gate charge

 $V_{GS}=f(Q_{\text{gate}}); I_D=2.3\ \text{A pulsed}$ 

parameter:  $V_{DD}$ 


### 15 Drain-source breakdown voltage

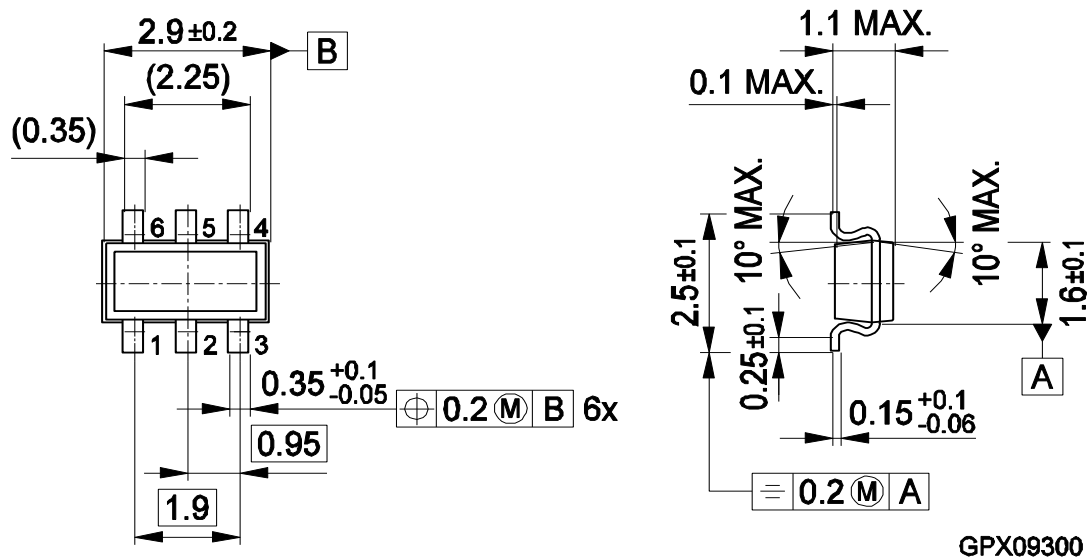
 $V_{BR(DSS)}=f(T_j); I_D=250\ \mu\text{A}$ 


### 16 Gate charge waveforms

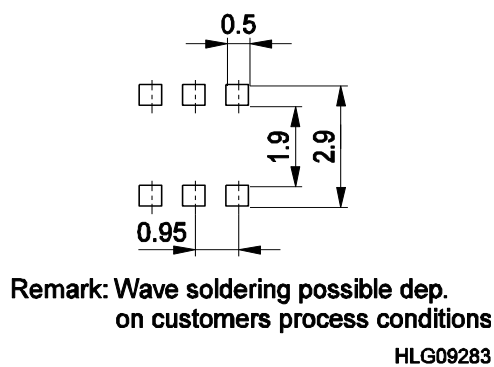


# TSOP6

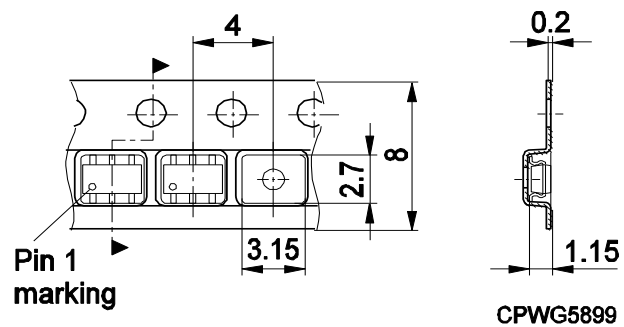
## Package Outline:



## Footprint:



## Packaging:



Dimensions in mm

**Published by**  
**Infineon Technologies AG**  
**81726 Munich, Germany**  
**© 2008 Infineon Technologies AG**  
**All Rights Reserved.**

**Legal Disclaimer**

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

**Information**

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office ([www.infineon.com](http://www.infineon.com)).

**Warnings**

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.