

**64Kx16 LOW VOLTAGE,
ULTRA LOW POWER CMOS STATIC RAM**

JUNE 2018

KEY FEATURES

- High-speed access time: 45ns, 55ns
- CMOS low power operation
 - Operating Current: 26 mA (max) at 125°C
 - CMOS Standby Current: 3 uA (typ) at 25°C
- TTL compatible interface levels
- Single power supply
 - 1.65V-2.2V V_{DD} (IS62/65WV6416FALL)
 - 2.2V-3.6V V_{DD} (IS62/65WV6416FBLL)
- Three state outputs
- Data Control for upper and lower bytes
- Industrial and Automotive temperature support
- 2CS Option Available
- Lead-free available

DESCRIPTION

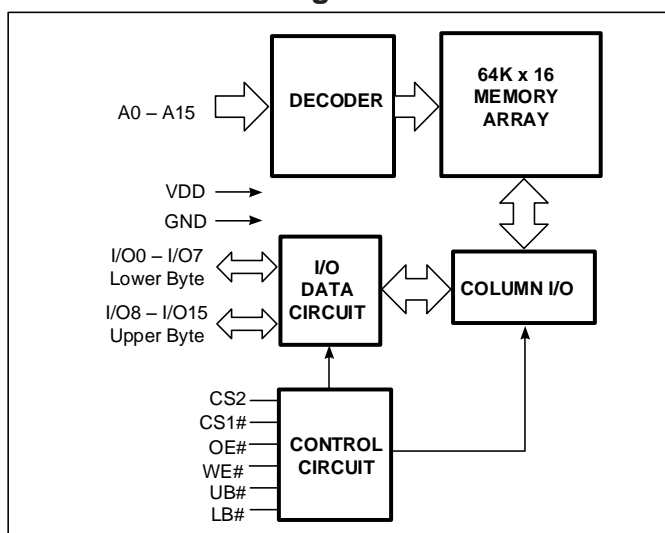
The *ISSI* IS62/65WV6416FALL/BLL are high-speed, 1M bit static RAMs organized as 64K words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When CS1# is HIGH (deselected) or when CS2 is LOW (deselected) or when CS1# is LOW, CS2 is HIGH and both LB# and UB# are HIGH, the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable (WE#) controls both writing and reading of the memory. A data byte allows Upper Byte (UB#) and Lower Byte (LB#) access.

The IS62/65WV6416FALL/BLL are packaged in the JEDEC standard 48-pin mini BGA (6mm x 8mm) and 44-Pin TSOP (TYPE II)

Functional Block Diagram



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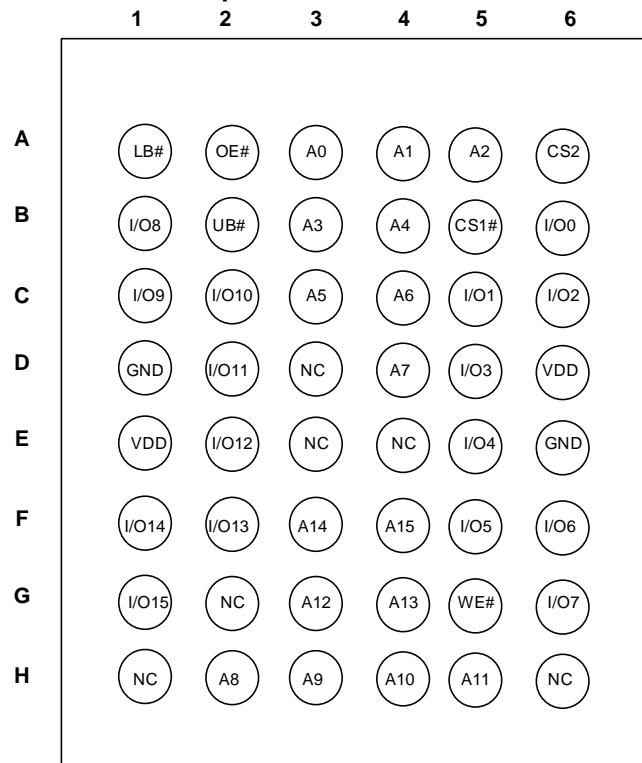
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PIN CONFIGURATIONS

48-Pin mini BGA (6mm x 8mm)



48-Pin mini BGA (6mm x 8mm)
2 CS Option



PIN DESCRIPTIONS

| | |
|------------|------------------------------------|
| A0-A15 | Address Inputs |
| I/O0-I/O15 | Data Inputs/Outputs |
| CS1#, CS2 | Chip Enable Input(2 CS) |
| CS# | Chip Enable Input(1 CS) |
| OE# | Output Enable Input |
| WE# | Write Enable Input |
| LB# | Lower-byte Control (I/O0-I/O7) |
| UB# | Upper-byte Control (I/O8-I/O15) |
| NC | No Connection |
| VDD | Power |
| GND | Ground |

44-Pin mini TSOP (Type II)



FUNCTION DESCRIPTION

SRAM is one of random access memories. Each byte or word has an address and can be accessed randomly. SRAM has three different modes supported. Each function is described below with Truth Table. Below description is based on the device with 2 CS pins.

STANDBY MODE

Device enters standby mode when deselected (CS1# HIGH or CS2 LOW or both UB# and LB# are HIGH). The input and output pins (I/O0-15) are placed in a high impedance state. The current consumption in this mode will be ISB1 or ISB2. CMOS input in this mode will maximize saving power.

WRITE MODE

Write operation issues with Chip selected (CS1# LOW and CS2 HIGH) and Write Enable (WE#) input LOW. The input and output pins (I/O0-15) are in data input mode. Output buffers are closed during this time even if OE# is LOW. UB# and LB# enables a byte write feature. By enabling LB# LOW, data from I/O pins (I/O0 through I/O7) are written into the location specified on the address pins. And with UB# being LOW, data from I/O pins (I/O8 through I/O15) are written into the location.

READ MODE

Read operation issues with Chip selected (CS1# LOW and CS2 HIGH) and Write Enable (WE#) input HIGH. When OE# is LOW, output buffer turns on to make data output. Any input to I/O pins during READ mode is not permitted. UB# and LB# enables a byte read feature. By enabling LB# LOW, data from memory appears on I/O0-7. And with UB# being LOW, data from memory appears on I/O8-15.

In the READ mode, output buffers can be turned off by pulling OE# HIGH. In this mode, internal device operates as READ but I/Os are in a high impedance state. Since device is in READ mode, active current is used.

TRUTH TABLE

| Mode | CS1# | CS2 | WE# | OE# | LB# | UB# | I/O0-I/O7 | I/O8-I/O15 | VDD Current |
|-----------------|------|-----|-----|-----|-----|-----|-----------|------------|-------------|
| Not Selected | H | X | X | X | X | X | High-Z | High-Z | ISB2 |
| | X | L | X | X | X | X | High-Z | High-Z | |
| | X | X | X | X | H | H | High-Z | High-Z | |
| Output Disabled | L | H | H | H | L | X | High-Z | High-Z | ICC |
| | L | H | H | H | X | L | High-Z | High-Z | |
| Read | L | H | H | L | L | H | DOUT | High-Z | ICC |
| | L | H | H | L | H | L | High-Z | DOUT | |
| | L | H | H | L | L | L | DOUT | DOUT | |
| Write | L | H | L | X | L | H | DIN | High-Z | ICC |
| | L | H | L | X | H | L | High-Z | DIN | |
| | L | H | L | X | L | L | DIN | DIN | |

Note:

1. Truth table for the device with 1 CS pin is the same with the above table without CS2 column.

ABSOLUTE MAXIMUM RATINGS AND OPERATING RANGE

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

| Symbol | Parameter | Value | Unit |
|---------------------------------|--------------------------------------|--------------------------------------|------|
| V _{term} | Terminal Voltage with Respect to GND | -0.2 to +3.9 (V _{DD} +0.3V) | V |
| tBIAS | Temperature Under Bias | -55 to +125 | °C |
| V _{DD} | V _{DD} Related to GND | -0.2 to +3.9 (V _{DD} +0.3V) | V |
| tStg | Storage Temperature | -65 to +150 | °C |
| I _{OUT} ⁽²⁾ | DC Output Current (LOW) | 20 | mA |

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This condition is not per pin. Total current of all pins must meet this value.

OPERATING RANGE ⁽¹⁾

| Range | Ambient Temperature | Device Marking | V _{DD} |
|------------|---------------------|----------------|-----------------|
| Commercial | 0°C to +70°C | IS62WV6416FALL | 1.65V-2.2V |
| Industrial | -40°C to +85°C | IS62WV6416FALL | 1.65V-2.2V |
| Commercial | 0°C to +70°C | IS62WV6416FBLL | 2.2V-3.6V |
| Industrial | -40°C to +85°C | IS62WV6416FBLL | 2.2V-3.6V |
| Automotive | -40°C to +125°C | IS65WV6416FBLL | 2.2V-3.6V |

Note:

1. Full device AC operation assumes a 100 μs ramp time from 0 to V_{DD}(min) and 200 μs wait time after V_{DD} stabilization.

PIN CAPACITANCE ⁽¹⁾

| Parameter | Symbol | Test Condition | Max | Units |
|---------------------------|------------------|---|-----|-------|
| Input capacitance | C _{IN} | T _A = 25°C, f = 1 MHz, V _{DD} = V _{DD} (typ) | 10 | pF |
| DQ capacitance (IO0–IO15) | C _{I/O} | | 10 | pF |

Note:

1. These parameters are guaranteed by design and tested by a sample basis only.

THERMAL CHARACTERISTICS ⁽¹⁾

| Parameter | Symbol | Rating | Units |
|--|------------------|--------|-------|
| Thermal resistance from junction to ambient (airflow = 1m/s) | R _{θJA} | TBD | °C/W |
| Thermal resistance from junction to pins | R _{θJB} | TBD | °C/W |
| Thermal resistance from junction to case | R _{θJC} | TBD | °C/W |

Note:

1. These parameters are guaranteed by design and tested by a sample basis only.

ELECTRICAL CHARACTERISTICS

IS62WV6416FALL DC ELECTRICAL CHARACTERISTICS-I (OVER THE OPERATING RANGE)

VDD=1.65V~2.2V

| Symbol | Parameter | Test Conditions | Min | Max | Unit |
|----------------------------------|---------------------|---|------|-----------------------|------|
| V _{OH} | Output HIGH Voltage | I _{OH} = -0.1 mA | 1.4 | — | V |
| V _{OL} | Output LOW Voltage | I _{OL} = 0.1 mA | — | 0.2 | V |
| V _{IH} (¹) | Input HIGH Voltage | | 1.4 | V _{DD} + 0.2 | V |
| V _{IL} (¹) | Input LOW Voltage | | -0.2 | 0.4 | V |
| I _{LI} | Input Leakage | GND < V _{IN} < V _{DD} | -1 | 1 | μA |
| I _{LO} | Output Leakage | GND < V _{IN} < V _{DD} , Output Disabled | -1 | 1 | μA |

Notes:

- V_{ILL}(min) = -1.0V AC (pulse width < 10ns). Not 100% tested.
V_{IHH}(max) = V_{DD} + 1.0V AC (pulse width < 10ns). Not 100% tested.

IS62 (5) WV6416FBLL DC ELECTRICAL CHARACTERISTICS-I (OVER THE OPERATING RANGE)

VDD=2.2V~3.6V

| Symbol | Parameter | Test Conditions | Min | Max | Unit |
|----------------------------------|---------------------|---|------|-----------------------|------|
| V _{OH} | Output HIGH Voltage | 2.2 ≤ V _{DD} < 2.7, I _{OH} = -0.1 mA | 2.0 | — | V |
| | | 2.7 ≤ V _{DD} ≤ 3.6, I _{OH} = -1.0 mA | 2.4 | — | V |
| V _{OL} | Output LOW Voltage | 2.2 ≤ V _{DD} < 2.7, I _{OL} = 0.1 mA | — | 0.4 | V |
| | | 2.7 ≤ V _{DD} ≤ 3.6, I _{OL} = 2.1 mA | — | 0.4 | V |
| V _{IH} (¹) | Input HIGH Voltage | 2.2 ≤ V _{DD} < 2.7 | 1.8 | V _{DD} + 0.3 | V |
| | | 2.7 ≤ V _{DD} ≤ 3.6 | 2.2 | V _{DD} + 0.3 | V |
| V _{IL} (¹) | Input LOW Voltage | 2.2 ≤ V _{DD} < 2.7 | -0.3 | 0.6 | V |
| | | 2.7 ≤ V _{DD} ≤ 3.6 | -0.3 | 0.8 | V |
| I _{LI} | Input Leakage | GND < V _{IN} < V _{DD} | -1 | 1 | μA |
| I _{LO} | Output Leakage | GND < V _{IN} < V _{DD} , Output Disabled | -1 | 1 | μA |

Note:

- V_{ILL}(min) = -2.0V AC (pulse width < 10ns). Not 100% tested.
V_{IHH}(max) = V_{DD} + 2.0V AC (pulse width < 10ns). Not 100% tested.

IS62WV6416FALL DC ELECTRICAL CHARACTERISTICS-II FOR POWER
(OVER THE OPERATING RANGE)

| Symbol | Parameter | Test Conditions ⁽²⁾ | Grade | Typ ⁽¹⁾ | Max | Unit | |
|--------|--|--|-------|--------------------|-----|------|----|
| ICC | V _{DD} Dynamic Operating Supply Current | V _{DD} = V _{DD(max)} , I _{OUT} = 0mA, f = f _{max} CS1# = V _{IL} , CS2 = V _{IH} | Com. | - | 26 | mA | |
| | | | Ind. | | 26 | | |
| ICC1 | V _{DD} Static Operating Supply Current | V _{DD} = V _{DD(max)} , I _{OUT} = 0mA, f = 0 CS1# = V _{IL} , CS2 = V _{IH} | Com. | - | 5 | mA | |
| | | | Ind. | | 5 | | |
| ISB2 | CMOS Standby Current (CMOS Inputs) | V _{DD} = V _{DD(max)} , f = 0 CS1# ≥ V _{DD} - 0.2V or CS2 ≤ 0.2V or LB# and UB# ≥ V _{DD} - 0.2V, VIN ≤ 0.2V or VIN ≥ V _{DD} - 0.2V | Com. | 25°C | 3.0 | - | μA |
| | | | | 45°C | 3.5 | - | |
| | | | | 70°C | 4.0 | 5 | |
| | | | Ind. | 85°C | 4.1 | 6 | |

Notes:

1. Typical values are measured at V_{DD} = 1.8V, and not 100% tested.
2. Test conditions are based on 2 CS option.

IS62 (65) WV6416FBLL DC ELECTRICAL CHARACTERISTICS-II FOR POWER
(OVER THE OPERATING RANGE)

| Symbol | Parameter | Test Conditions ⁽²⁾ | Grade | Typ ⁽¹⁾ | Max | Unit | |
|--------|--|--|-------|--------------------|-----|------|----|
| ICC | V _{DD} Dynamic Operating Supply Current | V _{DD} = V _{DD(max)} , I _{OUT} = 0mA, f = f _{max} CS1# = V _{IL} , CS2 = V _{IH} | Com. | - | 26 | mA | |
| | | | Ind. | | 26 | | |
| | | | Auto. | | 26 | | |
| ICC1 | V _{DD} Static Operating Supply Current | V _{DD} = V _{DD(max)} , I _{OUT} = 0mA, f = 0 CS1# = V _{IL} , CS2 = V _{IH} | Com. | - | 5 | mA | |
| | | | Ind. | | 5 | | |
| | | | Auto. | | 5 | | |
| ISB2 | CMOS Standby Current (CMOS Inputs) | V _{DD} = V _{DD(max)} , f = 0 CS1# ≥ V _{DD} - 0.2V or CS2 ≤ 0.2V or LB# and UB# ≥ V _{DD} - 0.2V, VIN ≤ 0.2V or VIN ≥ V _{DD} - 0.2V | Com. | 25°C | 3.0 | - | μA |
| | | | | 45°C | 3.5 | - | |
| | | | | 70°C | 4.0 | 5 | |
| | | | Ind. | 85°C | 4.1 | 6 | |
| | | | Auto. | 125°C | 9.0 | 18 | |

Notes:

1. Typical values are measured at V_{DD} = 3.0V, and not 100% tested.
2. Test conditions are based on 2 CS option

AC CHARACTERISTICS ⁽⁶⁾ (OVER OPERATING RANGE)

READ CYCLE AC CHARACTERISTICS

| Parameter | Symbol | 45ns | | 55ns | | unit | notes |
|----------------------------|--------------|------|-----|------|-----|------|-------|
| | | Min | Max | Min | Max | | |
| Read Cycle Time | tRC | 45 | - | 55 | - | ns | 1,5 |
| Address Access Time | tAA | - | 45 | - | 55 | ns | 1 |
| Output Hold Time | tOHA | 10 | - | 10 | - | ns | 1 |
| CS1#, CS2 Access Time | tACS1/tACS2 | - | 45 | - | 55 | ns | 1 |
| OE# Access Time | tDOE | - | 20 | - | 25 | ns | 1 |
| OE# to High-Z Output | tHZOE | - | 18 | - | 20 | ns | 2 |
| OE# to Low-Z Output | tLZOE | 5 | - | 5 | - | ns | 2 |
| CS1#, CS2 to High-Z Output | tHZCS/tHZCS2 | - | 18 | - | 18 | ns | 2 |
| CS1#, CS2 to Low-Z Output | tLZCS/tLZCS2 | 10 | - | 10 | - | ns | 2 |
| UB#, LB# Access Time | tBA | 45 | - | 55 | - | ns | 1,7 |
| UB#, LB# to High-Z Output | tHZB | - | 18 | - | 20 | ns | 2 |
| UB#, LB# to Low-Z Output | tLZB | 10 | - | 10 | - | ns | 2 |

WRITE CYCLE AC CHARACTERISTICS

| Parameter | Symbol | 45ns | | 55ns | | unit | notes |
|---------------------------------|-------------|------|-----|------|-----|------|-------|
| | | Min | Max | Min | Max | | |
| Write Cycle Time | tWC | 45 | - | 55 | - | ns | 1,3,5 |
| CS1#, CS2 to Write End | tSCS1/tSCS2 | 35 | - | 40 | - | ns | 1,3 |
| Address Setup Time to Write End | tAW | 35 | - | 40 | - | ns | 1,3 |
| Address Hold from Write End | tHA | 0 | - | 0 | - | ns | 1,3 |
| Address Setup Time | tSA | 0 | - | 0 | - | ns | 1,3 |
| UB#,LB# to Write End | tPWB | 35 | - | 40 | - | ns | 1,3 |
| WE# Pulse Width | tPWE | 35 | - | 40 | - | ns | 1,3,4 |
| Data Setup to Write End | tSD | 25 | - | 25 | - | ns | 1,3 |
| Data Hold from Write End | tHD | 0 | - | 0 | - | ns | 1,3 |
| WE# LOW to High-Z Output | tHZWE | - | 18 | - | 20 | ns | 2,3 |
| WE# HIGH to Low-Z Output | tLZWE | 10 | - | 10 | - | ns | 2,3 |

Notes:

1. Tested with the load in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. tHZOE, tHZCS, tHZB, and tHZWE transitions are measured when the output enters a high impedance state. Not 100% tested.
3. The internal write time is defined by the overlap of CS1# = LOW, CS2=HIGH, UB# or LB# = LOW, and WE# = LOW. All four conditions must be in valid states to initiate a Write, but any condition can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
4. tPWE > tHZWE + tSD when OE# is LOW.
5. Address inputs must meet V_{IH} and V_{IL} SPEC during this period. Any glitch or unknown inputs are not permitted. Unknown input with standby mode is acceptable.
6. Data retention characteristics are defined later in DATA RETENTION CHARACTERISTICS.

AC TEST CONDITIONS (OVER THE OPERATING RANGE)

| Parameter | Unit (1.65V~2.2V) | Unit (2.2V~3.6V) |
|-------------------------------|-------------------------|-----------------------|
| Input Pulse Level | 0V to V _{DD} | 0V to V _{DD} |
| Input Rise and Fall Time | 1V/ns | 1V/ns |
| Output Timing Reference Level | 0.9V | ½ V _{DD} |
| R1 | 13500 | 1005 |
| R2 | 10800 | 820 |
| V _{TM} | 1.8V | V _{DD} |
| Output Load Conditions | Refer to Figure 1 and 2 | |

OUTPUT LOAD CONDITIONS FIGURES

Figure1

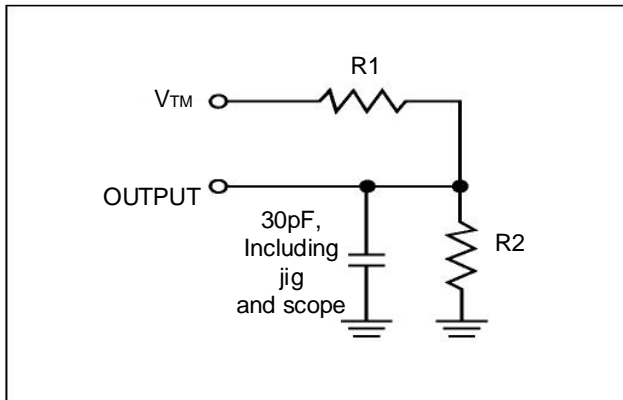
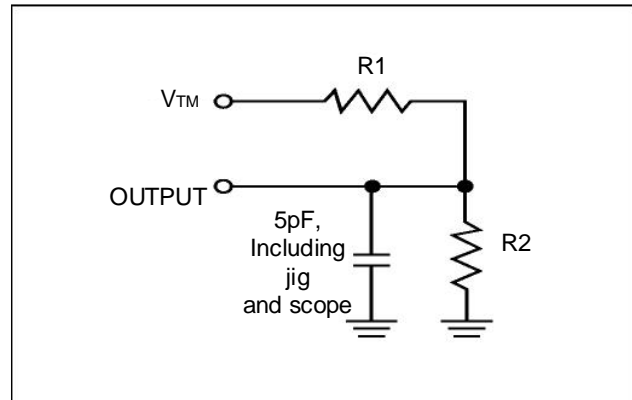
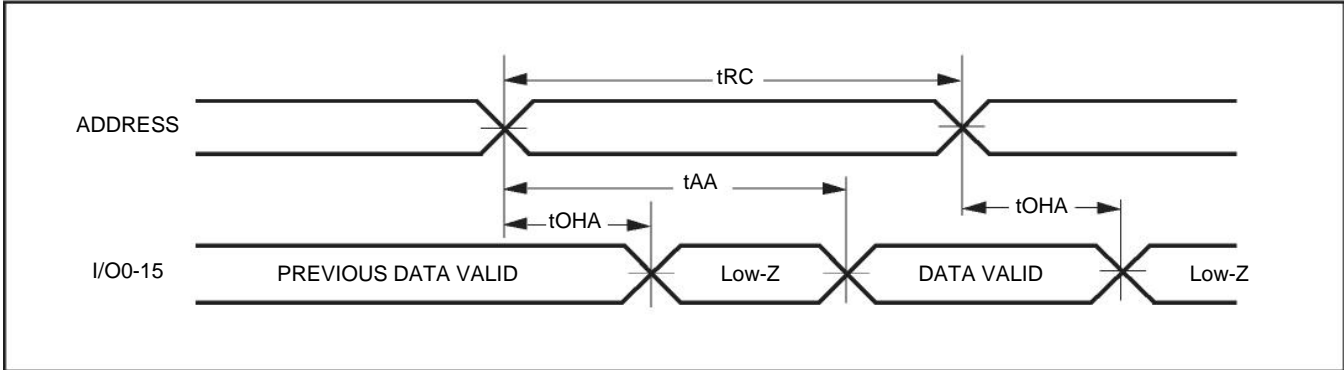


Figure2



TIMING DIAGRAM

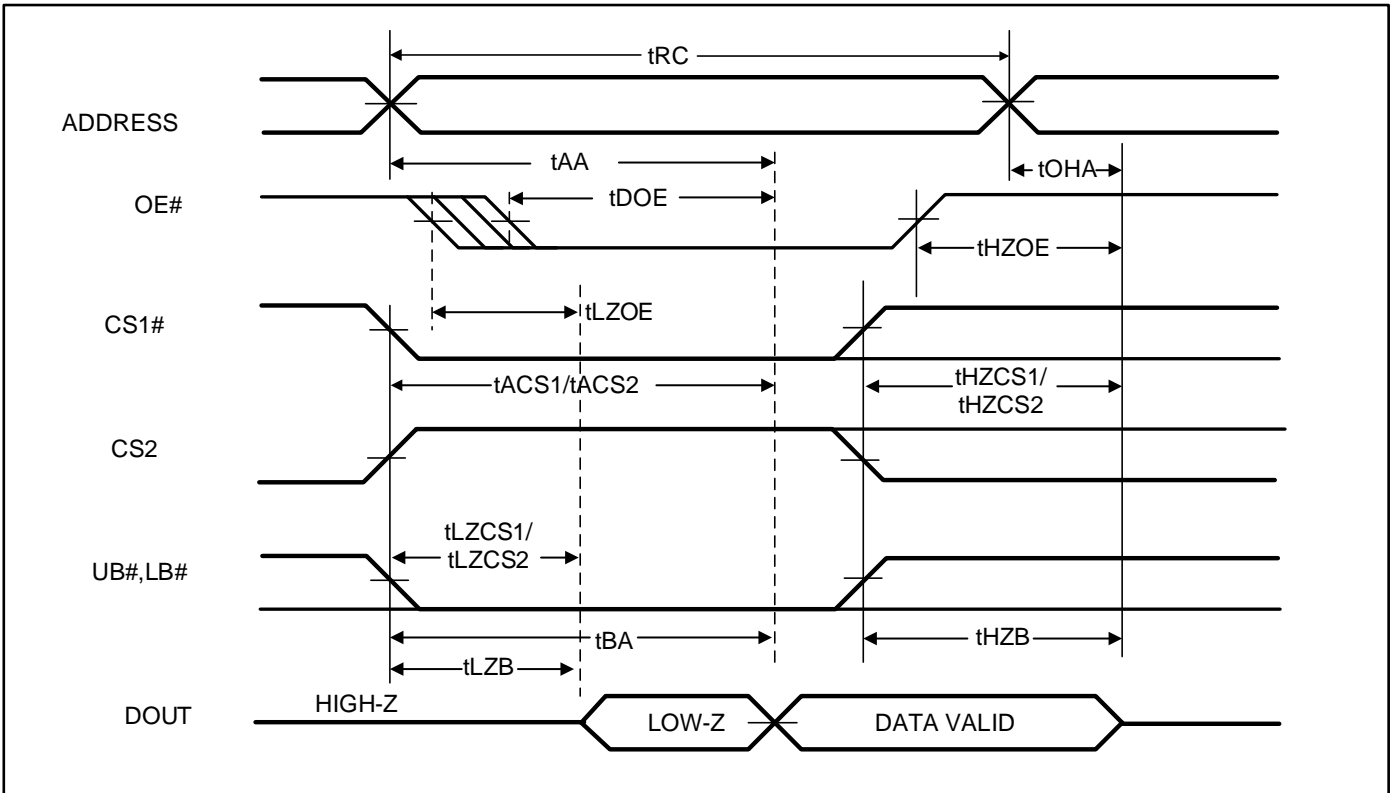
READ CYCLE NO. 1⁽¹⁾ (ADDRESS CONTROLLED, CS1# = OE# = UB# = LB# = LOW, CS2 = WE# = HIGH)



Note:

1. The device is continuously selected.

READ CYCLE NO.2⁽¹⁾ (OE# CONTROLLED, WE# = HIGH)



Note:

1. Address is valid prior to or coincident with CS1# LOW or CS2 HIGH transition.

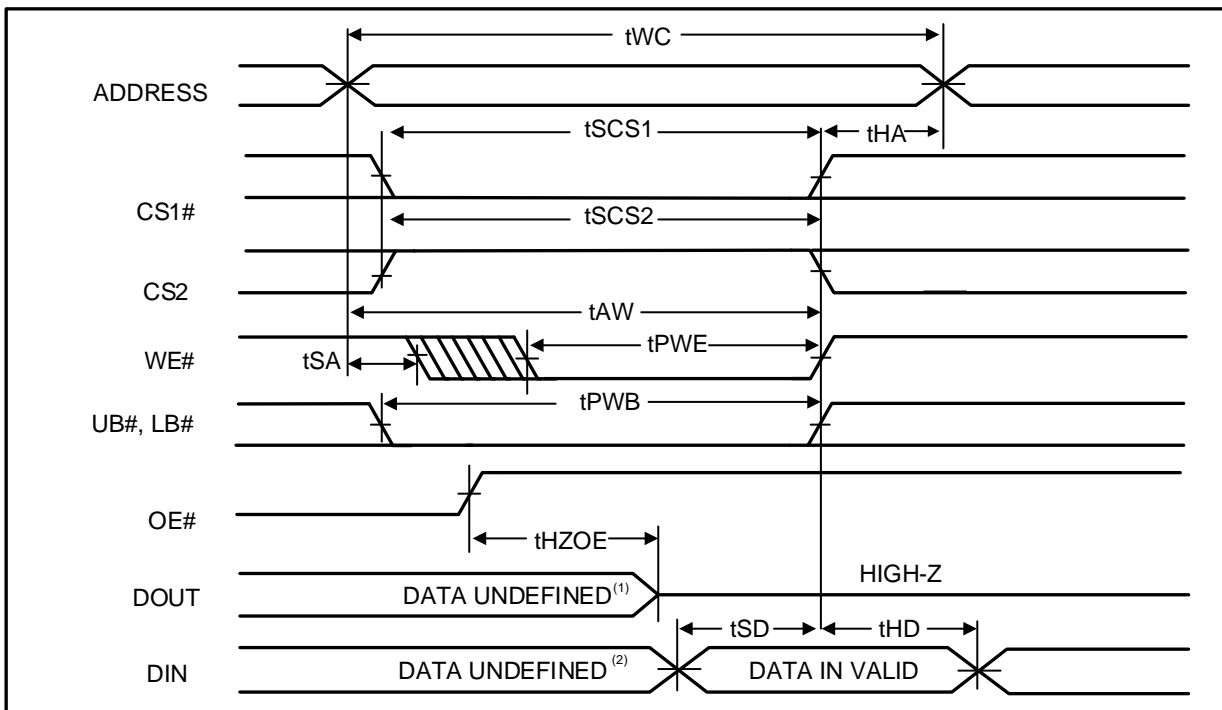
WRITE CYCLE NO.1 ^(1, 2) (CS1#, CS2 Controlled, OE# = HIGH or LOW)



Notes:

1. tHZWE is based on the assumption when tSA=0nS after READ operation. Actual DOUT for tHZWE may not appear if OE# goes high before Write Cycle. tHZOE is the time DOUT goes to High-Z after OE# goes high.
2. During this period the I/Os are in output state. Do not apply input signals.

WRITE CYCLE NO. 2 ^(1, 2) (WE# CONTROLLED: OE# IS HIGH DURING WRITE CYCLE)



Notes:

1. tHZOE is the time DOUT goes to High-Z after OE# goes high.
2. During this period the I/Os are in output state. Do not apply input signals.

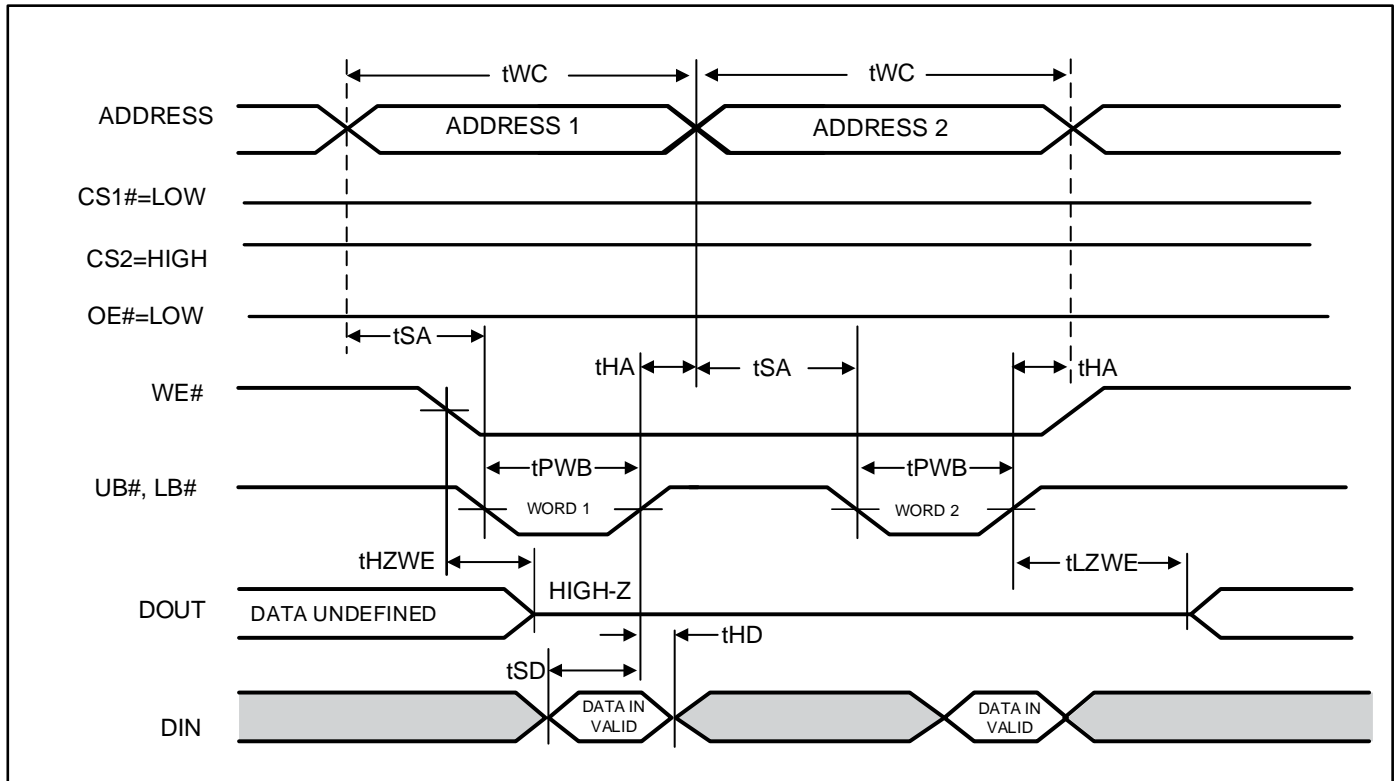
WRITE CYCLE NO. 3⁽¹⁾ (WE# CONTROLLED: OE# IS LOW DURING WRITE CYCLE)



Note:

1. If OE# is low during write cycle, tHZWE must be met in the application. Do not apply input signal during this period. Data output from the previous READ operation will drive IO BUS.

WRITE CYCLE NO. 4^(1, 2, 3) (UB# & LB# Controlled, OE# = LOW)



Notes:

1. If OE# is low during write cycle, tHZWE must be met in the application. Do not apply input signal during this period. Data output from previous READ operation will drive IO BUS.
2. Due to the restriction of note 1, OE# is recommended to be HIGH during write period.
3. WE# stays LOW in this example. If WE# toggles, tPWE and tHZWE must be considered.

DATA RETENTION CHARACTERISTICS

| Symbol | Parameter | Test Condition ⁽³⁾ | Min. | Typ. ⁽¹⁾ | Max. | Unit | |
|---------------------------------|------------------------------------|--|-------|---------------------|------|------|----|
| V _{DR} | V _{DD} for Data Retention | See Data Retention Waveform | 1.5 | - | - | V | |
| I _{DR} | Data Retention Current | V _{DD} = V _{DR} (min), CS1# ≥ V _{DD} - 0.2V or CS2 ≤ 0.2V or LB# and UB# ≥ V _{DD} - 0.2V, VIN ≤ 0.2V or VIN ≥ V _{DD} - 0.2V | 25°C | - | 3.0 | 5 | μA |
| | | | 85°C | - | - | 6 | |
| | | | 125°C | - | - | 18 | |
| t _{SDR} ⁽²⁾ | Data Retention Setup Time | See Data Retention Waveform | - | 0 | - | ns | |
| t _{RDR} | Recovery Time | See Data Retention Waveform | - | t _{RC} | - | ns | |

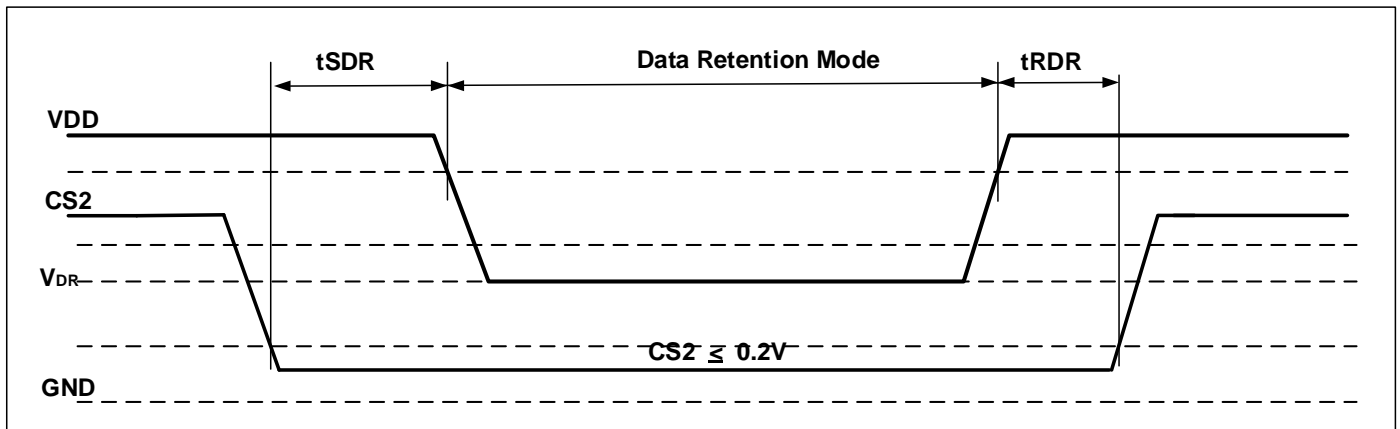
Notes:

1. Typical values are measured at 25°C, V_{DD} = V_{DR} (min.), and not 100% tested.
2. V_{DD} power down slope must be longer than 100 us/volt when enter into Data Retention Mode.
3. Test conditions are based on 2 CS option.

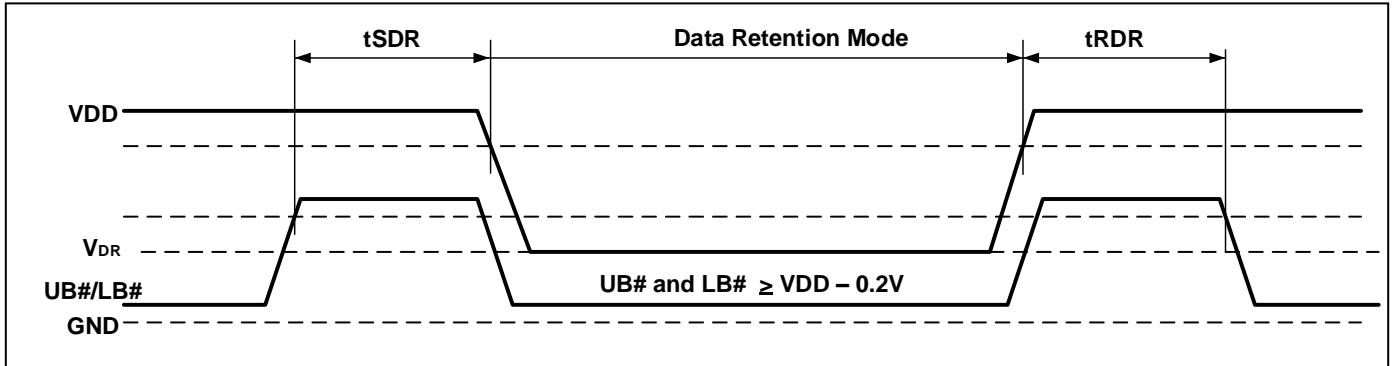
DATA RETENTION WAVEFORM (CS1# CONTROLLED)



DATA RETENTION WAVEFORM (CS2 CONTROLLED)



DATA RETENTION WAVEFORM (UB# AND LB# CONTROLLED)



Notes:

1. CS2 must satisfy either $CS2 \geq VDD - 0.2V$ or $CS2 \leq 0.2V$
2. CS1# must satisfy either $CS1\# \geq VDD - 0.2V$ or $CS1\# \leq 0.2V$

ORDERING INFORMATION

IS62WV6416FALL (1.65V - 2.2V)

Industrial Range: -40°C to +85°C

| Speed (ns) | Order Part No. | Package |
|------------|----------------------|---------------------------------|
| 55 | IS62WV6416FALL-55TLI | TSOP (Type II), Lead-free |
| 55 | IS62WV6416FALL-55BLI | mini BGA (6mm x 8mm), Lead-free |

IS62WV6416FBLL (2.2V - 3.6V)

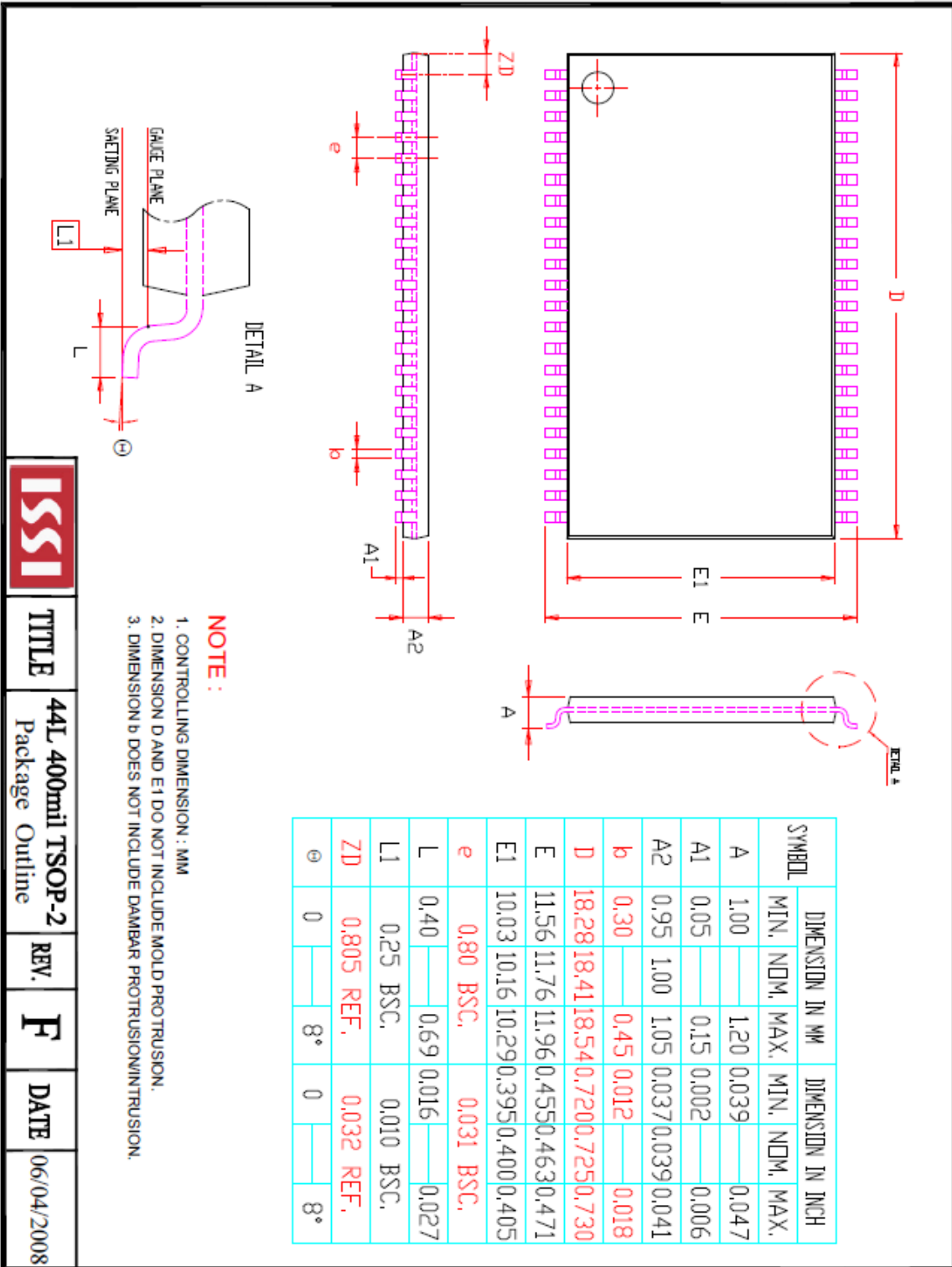
Industrial Range: -40°C to +85°C

| Speed (ns) | Order Part No. | Package |
|------------|-----------------------|--|
| 45 | IS62WV6416FBLL-45TLI | TSOP (Type II), Lead-free |
| 45 | IS62WV6416FBLL-45BI | mini BGA (6mm x 8mm) |
| 45 | IS62WV6416FBLL-45BLI | mini BGA (6mm x 8mm), Lead-free |
| 45 | IS62WV6416FBLL-45B2I | mini BGA (6mm x 8mm), 2 CS Option |
| 45 | IS62WV6416FBLL-45B2LI | mini BGA (6mm x 8mm), 2 CS Option, Lead-free |

Automotive Range (A3): -40°C to +125°C

| Speed (ns) | Order Part No. | Package |
|------------|------------------------|--|
| 55 | IS65WV6416FBLL-55CTLA3 | TSOP (Type II), Lead-free, Copper Lead frame |
| 55 | IS65WV6416FBLL-55BLA3 | mini BGA (6mm x 8mm), Lead-free |

PACKAGE INFORMATION



TITLE

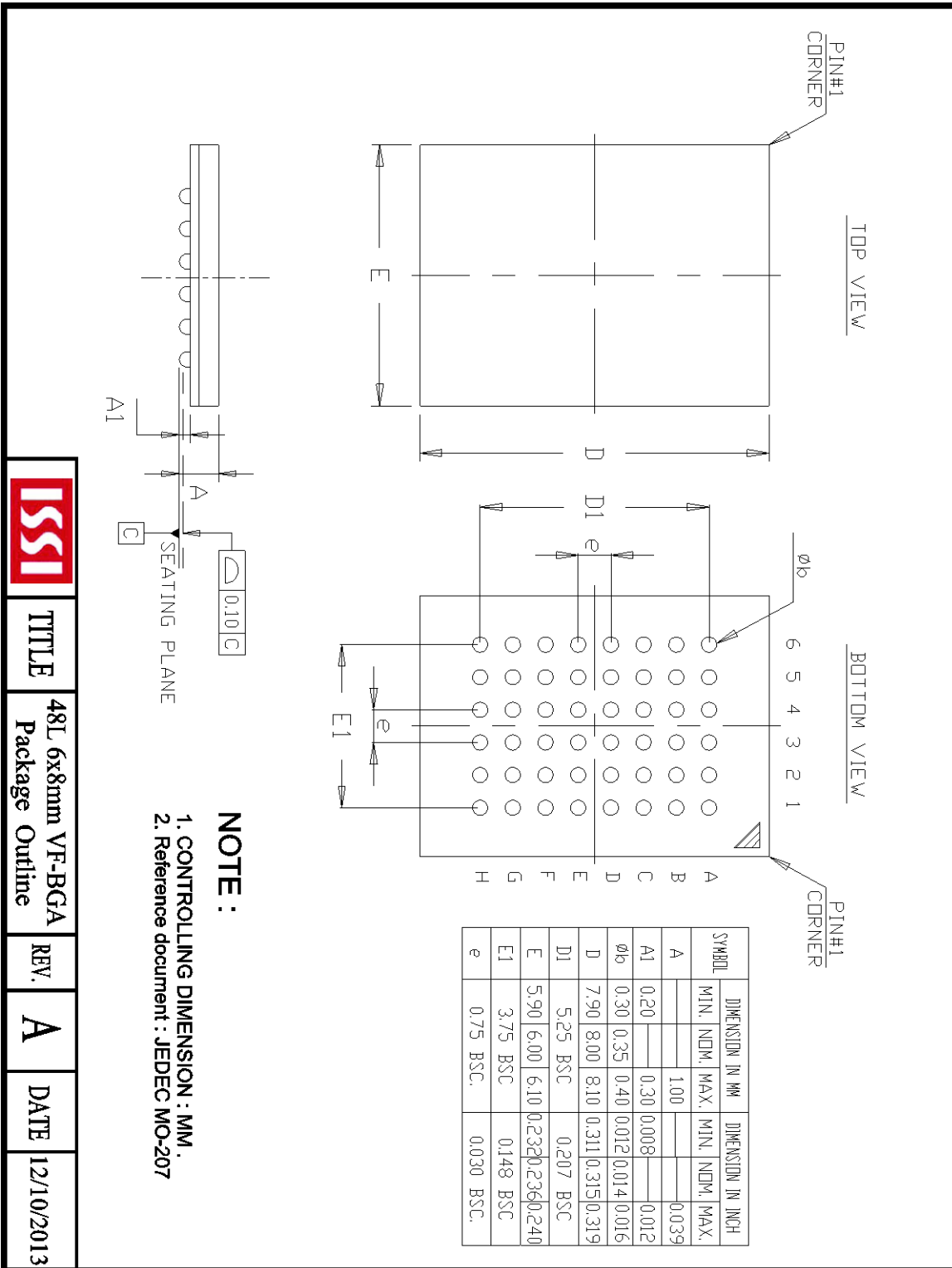
44L 400mil TSOP-2
Package Outline

REV.

F

DATE

06/04/2008



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|--|--------------|---|-------------|----------|-------------|-------------------|
| | TITLE | 48L 6x8mm VF-BGA Package Outline | REV. | A | DATE | 12/10/2013 |
|--|--------------|---|-------------|----------|-------------|-------------------|