

# MUN5231DW1, NSBC123EDXV6

## Dual NPN Bias Resistor Transistors

**R1 = 2.2 k $\Omega$ , R2 = 2.2 k $\Omega$**

### NPN Transistors with Monolithic Bias Resistor Network

This series of digital transistors is designed to replace a single device and its external resistor bias network. The Bias Resistor Transistor (BRT) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space.

#### Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### MAXIMUM RATINGS

(T<sub>A</sub> = 25°C, common for Q<sub>1</sub> and Q<sub>2</sub>, unless otherwise noted)

| Rating                         | Symbol               | Max | Unit |
|--------------------------------|----------------------|-----|------|
| Collector-Base Voltage         | V <sub>CBO</sub>     | 50  | Vdc  |
| Collector-Emitter Voltage      | V <sub>CEO</sub>     | 50  | Vdc  |
| Collector Current – Continuous | I <sub>C</sub>       | 100 | mAdc |
| Input Forward Voltage          | V <sub>IN(fwd)</sub> | 12  | Vdc  |
| Input Reverse Voltage          | V <sub>IN(rev)</sub> | 10  | Vdc  |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

#### ORDERING INFORMATION

| Device          | Package | Shipping <sup>†</sup> |
|-----------------|---------|-----------------------|
| MUN5231DW1T1G   | SOT-363 | 3,000/Tape & Reel     |
| NSBC123EDXV6T1G | SOT-563 | 4,000/Tape & Reel     |

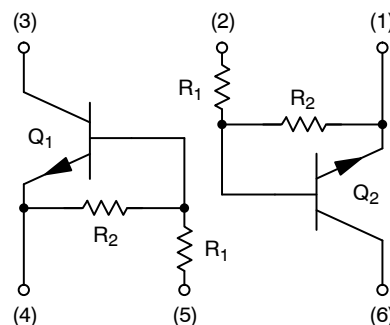
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



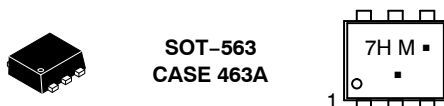
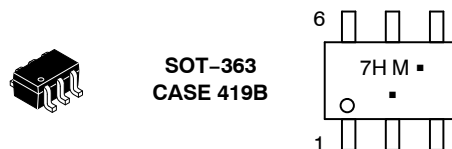
**ON Semiconductor®**

<http://onsemi.com>

#### PIN CONNECTIONS



#### MARKING DIAGRAMS



7H = Specific Device Code  
M = Date Code\*  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation may vary depending upon manufacturing location.

# MUN5231DW1, NSBC123EDXV6

## THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|----------------|--------|-----|------|
|----------------|--------|-----|------|

### MUN5231DW1 (SOT-363) ONE JUNCTION HEATED

|                                                                                         |                                              |                                   |                            |
|-----------------------------------------------------------------------------------------|----------------------------------------------|-----------------------------------|----------------------------|
| Total Device Dissipation<br>$T_A = 25^\circ\text{C}$<br>Derate above $25^\circ\text{C}$ | (Note 1)<br>(Note 2)<br>(Note 1)<br>(Note 2) | $P_D$<br>187<br>256<br>1.5<br>2.0 | mW<br>mW/ $^\circ\text{C}$ |
| Thermal Resistance,<br>Junction to Ambient                                              | (Note 1)<br>(Note 2)                         | $R_{\theta JA}$<br>670<br>490     | $^\circ\text{C/W}$         |

### MUN5231DW1 (SOT-363) BOTH JUNCTION HEATED (Note 3)

|                                                                                         |                                              |                                   |                            |
|-----------------------------------------------------------------------------------------|----------------------------------------------|-----------------------------------|----------------------------|
| Total Device Dissipation<br>$T_A = 25^\circ\text{C}$<br>Derate above $25^\circ\text{C}$ | (Note 1)<br>(Note 2)<br>(Note 1)<br>(Note 2) | $P_D$<br>250<br>385<br>2.0<br>3.0 | mW<br>mW/ $^\circ\text{C}$ |
| Thermal Resistance,<br>Junction to Ambient                                              | (Note 1)<br>(Note 2)                         | $R_{\theta JA}$<br>493<br>325     | $^\circ\text{C/W}$         |
| Thermal Resistance,<br>Junction to Lead                                                 | (Note 1)<br>(Note 2)                         | $R_{\theta JL}$<br>188<br>208     | $^\circ\text{C/W}$         |
| Junction and Storage Temperature Range                                                  |                                              | $T_J, T_{stg}$<br>-55 to +150     | $^\circ\text{C}$           |

### NSBC123EDXV6 (SOT-563) ONE JUNCTION HEATED

|                                                                                         |                      |                        |                            |
|-----------------------------------------------------------------------------------------|----------------------|------------------------|----------------------------|
| Total Device Dissipation<br>$T_A = 25^\circ\text{C}$<br>Derate above $25^\circ\text{C}$ | (Note 1)<br>(Note 1) | $P_D$<br>357<br>2.9    | mW<br>mW/ $^\circ\text{C}$ |
| Thermal Resistance,<br>Junction to Ambient                                              | (Note 1)             | $R_{\theta JA}$<br>350 | $^\circ\text{C/W}$         |

### NSBC123EDXV6 (SOT-563) BOTH JUNCTION HEATED (Note 3)

|                                                                                         |                      |                               |                            |
|-----------------------------------------------------------------------------------------|----------------------|-------------------------------|----------------------------|
| Total Device Dissipation<br>$T_A = 25^\circ\text{C}$<br>Derate above $25^\circ\text{C}$ | (Note 1)<br>(Note 1) | $P_D$<br>500<br>4.0           | mW<br>mW/ $^\circ\text{C}$ |
| Thermal Resistance,<br>Junction to Ambient                                              | (Note 1)             | $R_{\theta JA}$<br>250        | $^\circ\text{C/W}$         |
| Junction and Storage Temperature Range                                                  |                      | $T_J, T_{stg}$<br>-55 to +150 | $^\circ\text{C}$           |

- FR-4 @ Minimum Pad.
- FR-4 @  $1.0 \times 1.0$  Inch Pad.
- Both junction heated values assume total power is sum of two equally powered channels.

# MUN5231DW1, NSBC123EDXV6

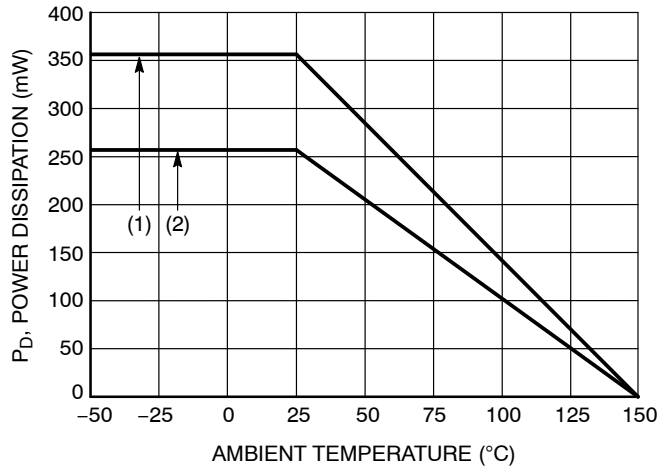
## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , common for $Q_1$ and $Q_2$ , unless otherwise noted)

| Characteristic                                                                        | Symbol        | Min | Typ | Max | Unit |
|---------------------------------------------------------------------------------------|---------------|-----|-----|-----|------|
| <b>OFF CHARACTERISTICS</b>                                                            |               |     |     |     |      |
| Collector-Base Cutoff Current<br>( $V_{CB} = 50\text{ V}$ , $I_E = 0$ )               | $I_{CBO}$     | –   | –   | 100 | nAdc |
| Collector-Emitter Cutoff Current<br>( $V_{CE} = 50\text{ V}$ , $I_B = 0$ )            | $I_{CEO}$     | –   | –   | 500 | nAdc |
| Emitter-Base Cutoff Current<br>( $V_{EB} = 6.0\text{ V}$ , $I_C = 0$ )                | $I_{EBO}$     | –   | –   | 2.3 | mAdc |
| Collector-Base Breakdown Voltage<br>( $I_C = 10\text{ }\mu\text{A}$ , $I_E = 0$ )     | $V_{(BR)CBO}$ | 50  | –   | –   | Vdc  |
| Collector-Emitter Breakdown Voltage (Note 4)<br>( $I_C = 2.0\text{ mA}$ , $I_B = 0$ ) | $V_{(BR)CEO}$ | 50  | –   | –   | Vdc  |

## ON CHARACTERISTICS

|                                                                                                          |               |     |     |      |                  |
|----------------------------------------------------------------------------------------------------------|---------------|-----|-----|------|------------------|
| DC Current Gain (Note 4)<br>( $I_C = 5.0\text{ mA}$ , $V_{CE} = 10\text{ V}$ )                           | $h_{FE}$      | 8.0 | 15  | –    |                  |
| Collector-Emitter Saturation Voltage (Note 4)<br>( $I_C = 10\text{ mA}$ , $I_B = 5.0\text{ mA}$ )        | $V_{CE(sat)}$ | –   | –   | 0.25 | V                |
| Input Voltage (Off)<br>( $V_{CE} = 5.0\text{ V}$ , $I_C = 1.0\text{ mA}$ )                               | $V_{i(off)}$  | –   | 1.3 | –    | Vdc              |
| Input Voltage (On)<br>( $V_{CE} = 0.2\text{ V}$ , $I_C = 20\text{ mA}$ )                                 | $V_{i(on)}$   | –   | 1.8 | –    | Vdc              |
| Output Voltage (On)<br>( $V_{CC} = 5.0\text{ V}$ , $V_B = 2.5\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ )   | $V_{OL}$      | –   | –   | 0.2  | Vdc              |
| Output Voltage (Off)<br>( $V_{CC} = 5.0\text{ V}$ , $V_B = 0.25\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ ) | $V_{OH}$      | 4.9 | –   | –    | Vdc              |
| Input Resistor                                                                                           | $R_1$         | 1.5 | 2.2 | 2.9  | $\text{k}\Omega$ |
| Resistor Ratio                                                                                           | $R_1/R_2$     | 0.8 | 1.0 | 1.2  |                  |

4. Pulsed Condition: Pulse Width = 300 ms, Duty Cycle  $\leq 2\%$ .



(1) SOT-363; 1.0 x 1.0 Inch Pad  
(2) SOT-563; Minimum Pad

Figure 1. Derating Curve

# MUN5231DW1, NSBC123EDXV6

## TYPICAL CHARACTERISTICS MUN5231DW1, NSBC123EDXV6

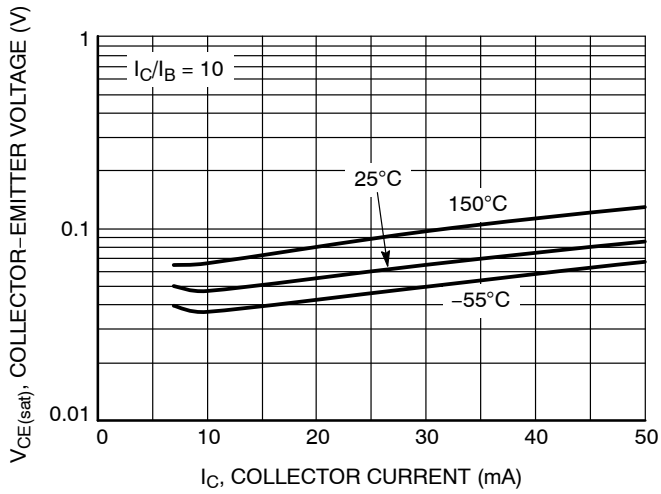


Figure 2.  $V_{CE(sat)}$  vs.  $I_C$

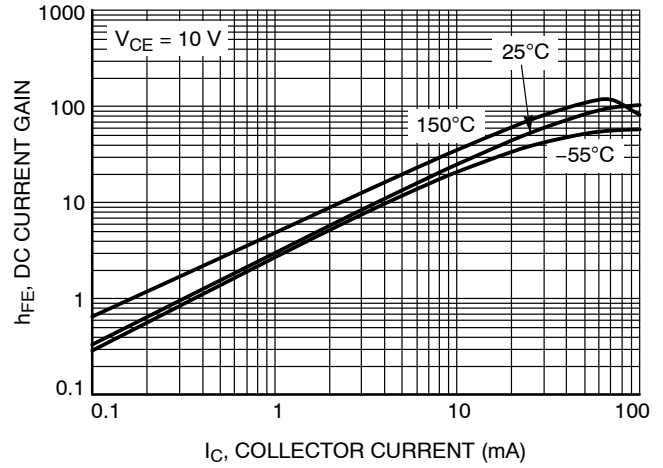


Figure 3. DC Current Gain

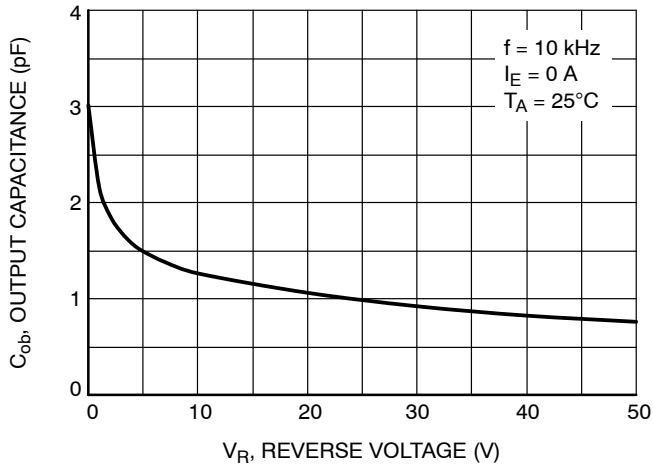


Figure 4. Output Capacitance

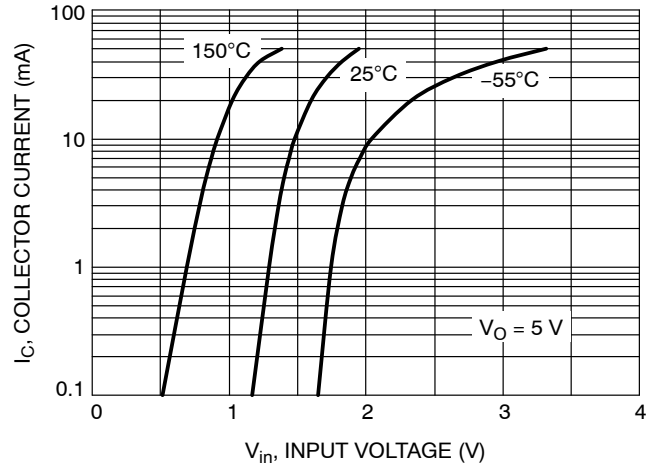


Figure 5. Output Current vs. Input Voltage

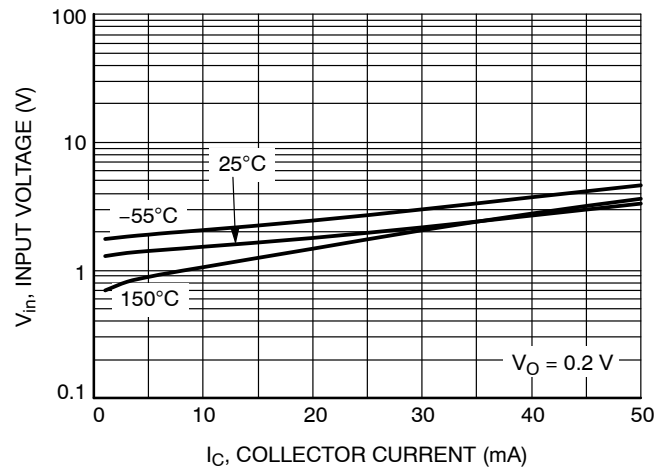
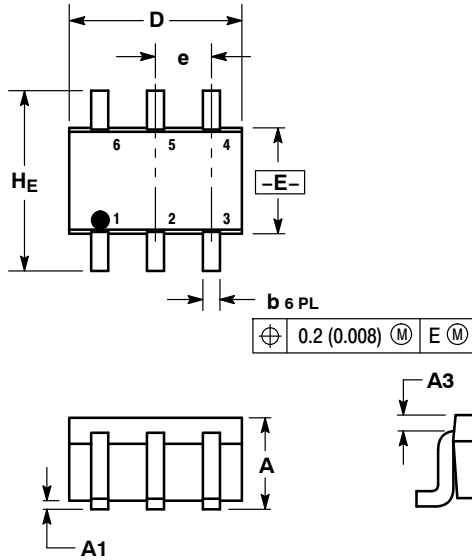


Figure 6. Input Voltage vs. Output Current

# MUN5231DW1, NSBC123EDXV6

## PACKAGE DIMENSIONS

**SC-88/SC70-6/SOT-363**  
CASE 419B-02  
ISSUE W

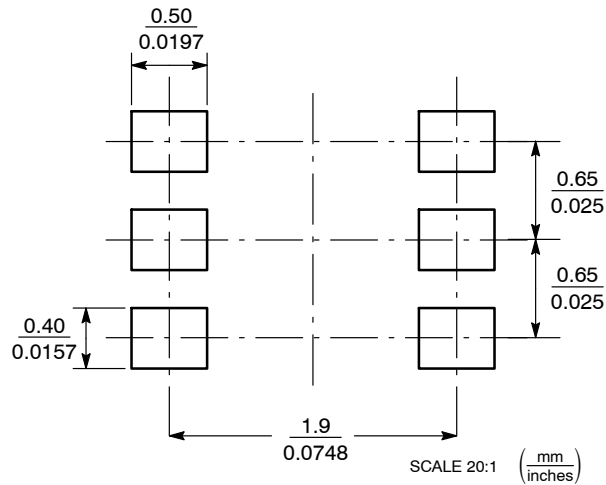


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419B-01 OBSOLETE, NEW STANDARD 419B-02.

| DIM | MILLIMETERS |      |      | INCHES    |       |       |
|-----|-------------|------|------|-----------|-------|-------|
|     | MIN         | NOM  | MAX  | MIN       | NOM   | MAX   |
| A   | 0.80        | 0.95 | 1.10 | 0.031     | 0.037 | 0.043 |
| A1  | 0.00        | 0.05 | 0.10 | 0.000     | 0.002 | 0.004 |
| A3  | 0.20 REF    |      |      | 0.008 REF |       |       |
| b   | 0.10        | 0.21 | 0.30 | 0.004     | 0.008 | 0.012 |
| C   | 0.10        | 0.14 | 0.25 | 0.004     | 0.005 | 0.010 |
| D   | 1.80        | 2.00 | 2.20 | 0.070     | 0.078 | 0.086 |
| E   | 1.15        | 1.25 | 1.35 | 0.045     | 0.049 | 0.053 |
| e   | 0.65 BSC    |      |      | 0.026 BSC |       |       |
| L   | 0.10        | 0.20 | 0.30 | 0.004     | 0.008 | 0.012 |
| HE  | 2.00        | 2.10 | 2.20 | 0.078     | 0.082 | 0.086 |

## SOLDERING FOOTPRINT\*



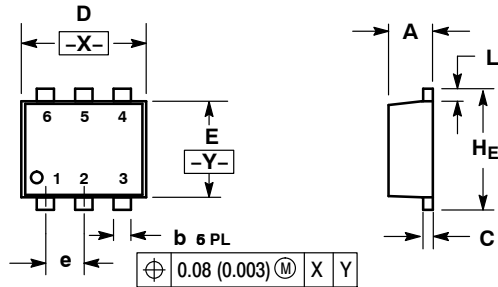
## SC-88/SC70-6/SOT-363

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MUN5231DW1, NSBC123EDXV6

## PACKAGE DIMENSIONS

### SOT-563, 6 LEAD CASE 463A ISSUE F

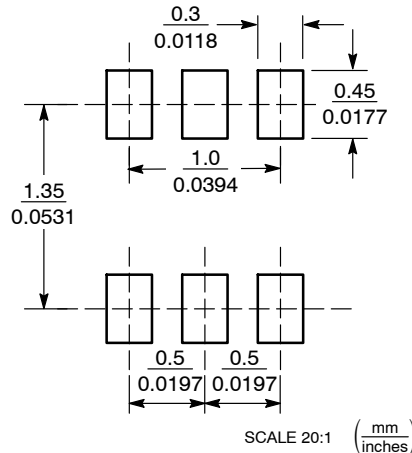


#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

| DIM            | MILLIMETERS |      |      | INCHES   |       |       |
|----------------|-------------|------|------|----------|-------|-------|
|                | MIN         | NOM  | MAX  | MIN      | NOM   | MAX   |
| A              | 0.50        | 0.55 | 0.60 | 0.020    | 0.021 | 0.023 |
| b              | 0.17        | 0.22 | 0.27 | 0.007    | 0.009 | 0.011 |
| C              | 0.08        | 0.12 | 0.18 | 0.003    | 0.005 | 0.007 |
| D              | 1.50        | 1.60 | 1.70 | 0.059    | 0.062 | 0.066 |
| E              | 1.10        | 1.20 | 1.30 | 0.043    | 0.047 | 0.051 |
| e              | 0.5 BSC     |      |      | 0.02 BSC |       |       |
| L              | 0.10        | 0.20 | 0.30 | 0.004    | 0.008 | 0.012 |
| H <sub>E</sub> | 1.50        | 1.60 | 1.70 | 0.059    | 0.062 | 0.066 |

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative