

BATTERY PROTECTION IC WITH CELL-BALANCE FUNCTION

The S-8209B Series is a protection IC for lithium-ion / lithium polymer rechargeable batteries and includes a high-accuracy voltage detection circuit and a delay circuit.

The S-8209B Series has a transmission function and two types of cell-balance function so that users are also able to configure a protection circuit with series multi-cell.

■ Features

- High-accuracy voltage detection circuit

| | | |
|--|--|------------------|
| Overcharge detection voltage* ¹ | 3.55 V to 4.40 V (5 mV step) | Accuracy ±25 mV |
| Overcharge release voltage* ¹ | 3.50 V to 4.40 V* ² | Accuracy ±50 mV |
| Cell-balance detection voltage* ¹ | 3.55 V to 4.40 V (5 mV step)* ³ | Accuracy ±25 mV |
| Cell-balance release voltage* ¹ | 3.50 V to 4.40 V* ⁴ | Accuracy ±50 mV |
| Overdischarge detection voltage | 2.0 V to 3.0 V (10 mV step) | Accuracy ±50 mV |
| Overdischarge release voltage | 2.0 V to 3.4 V* ⁵ | Accuracy ±100 mV |
- Settable delay time by external capacitor for output pin
- Control charging, discharging, cell-balance by CTLC pin, CTLD pin
- Two types of cell-balance function; charge / discharge*⁶
- Wide range of operation temperature Ta = -40°C to +85°C
- Low current consumption 7.0 μA max.
- Lead-free, Sn 100%, halogen-free*⁷

*1. Regarding selection of overcharge detection voltage, overcharge release voltage, cell-balance detection voltage and cell-balance release voltage, refer to **Remark 3** in "**3. Product name list**" of "**■ Product Name Structure**".

*2. Overcharge release voltage = Overcharge detection voltage – Overcharge hysteresis voltage
(Overcharge hysteresis voltage is selectable in 0 V to 0.4 V in 50 mV step.)

*3. Select as to overcharge detection voltage > cell-balance detection voltage.

*4. Cell-balance release voltage = Cell-balance detection voltage – Cell-balance hysteresis voltage
(Cell-balance hysteresis voltage is selectable in 0 V to 0.4 V in 50 mV step.)

*5. Overdischarge release voltage = Overdischarge detection voltage + Overdischarge hysteresis voltage
(Overdischarge hysteresis voltage is selectable in 0 V to 0.7 V in 100 mV step.)

*6. Also available the product without discharge cell-balance function

*7. Refer to "**■ Product Name Structure**" for details.

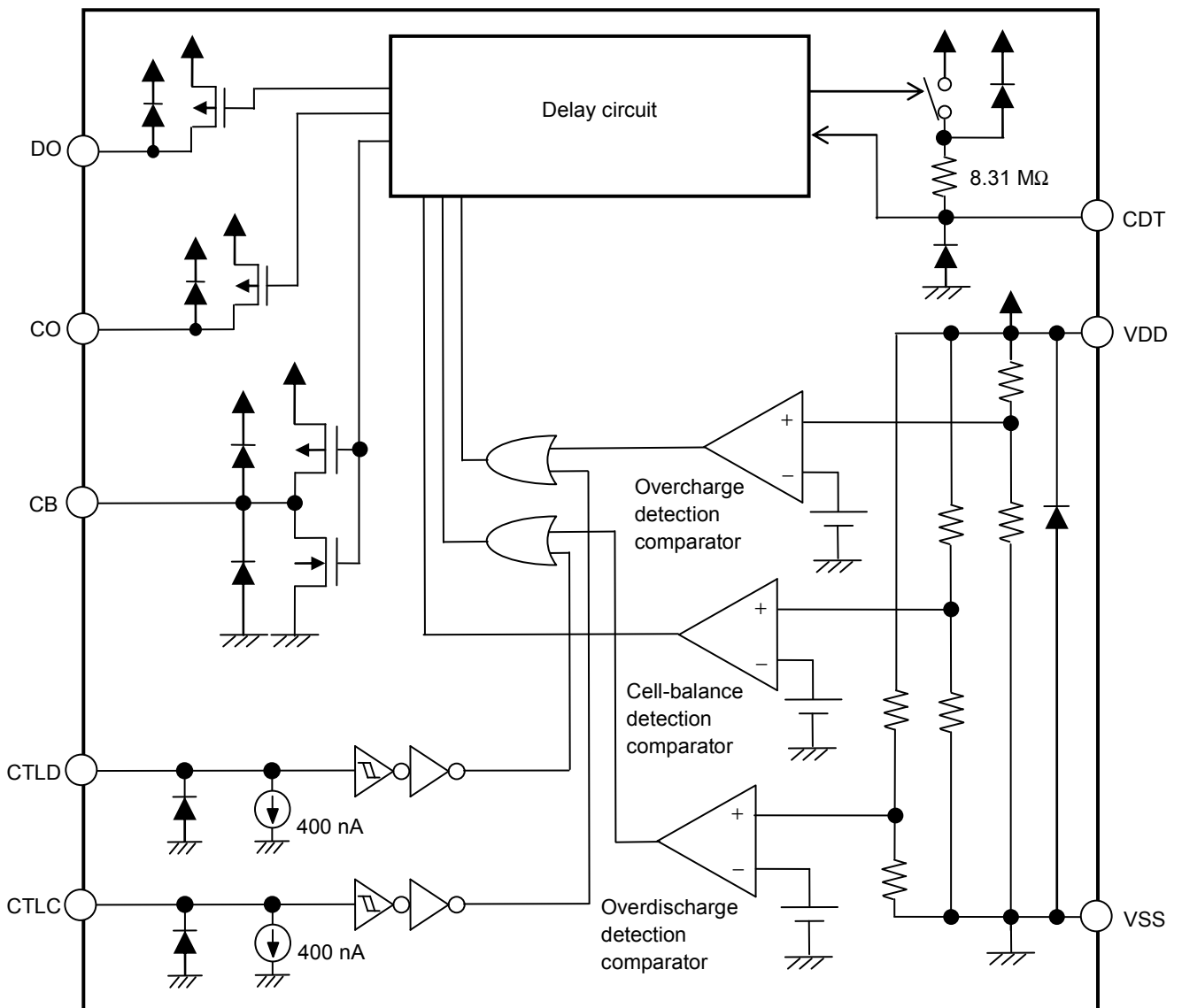
■ Applications

- Lithium-ion rechargeable battery pack
- Lithium polymer rechargeable battery pack

■ Packages

- SNT-8A
- 8-Pin TSSOP

■ **Block Diagram**



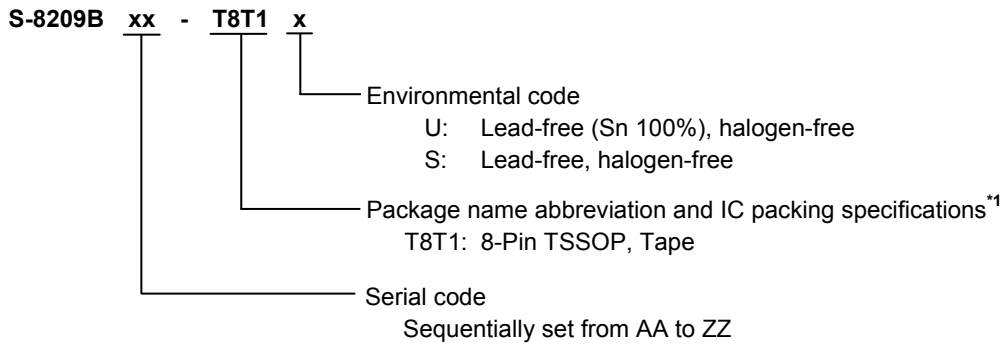
Remark The diodes in the IC are parasitic diodes.

Figure 1

■ Product Name Structure

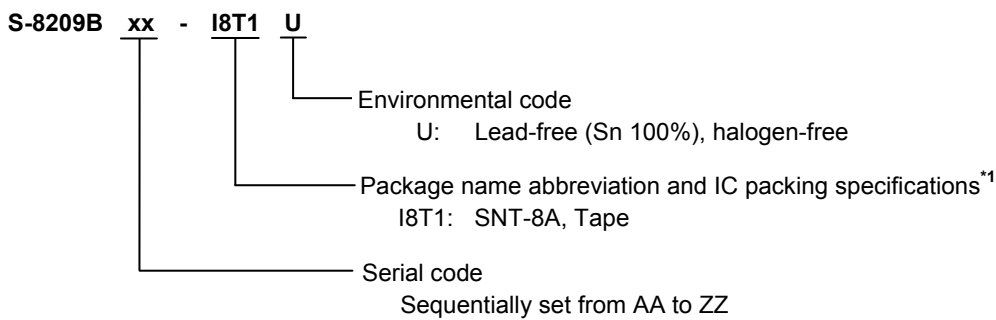
1. Product name

1.1 8-Pin TSSOP



*1. Refer to the tape drawing.

1.2 SNT-8A



*1. Refer to the tape drawing.

2. Packages

Table 1 Package Drawing Codes

| Package Name | | Dimension | Tape | Reel | Land |
|--------------|------------------------|--------------|--------------|--------------|--------------|
| 8-Pin TSSOP | Environmental code = S | FT008-A-P-SD | FT008-E-C-SD | FT008-E-R-SD | - |
| | Environmental code = U | FT008-A-P-SD | FT008-E-C-SD | FT008-E-R-S1 | |
| SNT-8A | | PH008-A-P-SD | PH008-A-C-SD | PH008-A-R-SD | PH008-A-L-SD |

3. Product name list

3.1 8-Pin TSSOP

Table 2

| Product Name | Overcharge Detection Voltage (V _{CU}) | Overcharge Release Voltage (V _{CL}) | Cell-balance Detection Voltage (V _{BU}) | Cell-balance Release Voltage (V _{BL}) | Overdischarge Detection Voltage (V _{DL}) | Overdischarge Release Voltage (V _{DU}) | Discharge Cell-balance Function |
|-----------------|---|---|---|---|--|--|---------------------------------|
| S-8209BAA-T8T1y | 4.100 V | 4.000 V | 4.050 V | 4.000 V | 2.50 V | 2.70 V | Yes |
| S-8209BAD-T8T1y | 4.150 V | 3.950 V | 3.900 V | 3.900 V | 2.00 V | 2.70 V | Yes |
| S-8209BAG-T8T1y | 3.800 V | 3.650 V | 3.700 V | 3.700 V | 2.20 V | 2.50 V | No |
| S-8209BAH-T8T1y | 4.250 V | 4.150 V | 4.200 V | 4.200 V | 2.50 V | 2.80 V | No |
| S-8209BAI-T8T1y | 4.250 V | 4.150 V | 4.100 V | 4.050 V | 2.50 V | 2.70 V | Yes |
| S-8209BAJ-T8T1y | 4.150 V | 3.950 V | 3.900 V | 3.900 V | 2.30 V | 3.00 V | No |
| S-8209BAK-T8T1y | 4.215 V | 4.215 V | 4.190 V | 4.190 V | 2.00 V | 2.50 V | Yes |
| S-8209BAL-T8T1y | 4.300 V | 4.100 V | 4.225 V | 4.225 V | 2.00 V | 2.50 V | Yes |
| S-8209BAN-T8T1U | 4.250 V | 4.150 V | 4.200 V | 4.200 V | 2.00 V | 2.10 V | No |

3.2 SNT-8A

Table 3

| Product Name | Overcharge Detection Voltage (V _{CU}) | Overcharge Release Voltage (V _{CL}) | Cell-balance Detection Voltage (V _{BU}) | Cell-balance Release Voltage (V _{BL}) | Overdischarge Detection Voltage (V _{DL}) | Overdischarge Release Voltage (V _{DU}) | Discharge Cell-balance Function |
|-----------------|---|---|---|---|--|--|---------------------------------|
| S-8209BAA-I8T1U | 4.100 V | 4.000 V | 4.050 V | 4.000 V | 2.50 V | 2.70 V | Yes |
| S-8209BAM-I8T1U | 4.000 V | 3.800 V | 3.900 V | 3.850 V | 3.00 V | 3.40 V | No |

Remark 1. y: S or U

2. Please select products of environmental code = U for Sn 100%, halogen-free products.

3. Please contact our sales office for the products with detection voltage value other than those specified above.

Users are able to select the overcharge detection voltage, overcharge release voltage, cell-balance detection voltage and cell-balance release voltage from the range shown in **Figure 2** and **Figure 3**.

Users are able to select how to combine the overcharge detection voltage (V_{CU}) and the overcharge release voltage (V_{CL}) from the range A or B shown in **Figure 2**^{*1}.

Similarly, select how to combine the cell-balance detection voltage (V_{BU}) and the cell-balance release voltage (V_{BL}) from the range of C or D in **Figure 3**^{*2}.

In selecting the combination of V_{CU} and V_{CL} from the range A, select the combination of V_{BU} and V_{BL} from the range C. Similarly, in selecting the combination of V_{CU} and V_{CL} from the B range, select the combination of V_{BU} and V_{BL} from the range D^{*3}.

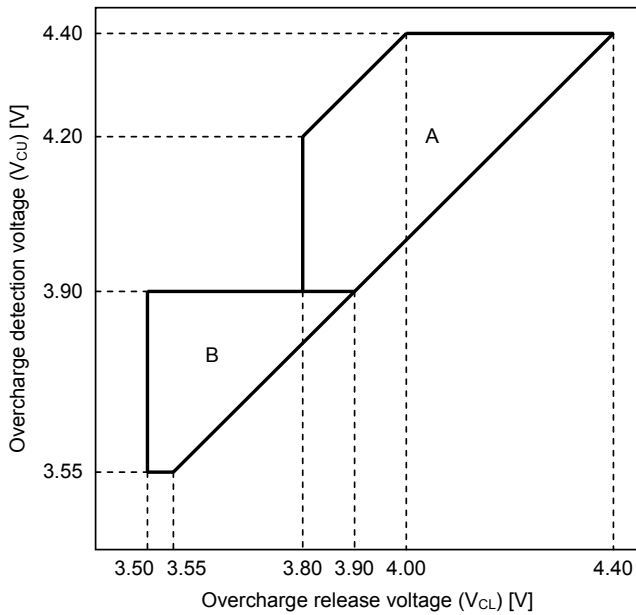


Figure 2

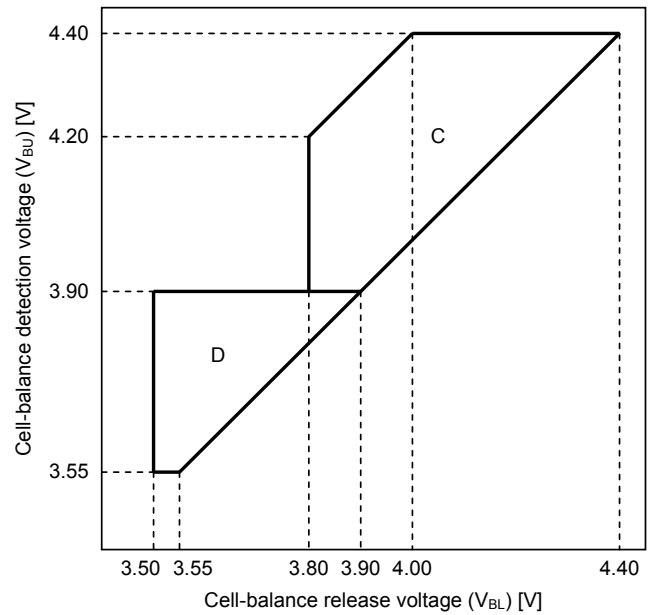


Figure 3

- *1. Users are able to select the overcharge hysteresis voltage ($V_{CU} - V_{CL}$) in 0 V to 0.4 V, in 50 mV step.
- *2. Users are able to select the cell-balance hysteresis voltage ($V_{BU} - V_{BL}$) in 0 V to 0.4 V, in 50 mV step.
- *3. Select as to set $V_{CU} > V_{BU}$.

■ **Pin Configurations**

1. 8-Pin TSSOP

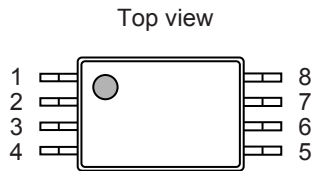


Figure 4

Table 4

| Pin No. | Symbol | Description |
|---------|--------|---|
| 1 | CTLC | Pin for charge control |
| 2 | CTLD | Pin for discharge control |
| 3 | VDD | Input pin for positive power supply; Connection pin for battery's positive voltage |
| 4 | CDT | Capacitor connection pin for overcharge detection delay, cell-balance detection delay and overdischarge detection delay |
| 5 | VSS | Input pin for negative power supply; Connection pin for batter's negative voltage |
| 6 | DO | Output pin for discharge control (Pch open-drain output) |
| 7 | CO | Output pin for charge control (Pch open-drain output) |
| 8 | CB | Output pin for cell-balance control (CMOS output) |

2. SNT-8A

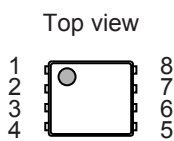


Figure 5

Table 5

| Pin No. | Symbol | Description |
|---------|--------|---|
| 1 | CTLC | Pin for charge control |
| 2 | CTLD | Pin for discharge control |
| 3 | VDD | Input pin for positive power supply; Connection pin for battery's positive voltage |
| 4 | CDT | Capacitor connection pin for overcharge detection delay, cell-balance detection delay and overdischarge detection delay |
| 5 | VSS | Input pin for negative power supply; Connection pin for battery's negative voltage |
| 6 | DO | Output pin for discharge control (Pch open-drain output) |
| 7 | CO | Output pin for charge control (Pch open-drain output) |
| 8 | CB | Output pin for cell-balance control (CMOS output) |

■ **Absolute Maximum Ratings**

Table 6

(Ta = +25°C unless otherwise specified)

| Item | Symbol | Applied pin | Absolute Maximum Rating | Unit | |
|-----------------------------------|--------------------|----------------|--|-------|----|
| Input voltage between VDD and VSS | V _{DS} | VDD | V _{SS} - 0.3 to V _{SS} + 12 | V | |
| CB pin output voltage | V _{CB} | CB | V _{SS} - 0.3 to V _{DD} + 0.3 | V | |
| CDT pin voltage | V _{CDT} | CDT | V _{SS} - 0.3 to V _{DD} + 0.3 | V | |
| DO pin output voltage | V _{DO} | DO | V _{DD} - 24 to V _{DD} + 0.3 | V | |
| CO pin output voltage | V _{CO} | CO | V _{DD} - 24 to V _{DD} + 0.3 | V | |
| CTLIC pin input voltage | V _{CTLIC} | CTLIC | V _{SS} - 0.3 to V _{SS} + 24 | V | |
| CTLD pin input voltage | V _{CTLD} | CTLD | V _{SS} - 0.3 to V _{SS} + 24 | V | |
| Power dissipation | 8-Pin TSSOP | P _D | - | 700*1 | mW |
| | SNT-8A | | | 450*1 | mW |
| Operating ambient temperature | T _{opr} | - | -40 to +85 | °C | |
| Storage temperature | T _{stg} | - | -55 to +125 | °C | |

*1. When mounted on board

[Mounted board]

- (1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
- (2) Board name: JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

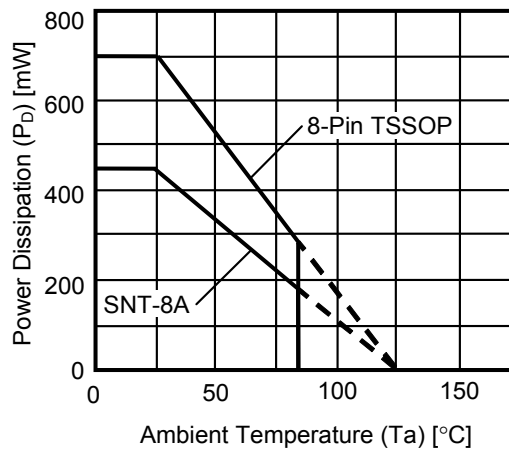


Figure 6 Power Dissipation of Package (When mounted on board)

■ **Electrical Characteristics**

Table 7

(Ta = +25°C unless otherwise specified)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|--|--------------------|--|-------------------------|------------------------|-------------------------|------|--------------|
| Overcharge detection voltage | V _{CU} | – | V _{CU} – 0.025 | V _{CU} | V _{CU} + 0.025 | V | 1 |
| Overcharge release voltage | V _{CL} | V _{CL} ≠ V _{CU} | V _{CL} – 0.05 | V _{CL} | V _{CL} + 0.05 | V | 1 |
| | | V _{CL} = V _{CU} | V _{CL} – 0.05 | V _{CL} | V _{CL} + 0.025 | V | 1 |
| Cell-balance detection voltage | V _{BU} | – | V _{BU} – 0.025 | V _{BU} | V _{BU} + 0.025 | V | 1 |
| Cell-balance release voltage | V _{BL} | V _{BL} ≠ V _{BU} | V _{BL} – 0.05 | V _{BL} | V _{BL} + 0.05 | V | 1 |
| | | V _{BL} = V _{BU} | V _{BL} – 0.05 | V _{BL} | V _{BL} + 0.025 | V | 1 |
| Overdischarge detection voltage | V _{DL} | – | V _{DL} – 0.05 | V _{DL} | V _{DL} + 0.05 | V | 1 |
| Overdischarge release voltage | V _{DU} | – | V _{DU} – 0.10 | V _{DU} | V _{DU} + 0.10 | V | 1 |
| CDT pin resistance*1 | R _{CDT} | V _{DS} = 3.5 V, V _{CDDT} = 0 V | 4.76 | 8.31 | 10.9 | MΩ | 2 |
| CDT pin detection voltage*1 | V _{CDET} | V _{DS} = 3.5 V | V _{DS} × 0.65 | V _{DS} × 0.70 | V _{DS} × 0.75 | V | 3 |
| Operating voltage between VDD and VSS | V _{DSOP} | Output voltage of CO pin, DO pin and CB pin are determined | 1.5 | – | 8.0 | V | – |
| CTLCH pin H voltage | V _{CTLCH} | V _{DS} = 3.5 V | V _{DS} × 0.55 | – | V _{DS} × 0.90 | V | 4 |
| CTLDH pin H voltage | V _{CTLDH} | V _{DS} = 3.5 V | V _{DS} × 0.55 | – | V _{DS} × 0.90 | V | 4 |
| CTLCL pin L voltage | V _{CTLCL} | V _{DS} = 3.5 V | V _{DS} × 0.10 | – | V _{DS} × 0.45 | V | 4 |
| CTLDL pin L voltage | V _{CTLDL} | V _{DS} = 3.5 V | V _{DS} × 0.10 | – | V _{DS} × 0.45 | V | 4 |
| Current consumption during operation*2 | I _{OPE} | V _{DS} = 3.5 V | – | 3.5 | 7.0 | μA | 5 |
| Sink current CTLCH*2 | I _{CTLCL} | V _{DS} = 3.5 V, V _{CTLCH} = 3.5 V | 320 | 400 | 480 | nA | 6 |
| Sink current CTLDH*2 | I _{CTLDL} | V _{DS} = 3.5 V, V _{CTLDH} = 3.5 V | 320 | 400 | 480 | nA | 6 |
| Source current CB | I _{CBH} | V _{CB} = 4.0 V, V _{DS} = 4.5 V | 30 | – | – | μA | 7 |
| Sink current CB | I _{CBL} | V _{CB} = 0.5 V, V _{DS} = 3.5 V | 30 | – | – | μA | 7 |
| Source current CO | I _{COH} | V _{CO} = 3.0 V, V _{DS} = 3.5 V | 30 | – | – | μA | 7 |
| Leakage current CO | I _{COL} | V _{CO} = 24 V, V _{DS} = 4.5 V | – | – | 0.1 | μA | 8 |
| Source current DO | I _{DOH} | V _{DO} = 3.0 V, V _{DS} = 3.5 V | 30 | – | – | μA | 7 |
| Leakage current DO | I _{DOL} | V _{DO} = 24 V, V _{DS} = 1.8 V | – | – | 0.1 | μA | 8 |

*1. In the S-8209B Series, users are able to set delay time for the output pins. By using the following formula, delay time is calculated with the value of CDT pin's resistance in the IC (R_{CDT}) and the value of capacitor set externally at the CDT pin (C_{CDT}).

$$\begin{aligned}
 t_D [s] &= -\ln(1 - V_{CDET} / V_{DS}) \times C_{CDT} [\mu F] \times R_{CDT} [M\Omega] \\
 &= -\ln(1 - 0.7 \text{ (typ.)}) \times C_{CDT} [\mu F] \times 8.31 \text{ M}\Omega \text{ (typ.)} \\
 &= 10.0 \text{ M}\Omega \text{ (typ.)} \times C_{CDT} [\mu F]
 \end{aligned}$$

In case of the capacitance of CDT pin C_{CDT} = 0.01 μF, the output pin delay time t_D is calculated by using the above formula and as follows.

$$t_D [s] = 10.0 \text{ M}\Omega \text{ (typ.)} \times 0.01 \mu F = 0.1 \text{ s (typ.)}$$

Test R_{CDT} and the CDT pin detection voltage (V_{CDET}) by test circuits shown in this datasheet after applying the power supply while pulling-up the CTLCH pin, CTLDH pin to the level of VDD pin outside the IC.

*2. In case of using CTLCH pin, CTLDH pin pulled-up to the level of VDD pin externally, the current flows from the VSS pin (I_{SS}) is calculated by the following formula.

$$I_{SS} = I_{OPE} + I_{CTLCL} + I_{CTLDL}$$

■ **Test Circuits**

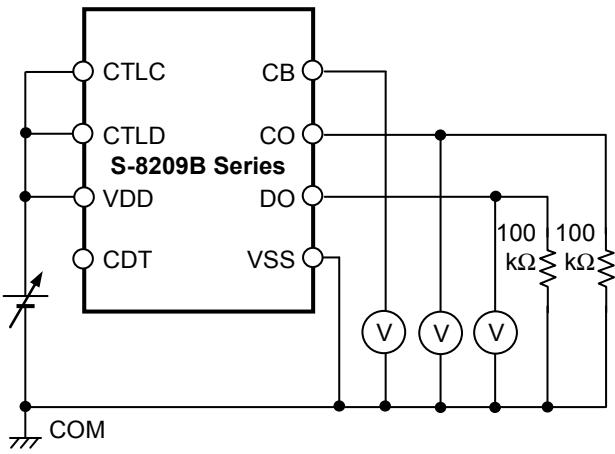


Figure 7 Test circuit 1

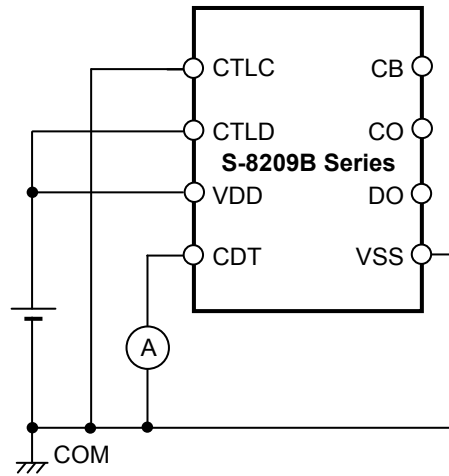


Figure 8 Test circuit 2

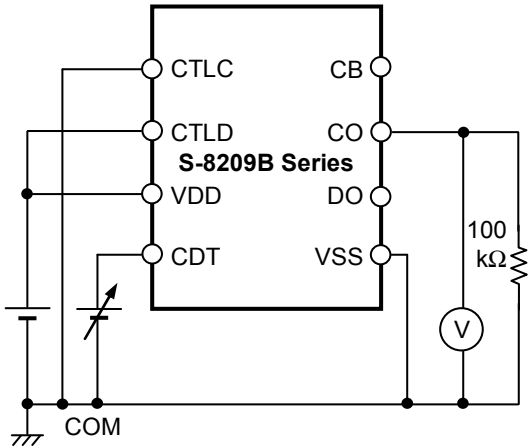


Figure 9 Test circuit 3

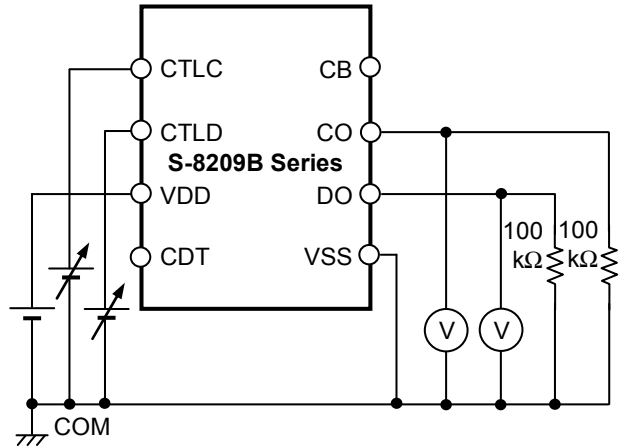


Figure 10 Test circuit 4

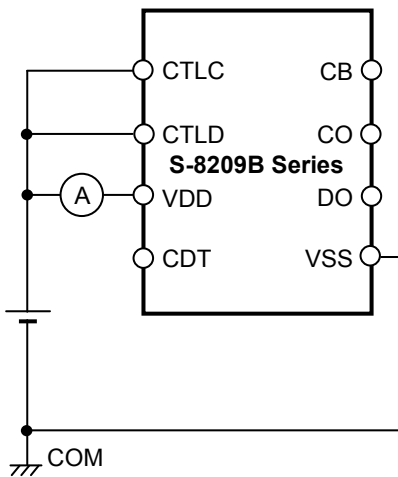


Figure 11 Test circuit 5

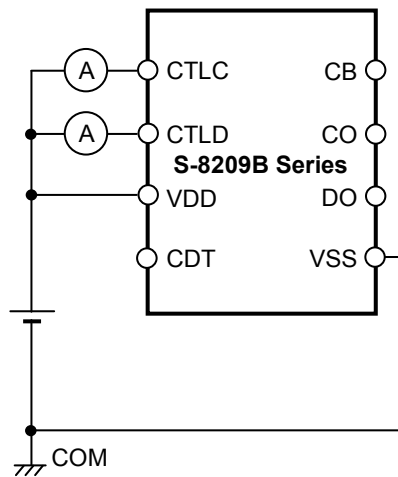


Figure 12 Test circuit 6

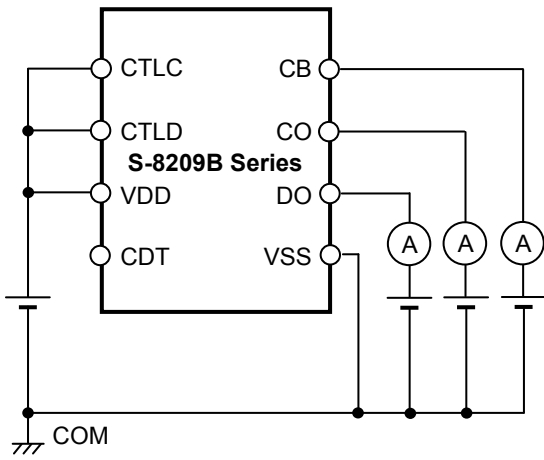


Figure 13 Test circuit 7

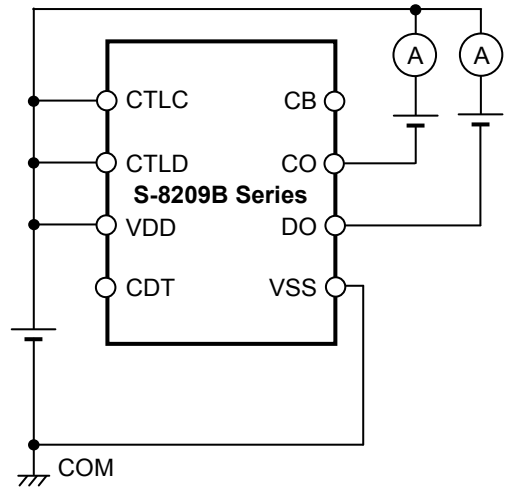


Figure 14 Test circuit 8

■ **Operation**

Figure 15 shows the operation transition of the S-8209B Series

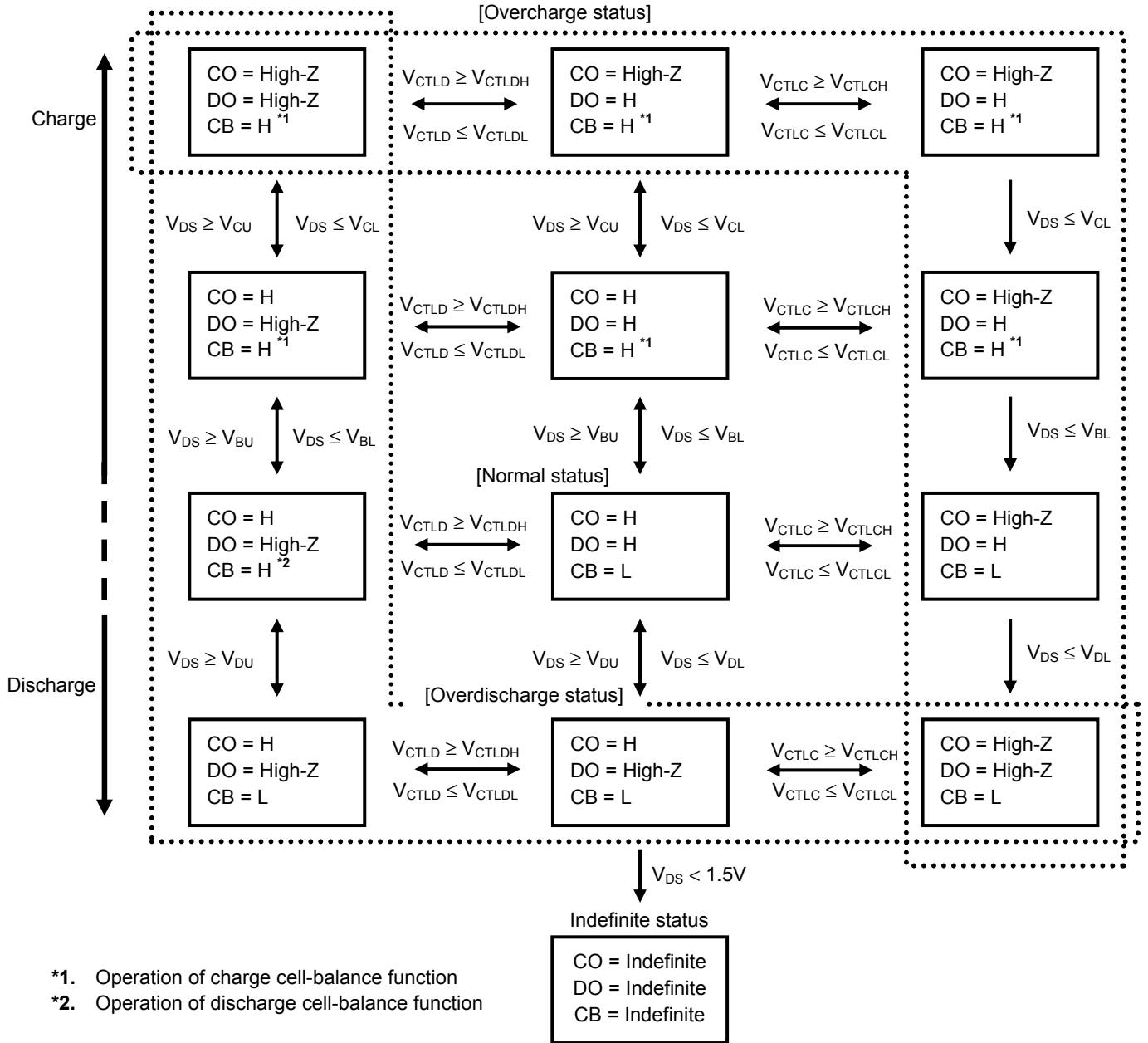


Figure 15 Operation Transition

1. Normal status

In the S-8209B Series, both of CO and DO pin get the V_{DD} level; the voltage between V_{DD} and V_{SS} (V_{DS}) is more than the overdischarge detection voltage (V_{DL}), and is less than the overcharge detection voltage (V_{CU}) and respectively, the CTLC pin input voltage (V_{CTLC}) > the CTLC pin voltage "L" ($V_{CTLC(L)}$), the CTLD pin input voltage (V_{CTLD}) > the CTLD pin voltage "L" ($V_{CTLD(L)}$). This is the normal status.

2. Overcharge status

In the S-8209B Series, the CO pin is in high impedance; when V_{DS} gets V_{CU} or more, or V_{CTLC} gets $V_{CTLC(L)}$ or less. This is the overcharge status.

If V_{DS} gets the overcharge release voltage (V_{CL}) or less, and V_{CTLC} gets the CTLC pin voltage "H" ($V_{CTLC(H)}$) or more, the S-8209B Series releases the overcharge status to return to the normal status.

3. Overdischarge status

In the S-8209B Series, the DO pin is in high impedance; when V_{DS} gets V_{DL} or less, or V_{CTLD} gets $V_{CTLD(L)}$ or less. This is the overdischarge status.

If V_{DS} gets the overdischarge release voltage (V_{DU}) or more, and V_{CTLD} gets the CTLD pin voltage "H" ($V_{CTLD(H)}$) or more, the S-8209B Series releases the overdischarge status to return to the normal status.

4. Cell-balance function

In the S-8209B Series, the CB pin gets the level of V_{DD} pin; when V_{DS} gets the cell-balance detection voltage (V_{BU}) or more. This is the charge cell-balance function.

If V_{DS} gets the cell-balance release voltage (V_{BL}) or less again, the S-8209B Series sets the CB pin the level of V_{SS} pin.

In addition, the CB pin gets the level of V_{DD} pin; when V_{DS} is more than V_{DL} , and V_{CTLD} is $V_{CTLD(L)}$ or less. This is the discharge cell-balance function.

If V_{CTLD} gets $V_{CTLD(H)}$ or more, or V_{DS} is V_{DL} or less again, the S-8209B Series sets the CB pin the level of V_{SS} pin.

5. Delay circuit

In the S-8209B Series, users are able to set delay time which is from detection of changes in V_{DS} , V_{CTLC} , V_{CTLD} to output to the CO, DO, CB pin.

For example in the detection of overcharge status, when V_{DS} exceeds V_{CU} , or V_{CTLC} gets $V_{CTLC(L)}$ or less, charging to C_{CDT} starts via R_{CDT} . If the voltage between CDT and V_{SS} (V_{CDT}) reaches the CDT pin detection voltage (V_{CDET}), the CO pin is in high impedance. The output pin delay time t_D is calculated by the following formula.

$$t_D [s] = 10.0 \text{ M}\Omega (\text{typ.}) \times C_{CDT} [\mu\text{F}]$$

The electric charge in C_{CDT} starts to be discharged when the delay time has finished.

The delay time that users have set for the CO pin, as seen above, is settable for each output pin DO, CB.

■ Battery Protection IC Connection Examples

Regarding the operation of protection circuit with the S-8209B Series for series-connected batteries, refer to the application note "S-8209B Series Usage Guidelines".

1. Example of Protection Circuit with the S-8209B Series (Without Discharge Cell-balance Function) for Series Multi-Cells

Figure 16 shows the example of protection circuit with the S-8209B Series (without discharge cell-balance function) for series multi-cells.

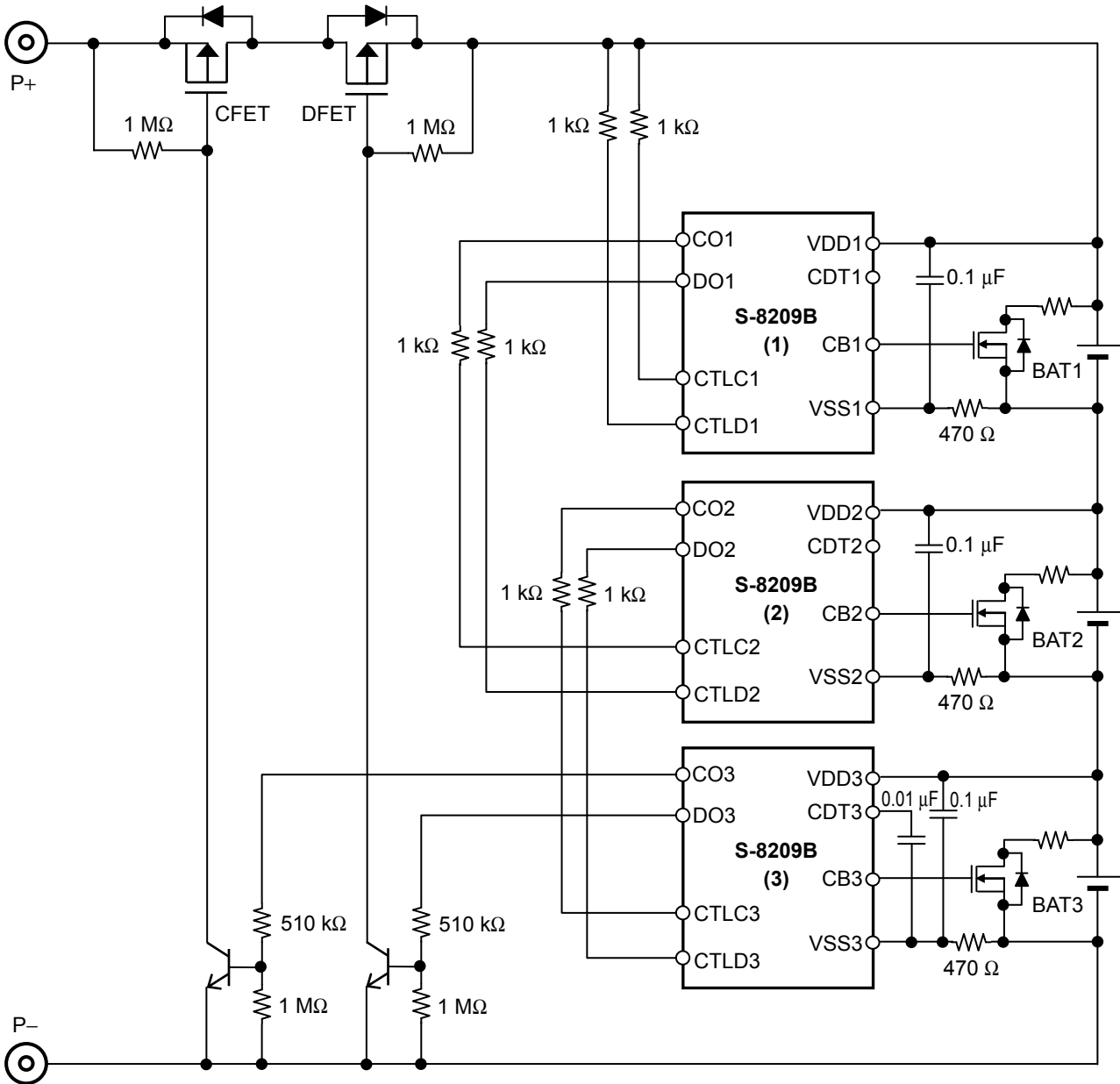


Figure 16

- Caution 1.** The above constants may be changed without notice.
2. The example of connection shown above and the constant do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constant.

2. Example of Protection Circuit with the S-8209B Series (With Discharge Cell-balance Function) for Series Multi-Cells

Figure 17 shows the example of protection circuit with the S-8209B Series (with discharge cell-balance function) for series multi-cells.

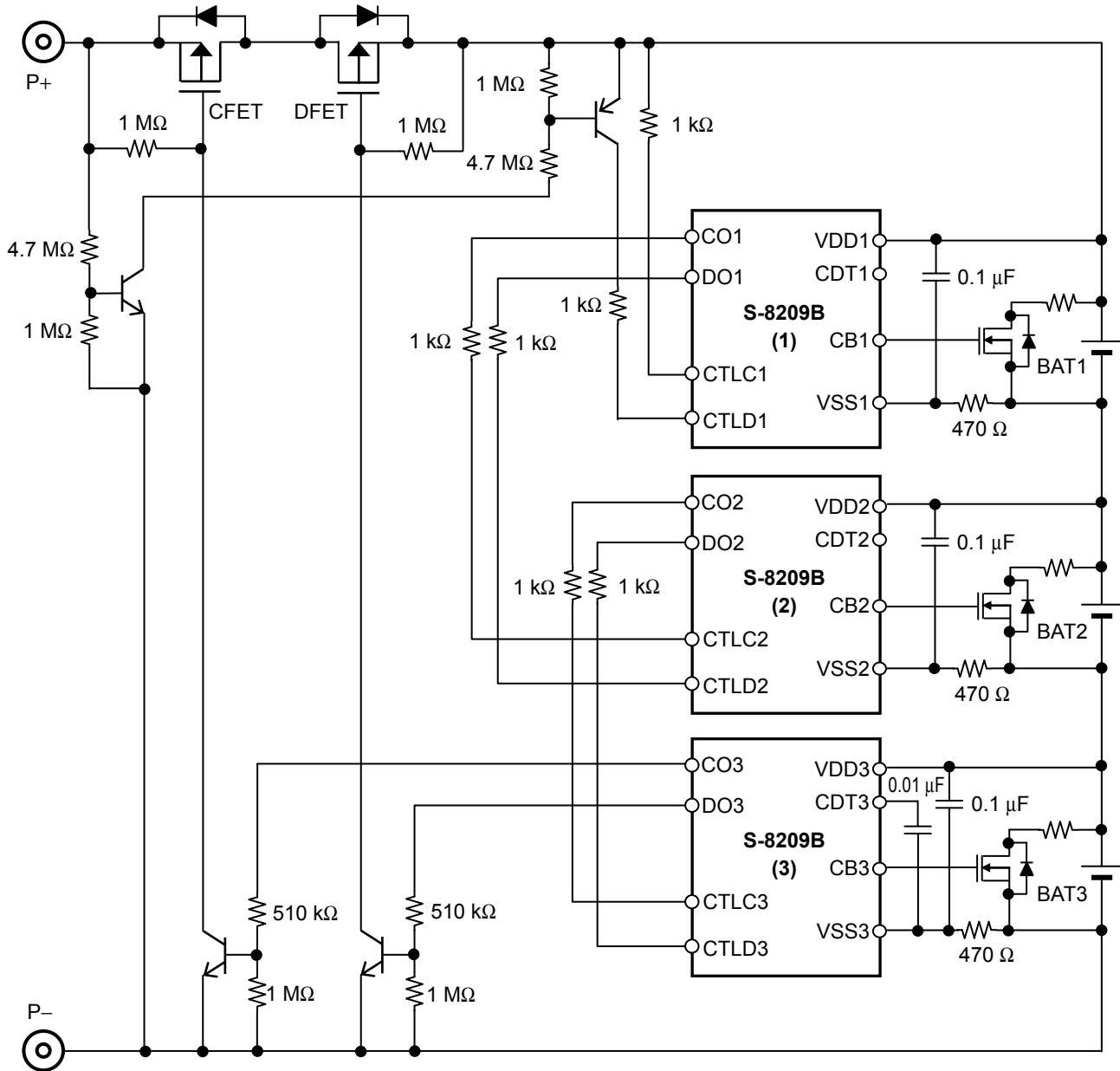


Figure 17

- Caution 1.** The above constants may be changed without notice.
2. The example of connection shown above and the constant do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constant.

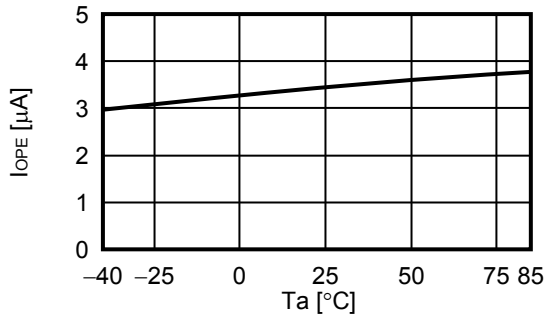
■ Precautions

- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- SII Semiconductor Corporation claims no responsibility for any and all disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

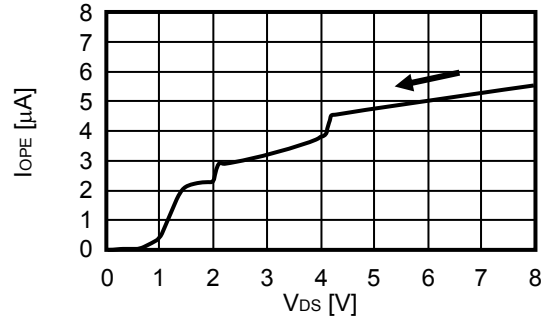
■ **Characteristics (Typical Data)**

1. Current consumption

1.1 I_{OPe} vs. T_a

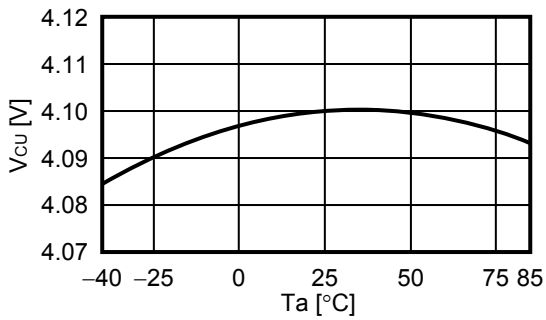


1.2 I_{OPe} vs. V_{Ds}

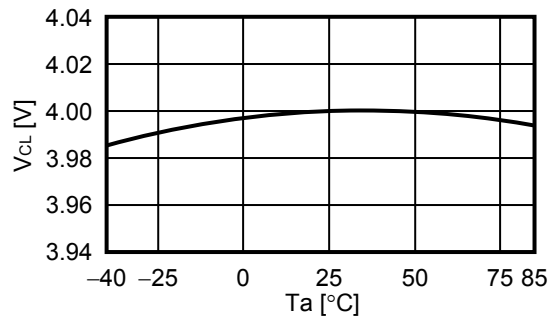


2. Overcharge detection / release voltages, Cell-balance detection / release voltages, Overdischarge detection / release voltages

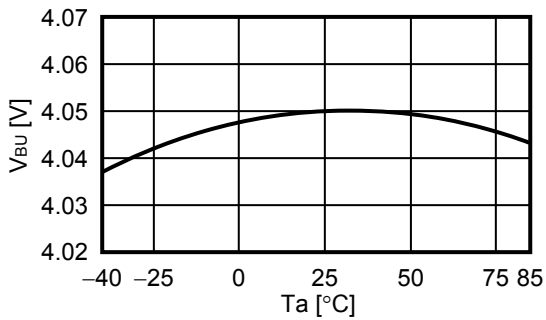
2.1 V_{CU} vs. T_a



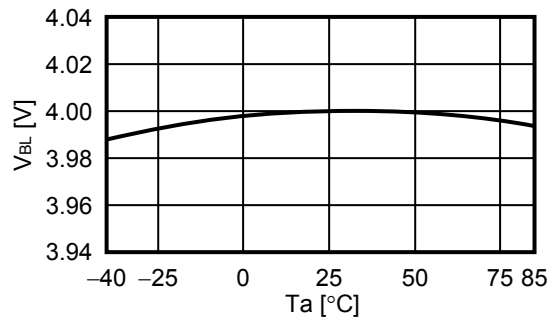
2.2 V_{CL} vs. T_a



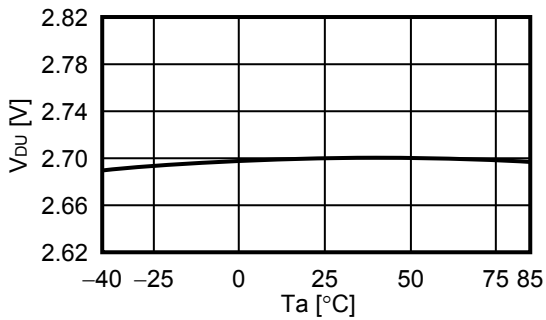
2.3 V_{BU} vs. T_a



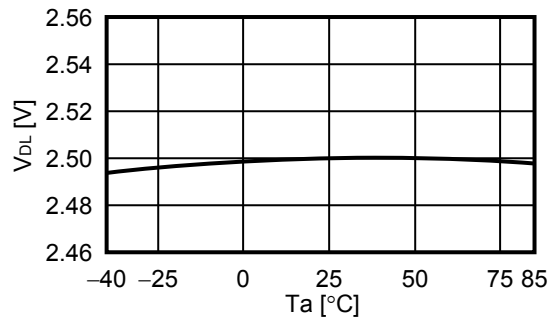
2.4 V_{BL} vs. T_a



2.5 V_{DU} vs. T_a

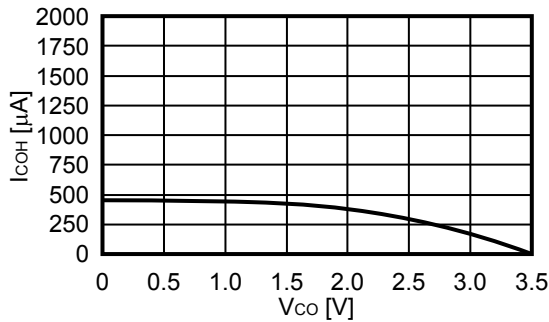


2.6 V_{DL} vs. T_a

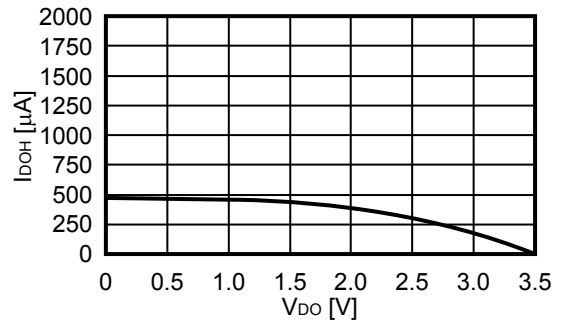


3. CO / DO / CB pin current

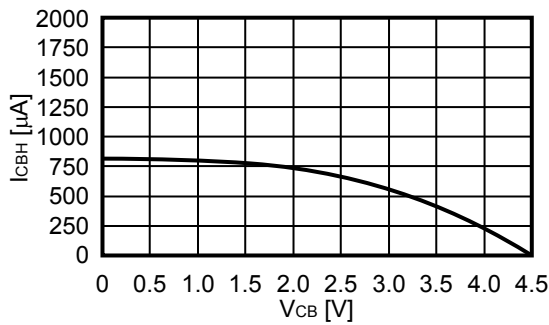
3.1 I_{COH} vs. V_{CO} (V_{DS} = 3.5 V)



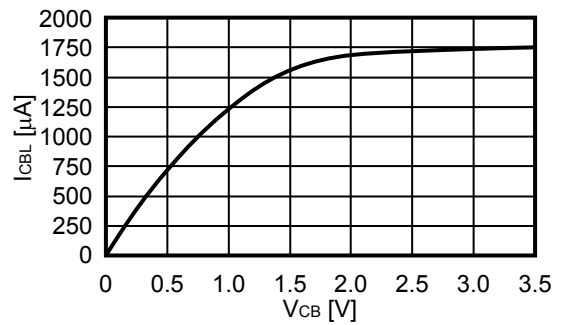
3.2 I_{DOH} vs. V_{DO} (V_{DS} = 3.5 V)



3.3 I_{CBH} vs. V_{CB} (V_{DS} = 4.5 V)

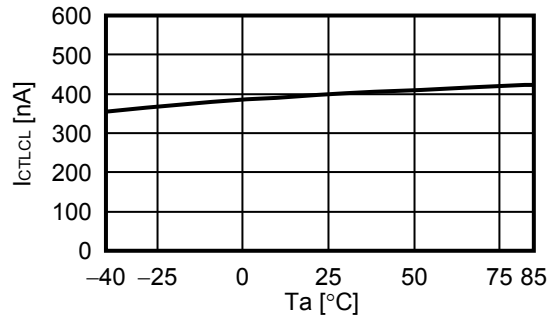


3.4 I_{CBL} vs. V_{CB} (V_{DS} = 3.5 V)

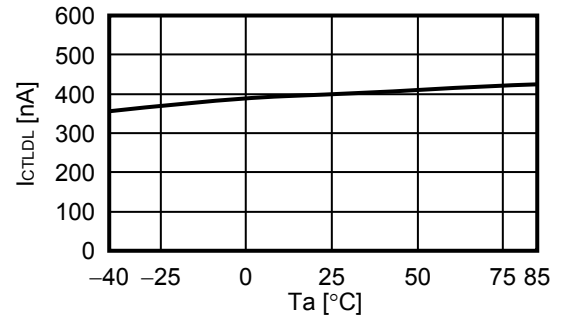


4. CTLC / CTLD pin current

4.1 I_{CTLCL} vs. Ta (V_{DS} = 3.5 V)

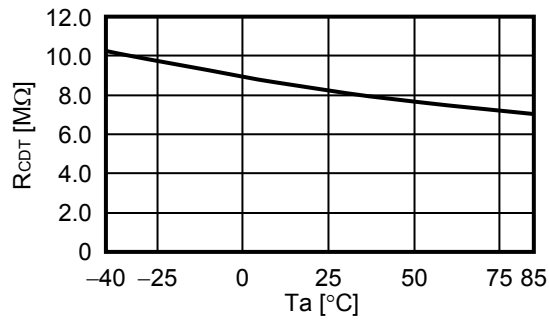


4.2 I_{CTLDL} vs. Ta (V_{DS} = 3.5 V)

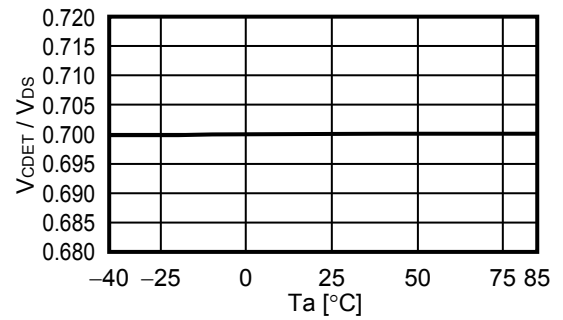


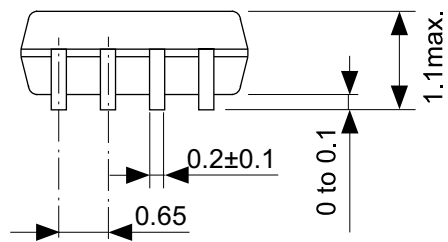
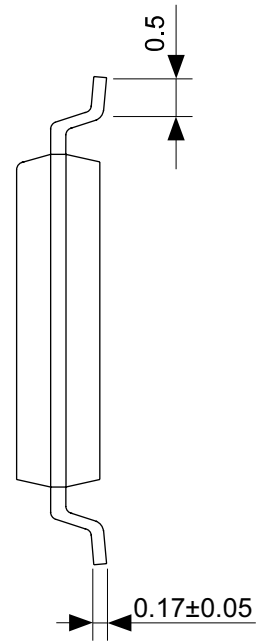
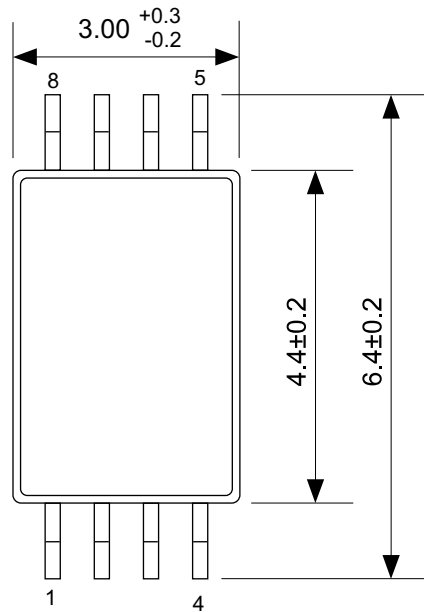
5. CDT pin resistance / CDT pin detection voltage

5.1 R_{CDT} vs. Ta



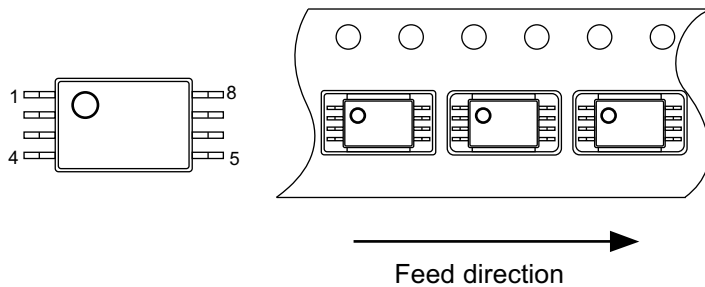
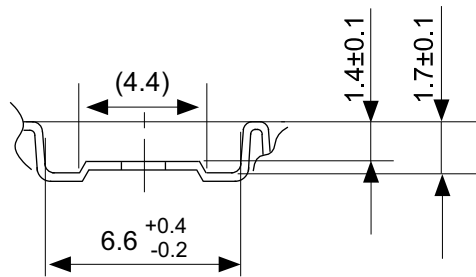
5.2 V_{CDDET} / V_{DS} vs. Ta





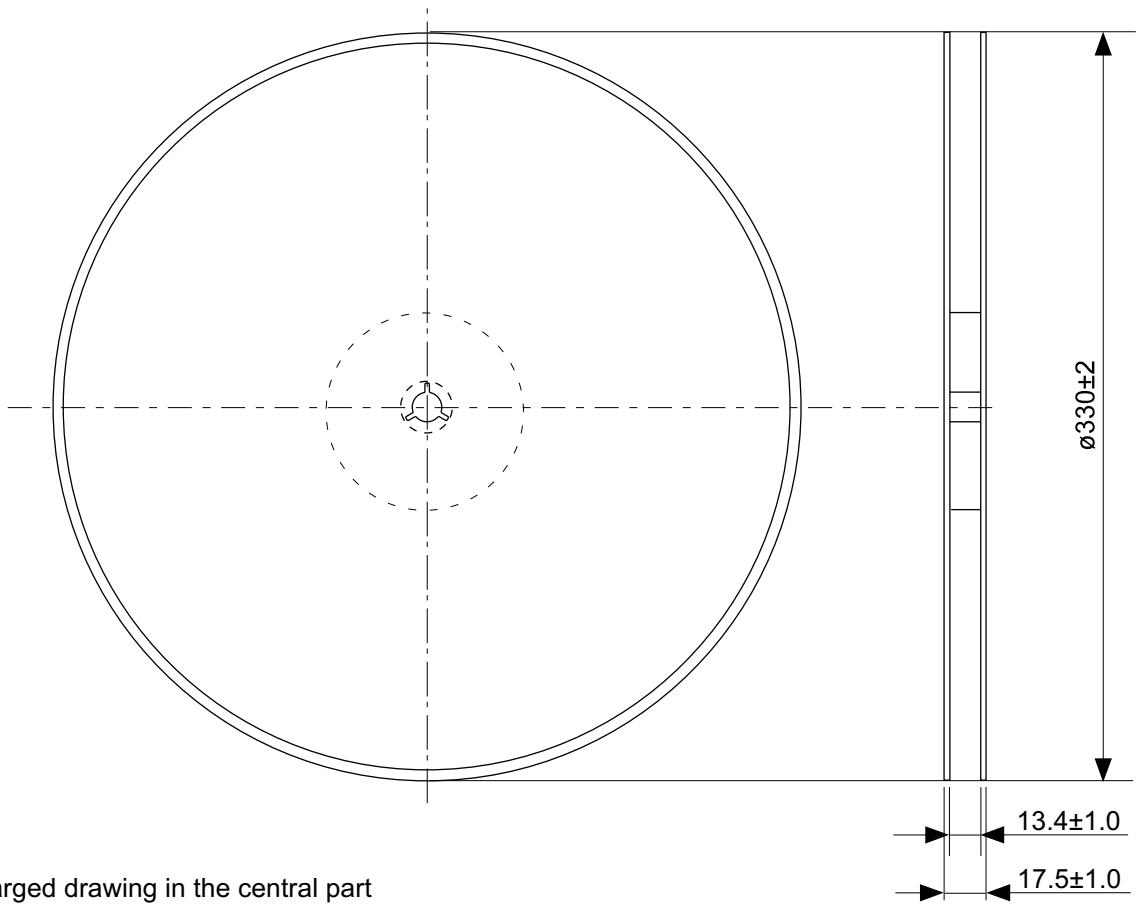
No. FT008-A-P-SD-1.1

| | |
|-------------------------------|-------------------------|
| TITLE | TSSOP8-E-PKG Dimensions |
| No. | FT008-A-P-SD-1.1 |
| SCALE | |
| UNIT | mm |
| | |
| SII Semiconductor Corporation | |

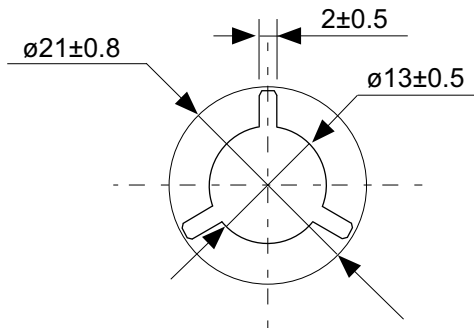


No. FT008-E-C-SD-1.0

| | |
|-------------------------------|-----------------------|
| TITLE | TSSOP8-E-Carrier Tape |
| No. | FT008-E-C-SD-1.0 |
| SCALE | |
| UNIT | mm |
| SII Semiconductor Corporation | |

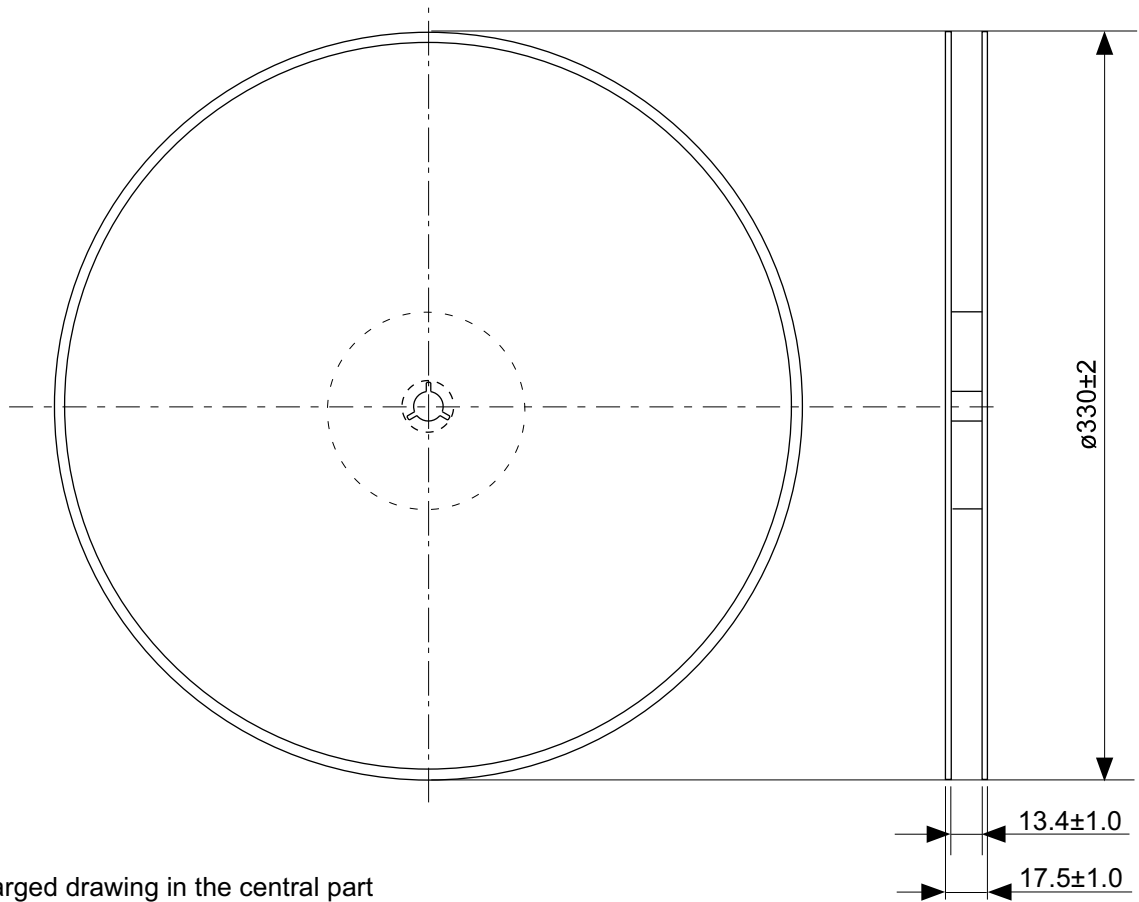


Enlarged drawing in the central part

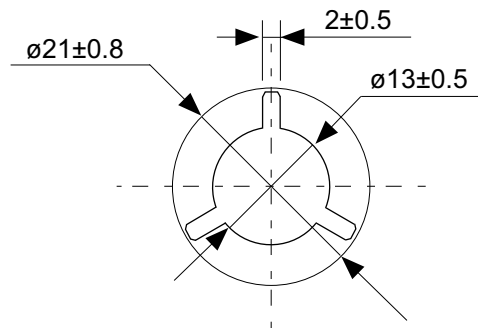


No. FT008-E-R-SD-1.0

| | | | |
|-------------------------------|------------------|------|-------|
| TITLE | TSSOP8-E-Reel | | |
| No. | FT008-E-R-SD-1.0 | | |
| SCALE | | QTY. | 3,000 |
| UNIT | mm | | |
| | | | |
| SII Semiconductor Corporation | | | |

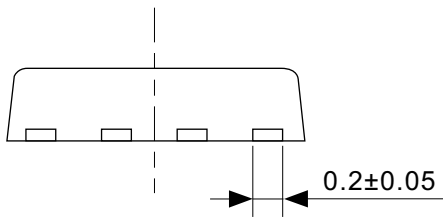
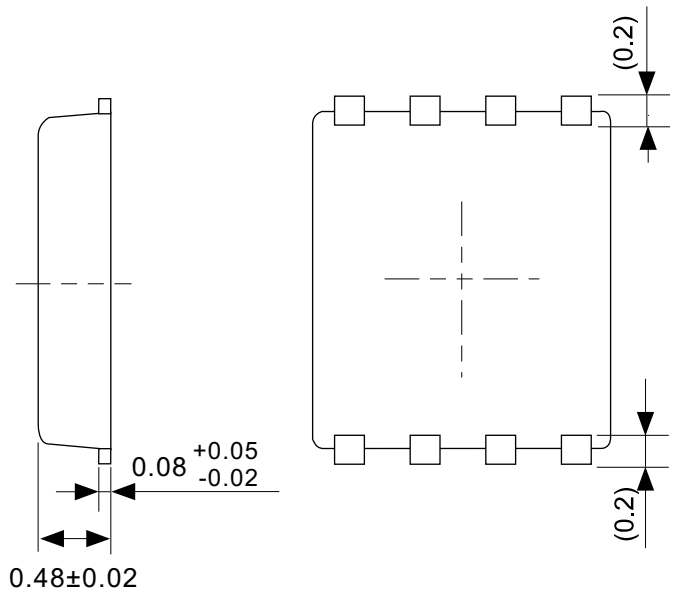
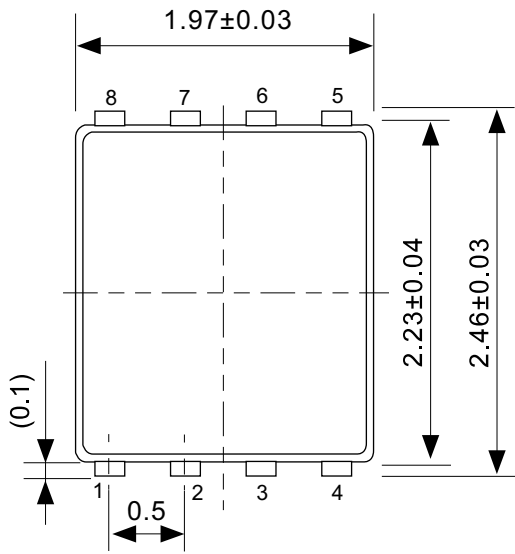


Enlarged drawing in the central part



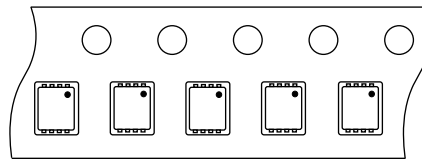
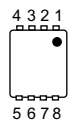
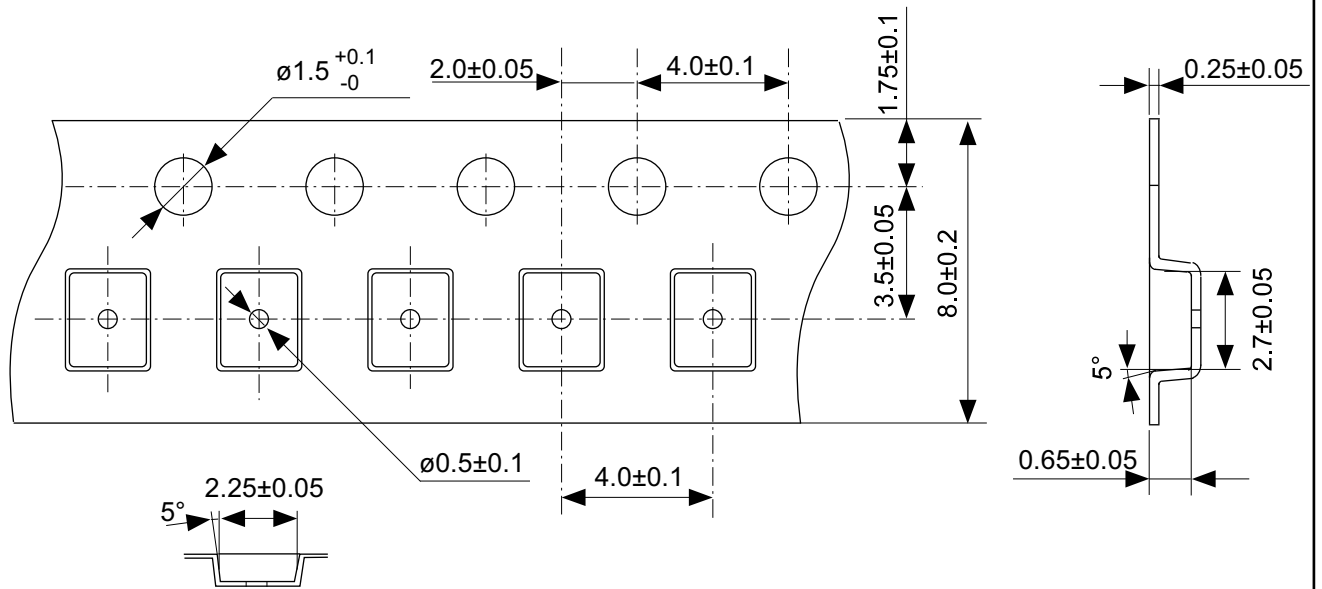
No. FT008-E-R-S1-1.0

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|-------------------------------|------------------|------|-------|
| TITLE | TSSOP8-E-Reel | | |
| No. | FT008-E-R-S1-1.0 | | |
| SCALE | | QTY. | 4,000 |
| UNIT | mm | | |
| | | | |
| SII Semiconductor Corporation | | | |



No. PH008-A-P-SD-2.0

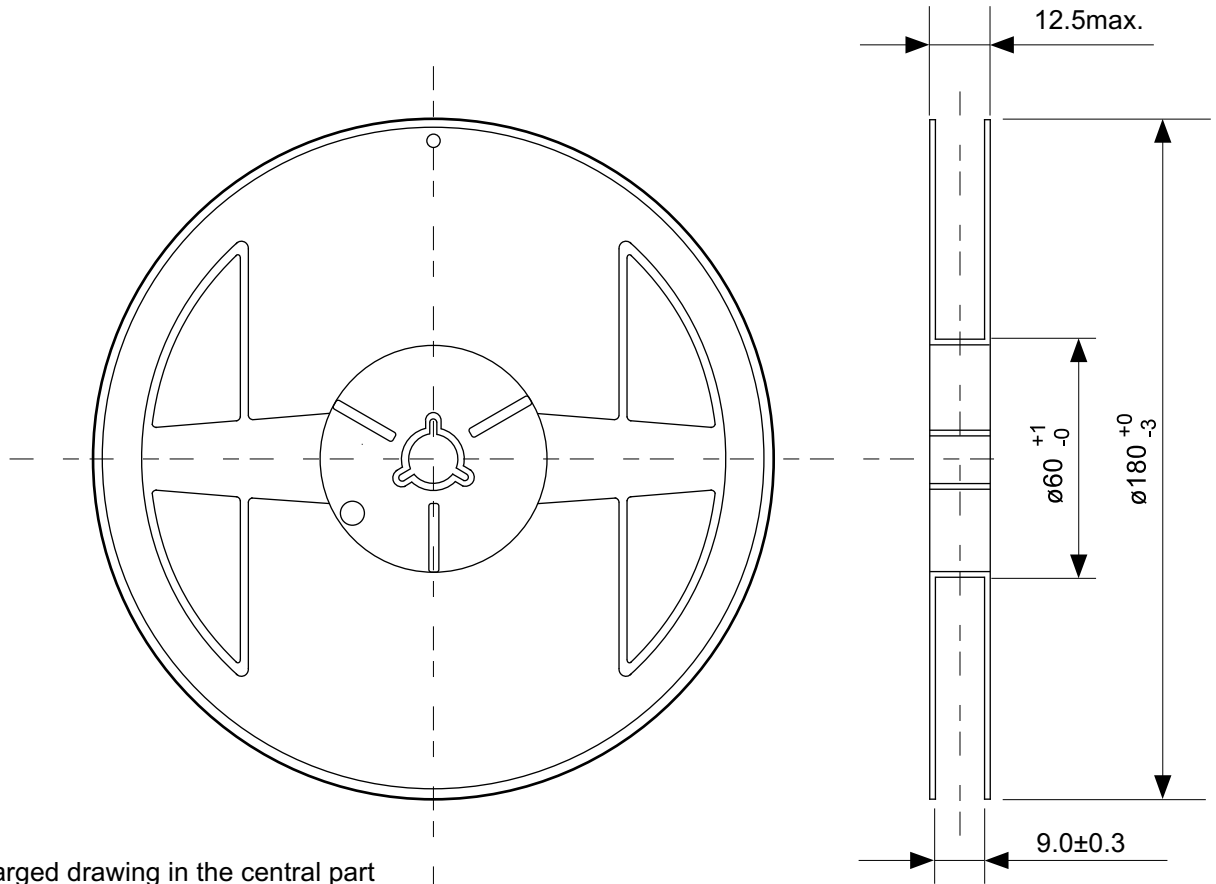
| | |
|-------------------------------|-------------------------|
| TITLE | SNT-8A-A-PKG Dimensions |
| No. | PH008-A-P-SD-2.0 |
| SCALE | |
| UNIT | mm |
| | |
| SII Semiconductor Corporation | |



Feed direction

No. PH008-A-C-SD-1.0

| | |
|-------------------------------|-----------------------|
| TITLE | SNT-8A-A-Carrier Tape |
| No. | PH008-A-C-SD-1.0 |
| SCALE | |
| UNIT | mm |
| | |
| SII Semiconductor Corporation | |



Enlarged drawing in the central part



No. PH008-A-R-SD-1.0

| | | | |
|-------------------------------|------------------|------|-------|
| TITLE | SNT-8A-A-Reel | | |
| No. | PH008-A-R-SD-1.0 | | |
| SCALE | | QTY. | 5,000 |
| UNIT | mm | | |
| | | | |
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