TEXAS INSTRUMENTS

SN65DPHY440SS, SN75DPHY440SS

SLLSEO9A – MARCH 2016 – REVISED APRIL 2016

SNx5DPHY440SS CSI-2/DSI DPHY Re-timer

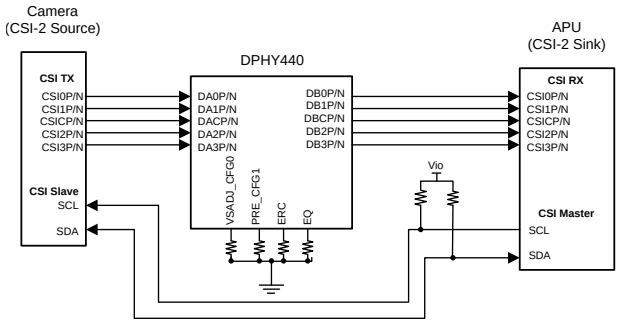
1 Features

- MIPI DPHY 1.1 Specification Compliant
- Enables Low-cost Cable Solutions
- Supports up to 4 Lanes at 1 Gbps
  - CSI-2/DSI Clock Rates From 100 MHz to 500 MHz
- Sub mW Power in Shutdown State
- MIPI DSI Bi-Directional LP Mode Supported
- Supports for Both ULPS and LP Power States
- Adjustable Output Voltage Swing
- Selectable TX Pre-emphasis Levels
- Adjustable Rx EQ to Compensate for ISI Loss
- Configurable Edge Rate Control
- Dynamic Data and Clock Skew Compensation
- 3-kV ESD HBM Protection
- Industrial Temperature Range: –40°C to 85°C (SN65DPHY440SS)
- Commercial Temperature Range: 0°C to 70°C (SN75DPHY440SS)
- Available in Single 1.8-V Supply

2 Applications

- Notebook PC
- Clam Shell
- Tablets
- Camera

Simplified Schematic



3 Description

The DPHY440 is a one to four lane and clock MIPI DPHY re-timer that regenerates the DPHY signaling. The device complies with MIPI DPHY 1.1 standard and can be used in either a MIPI CSI-2 or MIPI DSI application at datarates of up to 1 Gbps.

The device compensates for PCB, connector, and cable related frequency loss and switching related loss to provide the optimum electrical performance from a CSI2/DSI source to sink. The DPHY440's DPHY inputs feature configurable equalizers.

The output pins automatically compensate for uneven skew between clock and data lanes received on its inputs ports. The DPHY440 output voltage swing and edge rate can be adjusted by changing the state of the VSADJ_CFG0 pin and ERC pin respectively.

The DPHY440 is optimized for mobile applications, and contains activity detection circuitry on the DPHY Link interface that can transition into a lower power mode when in ULPS and LP states.

The SN65DPHY440SS is characterized for an industrial temperature range from -40ºC to 85ºC while SN75DPHY440SS is characterized for commercial temperature range from 0ºC to 70ºC.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65DPHY440SS SN75DPHY440SS	WQFN (28)	3.50 mm x 5.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application

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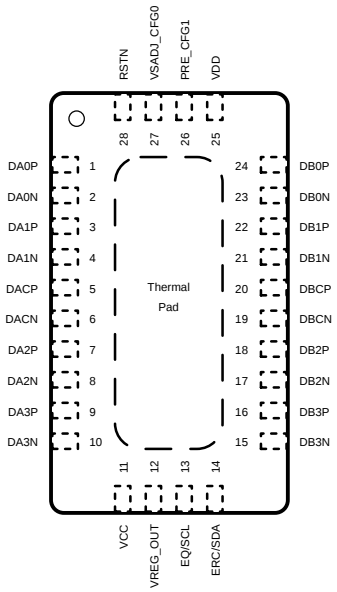
4 Revision History

Changes from Original (March 2016) to Revision A **Page**

- Changed Features From: 3-kV ESD HBM Protection To: 2-kV ESD HBM Protection ... 1
- Changed From: (approx. 100K) To: (100K) in the *Pin Functions* table for pins 13 and 14 ... 3
- Changed From: (approx. 100K) To: (100K) in the *Pin Functions* table for pins 26, 27, and 28 ... 4
- Changed *ESD Ratings* values. HBM From: ±2000 To: ±3000, and CDM Form: ±500 To: ±1000 ... 5
- Changed $V_{(RXEQ2)}$ TYP value From: 5 dB To: 4 dB in the *Electrical Characteristics* table ... 6
- Added MIN and MAX values to $|V_{OD(VD0)}|$, $|V_{OD(VD1)}|$, and $|V_{OD(VD2)}|$ in the *Electrical Characteristics* table ... 6
- Deleted rows Z_{OS} and ΔZ_{OS} from the *Electrical Characteristics* table ... 7
- Updated the MIPI DPHY LP Transmitter Interface section of the Switching Characteristics table ... 8
- Changed 5 dB to 4 dB in *HS Receive Equalization* and Table 1 ... 11
- Changed 11 – 5 dB To: 11 – 4 dB in Table 8 ... 16

5 Pin Configuration and Functions

RHR Package
28 Pin (WQFN)
Top View



Pin Functions

PIN		I/O	INTERNAL PULLUP/PULLDOWN	DESCRIPTION
NAME	NO.			
DA0P	1	100-Ω Differential Input		CSI-2/DSI Lane 0 Differential positive Input. Supports DSI LP Backchannel. If unused, this pin should be tied to GND.
DA0N	2			CSI-2/DSI Lane 0 Differential negative Input. Supports DSI LP Backchannel. If unused, this pin should be tied to GND.
DA1P	3	100-Ω Differential Input (Failsafe)		CSI-2/DSI Lane 1 Differential positive Input. If unused, this pin should be tied to GND.
DA1N	4			CSI-2/DSI Lane 1 Differential negative input. If unused, this pin should be tied to GND.
DACP	5	100-Ω Differential Input (Failsafe)		CSI-2/DSI Differential Clock positive Input
DACN	6			CSI-2/DSI Differential Clock negative Input
DA2P	7	100-Ω Differential Input (Failsafe)		CSI-2/DSI Lane 2 Differential positive Input. If unused, this pin should be tied to GND.
DA2N	8			CSI-2/DSI Lane 2 Differential negative Input. If unused, this pin should be tied to GND.
DA3P	9	100-Ω Differential Input (Failsafe)		CSI-2/DSI Lane 3 Differential positive Input. If unused, this pin should be tied to GND.
DA3N	10			CSI-2/DSI Lane 3 Differential negative Input. If unused, this pin should be tied to GND.
VCC	11	Power		1.8V (±10%) Supply.
VREG_OUT	12	Power		1.2 V Regulator Output. Requires a 0.1 µF capacitor to GND.
EQ/SCL	13	I/O (3-level)	PU (100K) PD (100K)	RX Equalization Select. Pin state sampled on rising edge of RSTN. This pin also functions as I2C SCL pin. V_{IL} = 0 dB V_{IM} = 2.5 dB V_{IH} = 4 dB
ERC/SDA	14	I/O (3-level)	PU (100K) PD (100K)	Edge Rate Control for DB[4:0]P/N High speed transmitter rise and fall time. Pin state sampled on rising edge of RSTN. This pin also functions as I2C SDA pin. V_{IL} = 200 ps typical V_{IM} = 150 ps typical V_{IH} = 250 ps typical

Pin Functions (continued)

PIN		I/O	INTERNAL PULLUP/PULLDOWN	DESCRIPTION
NAME	NO.			
DB3N	15	100-Ω Differential Output		CSI-2/DSI Lane 3 Differential negative Output. If unused, this pin should be left unconnected.
DB3P	16			CSI-2/DSI Lane 3 Differential positive Output. If unused, this pin should be left unconnected.
DB2N	17	100-Ω Differential Output		CSI-2/DSI Lane 2 Differential negative Output. If unused, this pin should be left unconnected.
DB2P	18			CSI-2/DSI Lane 2 Differential positive Output. If unused, this pin should be left unconnected.
DBCN	19	100-Ω Differential Output		CSI-2/DSI Differential Clock negative Output
DBCP	20			CSI-2/DSI Differential Clock positive Output
DB1N	21	100-Ω Differential Output		CSI-2/DSI Lane 1 Differential negative Output. If unused, this pin should be left unconnected.
DB1P	22			CSI-2/DSI Lane 1 Differential positive Output. If unused, this pin should be left unconnected.
DB0N	23	100-Ω Differential Output		CSI-2/DSI Lane 0 Differential negative Output. Supports DSI LP Back channel. If unused, this pin should be left unconnected.
DB0P	24			CSI-2/DSI Lane 0 Differential positive Output. Supports DSI LP Back channel. If unused, this pin should be left unconnected.
VDD	25	Power		This pin must be connected to the VREG_OUT pin through at least a 10-mil trace and a 0.1 µF capacitor to ground.
PRE_CFG1	26	I/O (3-level)	PU (100K) PD (100K)	Controls DPHY TX HS pre-emphasis level and the LP TX rise and fall times. Pin state is sampled on the rising edge of RSTN. V_{IL} = 0 dB V_{IM} = 0 dB V_{IH} = 2.5 dB
VSADJ_CFG0	27	I (3-level)	PU (100K) PD (100K)	Controls output voltage swing for DB HS transmitters and the LP TX rise and fall times. Pin state is sampled on the rising edge of RSTN. Refer to Table 3 for details on voltage swing settings based on this pin and PRE_CFG1 sampled state. V_{IL} = 200 mV or 220 mV based on PRE_CFG1 sampled state. V_{IM} = 200 mV typical V_{IH} = 220 mV typical
RSTN	28	I	PU (300K)	Reset, active low. When low, all internal CSR are reset to default and DPHY440 is placed in low power state.
GND	Thermal pad	GND		Ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage range	V_{CC}	–0.3	2.175	V
Voltage range	DPHY Lane I/O Differential Voltage	–0.3	1.4	V
	RSTN	–0.3	2.175	V
	All other terminals	–0.3	2.175	V
Maximum junction temperature, T_J			105	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±3000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	1.62	1.8	1.98	V
T_A	Operating free-air temperature [SN65DPHY440SS]	–40		85	°C
	Operating free-air temperature [SN75DPHY440SS]	0		70	

6.4 Thermal Information

THERMAL METRIC (1)		SNx5DPHY440SS RHR (WQFN) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	42.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	12.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics, Power Supply

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
PACTIVE1_SS	Power under normal operation for 4 data lanes + clock.	DPHY Lanes at 1 Gbps; V_{CC} supply stable, V_{CC} = 1.8 V;		150		mW
PACTIVE2_SS	Power under normal operation for 2 data lanes + clock.	DPHY Lanes 1 Gbps; V_{CC} supply stable, V_{CC} = 1.8 V;		115		mW
PLP11_SS	LP11 Power	All DPHY lanes in LP11; V_{CC} supply stable; V_{CC} = 1.8 V;		14		mW
PRSTN_SS	RSTN Power	RSTN held in asserted state (low); V_{CC} supply stable; V_{CC} = 1.8 V;		0.75		mW

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Standard IO (RSTN, ERC, EQ, CFG[1:0])						
V_{IL}	Low-level control signal input voltage				0.2 x V_{CC}	V
V_{IM}	Mid-level control signal input voltage			V_{CC} / 2		V
V_{IH}	High-level control signal input voltage		0.8 x V_{CC}			V
V_F	Floating Voltage	V_{IN} = High Impedance		V_{CC} / 2		V
V_{OL}	Low level output voltage (open-drain). ERC (SDA) only	At I_{OL} max.			0.2 x V_{CC}	V
I_{OL}	Low Level Output Current				3	mA
I_{IH}	High level input current				±36	µA
I_{IL}	Low level input current				±36	µA
R_{PU}	Internal pull-up resistance			100		kΩ
R_{PD}	Internal pull-down resistance			100		kΩ
$R_{(RSTN)}$	RSTN control input pullup resistor			300		kΩ
MIPI Input Leakage (DA1P/N, DA2P/N, DA3P/N, DACP/N)						
I_{lkg}	Input failsafe leakage current	V_{CC} = 0 V; V_{DD} = 0 V; MIPI DPHY pulled up to 1.35 V	–65		65	µAV
MIPI DPHY HS RECIEVER INTERFACE (DA0P/N, DA1P/N, DA2P/N, DA3P/N, DACP/N)						
$V_{(CM\text{-}RX\_DC)}$	Differential Input Common-mode voltage HS Receive mode	$V_{(CM\text{-}RX)} = (V_{A\ x\ P} + V_{A\ x\ N})/2$	70		330	mV
$\lvert V_{ID} \rvert$	HS Receiver input differential input voltage	$\lvert V_{ID} \rvert = \lvert V_{A\ x\ P} – V_{A\ x\ N} \rvert$	70			mV
$V_{IH(HS)}$	Single-ended input high voltage				460	mV
$V_{IL(HS)}$	Single-ended input low voltage		–40			mV
$R_{(DIFF\text{-}HS)}$	Differential input impedance		80	100	125	Ω
$V_{(RXEQ0)}$	Rx EQ gain when EQ/SCL pin ≤ V_{IL}			0		dB
$V_{(RXEQ1)}$	Rx EQ gain when EQ/SCL pin = V_{IM}			2.5		dB
$V_{(RXEQ2)}$	Rx EQ gain when EQ/SCL pin ≥ V_{IH}			4		dB
MIPI DPHY LP Receiver Interface (DA0P/N, DA1P/N, DA2P/N, DA3P/N, DACP/N, DB0P/N)						
$V_{(LPIH)}$	LP Logic 1 Input Voltage		880			mV
$V_{(LPIL)}$	LP Logic 0 Input voltage				550	mV
$V_{(HYST)}$	LP Input Hysteresis		25			mV
MIPI DPHY HS Transmitter Interface (DB0P/N, DB1P/N, DB2P/N, DB3P/N, DBCP/N)						
$V_{(CMTX)}$	HS Transmit static common-mode voltage	$V_{(CMTX)} = (V_{(BP)} + V_{(BN)}) / 2$	150	200	300	mV
$\lvert \Delta V_{(CMTX)\ (1,0)} \rvert$	VCMTX mismatch when output is Differential-1 or differential-0.	$\Delta V_{(CMTX)\ (1,0)} = (V_{(CMTX)\ (1)} – V_{(CMTX)\ (0)}) /2$			5	mV
$\lvert V_{OD(VD0)} \rvert$	HS Transmit differential voltage for CFG0 = 2'b00 with TX pre-emphasis disabled or for non-transition bit when TX pre-emphasis is enabled.	$\lvert V_{OD} \rvert = \lvert V_{(DP)} - V_{(DN)} \rvert$	140	180	220	mV

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OD(VD1)}\|$	HS Transmit differential voltage for CFG0 = V_{IM} with TX pre-emphasis disabled or for non-transition bit when TX pre-emphasis is enabled.	$\|V_{OD}\| = \|V_{(DP)} - V_{(DN)}\|$ CFG0 = V_{IM}	160	200	250	mV
$\|V_{OD(VD2)}\|$	HS Transmit differential voltage for CFG0 = V_{IH} with TX pre-emphasis disabled or for non-transition bit when pre-emphasis is enabled..	$\|V_{OD}\| = \|V_{(DP)} - V_{(DN)}\|$ CFG0 ≥ V_{IH}	170	220	270	mV
$\|\Delta V_{OD}\|$	V_{OD} mismatch when output is differential-1 or differential-0.	$\Delta V_{OD} = \|\Delta V_{O(D1)}\| - \|\Delta V_{O(D0)}\|$			14	mV
$V_{OH(HS)}$	HS Output high voltage for non-transition bit.	CFG0 ≥ V_{IH} HS Pre = 2.5 dB			430	mV
$V_{(PRE1)}$	Pre-emphasis Level for HSTX_PRE = 2'b00.. Refer to Figure 3	PRE = 20 x LOG ($V_{OD(TBx)}$ / $V_{OD(VDX)}$)		1.5		dB
$V_{(PRE2)}$	Pre-emphasis level for HSTX_PRE = 2'b1X. Refer to Figure 3	PRE = 20 x LOG ($V_{OD(TBx)}$ / $V_{OD(VDX)}$)		2.5		dB
MIPI DPHY LP Transmitter Interface (DB0P/N, DB1P/N, DB2P/N, DB3P/N, DBCP/N, DA0P/N)						
$V_{(LPOH)}$	LP Output High Level		1.1	1.2	1.3	V
$V_{(LPOL)}$	LP Output Low Level		–50		50	mV
$V_{IH(CD)}$	LP Logic 1 contention threshold		450			mV
$V_{IL(CD)}$	LP Logc 0 contention threshold				200	mV
$Z_{O(LP)}$	Output Impedance of LP transmitter		110			Ω

6.7 Timing Requirements

			MIN	NOM	MAX	UNIT
I2C (ERC (SDA), EQ (SCL))						
$t_{HD;STA}$	Hold Time (repeated) START condition. After this period, the first clock pulse is generated		4			µs
t_{LOW}	Low period of SCL clock		4.7			µs
t_{HIGH}	High period of SCL clock		4			µs
$t_{SU;STA}$	Setup time for a repeated START condition		4.7			µs
$t_{HD;DAT}$	Data hold time		5			µs
$t_{SU;DAT}$	Data setup time		4			µs
$t_{SU;STO}$	Setup time for STOP condition		4			µs
t_{BUF}	Bus free time between a STOP and START condition		4.7			µs
MIPI DPHY HS Interface						
t_{HSPD}	Propagation delay from DA to DB.		4 + 12ns		4 + 40ns	UI
$t_{SKEW-TX}$	Data to Clock variation from 0.5UI. Refer to Figure 2	Datarate ≤ 1 Gbps	–0.1		0.1	UI
$t_{SETUP-RX}$	Data to Clock setup time. Refer to Figure 2	Datarate ≤ 1 Gbps	0.15			UI
$t_{HOLD-RX}$	Clock to data hold time. Refer to Figure 2	Datarate ≤ 1 Gbps	0.15			UI

6.8 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
I2C (ERC (SDA), EQ (SCL))						
$F_{(SCL)}$	I2C Clock Freqency				100	kHz
t_{F_I2C}	Fall time of both SDA and SCL signals	Load of 350 pF with 2-K pullup resistor. Measure at 30% - 70%			300	ns
t_{R_I2C}	Rise Time of both SDA and SCL signals				1000	ns
DPHY LINK						
$F_{(BR)}$	Bit Rate				1	Gbps
$F_{(HSCLK)}$	HS Clock Input range		100		500	µsMHz
$F_{(DESKEW)}$	Automatic Deskew range		220		500	MHz
MIPI DPHY HS Receiver Interface (DA0P/N, DA1P/N, DA2P/N, DA3P/N, DACP/N)						
$\Delta V_{(CMRX\_HF)}$	Common-mode Interface beyond 450 MHz				100	mV
$\Delta V_{(CMRX\_LF)}$	Common-mode interference 50 MHz – 450 MHz		–50		50	mV
MIPI DPHY HS Transmitter Interface (DB0P/N, DB1P/N, DB2P/N, DB3P/N, DBCP/N)						
$\Delta V_{(CMRX\_HF)}$	Common-level variations above 450 MHz				5	mVrms
$\Delta V_{(CMRX\_LF)}$	Common-level variation between 50 MHz – 450 MHz.				25	mVpeak
t_R and t_F	20% - 80% rise time and fall time	Datarate ≤ 1 Gbps			0.3	ns
			100			ns
MIPI DPHY LP Receiver Interface (DA0P/N, DA1P/N, DA2P/N, DA3P/N, DACP/N, DB0P/N)						
e_{SPIKE}	Input Pulse rejection				300	V ps
$t_{MIN(RX)}$	Minimum pulse width response		20			ns
$V_{(INT)}$	Peak interference amplitude				200	mv
$F_{(INT)}$	Interference Frequency		450			Mhz
$t_{(LP\text{-}PULSE\text{-}RX)}$	Pulse Width of the XOR of DAxP and DAxN	First LP XOR clock pulse after Stop state or last pulse before Stop state.	42			ns
		All other pulses.	22			ns
MIPI DPHY LP Transmitter Interface (DB0P/N, DB1P/N, DB2P/N, DB3P/N, DBCP/N, DA0P/N)						
t_{REOT}	30% - 85% rise time and fall time	Measured at end of HS transmission.			35	ns
$t_{(LP\text{-}PULSE\text{-}TX)}$	Pulse Width of the LP XOR clock	First LP XOR clock pulse after Stop state or last pulse before Stop state	40			ns
		All other pulses	20			ns
$t_{(LP\text{-}PER\text{-}TX)}$	Period of the LP XOR clock		90			ns
δV/δtsr	Slew Rate at C_{LOAD} = 70 pF				150	mV/ns
	Slew Rate at C_{LOAD} = 0 pF Fallng edge only		30			mV/ns
	Slew Rate at C_{LOAD} = 0 pF Rising edge only		30			mV/ns
C_{LOAD}	Load Capacitance				70	pF

(1) (1) All typical values are at V_{CC} = 3.3 V, and T_A = 25°C.

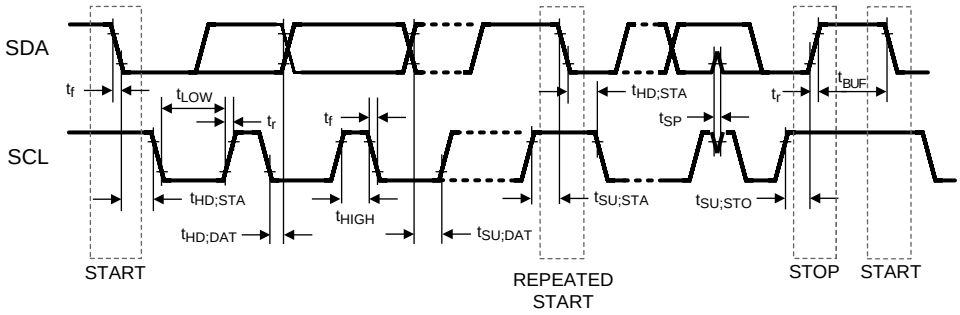


Figure 1. I²C Timing

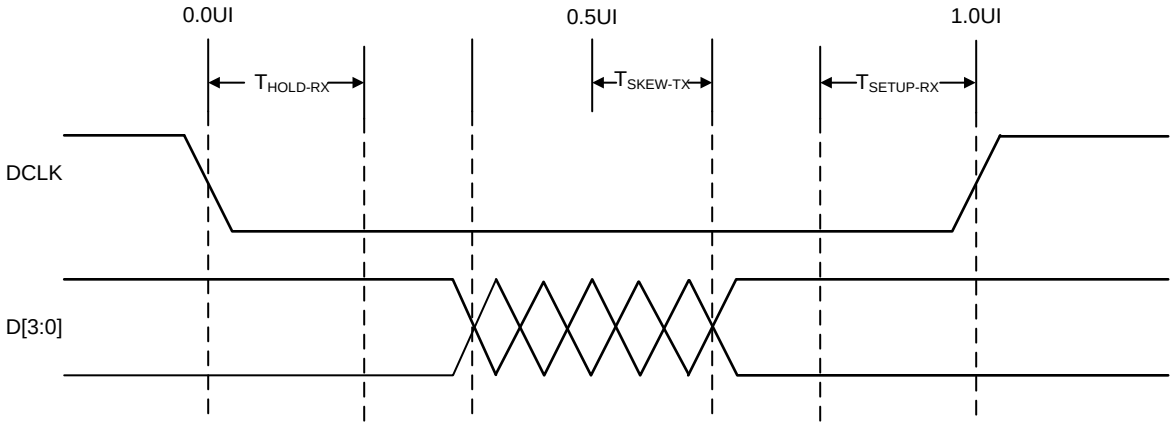


Figure 2. DPHY HS RX and TX Timing

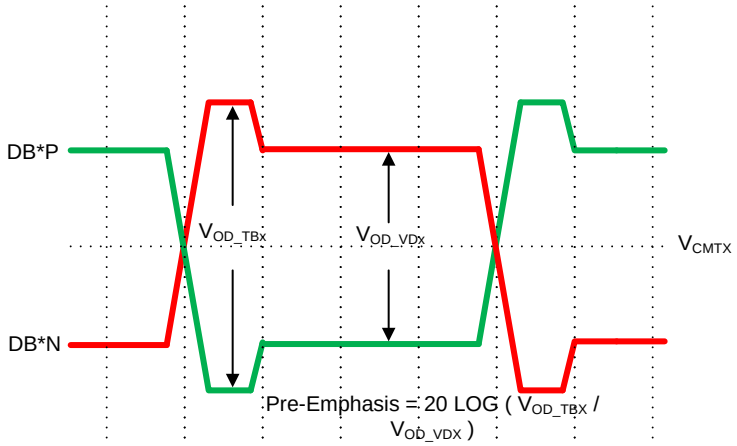


Figure 3. DPHY HS TX Pre-emphasis

6.9 Typical Characteristics

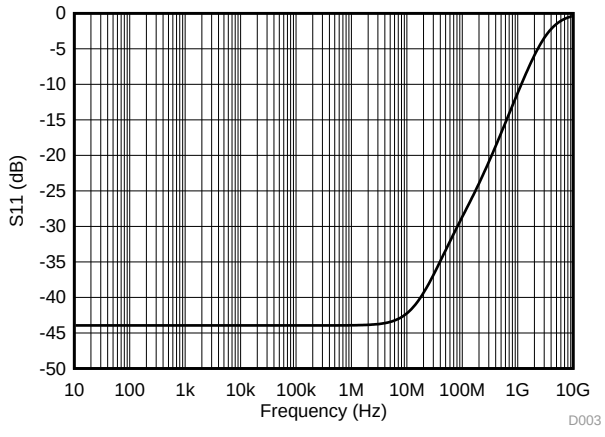


Figure 4. Return Loss (R_L), Transmitter

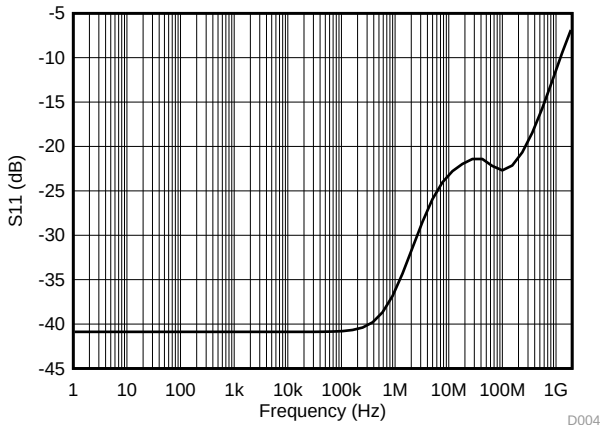


Figure 5. Return Loss (R_L), Receiver

7 Detailed Description

7.1 Overview

The DPHY440SS is a one to four lane and clock MIPI DPHY re-driver that regenerates the DPHY signaling. The device complies with MIPI DPHY 1.1 standard and can be used in either a MIPI CSI-2 or MIPI DSI application at datarates of up to 1 Gbps

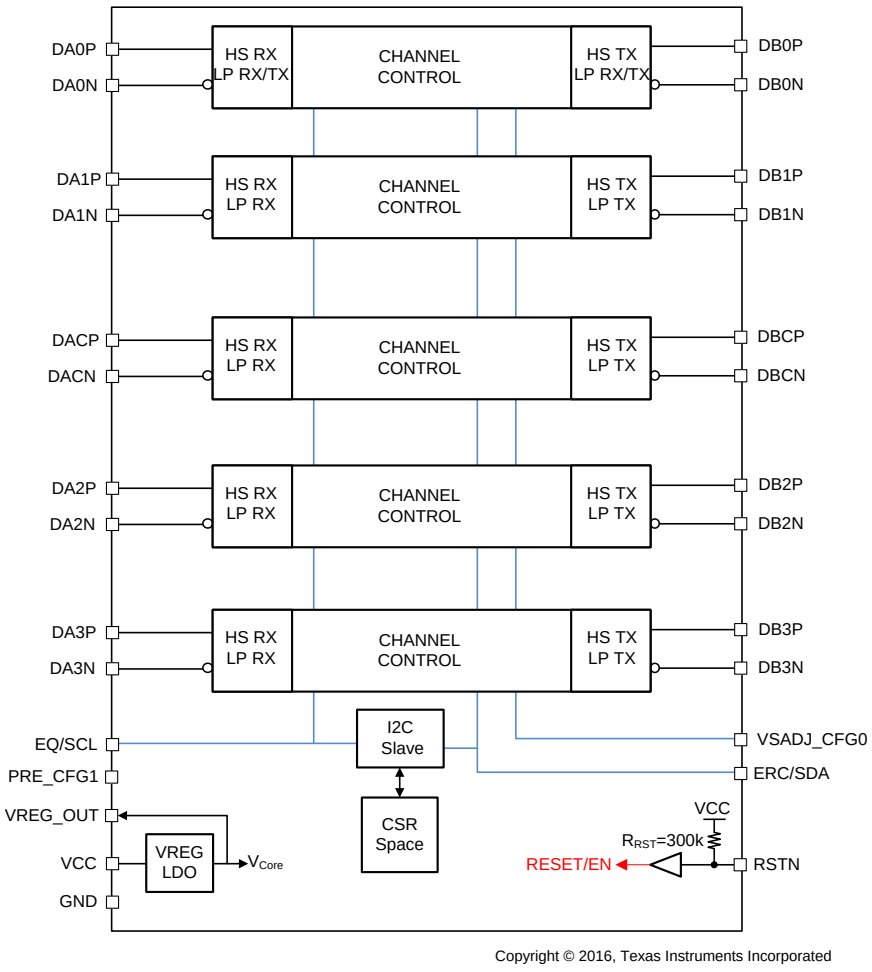
The device compensates for PCB, connector, and cable related frequency loss and switching related loss to provide the optimum electrical performance from a CSI2/DSI source to sink. The DPHY440 DPHY inputs feature configurable equalizers.

The output pins will automatically compensate for uneven skew between clock and data lanes. The DPHY440 output swing and edge rate can be adjusted by changing the state of the VSADJ_CFG0 pin and ERC pin respectively.

The DPHY440 is optimized for mobile applications, and contains activity detection circuitry on the DPHY Link interface that can transition into a lower power mode when in ULPS and LP states.

The device is characterized for an extended operational temperature range from –40ºC to 85ºC.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 HS Receive Equalization

The DPHY440 supports three levels of receive equalization to compensate for ISI loss in the channel. These three levels are 0dB, 2.5 dB, and 4 dB. The equalization level used by the DPHY440 is determined by the state of the EQ/SCL pin at the rising edge of RSTN. If necessary, the receiver equalization level can also be set through writing to the RXEQ register via the local I2C interface

Table 1. EQ/SCL pin Function

EQ/SCL PIN	HS Rx EQUALIZATION
≤ V_{IL}	0 dB
V_{IM}	2.5 dB
≥ V_{IH}	4 dB

7.3.2 HS TX Edge Rate Control

The DPHY440 supports control of the rise and fall time for the DB[3:0]P/N and DBCP/N High Speed (HS) transmitters. Depending on system operating datarate, the HS edge rate may need to be adjusted to help improve EMI performance. The HS edge rate setting is determined through the sampled state of ERC/SDA pin at the rising edge of RSTN. If necessary, the HS edge rate can be adjusted by writing to the HS_ERC register via the local I2C interface.

Table 2. 8.3.2 HS TX Edge Rate Control

ERC/SDA PIN	HS RISE/FALL TIMES
≤ V_{IL}	200 ps typical
V_{IM}	150 ps typical
≥ V_{IH}	250 ps typical

The DPHY440 also supports edge rate control for the LP interface. The adjustment of LP TX edge rate is determined by the state of the VSADJ_CFG0 and PRE_CFG1 pins as depicted in Table 3, but can also be modified by changing LP_ERC register through the local I2C interface

7.3.3 TX Voltage Swing and Pre-Emphasis Control

In some applications, the DPHY440 may be placed at a location in the system where the channel from DPHY440 DB[3:0]P/N interface to the DPHY Sink (CSI-2 or DSI) is extremely long and the DPHY Sink does not have enough receive equalization to compensate for the ISI loss. In this application, the system architect may want to use the DPHY440 TX pre-emphasis feature to compensate for the lack of equalization at the DPHY sink. The DPHY440 provides two levels of pre-emphasis: 0 dB, and 2.5 dB. The TX Pre-emphasis settings is determined through the sampled sate of PRE_CFG[1:0] pins at the rising edge of RSTN. If necessary, the TX Pre-emphasis settings can be adjusted by writing to the HSTX_PRE register through the local I2C interface.

This feature must only be used when the HS pre-emphasis bit (transition bit) is attenuated by the channel. Enabling pre-emphasis in a system that has little channel loss (transition bit is not attenuated) may result in negative impact to system performance.

Table 3. HS Voltage Swing, HS Pre-emphasis, LPTX Edge Rate Controls

VSADJ_CFG0	PRE_CFG1	HS TX VOD	HS TX PRE-EMPHASIS	DB[3:0] LP TX RISE/FALL TIME
≤ V_{IL}	≤ V_{IL}	200 mV	0 dB	18 ns
V_{IM}	≤ V_{IL}	200 mV	0 dB	27 ns
≥ V_{IH}	≤ V_{IL}	220 mV	0 dB	18 ns
≤ V_{IL}	V_{IM}	200 mV	0 dB	27 ns
V_{IM}	V_{IM}	200 mV	0 dB	21 ns
≥ V_{IH}	V_{IM}	220 mV	0 dB	21 ns
≤ V_{IL}	≥ V_{IH}	220 mV	2.5 dB	27 ns
V_{IM}	≥ V_{IH}	200 mV	2.5 dB	21 ns
≥ V_{IH}	≥ V_{IH}	220 mV	2.5 dB	21 ns

7.3.4 Dynamic De-skew

The DPHY440 implements a dynamic de-skew feature which will continuously de-skew the HS data received on the DA[3:0]P/N interface and provide a retimed version on the DB[3:0]P/N interface. The retimed version is centered within the DBCP/N clock.

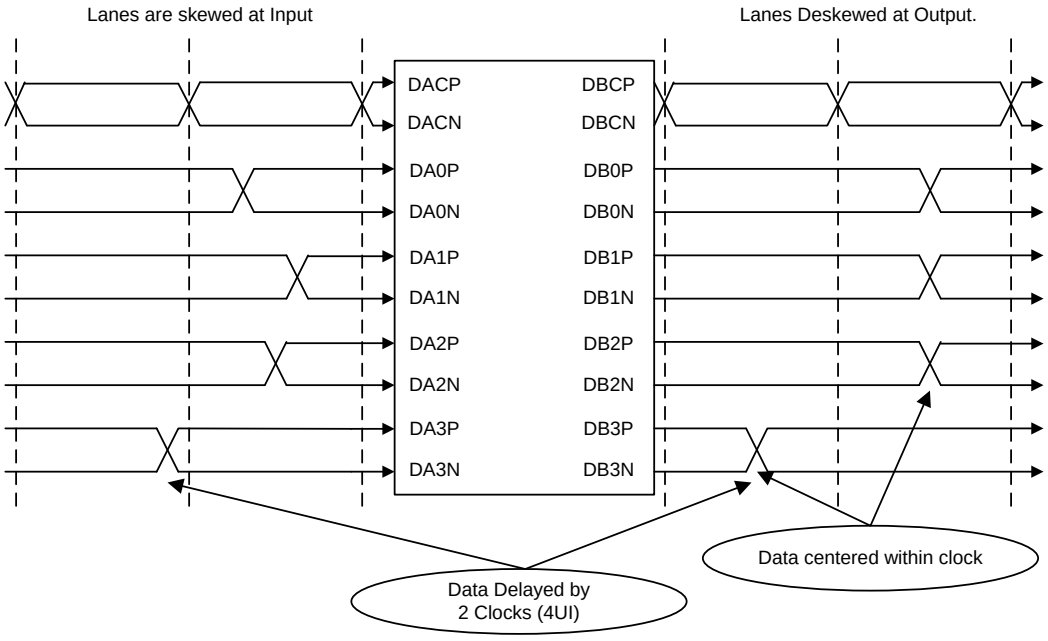


Figure 6. Dynamic De-skew

NOTE

The dynamic de-skew feature is only enabled in HS mode, and causes a 2 clock (4 UI) delay of data while data traverses from DA to DB.

7.4 Device Functional Modes

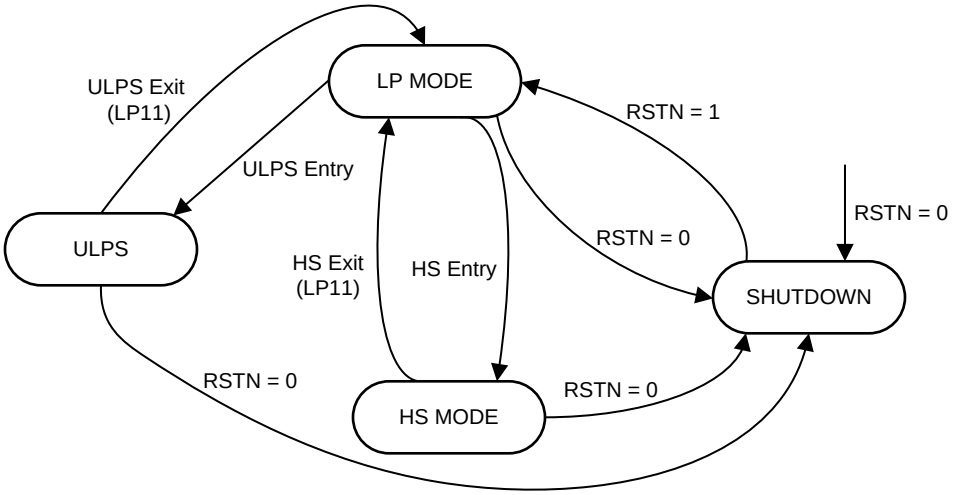


Figure 7. Functional Modes

7.4.1 Shutdown Mode

The DPHY440 can be placed into a low power consumption state by asserting the RSTN pin low while maintaining a stable V_{CC} and V_{DD} power supply. While in the Shutdown state, the DPHY440 drives DB[3:0]P/N and DBCP/N pins to the LP00 state. The DPHY440 ignores all activity on the DA[3:0]P/N and DACP/N pins while in Shutdown mode. The Shutdown mode is exited by de-asserting the RSTN pin high. Upon exiting Shutdown mode, the DPHY440 enters LP Mode operation and pass what is received on the DA interface to the DB interface.

7.4.2 LP Mode

In this mode, the DPHY440 passes LP signals between DA[3:0]P/N and DB[3:0]P/N. The internal terminations for the HS receiver and HS transmitter are disabled when operating in this mode.

The MIPI DSI specification defines bidirectional communication between the host and peripheral. When a response is needed by the peripheral, the response is returned using LP signaling from DB0P/N to DA0P/N. The DPHY440 only supports this communication over lane 0 (DB0P/N to DA0P/N). The remaining lanes cannot be used for LP communications from peripheral to host (reverse direction).

7.4.3 ULPS Mode

The DPHY440 is continuously monitoring the DPHY LP protocol for entry into the ULPS state. Upon entry into the ULPS state, the DPHY440 keeps active the logic necessary for LP signaling (LP rx, LPtx, LP state machine, so forth). All logic needed for HS operation are disabled. This allows for a lower power state than can be achieved when in operating other LP power states.

NOTE

ULPS mode can only be entered from LP Mode.

7.4.4 HS Mode

The HS mode is entered when the required sequence of LP signals is detected by the LP state machine. In this mode, the internal termination for both the HS receiver and HS transmitter is enabled and the dynamic de-skew feature is enabled. The DPHY440 remains in this mode until a HS exit is detected by the LP state machine. Upon detecting the HS exit, the DPHY440 immediately transitions to *LP Mode*.

7.5 Register Maps

The DPHY440 local I2C interface is enabled when RSTN is input high. Access to the CSR registers is supported during ultra-low power state (ULPS). The EQ/SCL and ERC/SDA terminals are used for I^2C clock and I^2C data respectively. The DPHY440 I2C interface conforms to the two-wire serial interface defined by the I^2C Bus Specification, Version 2.1 (January 2000) and supports up to 100 kHz.

The device address byte is the first byte received following the START condition from the master device. The 7 bit device address for DPHY440 is factory preset to 1101100.

Table 4. DPHY440 I^2C Target Address Description

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (W/R)
1	1	0	1	1	0	0	0/1
Address Cycle is 0xD8 (Write) and 0xD9 (Read)							

The following procedure should be followed to write to the DPHY440 I^2C registers:

1. The master initiates a write operation by generating a start condition (S), followed by the DPHY440 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The DPHY440 acknowledges the address cycle.
3. The master presents the sub-address (I^2C register within DPHY440) to be written, consisting of one byte of data, MSB-first
4. The DPHY440 acknowledges the sub-address cycle.
5. The master presents the first byte of data to be written to the I^2C register.
6. The DPHY440 acknowledges the byte transfer.
7. The master may continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the DPHY440.
8. The master terminates the write operation by generating a stop condition (P).

The following procedure should be followed to read the DPHY440 I^2C registers:

1. The master initiates a read operation by generating a start condition (S), followed by the DPHY440 7-bit address and a one-value “W/R” bit to indicate a read cycle
2. The DPHY440 acknowledges the address cycle.
3. The DPHY440 transmit the contents of the memory registers MSB-first starting at register 00h or last read sub-address+1. If a write to the DPHY440 I^2C register occurred prior to the read, then the DPHY440 starts at the sub-address specified in the write.
4. The DPHY440 will wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the master after each byte transfer; the I2C master acknowledges reception of each data byte transfer.
5. If an ACK is received, the DPHY440 transmits the next byte of data.
6. The master terminates the read operation by generating a stop condition (P).

The following procedure should be followed for setting a starting sub-address for I^2C reads:

1. The master initiates a write operation by generating a start condition (S), followed by the DPHY440 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The DPHY440 acknowledges the address cycle.
3. The master presents the sub-address (I^2C register within DPHY440) to be written, consisting of one byte of data, MSB-first.
4. The DPHY440 acknowledges the sub-address cycle.
5. The master terminates the write operation by generating a stop condition (P).

NOTE

If no sub-addressing is included for the read procedure, and reads start at register offset 00h and continue byte by byte through the registers until the I2C master terminates the read operation. If a I^2C write occurred prior to the read, then the reads start at the sub-address specified by the write.

7.5.1 BIT Access Tag Conventions

A table of bit descriptions is typically included for each register description that indicates the bit field name, field description, and the field access tags. The field access tags are described in Table 5.

Table 5. Tag Conventions

ACCESS TAG	NAME	DEFINITION
R	Read	The field may be read by software.
W	Write	The field may be written by software
S	Set	The field may be set by a write of one. Writes of zero to the field have no effect.
C	Clear	The field may be cleared by a write of one. Write of zero to the field have no effect.
U	Update	Hardware may autonomously update this field
N/A	No Access	Not accessible or not applicable

7.5.2 Standard CSR Registers (address = 0x000 - 0x07)

Figure 8. Standard CSR Registers (0x000 - 0x07)

7	6	5	4	3	2	1	0
DEVICE_ID							
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6. Standard CSR Registers (0x000 - 0x07)

Bit	Field	Type	Reset	Description
7:0	DEVICE_ID	R	0	For the DPHY440 these fields return a string of ASCII characters returning “DPHY100”. Addresses 0x07 - 0x00 = {0x20, 0x30, 0x30, 0x31, 0x59, 0x48, 0x50, 0x44}

7.5.3 Standard CSR Register (address = 0x08)

Figure 9. Standard CSR Register (0x08)

7	6	5	4	3	2	1	0
DEVICE_REV							
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7. Standard CSR Register (0x08)

Bit	Field	Type	Reset	Description
7:0	DEVICE_REV	R	0	Device revision.

7.5.4 Standard CSR Register (address = 0x09)

Figure 10. Standard CSR Register(0x09)

7	6	5	4	3	2	1	0
Reserved				RXEQ_CLK.		RXEQ_DATA	
R	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8. Standard CSR Register (0x09)

Bit	Field	Type	Reset	Description
7:4	Reserved	R	0	Reserved
3:2	RXEQ_CLK.	RW	0	This field selects the EQ level of the DACP/N. The value in this field will match the sampled state of EQ/SCL pin at the rising edge of RSTN. Software can change the value of this field at a later time. 00 – 0 dB (EQ/SCL pin = V_{IL}) 01 – 2.5 dB (EQ/SCL pin = V_{IM}) 10 – Reserved. 11 – 4 dB (EQ/SCL pin = V_{IH})
1:0	RXEQ_DATA	RW	0	This field selects the EQ level of the DA[3:0]P/N . The value in this field will match the sampled state of EQ/SCL pin at the rising edge of RSTN. Software can change the value of this field at a later time. 00 – 0 dB. (EQ/SCL pin = V_{IL}) 01 – 2.5 dB (EQ/SCL pin = V_{IM}) 10 – Reserved. 11 – 4 dB. (EQ/SCL pin = V_{IH})

7.5.5 Standard CSR Register (address = 0x0A)

Figure 11. Standard CSR Register (0x0A)

7	6	5	4	3	2	1	0
LPTXDA_ERC		LPTXDB_ERC		Reserved		HSC_ERC	
RW	RW	RW	RW	R	R	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. Standard CSR Register (0x0A)

Bit	Field	Type	Reset	Description
7:6	LPTXDA_ERC	RW	0	This field controls the edge rate of the DA0P/N LP transmitters. 00 – 18 ns at 70 pF (Default) 01 – 21 ns at 70 pF 10 – 15 ns at 70 pF 11 – 27 ns at 70 pF
5:4	LPTXDB_ERC	RW	0	This field controls the edge rate of the DB[3:0]P/N LP transmitters. The value in this field will be updated by hardware based on the state of the CFG[1:0] pin. Refer to Table 3 for settings based on sampled state of CFG[1:0] Software can change the value of this field at a later time. 00 – 18 ns at 70 pF 01 – 21 ns at 70 pF 10 – 15 ns at 70 pF 11 – 27 ns at 70 pF
3:2	Reserved	R		Reserved
1:0	HSC_ERC	RW	0	This field controls the edge rate of the DBCP/N high speed transmitter. The value of this field will match the sampled state of the ERC pin. Software can change the value of this field at a later time. 00 – 200 ps at 1 Gbps. (ERC pin = V_{IL}) 01 – 150 ps at 1 Gbps. (ERC pin = V_{IM}) 10 – 250 ps at 1 Gbps. (ERC pin = V_{IH}) 11 – 300 ps at 1 Gbps

7.5.6 Standard CSR Register (address = 0x0B)

Figure 12. Standard CSR Register (0x0B)

7	6	5	4	3	2	1	0
HSDB3_ERC		HSDB2_ERC		RHSDB1_ERC		HSDB0_ERC	
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. Standard CSR Register (0x0B)

Bit	Field	Type	Reset	Description
7:6	HSDB3_ERC	RW	0	This field controls the edge rate of the DB3P/N high speed transmitter. The value of this field will match the sampled state of the ERC pin. Software can change the value of this field at a later time. 00 – 200 ps at 1 Gbps. (ERC pin = V_{IL}) 01 – 150 ps at 1 Gbps. (ERC pin = V_{IM}) 10 – 250 ps at 1 Gbps. (ERC pin = V_{IH}) 11 – 300 ps at 1 Gbps
5:4	HSDB2_ERC	RW	0	This field controls the edge rate of the DB2P/N high speed transmitter. The value of this field will match the sampled state of the ERC pin. Software can change the value of this field at a later time. 00 – 200 ps at 1 Gbps. (ERC pin = V_{IL}) 01 – 150 ps at 1 Gbps. (ERC pin = V_{IM}) 10 – 250 ps at 1 Gbps. (ERC pin = V_{IH}) 11 – 300 ps at 1 Gbps
3:2	RHSDB1_ERC	RW	0	This field controls the edge rate of the DB1P/N high speed transmitter. The value of this field will match the sampled state of the ERC pin. Software can change the value of this field at a later time. 00 – 200 ps at 1 Gbps. (ERC pin = V_{IL}) 01 – 150 ps at 1 Gbps. (ERC pin = V_{IM}) 10 – 250 ps at 1 Gbps. (ERC pin = V_{IH}) 11 – 300 ps at 1 Gbps
1:0	HSDB0_ERC	RW	0	This field controls the edge rate of the DB0P/N high speed transmitter. The value of this field will match the sampled state of the ERC pin. Software can change the value of this field at a later time. 00 – 200 ps at 1 Gbps. (ERC pin = V_{IL}) 01 – 150 ps at 1 Gbps. (ERC pin = V_{IM}) 10 – 250 ps at 1 Gbps. (ERC pin = V_{IH}) 11 – 300 ps at 1 Gbps

7.5.7 Standard CSR Register (address = 0x0D)

Figure 13. Standard CSR Register (0x0D)

7	6	5	4	3	2	1	0
Reserved.		CDB0N_STATUS	CDB0P_STATUS	Reserved		CDA0N_STATUS	CDA0P_STATUS
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. Standard CSR Register (0x0D)

Bit	Field	Type	Reset	Description
7:6	Reserved.	R		Reserved.
5	CDB0N_STATUS	R	0	0 – Contention not detected on DB0N interface.(default) 1 – Contention detected on DB0N interface
4	CDB0P_STATUS	R	0	0 – Contention not detected on DB0P interface.(default) 1 – Contention detected on DB0P interface
3:2	Reserved	R		Reserved
1	CDA0N_STATUS	R	0	0 – Contention not detected on DA0N interface.(default) 1 – Contention detected on DA0N interface
0	CDA0P_STATUS	R	0	0 – Contention not detected on DA0P interface.(default) 1 – Contention detected on DA0P interface

7.5.8 Standard CSR Register (address = 0x0E)

Figure 14. Standard CSR Register (0x0E)

7	6	5	4	3	2	1	0
Reserved		HSTX_VSADJ		Reserved		HSTX_PRE	
R	R	RW	RW	R	R	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. Standard CSR Register (0x0E)

Bit	Field	Type	Reset	Description
7:6	Reserved	R		Reserved
5:4	HSTX_VSADJ	RWU	0	This field controls the HS TX voltage swing level. The value of this field will match the sampled state of the CFG[1:0] pins. Software can change the value of this field at a later time. 00 – 180 mV 01 – 200 mV (CFG0 = V_{IM} or (CFG0 = V_{IL} and !CFG1 = V_{IH})) 1X – 220mV (CFG0 = V_{IH} or (CFG0 = V_{IL} and CFG1 = V_{IH}))
3:2	Reserved	R		Reserved
1:0	HSTX_PRE	RWU	0	This field controls the HS TX pre-emphasis level. The value of this field will match the sampled state of CFG1 pin. Software can change the value of this field at a later time. 00 – 1.5 dB 01 – 0 dB (CFG1 = V_{IM} or V_{IL}) 1X – 2.5 dB (CFG1 = V_{IH})

7.5.9 Standard CSR Register (address = 0x10) [reset = 0xFF]

Figure 15. Standard CSR Register (0x10)

7	6	5	4	3	2	1	0
LPTXDA_ERC							
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 13. Standard CSR Register (0x10)

Bit	Field	Type	Reset	Description
7:0	LPTXDA_ERC	RW	0xFF	This field represents the lower 8-bits of the 16-bit BTA_TIMEOUT register. Timer is reset to default state when BTA request is detected and is stopped when BTA is acknowledged. If BTA is not acknowledged before this timer expires, then DPHY440 will terminate BTA operation. This counter operates on the LPTX clock. Defaults to 0xFF.

7.5.10 Standard CSR Register (address = 0x11) [reset = 0xFF]

Figure 16. Standard CSR Register (0x11)

7	6	5	4	3	2	1	0
BTA_TIMEOUT_HI							
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. Standard CSR Register (0x11)

Bit	Field	Type	Reset	Description
7:0	BTA_TIMEOUT_HI	RW	0xFF	This field represents the upper 8-bits of the 16-bit BTA_TIMEOUT register. Timer is reset to default state when BTA request is detected and is stopped when BTA is acknowledged. If BTA is not acknowledged before this timer expires, then DPHY440 will terminate BTA operation. This counter operates on the LPTX clock. Defaults to 0xFF.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information,

The DPHY440 supports up to 4 DSI DPHY lanes and a clock lane. One of the four lanes is used for back channel communications between GPU and DSI panel. DPHY440's lane 0 is the only lane that supports the back channel. For this reason, DPHY440 lane 0 must always be connected to lane 0 of GPU and panel.

Other combinations, like 1 and 3 lane, examples are not shown, but are fully supported by the DPHY440. For all DSI implementations, the polarity must be maintained between the DSI Source and DSI Sink. The DPHY440 does not support polarity inversion.

8.2 Typical Application, CSI-2 Implementations

The DPHY440 supports 4 CSI-2 DPHY lanes plus a clock. Unlike DSI, CSI-2 does not have a back channel path. Because of this, there is no requirement on lane ordering. Because there is no lane ordering requirement, there are more combinations which can be implemented. All possible combinations are supported by the DPHY440. For all CSI-2 implementations, the polarity must be maintained between the CSI-2 Source and CSI-2 Sink. The DPHY440 does not support polarity inversion.

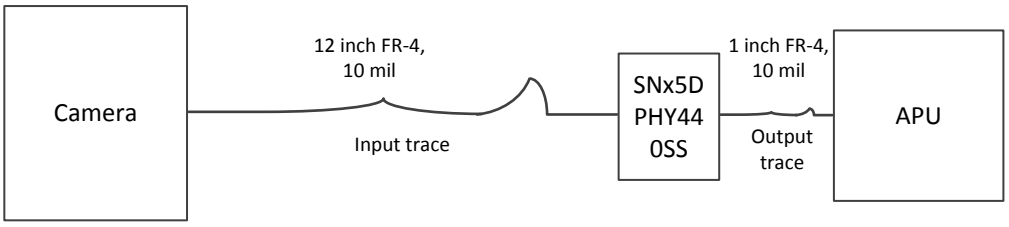


Figure 17. CSI-2 Example: Typical SNx5DPHY440SS Placement in the System

Typical Application, CSI-2 Implementations (continued)

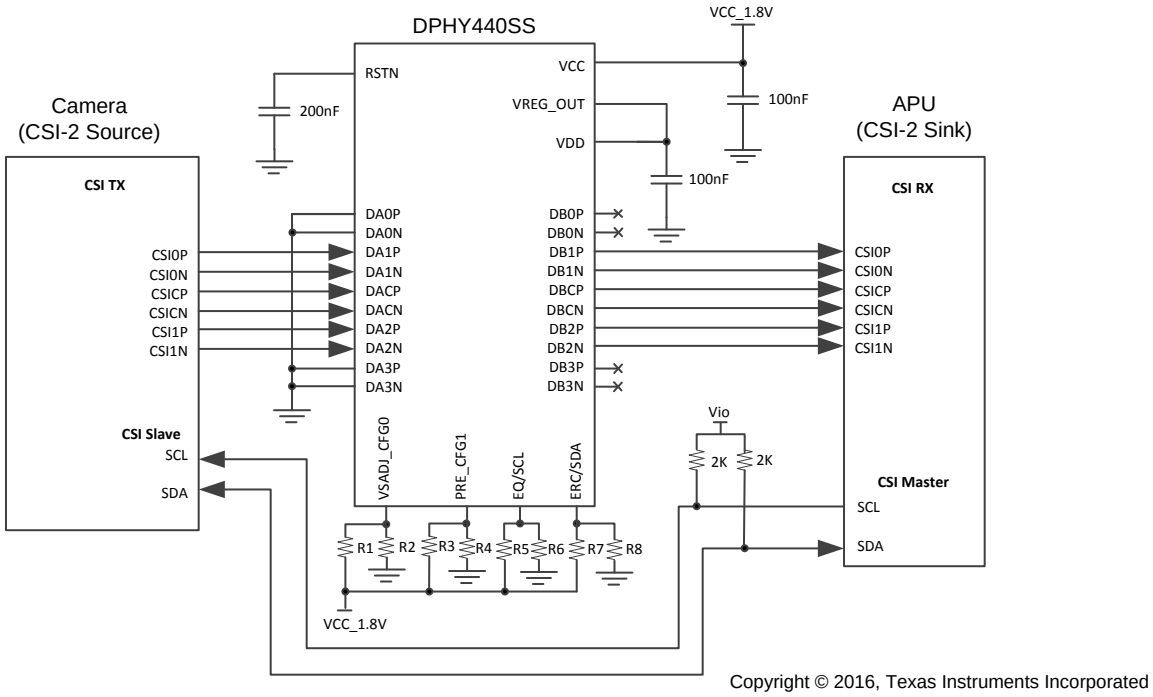


Figure 18. CSI-2 Two Lane Example

8.2.1 Design Requirements

Typically, in CSI-2 applications, the system trace length from the Camera (Source) to the DPHY440 device is different from that of the trace length from DPHY440 to the APU (Sink). Consequently, different pre-emphasis and equalization settings are required on the receiver and transmitter side of the device respectively.

For this design example, refer to Figure 17 and Figure 18. Shown is a CSI-2 system implementation in which the DPHY device is placed close to the Sink (APU). Here, the input trace length is about 12 inch while the output trace length is just 1 inch. The input signal characteristics assumed are shown in Table 15.

Table 15. Design Parameters

PARAMETER	VALUE
Data Rate	1 Gbps
Input trace length	12 inch
Output trace length	1 inch
Trace width	10 mils

8.2.2 Detailed Design Procedure

The typical example describes how to configure the VSADJ, PRE, EQ and ERC configuration pins of the DPHY440 device based on the board trace length between the Source (Camera) and DPHY440 and the DPHY440 and Sink (APU). Actual configuration settings might differ due to additional factors such as board layout, and connectors used in the signal path.

Though the data rate in this example is 1 Gbps, device is placed near to the Sink, with a short output trace of 1 inch. Consequently, the ERC pin can be configured to have a rise/fall time of 250 ps for the edge. Further, due to the short output trace, the PRE pin must be configured to a setting of 0 dB and the VSADJ to be 200 mV. The Application Curve in Figure 22 shows the FR-4 loss characteristics of a 10 mil wide, 12 inch long trace. From this plot, the input signal trace suffers a loss of 1.5 dB at 500 MHz. Thus, the EQ setting can be either 0 dB or 2.5 dB. All the configuration settings and their corresponding inputs are tabulated in Table 16.

Table 16. Configuration Pin Settings

PIN	SETTING	INPUT VALUE
VSADJ	200 mV	V_{IM}
PRE	0 dB	V_{IM}
EQ	0 dB or 2.5 dB	V_{IL} or V_{IM}
ERC	250 ps	V_{IH}

The configuration pins each have internal pull-up and pull-down resistors of 100 kΩ each. Thus, the recommendation is an external pull-up/pull-down resistors of about 10 kΩ each, to meet the requirement of the threshold levels for the V_{IL} and V_{IH} listed in the *Electrical Characteristics* table. The external resistors shown in Figure 18 should be populated to produce corresponding configuration settings, according to the list given in Table 17.

Table 17. Resistor Parameters

RESISTOR NAME	VALUE
R1	Leave unpopulated
R2	Leave unpopulated
R3	Leave unpopulated
R4	Leave unpopulated
R5	Leave unpopulated
R6	10 kΩ (EQ = 0 dB) or Leave unpopulated (EQ = 2.5 dB)
R7	10 kΩ
R8	Leave unpopulated

8.2.2.1 Reset Implementation

The DPHY440 RSTN input gives control over the device reset and to place the device into low power mode. It is critical to reset the digital logic of the DPHY440 after the VCC supply is stable (that is, the power supply has reached the minimum recommended operating voltage). This is achieved by transitioning the RSTN input from a low level to a high level. A system may provide a control signal to the RSTN signal that transitions low to high after the power supply is (or supplies are) stable, or implement an external capacitor connected between RSTN and GND, to allow delaying the RSTN signal during power up. Both implementations are shown in Figure 19 and Figure 20.

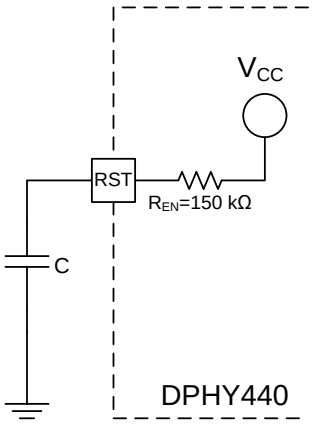


Figure 19. External Capacitor Controlled RSTN

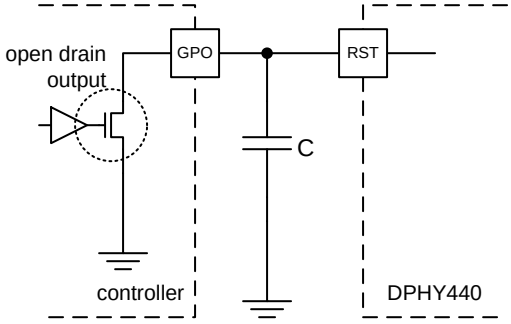


Figure 20. RSTN Input from Active Controller

When implementing the external capacitor, the size of the external capacitor depends on the power up ramp of the V_{CC} supply, where a slower ramp-up results in a larger value external capacitor.

Refer to the latest reference schematic for the DPHY440 device and/or consider approximately 200-nF capacitor as a reasonable first estimate for the size of the external capacitor.

When implementing an RSTN input from an active controller, it is recommended to use an open drain driver if the RSTN input is driven. This protects the RSTN input from damage of an input voltage greater than V_{CC}.

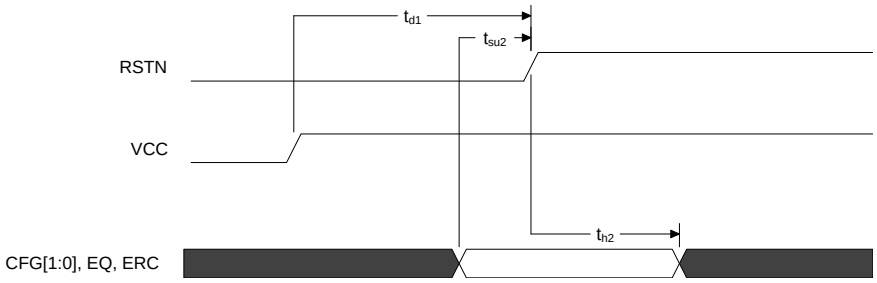


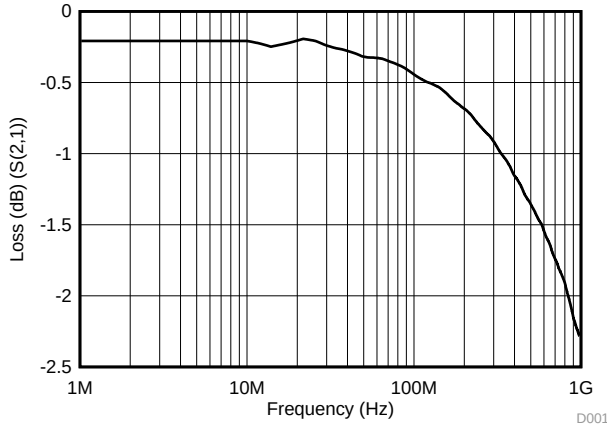
Figure 21. Power-Up Timing Requirements

Table 18. Timing Requirements

	DESCRIPTION(1)	MIN	MAX
t_{D1}	V_{CC} stable before de-assertion of RSTN.	100 µs	
t_{su2}	Setup of VSADJ_CFG0, PRE_CFG1, EQ and ERC pin before de-assertion of RSTN.	0	
t_{h2}	Hold of VSADJ_CFG0, PRE_CFG1, EQ and ERC pin after de-assertion of RSTN.	250 µs	
t_{VCC_RAMP}	V_{CC} supply ramp requirements	0.2 ms	100 ms

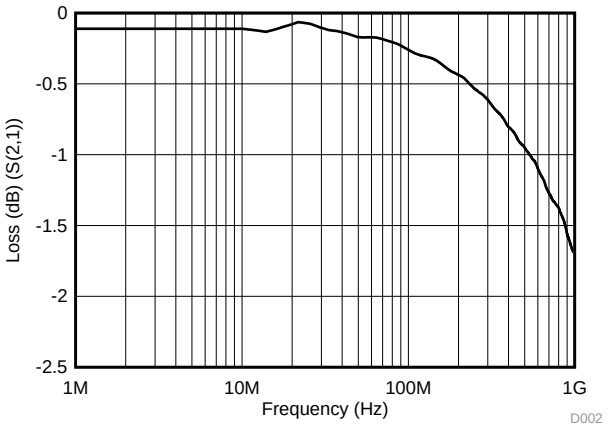
(1) Unused DAxP/N pins shall be tied to GND.

8.2.3 Application Curves



12 inch long, 10 mil wide FR4 trace

Figure 22. Loss vs Frequency



12 inch long, 5 mil wide FR4 trace

Figure 23. Loss vs Frequency

9 Power Supply Recommendations

Texas Instruments recommends a 0.1-µF capacitor on each power pin.

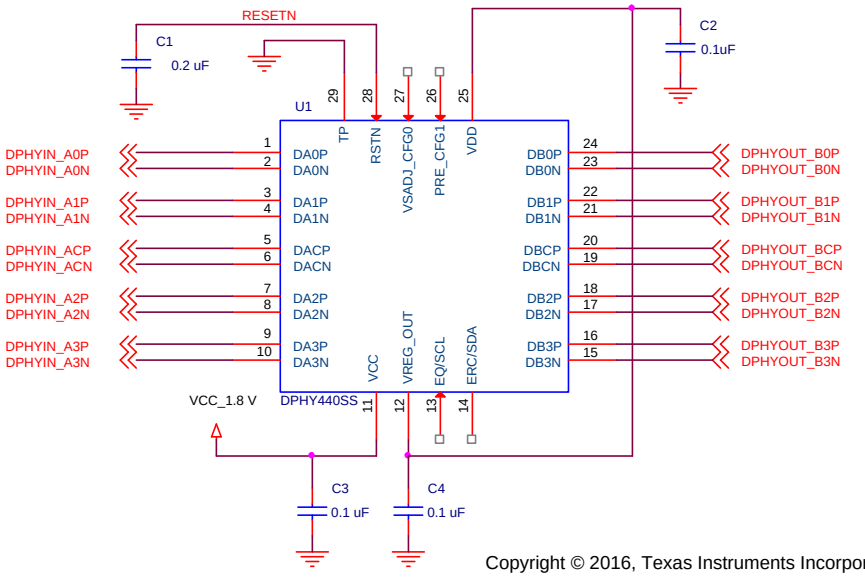


Figure 24. Supply Implementation

10 Layout

10.1 Layout Guidelines

- DAxP/N and DB*P/N pairs should be routed with controlled 100-Ω differential impedance (± 15%) or 50-Ω single-ended impedance (± 15%).
- Keep away from other high speed signals.
- Keep lengths to within 5 mils of each other.
- Length matching should be near the location of mismatch.
- Each pair should be separated at least by 3 times the signal trace width.
- The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥ 135 degrees. This will minimize any length mismatch causes by the bends and; therefore, minimize the impact bends have on EMI.
- Route all differential pairs on the same of layer.
- The number of VIAS should be kept to a minimum. It is recommended to keep the VIAS count to 2 or less.
- Keep traces on layers adjacent to ground plane.
- Do NOT route differential pairs over any plane split.
- Adding Test points will cause impedance discontinuity and will; therefore, negatively impact signal performance. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes a stub on the differential pair.

10.2 Layout Example

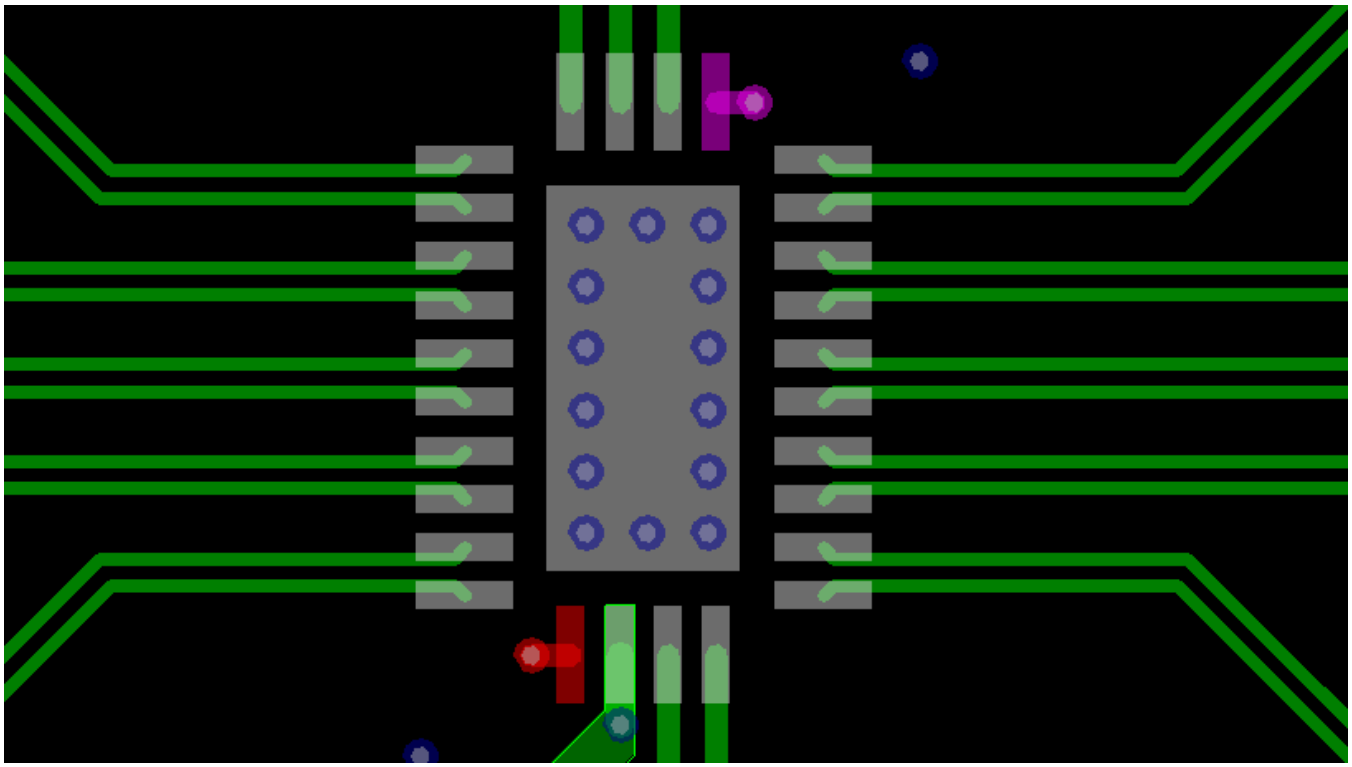


Figure 25. Example Layout

11 Device and Documentation Support

11.0.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 19. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN65DPHY440SS	Click here	Click here	Click here	Click here	Click here
SN75DPHY440SS	Click here	Click here	Click here	Click here	Click here

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65DPHY440SSRHRR	ACTIVE	WQFN	RHR	28	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DPHY440	Samples
SN65DPHY440SSRHRT	ACTIVE	WQFN	RHR	28	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DPHY440	Samples
SN75DPHY440SSRHRR	ACTIVE	WQFN	RHR	28	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	DPHY440	Samples
SN75DPHY440SSRHRT	ACTIVE	WQFN	RHR	28	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	DPHY440	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

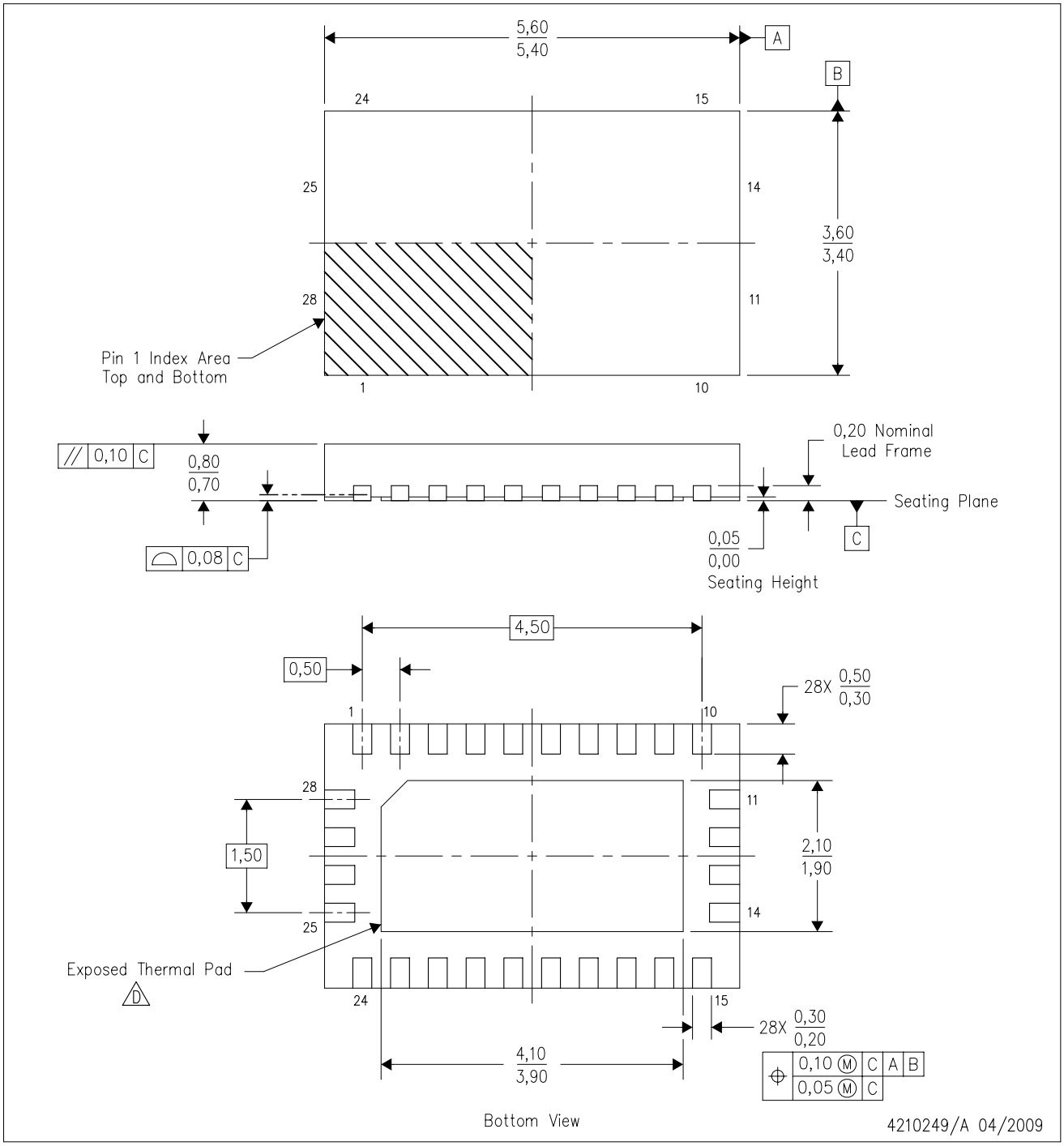
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

RHR (R–PWQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. Reference JEDEC MO–220.

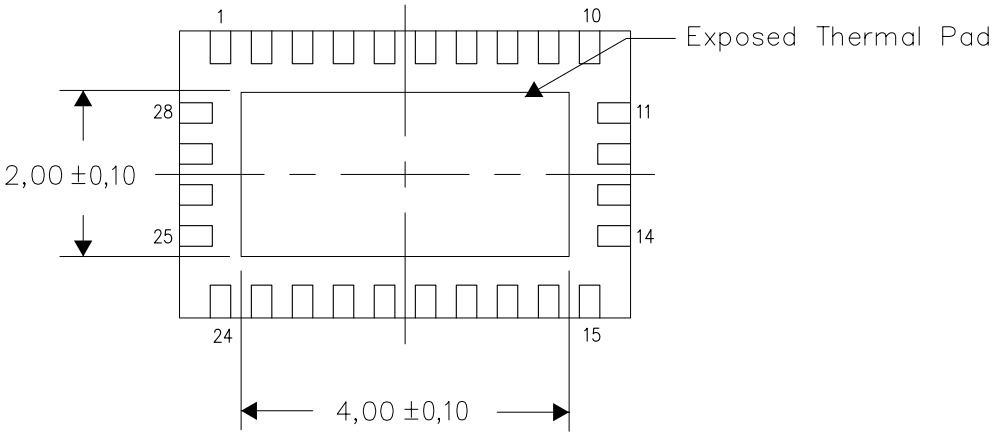
RHR (R–PWQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4210524/D 04/11

NOTE: A. All linear dimensions are in millimeters

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