

## Automotive-grade N-channel 100 V, 25 mΩ typ., 7.8 A STripFET™ F3 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

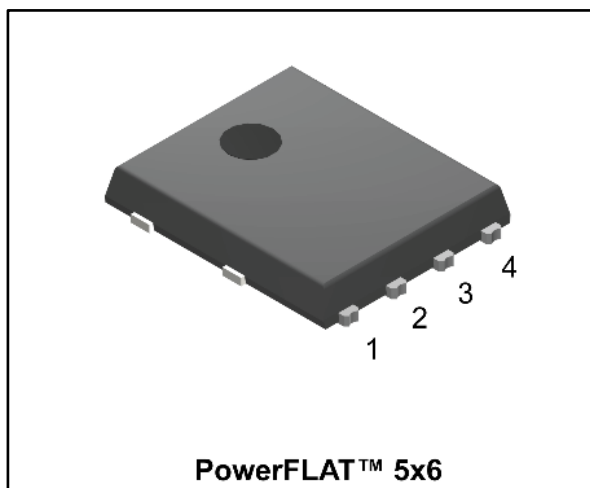
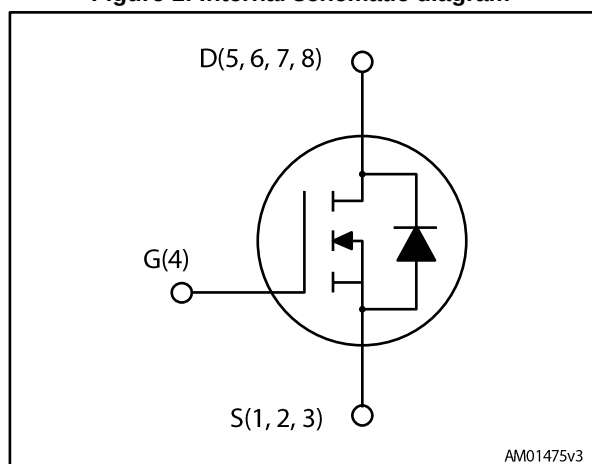


Figure 1: Internal schematic diagram



### Features

| Order code | V <sub>DS</sub> | R <sub>DS(on)</sub> max. | I <sub>D</sub> |
|------------|-----------------|--------------------------|----------------|
| STL8N10LF3 | 100 V           | 35 mΩ                    | 7.8 A          |



- AEC-Q101 qualified
- Logic level V<sub>GS(th)</sub>
- 175 °C maximum junction temperature
- 100% avalanche rated
- Wetable flank package

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using STripFET™ F3 technology. It is designed to minimize on-resistance and gate charge to provide superior switching performance.

Table 1: Device summary

| Order code | Marking | Package        | Packing       |
|------------|---------|----------------|---------------|
| STL8N10LF3 | 8N10LF3 | PowerFLAT™ 5x6 | Tape and reel |

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## Contents

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# 1 Electrical ratings

Table 2: Absolute maximum ratings

| Symbol            | Parameter                                                           | Value      | Unit             |
|-------------------|---------------------------------------------------------------------|------------|------------------|
| $V_{DS}$          | Drain-source voltage                                                | 100        | V                |
| $V_{GS}$          | Gate-source voltage                                                 | $\pm 20$   | V                |
| $I_D^{(1)}$       | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$      | 20         | A                |
| $I_D^{(1)}$       | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$     | 20         | A                |
| $I_D^{(2)}$       | Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$  | 7.8        | A                |
| $I_D^{(2)}$       | Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$ | 5.5        | A                |
| $I_{DM}^{(2)(3)}$ | Drain current (pulsed)                                              | 31.2       | A                |
| $P_{TOT}^{(1)}$   | Total dissipation at $T_C = 25\text{ }^\circ\text{C}$               | 70         | W                |
| $P_{TOT}^{(2)}$   | Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$           | 4.3        | W                |
| $I_{AV}$          | Not-repetitive avalanche current                                    | 7.8        | A                |
| $E_{AS}^{(4)}$    | Single pulse avalanche energy                                       | 190        | mJ               |
| $T_J$             | Operating junction temperature range                                | -55 to 175 | $^\circ\text{C}$ |
| $T_{stg}$         | Storage temperature range                                           |            |                  |

**Notes:**

- (1) This value is rated according to  $R_{thj-case}$  and limited by package  
 (2) This value is rated according to  $R_{thj-pcb}$   
 (3) Pulse width limited by safe operating area.  
 (4) Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $I_D = 7.8\text{ A}$ ,  $V_{DD} = 25\text{ V}$ .

Table 3: Thermal resistance

| Symbol              | Parameter                        | Value | Unit               |
|---------------------|----------------------------------|-------|--------------------|
| $R_{thj-case}$      | Thermal resistance junction-case | 2.1   | $^\circ\text{C/W}$ |
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-pcb  | 35    | $^\circ\text{C/W}$ |

**Notes:**

- (1) When mounted on FR-4 board of 1 inch<sup>2</sup>, 2oz Cu,  $t < 10\text{ s}$

## 2 Electrical characteristics

(T<sub>C</sub> = 25 °C unless otherwise specified)

Table 4: On/Off states

| Symbol               | Parameter                         | Test conditions                                             | Min. | Typ. | Max. | Unit |
|----------------------|-----------------------------------|-------------------------------------------------------------|------|------|------|------|
| V <sub>(BR)DSS</sub> | Drain-source breakdown voltage    | V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA              | 100  |      |      | V    |
| I <sub>DSS</sub>     | Zero gate voltage drain current   | V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 100 V              |      |      | 1    | μA   |
| I <sub>GSS</sub>     | Gate-body leakage current         | V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V              |      |      | ±100 | nA   |
| V <sub>GS(th)</sub>  | Gate threshold voltage            | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA | 1    |      | 3    | V    |
| R <sub>DS(on)</sub>  | Static drain-source on-resistance | V <sub>GS</sub> = 10 V, I <sub>D</sub> = 4 A                |      | 25   | 35   | mΩ   |
|                      |                                   | V <sub>GS</sub> = 5 V, I <sub>D</sub> = 4 A                 |      | 40   | 50   | mΩ   |

Table 5: Dynamic

| Symbol           | Parameter                    | Test conditions                                                                                                                                     | Min. | Typ. | Max. | Unit |
|------------------|------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| C <sub>iss</sub> | Input capacitance            | V <sub>DS</sub> = 25 V, f = 1 MHz,<br>V <sub>GS</sub> = 0 V                                                                                         | -    | 970  | -    | pF   |
| C <sub>oss</sub> | Output capacitance           |                                                                                                                                                     | -    | 115  | -    |      |
| C <sub>rss</sub> | Reverse transfer capacitance |                                                                                                                                                     | -    | 11.5 | -    |      |
| Q <sub>g</sub>   | Total gate charge            | V <sub>DD</sub> = 50 V, I <sub>D</sub> = 7.8 A,<br>V <sub>GS</sub> = 10 V (see <a href="#">Figure 13: "Test circuit for gate charge behavior"</a> ) | -    | 20.5 | -    | nC   |
| Q <sub>gs</sub>  | Gate-source charge           |                                                                                                                                                     | -    | 4    | -    |      |
| Q <sub>gd</sub>  | Gate-drain charge            |                                                                                                                                                     | -    | 5    | -    |      |
| R <sub>G</sub>   | Intrinsic gate resistance    | f = 1 MHz open drain                                                                                                                                | -    | 3.65 | -    | Ω    |

Table 6: Switching times

| Symbol              | Parameter           | Test conditions                                                                                                                                                                       | Min. | Typ. | Max. | Unit |
|---------------------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| t <sub>d(on)</sub>  | Turn-on delay time  | V <sub>DD</sub> = 50 V, I <sub>D</sub> = 7.8 A,<br>R <sub>G</sub> = 4.7 Ω, V <sub>GS</sub> = 10 V (see <a href="#">Figure 12: "Test circuit for resistive load switching times"</a> ) | -    | 8.7  | -    | ns   |
| t <sub>r</sub>      | Rise time           |                                                                                                                                                                                       | -    | 9.6  | -    |      |
| t <sub>d(off)</sub> | Turn-off delay time |                                                                                                                                                                                       | -    | 50.6 | -    |      |
| t <sub>f</sub>      | Fall time           |                                                                                                                                                                                       | -    | 5.2  | -    |      |

Table 7: Source-drain diode

| Symbol          | Parameter                     | Test conditions                                                                                                                                                                                                                  | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $I_{SD}$        | Source-drain current          |                                                                                                                                                                                                                                  | -    |      | 7.8  | A    |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |                                                                                                                                                                                                                                  | -    |      | 31.2 | A    |
| $V_{SD}^{(2)}$  | Forward on voltage            | $I_{DS} = 7.8 \text{ A}$ , $V_{GS} = 0$                                                                                                                                                                                          |      |      | 1.3  | V    |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 7.8 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$<br>$V_{DD} = 48 \text{ V}$ , $T_j = 150 \text{ }^\circ\text{C}$ (see<br><i>Figure 14: "Test circuit for inductive load switching and diode recovery times")</i> ) | -    | 42.5 |      | ns   |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                                                                                                  | -    | 87   |      | nC   |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                                                                                                  | -    | 4.08 |      | A    |

**Notes:**

<sup>(1)</sup>Pulse width limited by safe operating area

<sup>(2)</sup>Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %

## 2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

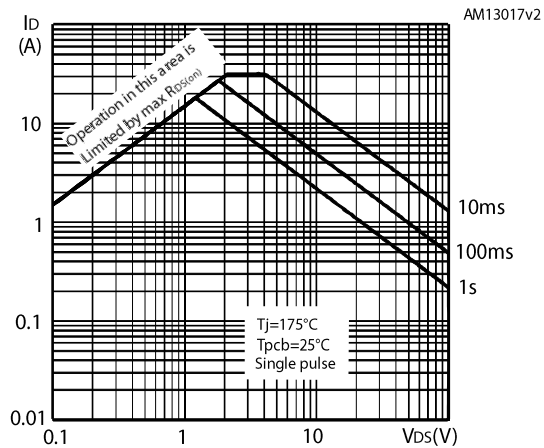


Figure 3: Thermal impedance

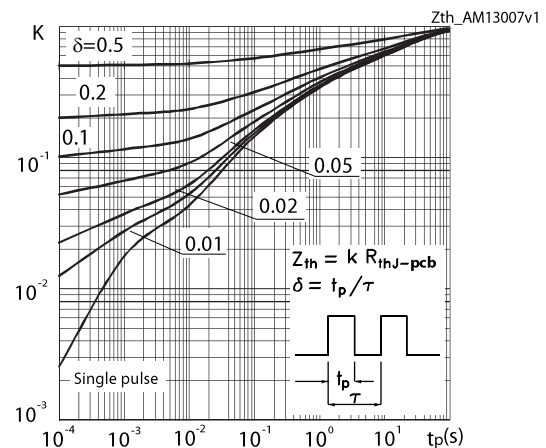


Figure 4: Output characteristics

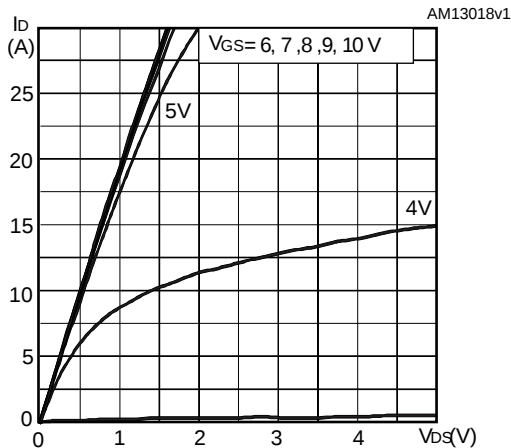


Figure 5: Transfer characteristics

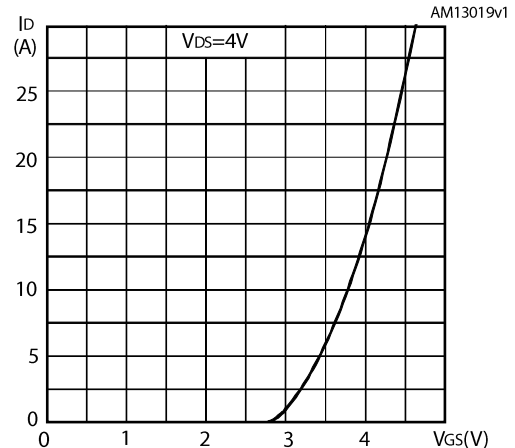


Figure 6: Normalized V(BR)DSS vs temperature

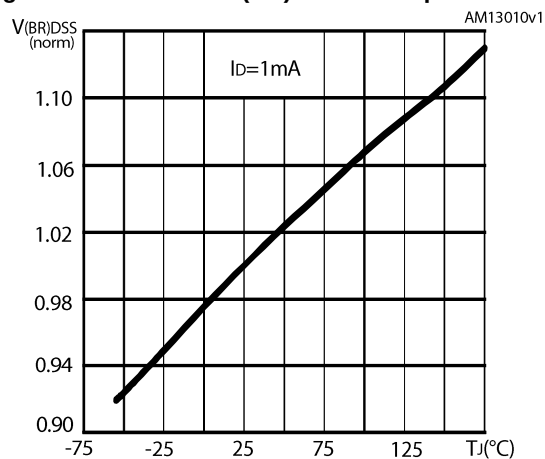


Figure 7: Static drain-source on-resistance

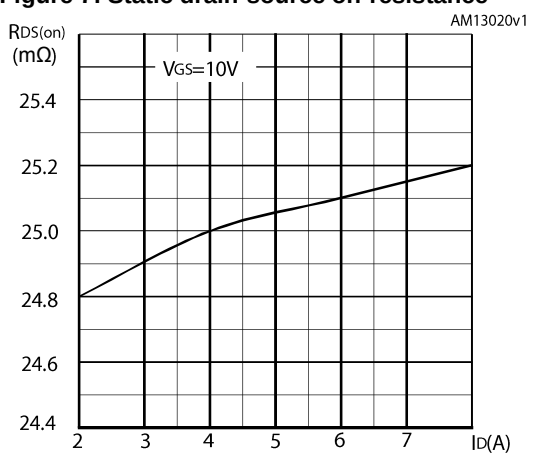


Figure 8: Gate charge vs gate-source voltage

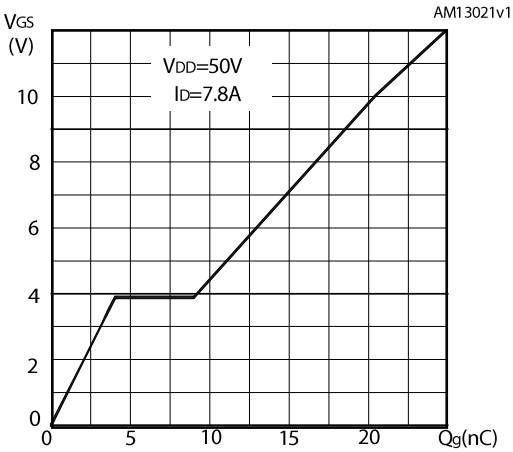


Figure 9: capacitance variation

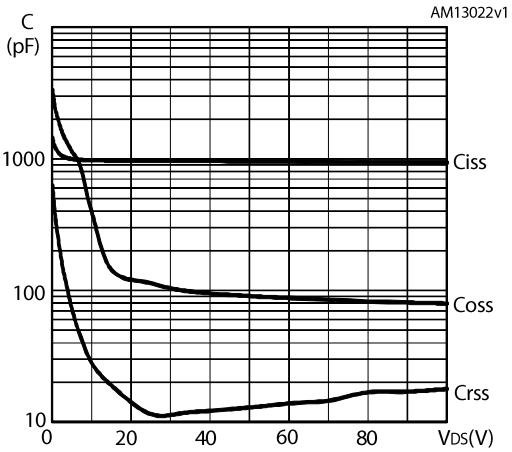


Figure 10: Normalized gate threshold voltage vs temperature

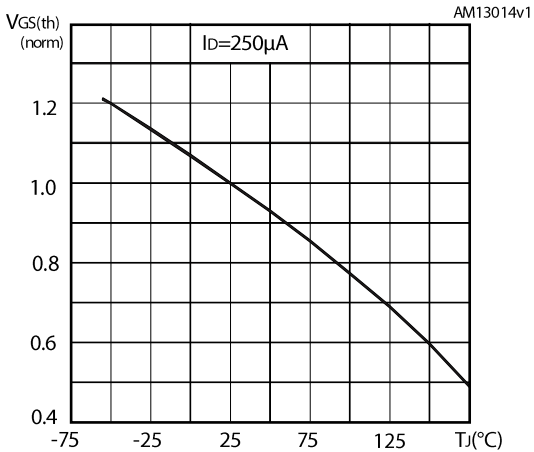
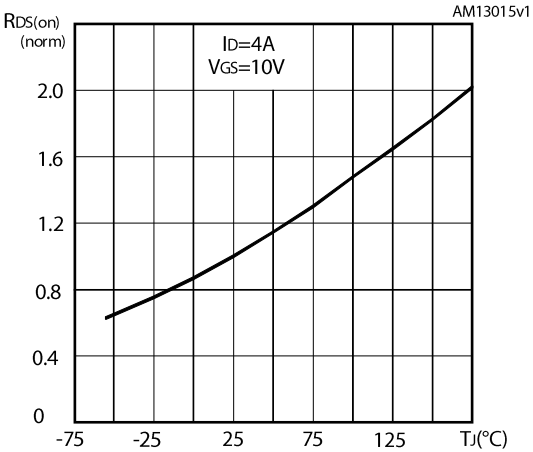


Figure 11: Normalized on resistance vs temperature



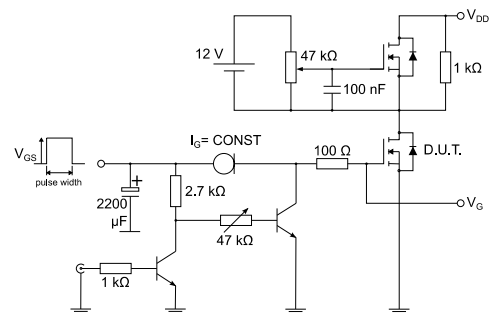
### 3 Test circuits

**Figure 12: Test circuit for resistive load switching times**



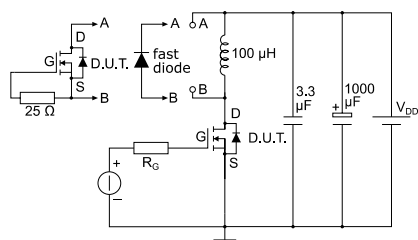
AM01468v1

**Figure 13: Test circuit for gate charge behavior**



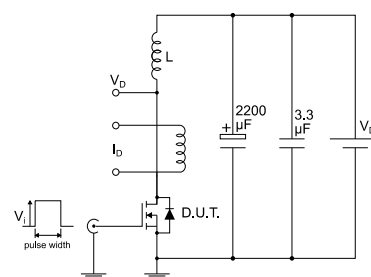
AM01469v1

**Figure 14: Test circuit for inductive load switching and diode recovery times**



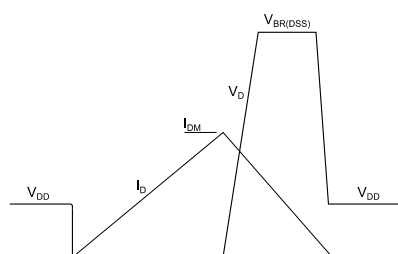
AM01470v1

**Figure 15: Unclamped inductive load test circuit**



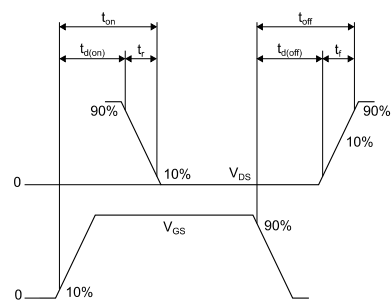
AM01471v1

**Figure 16: Unclamped inductive waveform**



AM01472v1

**Figure 17: Switching time waveform**



AM01473v1

## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 PowerFLAT 5x6 type R package information

Figure 18: PowerFLAT™ 5x6 WF type R package outline

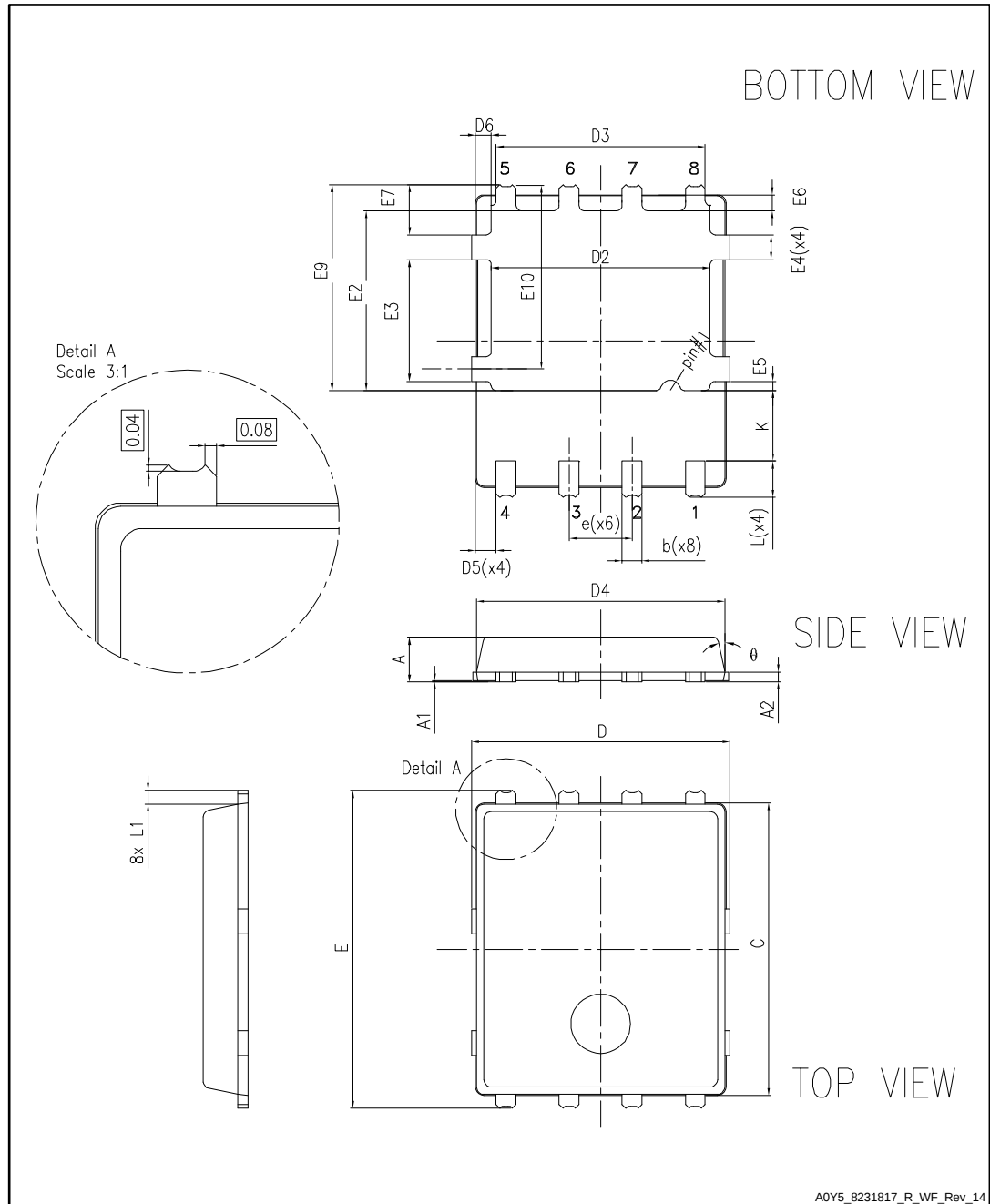
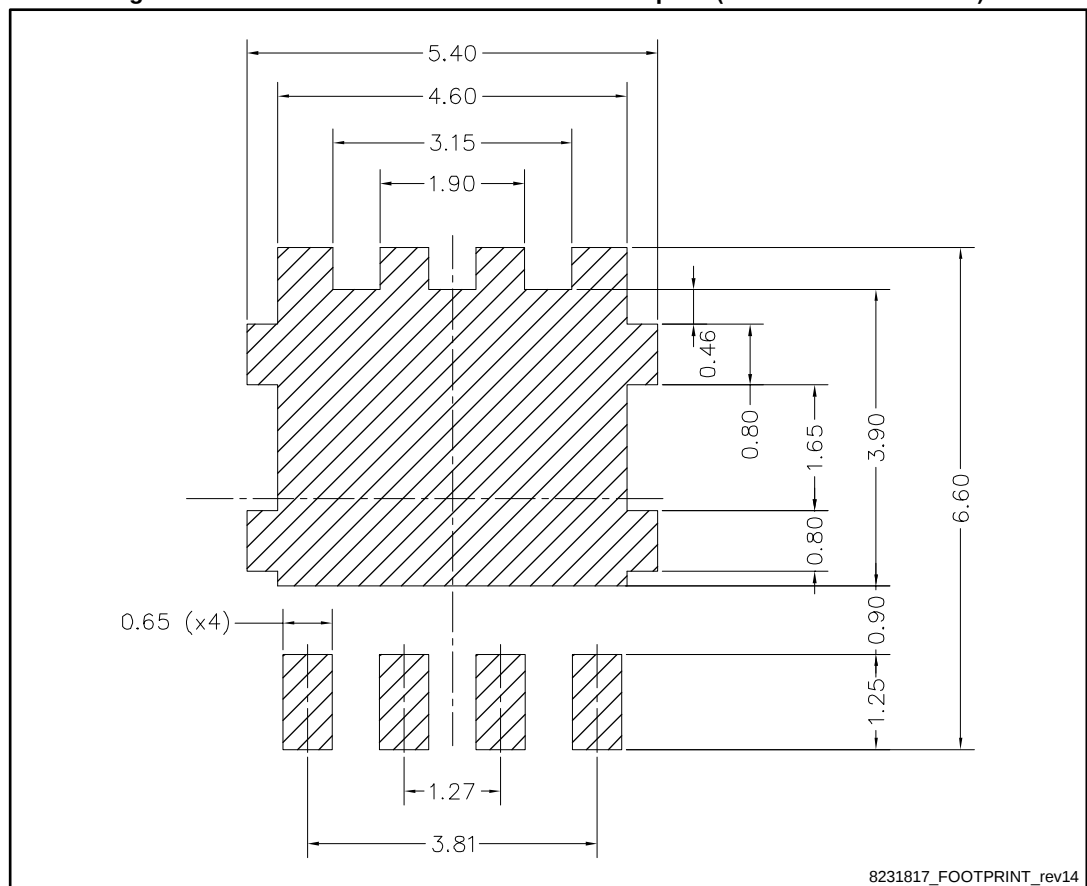


Table 8: PowerFLAT™ 5x6 WF type R mechanical data

| Dim. | mm    |       |       |
|------|-------|-------|-------|
|      | Min.  | Typ.  | Max.  |
| A    | 0.80  |       | 1.00  |
| A1   | 0.02  |       | 0.05  |
| A2   |       | 0.25  |       |
| b    | 0.30  |       | 0.50  |
| C    | 5.80  | 6.00  | 6.10  |
| D    | 5.00  | 5.20  | 5.40  |
| D2   | 4.15  |       | 4.45  |
| D3   | 4.05  | 4.20  | 4.35  |
| D4   | 4.80  | 5.00  | 5.10  |
| D5   | 0.25  | 0.4   | 0.55  |
| D6   | 0.15  | 0.3   | 0.45  |
| e    |       | 1.27  |       |
| E    | 6.20  | 6.40  | 6.60  |
| E2   | 3.50  |       | 3.70  |
| E3   | 2.35  |       | 2.55  |
| E4   | 0.40  |       | 0.60  |
| E5   | 0.08  |       | 0.28  |
| E6   | 0.20  | 0.325 | 0.45  |
| E7   | 0.85  | 1.00  | 1.15  |
| E9   | 4.00  | 4.20  | 4.40  |
| E10  | 3.55  | 3.70  | 3.85  |
| K    | 1.275 |       | 1.575 |
| L    | 0.725 | 0.825 | 0.925 |
| L1   | 0.175 | 0.275 | 0.375 |
| Θ    | 0°    |       | 12°   |

Figure 19: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



## 4.2 Packing information

Figure 20: PowerFLAT™ 5x6 WF tape (dimensions are in mm)

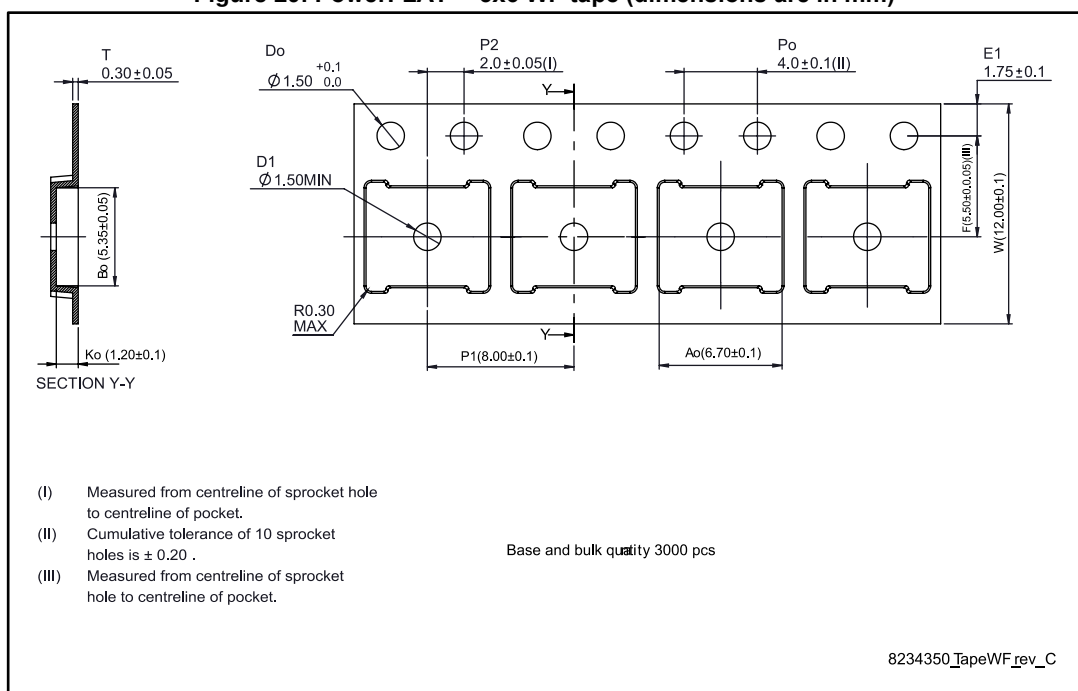
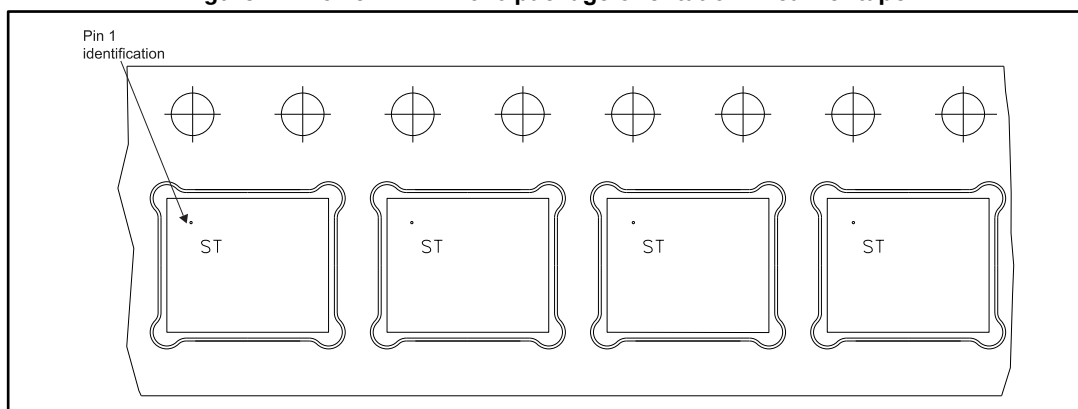
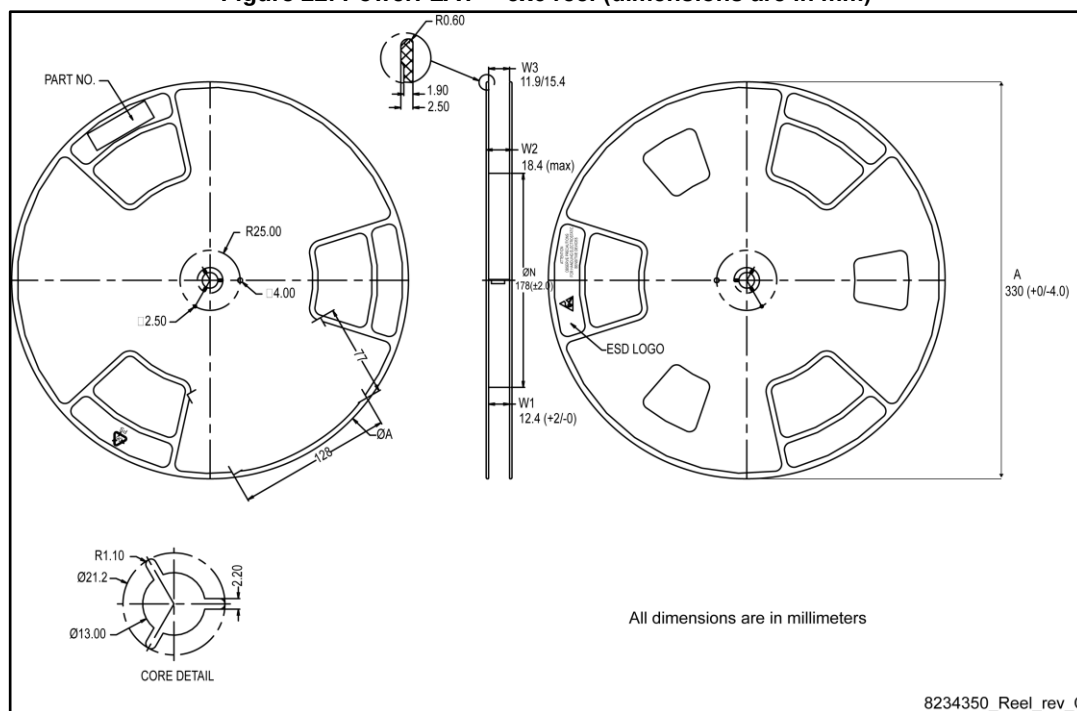


Figure 21: PowerFLAT™ 5x6 package orientation in carrier tape



**Figure 22: PowerFLAT™ 5x6 reel (dimensions are in mm)**



## 5 Revision history

**Table 9: Document revision history**

| Date        | Revision | Changes                                                                                                                                           |
|-------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| 17-Jan-2013 | 1        | First release.                                                                                                                                    |
| 18-May-2015 | 2        | Updated Section 4: Package information. Added Section 5: Packing information. Minor text changes.                                                 |
| 09-Nov-2016 | 3        | Updated features in cover page and <i>Table 2: Absolute maximum ratings</i> . Updated <i>Section 4: Package information</i><br>Minor text changes |
| 28-Nov-2016 | 4        | Updated test conditions in <i>Table 4: "On/Off states"</i> .                                                                                      |

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