# DS90C185 Low Power 1.8V FPD-Link (LVDS) Serializer

**Check for Samples: DS90C185**

## FEATURES

- **Typical power 50 mW at 75-MHz pclk**
- **Drives up to 1400x1050 at 60-Hz (SXGA+) Displays**
- **2.94 Gbps of throughput**
- **Two operating modes: 24-bit and 18-bit RGB**
- **25- to 105-MHz Pixel Clock support**
- **Single 1.8-V Supply**
- **Sleep Mode**
- **Spread Spectrum Clock compatibility**
- **Small 6mm x 6mm x 0.8mm WQFN package**

## APPLICATIONS

- **eBooks**
- **Media Tablet Devices**
- **Netbooks**
- **Portable Display Monitors**

## DESCRIPTION

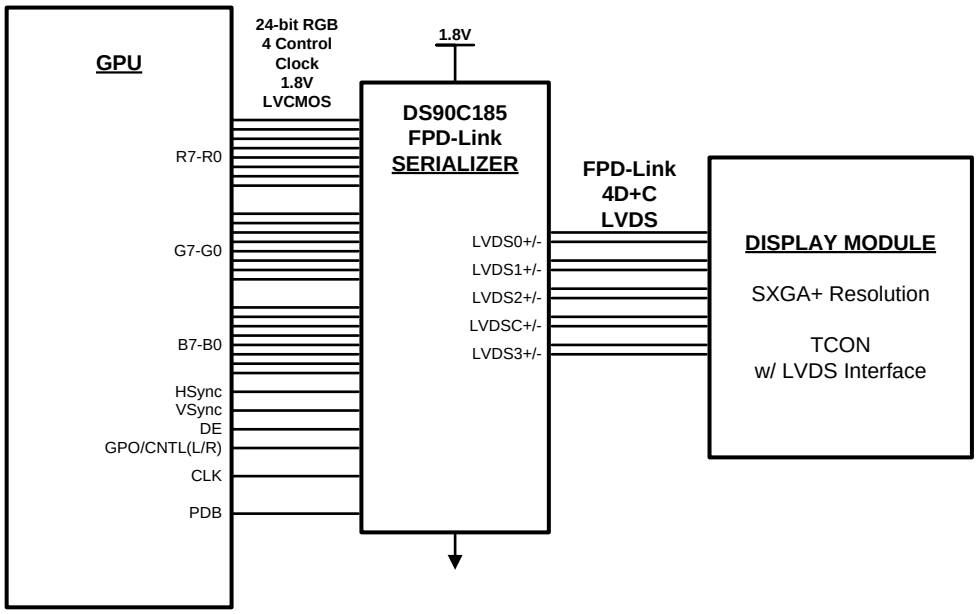
The DS90C185 is a low-power serializer for portable battery-powered applications that reduces the size of the RGB interface between the host GPU and the display.

24-bit RGB plus three video control signals are serialized and translated to LVDS-compatible levels and sent as a 4 data + clock (4D+C) reduced-width LVDS compatible interface. The LVDS Interface is compatible with FPD-Link (1) deserializers and many LVDS based displays. These interfaces are commonly supported in LCD modules with “LVDS” or FPD-Link / FlatLink single-pixel input interfaces.

Displays up to 1400x1050 at 60 fps are supported with 24-bpp color depth. 18 bpp may also be supported by a dedicated mode with a 3D+C output. Power dissipation is minimized by the full LVCMOS design and 1.8-V powered core and $V_{DDIO}$ rails.

The DS90C185 is offered in the small 48-pin WQFN package and features single 1.8-V supply operation for minimum power dissipation (50 mW typ).

### System Diagram

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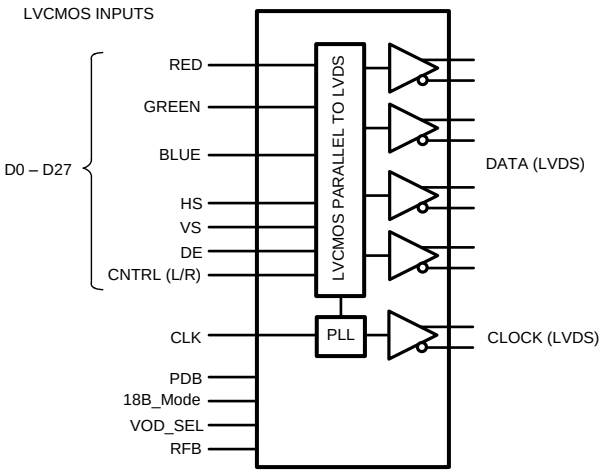
## Functional Block Diagram




**DS90C185 - SERIALIZER**

## Connection Diagram

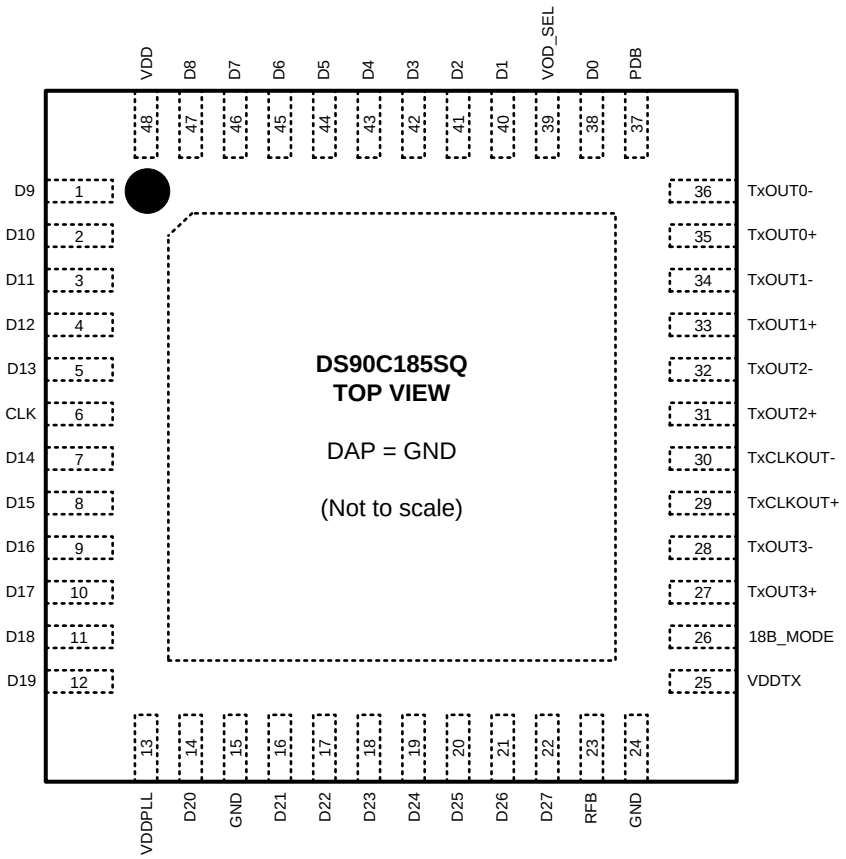




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**Table 1. DS90C185 Pin Descriptions**

| Pin Name | I/O | No. | Description |
|---|---|---|---|
| **1.8 V LVCMOS VIDEO INPUTS** | | | |
| D27-D21,<br>D20,<br>D19-D14,<br>D13-D9,<br>D8-D1,<br>D0 | I | 22-16,<br>14,<br>12-7,<br>5-1,<br>47-40,<br>38 | Data input pins.<br>This includes: 8 Red, 8 Green, 8 Blue, and 3 video control lines and a general purpose or L/R control bit. Includes pull down. |
| CLK | I | 6 | Clock input.<br>Includes pull down. |
| **LVDS VIDEO OUTPUTS** | | | |
| TxOUT0 –/+,<br>TxOUT1 –/+,<br>TxOUT2 –/+,<br>TxOUT3 –/+, | O | 36, 35<br>34, 33<br>32, 31<br>28, 27 | LVDS Output Data — Expects 100 Ω DC load. |
| TxCLK OUT -/+ | O | 30, 29 | LVDS Output Clock — Expects 100 Ω DC load. |
| **1.8 V LVCMOS CONTROL INPUTS** | | | |
| R_FB | I | 23 | LVCMOS level programmable strobe select<br>1 = Rising Edge Clock<br>0 = Falling Edge Clock — default<br>Includes pull down. |
| 18B_Mode | I | 26 | Mode Configuration Input<br>1 = 3D+C (18 bit RGB mode)<br>0 = 4D+C (24 bit RGB mode) — default<br>Includes pull down. |
| VOD_SEL | I | 39 | VOD Select Input<br>0 = Reduced $V_{OD}$ (lower power)<br>1 = Normal $V_{OD}$ — default<br>Includes pull down. |
| PDB | I | 37 | Power Down Bar(Sleep) Input<br>1 = ACTIVE<br>0 = Sleep State (low power idle) — default<br>Includes pull down. |
| **POWER and GROUND** | | | |
| VDD | P | 48 | Digital power input |
| VDDTX | P | 25 | LVDS driver power input |
| VDDPLL | P | 13 | PLL power input |
| GND | G | 15, 24 | Ground pins |
| DAP | G | | Connect DAP to ground plane |

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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## Absolute Maximum Ratings (1)

| | |
|---|---|
| Supply Voltage ($V_{DD}$) | −0.3V to +2.5V |
| LVCMOS Input Voltage | −0.5V to ($V_{DD}$ + 0.3V) |
| LVDS Driver Output Voltage | −0.3V to ($V_{DD}$ + 0.3V) |
| LVDS Output Short Circuit Duration | Continuous |
| Junction Temperature | +150°C |
| Storage Temperature | −65°C to +150°C |
| Lead Temperature (Soldering, 4 sec) | +260°C |
| Package Derating: $\theta_{JA}$ | 26.6 °C/W above +22°C |
| ESD Ratings | |
| HBM | >4kV |
| CDM | >1.25kV |
| MM | >250V |

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

## Recommended OperatingConditions

| | Min | Nom | Max | Units |
|---|---|---|---|---|
| Supply Voltage ($V_{DD}$) | 1.71 | 1.8 | 1.89 | V |
| Operating Free Air Temperature ($T_A$) | −10 | +22 | +70 | °C |
| Supply Noise Voltage ($V_{DD}$) | | | <90 | $mV_{PP}$ |
| Differential Load Impedance | 80 | 100 | 120 | Ω |
| Input Clock Frequency | 25 | | 105 | MHz |


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## Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **LVCMOS DC SPECIFICATIONS** | | | | | | | |
| $V_{IH}$ | High Level Input Voltage | | | 0.65 $V_{DD}$ | | $V_{DD}$ | V |
| $V_{IL}$ | Low Level Input Voltage | | | GND | | 0.35 $V_{DD}$ | V |
| $I_{IN}$ | Input Current | $V_{IN}$ = 0V or $V_{DD}$ = 1.71 V to 1.89 V | | –10 | ±1 | +10 | µA |
| **LVDS DC SPECIFICATIONS** | | | | | | | |
| $V_{OD}$ | Differential Output Voltage | $R_L$ = 100Ω Figure 3 | VODSEL = H | 160 (320) | 300 (600) | 450 (900) | mV ($mV_{P-P}$) |
| | | | VODSEL = L | 115 (230) | 180 (360) | 300 (600) | mV ($mV_{P-P}$) |
| $\Delta V_{OD}$ | Change in $V_{OD}$ between complimentary output states | $R_L$ = 100Ω | | | | 50 | mV |
| $V_{OS}$ | Offset Voltage | | | 0.8 | 0.9 | 1.0 | V |
| $\Delta V_{OS}$ | Change in $V_{OS}$ between complimentary output states | | | | | 50 | mV |
| $I_{OS}$ | Output Short Circuit Current | $V_{OUT}$ = 0V, $R_L$ = 100Ω | | –45 | −35 | −25 | mA |
| $I_{OZ}$ | Output LVDS Driver Power Down Current | PDB = 0V | | | ±1 | ±10 | mA |
| **SERIALIZER SUPPLY CURRENT** | | | | | | | |
| $I_{DDT1}$ | Serializer Supply Current Worst Case | Checkerboard pattern, $R_L$ = 100Ω, 18B_MODE = L, VOD_SEL = H, VDD = 1.89 Figure 1 | f = 105 MHz | | 60 | 85 | mA |
| $I_{DDTG}$ | Serializer Supply Current 16 Grayscale | $R_L$ = 100Ω, 18B_MODE = L, VOD_SEL = L, VDD = 1.8 16 Grayscale Pattern | f = 75 MHz | | 31 | | mA |
| | | $R_L$ = 100Ω, 18B_MODE = L, VOD_SEL = H, VDD = 1.8 16 Grayscale Pattern | | | 41 | | mA |
| | | $R_L$ = 100Ω, 18B_MODE = H, VOD_SEL = L, VDD = 1.8 16 Grayscale Pattern | | | 28 | | mA |
| | | $R_L$ = 100Ω, 18B_MODE = H, VOD_SEL = H, VDD = 1.8 16 Grayscale Pattern | | | 36 | | mA |

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## Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $I_{DDTP}$ | Serializer Supply Current PRBS-7 | $R_L$ = 100Ω, 18B_MODE = L, VOD_SEL = L, VDD = 1.8 PRBS-7 Pattern | f = 75 MHz Figure 11 | | 33 | | mA |
| | | $R_L$ = 100Ω, 18B_MODE = L, VOD_SEL = H, VDD = 1.8 PRBS-7 Pattern | | | 45 | | mA |
| | | $R_L$ = 100Ω, 18B_MODE = H, VOD_SEL = L, VDD = 1.8 PRBS-7 Pattern | | | 29 | | mA |
| | | $R_L$ = 100Ω, 18B_MODE = H, VOD_SEL = H, VDD = 1.8 PRBS-7 Pattern | | | 38 | | mA |
| $I_{DDZ}$ | Serializer Power Down Current | | | | 18 | 200 | µA |


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## Recommended Transmitter Input Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| TCIT | TxCLK IN Transition Time (Figure 5) | 1.0 | | 6.0 | ns |
| TCIP | TxCLK IN Period (Figure 6) | 9.52 | T | 40 | ns |
| TCIH | TxCLK IN High Time (Figure 6) | 0.35T | 0.5T | 0.65T | ns |
| TCIL | TxCLK IN Low Time (Figure 6) | 0.35T | 0.5T | 0.65T | ns |

## Transmitter Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

| Symbol | Parameter | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| LLHT | LVDS Low-to-High Transition Time (Figure 4 (1)) | | | 0.18 | 0.5 | ns |
| LHLT | LVDS High-to-Low Transition Time (Figure 4 (1)) | | | 0.18 | 0.5 | ns |
| TPPOS0 | Transmitter Output Pulse Positions Normalized for Bit 0 | f = 105 MHz Figure 10 | | 1 | | UI |
| TPPOS1 | Transmitter Output Pulse Positions Normalized for Bit 1 | | | 2 | | UI |
| TPPOS2 | Transmitter Output Pulse Positions Normalized for Bit 2 | | | 3 | | UI |
| TPPOS3 | Transmitter Output Pulse Positions Normalized for Bit 3 | | | 4 | | UI |
| TPPOS4 | Transmitter Output Pulse Positions Normalized for Bit 4 | | | 5 | | UI |
| TPPOS5 | Transmitter Output Pulse Positions Normalized for Bit 5 | | | 6 | | UI |
| TPPOS6 | Transmitter Output Pulse Positions Normalized for Bit 6 | | | 7 | | UI |
| ΔTPPOS | Variation in Transmitter Pulse Position (Bit 6 — Bit 0) | | | ±0.06 | | UI |
| TSTC | Required TxIN Setup to TxCLK IN | Figure 6 | 0 | | | ns |
| THTC | Required TxIN Hold to TxCLK IN | | 2.5 | | | ns |
| TCCJ | Cycle to Cycle Jitter | f = 105 MHz (1) | | 0.028 | 0.035 | UI |
| TSD | Serializer Propagation Delay | f = 105 MHz Figure 7 | | 2*TCIP + 10.54 | 2*TCIP + 13.96 | ns |
| TCCS | TxOUT Channel to Channel Skew | | | 110 | | ps |
| TPLLS | Transmitter Phase Lock Loop Set | Figure 8 | | | 1 | ms |
| TPPD | Transmitter Power Down Delay | Figure 9 (2) | | | 100 | ns |

(1) Parameter is guaranteed by characterization and is not tested at final test.
(2) Parameter is guaranteed by design and is not tested at final test.

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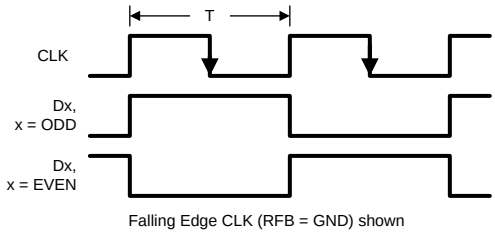
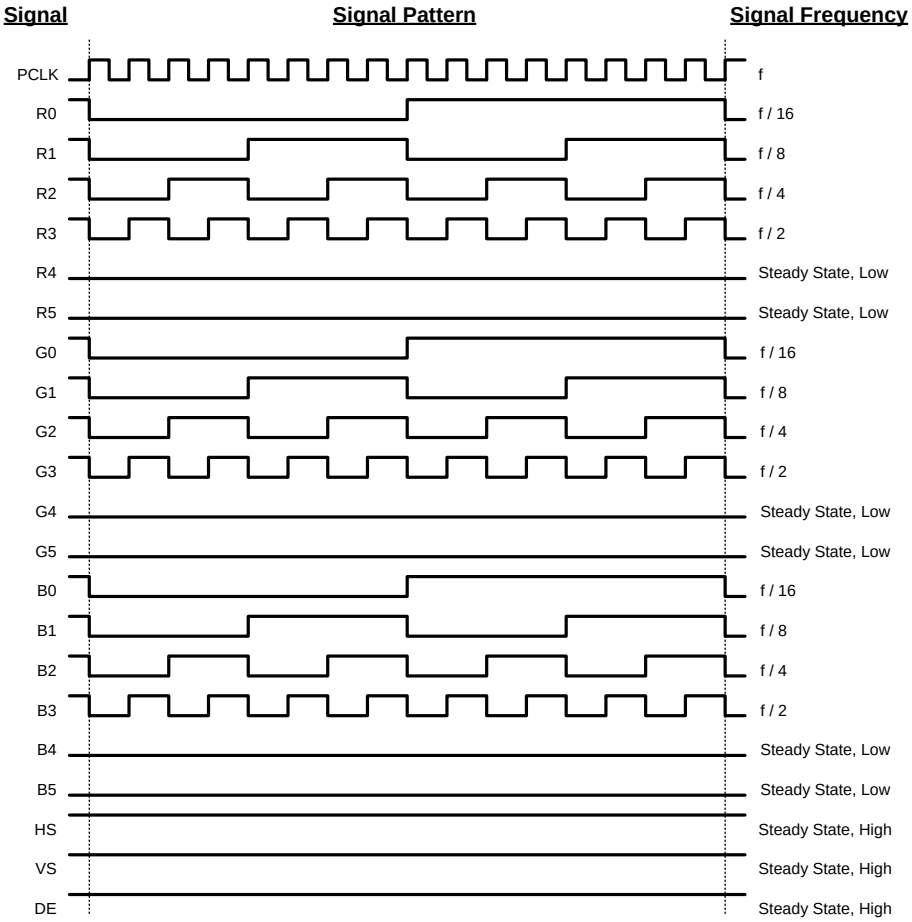
## AC Timing Diagrams




NOTE: The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and LVCMOS I/O.

**Figure 1. "Worst Case" Test Pattern**




NOTE: Recommended pin to signal mapping for 18 bits per pixel, customer may choose to define differently. The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

NOTE: Figure 1 and Figure 2 show a falling edge data strobe (CLK).

**Figure 2. "16 Grayscale" Test Pattern - DS90C185**

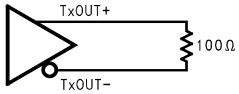



**Figure 3. DS90C185 (Transmitter) LVDS Output Load**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## AC Timing Diagrams (continued)

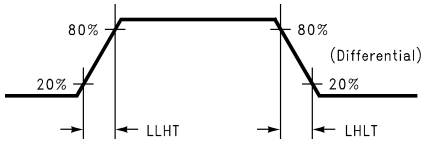


**Figure 4. DS90C185 (Transmitter) LVDS Transition Times**

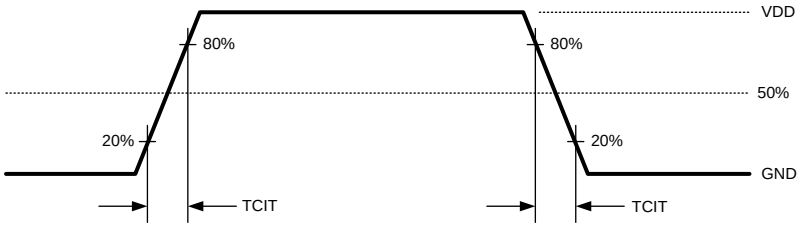


**Figure 5. DS90C185 (Transmitter) Input Clock Transition Time**

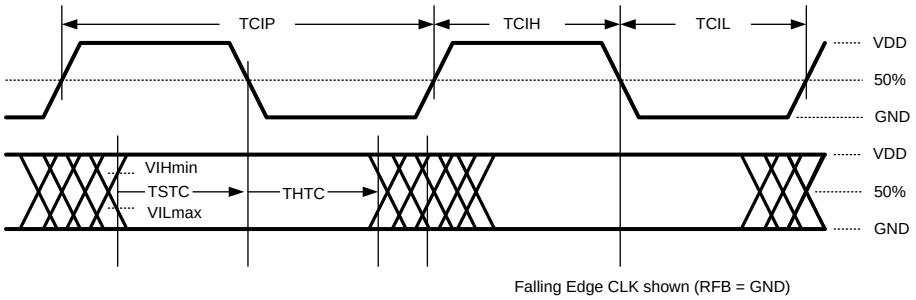


**Figure 6. DS90C185 (Transmitter) Setup/Hold and High/Low Times with R_FB pin = GND (Falling Edge Strobe)**

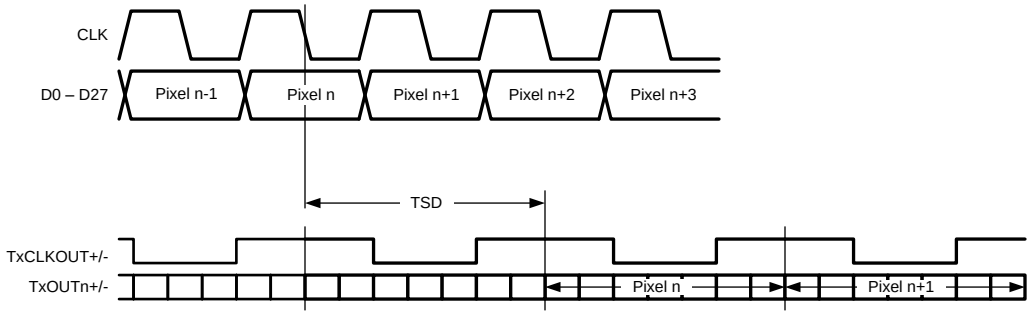


**Figure 7. DS90C185 Propagation Delay**

## AC Timing Diagrams (continued)

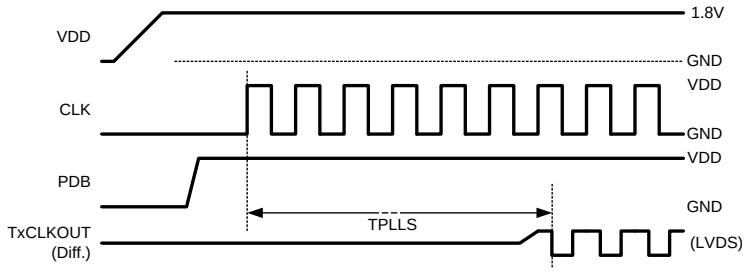


**Figure 8. DS90C185 (Transmitter) Phase Lock Loop Set Time**

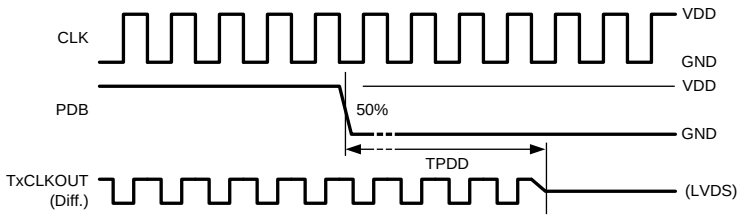


**Figure 9. Transmitter Power Down Delay**

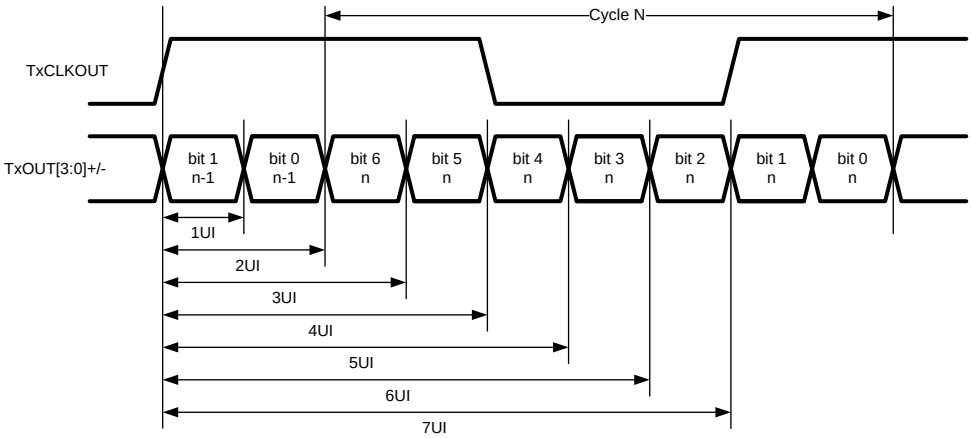


**Figure 10. Transmitter LVDS Output Pulse Position Measurement - DS90C185**

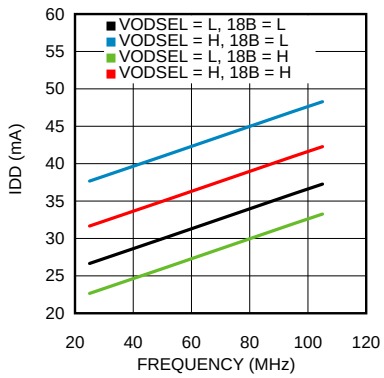


**Figure 11. Typ Current Draw — PRBS-7 Data Pattern**


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## LVDS INTERFACE, TFT COLOR DATA RECOMMENDED MAPPING

Different color mapping options exist. Check with the color mapping of the Deserializer / TCON device that is used to ensure compatible mapping for the application. The DS90C185 supports single pixel interfaces with either 24bpp or 18bpp color depths.

The DS90C185 provides four LVDS data lines along with an LVDS clock line (4D+C) for the 28 LVCMOS data inputs. The 28 bit interface typically assigns 24 bits to RGB color data, 3 bits to video control (HS, VS and DE) and one spare bit can be ignored, used for L/R signaling or function as a general purpose bit. The single pixel 24bpp 4D+C LVDS interface mapping is shown Figure 13. A single pixel 18bpp mode is also supported by utilizing the 18B_MODE pin. In this configuration the TxOUT3 output channel is place in TRI-STATE® to save power. Its respective inputs are ignored. This mapping is shown in Figure 12.

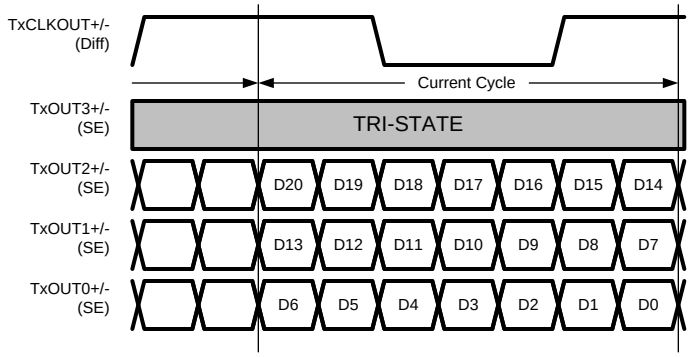


**Figure 12. DS90C185 LVDS Map — 18B_MODE = H**

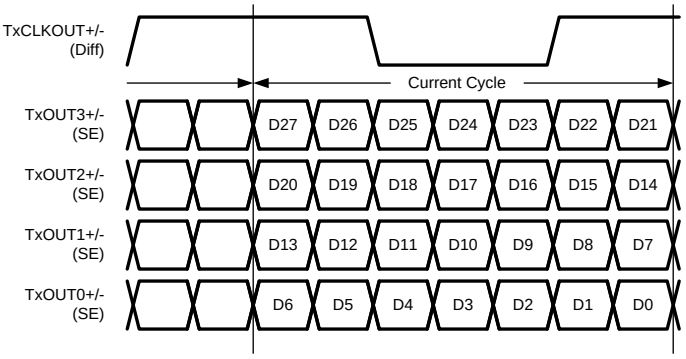


**Figure 13. DS90C185 LVDS Map — 18B_MODE = L**

### COLOR MAPPING INFORMATION

A defacto color mapping is shown next. Different color mapping options exist. Check with the color mapping of the Deserializer / TCON device that is used to ensure compatible mapping for the application.

**Table 2. 24bpp / MSB on CH3**

| DS90C187 Input | Color Mapping | Note |
|---|---|---|
| D22 | R7 | MSB |
| D21 | R6 | |
| D5 | R5 | |
| D4 | R4 | |
| D3 | R3 | |
| D2 | R2 | |
| D1 | R1 | |
| D0 | R0 | LSB |

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**Table 2. 24bpp / MSB on CH3 (continued)**

| DS90C187 Input | Color Mapping | Note |
|---|---|---|
| D24 | G7 | MSB |
| D23 | G6 | |
| D11 | G5 | |
| D10 | G4 | |
| D9 | G3 | |
| D8 | G2 | |
| D7 | G1 | |
| D6 | G0 | LSB |
| D26 | B7 | MSB |
| D25 | B6 | |
| D17 | B5 | |
| D16 | B4 | |
| D15 | B3 | |
| D14 | B2 | |
| D13 | B1 | |
| D12 | B0 | |
| D20 | DE | $\overline{\text{Data Enable}}$ |
| D19 | VS | Vertical Sync |
| D18 | HS | Horizontal Sync |
| D27 | GP | General Purpose |

**Table 3. 24bpp / LSB on CH3**

| DS90C187 Input | Color Mapping | Note |
|---|---|---|
| D5 | R7 | MSB |
| D4 | R6 | |
| D3 | R5 | |
| D2 | R4 | |
| D1 | R3 | |
| D0 | R2 | |
| D22 | R1 | |
| D21 | R0 | LSB |
| D11 | G7 | MSB |
| D10 | G6 | |
| D9 | G5 | |
| D8 | G4 | |
| D7 | G3 | |
| D6 | G2 | |
| D24 | G1 | |
| D23 | G0 | LSB |
| D17 | B7 | MSB |
| D16 | B6 | |
| D15 | B5 | |
| D14 | B4 | |
| D13 | B3 | |
| D12 | B2 | |
| D26 | B1 | |
| D25 | B0 | |


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**Table 3. 24bpp / LSB on CH3 (continued)**

| DS90C187 Input | Color Mapping | Note |
|---|---|---|
| D20 | DE | Data Enable |
| D19 | VS | Vertical Sync |
| D18 | HS | Horizontal Sync |
| D27 | GP | General Purpose |

**Table 4. 18bpp**

| DS90C187 Input | Color Mapping | Note |
|---|---|---|
| D5 | R5 | MSB |
| D4 | R4 | |
| D3 | R3 | |
| D2 | R2 | |
| D1 | R1 | |
| D0 | R0 | LSB |
| D11 | G5 | MSB |
| D10 | G4 | |
| D9 | G3 | |
| D8 | G2 | |
| D7 | G1 | |
| D6 | G0 | LSB |
| D17 | B5 | MSB |
| D16 | B4 | |
| D15 | B3 | |
| D14 | B2 | |
| D13 | B1 | |
| D12 | B0 | |
| D20 | DE | Data Enable |
| D19 | VS | Vertical Sync |
| D18 | HS | Horizontal Sync |

## FUNCTIONAL DESCRIPTION

DS90C185 converts a wide parallel LVCMOS input bus into FPD-Link LVDS data. The device can be configured to support RGB-888 (24 bit color) or RGB-666 (18 bit color). The DS90C185 has several power saving features including: selectable VOD, 18 bit / 24 bit mode select, and a power down pin control.

In each input pixel clock cycle, data from D[27:0] is serialized and driven out on TxOUT[3:0] +/- with TxCLKOUT +/-. If 18B_MODE is LOW, then TxOUT3 +/- is powered down and the corresponding LVCMOS input signals are ignored.

The input pixel clock can range from 25 MHz to 105 MHz, resulting in a total maximum payload of 700 Mbps (28 bits * 25MHz) to 2.94 Gbps (28 bits * 105 MHz). Each LVDS driver will operate at a speed of 7 bits per input clock cycle, resulting in a serial line rate of 175 Mbps to 735 Mbps. TxCLKOUT +/- will operate at the same rate as CLK with a duty cycle ratio of 57:43.

### Pixel Clock Edge Select (RFB)

The RFB pin determines the edge that the input LVCMOS data is latched on. If RFB is HIGH, input data is latched on the RISING EDGE of the pixel clock (CLK). If RFB is LOW, the input data is latched on the FALLING EDGE of the pixel clock. Note: This can be set independently of receiver's output clock strobe.

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**Table 5. Pixel Clock Edge**

| RFB | Result |
|---|---|
| 0 | FALLING edge |
| 1 | RISING edge |

### Power Management

The DS90C185 has several features to assist with managing power consumption. The 18B_MODE pin allows the DS90C185 to power down the unused LVDS driver for RGB-666 (18 bit color) applications. If no clock is applied to the CLK pin, the DS90C185 will enter a low power state. To place the DS90C185 in its lowest power state, the device can be powered down by driving the PDB pin to LOW.

### Sleep Mode (PDB)

The DS90C185 provides a power down feature. When the device has been powered down, current draw through the supply pins is minimized and the PLL is shut down. The LVDS drivers are also powered down with their outputs pulled to GND through 100Ω resistors.

**Table 6. Power Down Select**

| PDB | Result |
|---|---|
| 0 | SLEEP Mode (default) |
| 1 | ACTIVE (enabled) |

### LVDS Outputs

The DS90C185's LVDS drivers are compatible with ANSI/TIA/EIA-644–A LVDS receivers. The LVDS drivers an output a power saving low $V_{OD}$ or a higher $V_{OD}$ to enable longer trace and cable lengths by configuring the VODSEL pin.

**Table 7. VOD Select**

| VODSEL | Result |
|---|---|
| 0 | ±180 mV (360mVpp) |
| 1 | ±300 mV (600mVpp) |

For more information regarding the electrical characteristics of the LVDS outputs, refer to the LVDS DC Characteristics and LVDS Switching Specifications.

### 18 bit / 24 bit Color Mode (18B)

The 18B pin can be used to further save power by powering down the 4th LVDS driver in each used bank when the application requires only 18 bit color or 3D+C LVDS. Set the 18B pin to logic HIGH to TRI-STATE® TxOUT3 +/-. For 24 bit color applications this pin should be set to logic LOW. Note that the power down function takes priority over the TRI-STATE® function.

**Table 8. Color Depth Configurations**

| 18B_Mode | Result |
|---|---|
| 0 | 24bpp, LVDS 4D+C |
| 1 | 18bpp, LVDS 3D+C |

### LVCMOS Inputs

The DS90C185 has 28 data inputs. These inputs are typically used for 24 or 18 bits of RGB video with 1, 2 or 3 video control signal (HS, VS and DE) inputs and one spare bit that can be used for L/R signaling or function as a general purpose bit. All LVCMOS input pins are designed for 1.8V LVCMOS logic. All LVCMOS inputs, including clock, data and configuration pins have an internal pull down resistor to set a default state. If any LVCMOS inputs are unused, they can be left as no connect (NC) or connected to ground.


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## APPLICATIONS INFORMATION

### Power Up Sequence

The $V_{DD}$ power supply pins do not require a specific power on sequence and can be powered on in any order. However, the PDB pin should only be set to logic HIGH once the power sent to all supply pins is stable. Active clock and data inputs should not be applied to the DS90C185 until all of the input power pins have been powered on, settled to the recommended operating voltage and the PDB pin has be set to logic HIGH.

The user experience can be impacted by the way a system powers up and powers down an LCD screen. The following sequence is recommended:

Power up sequence (DS90C185 PDB input initially LOW):

1. Ramp up LCD power (maybe 0.5ms to 10ms) but keep backlight turned off.
2. Wait for additional 0-200ms to ensure display noise won't occur.
3. Toggle DS90C185 power down pin to PDB = $V_{IH}$.
4. Enable video source output; start sending black video data.
5. Send >1ms of black video data; this allows the DS90C185 to be phase locked, and the display to show black data first.
6. Start sending true image data.
7. Enable backlight.

Power Down sequence (DS90C185 PDB input initially HIGH):

1. Disable LCD backlight; wait for the minimum time specified in the LCD data sheet for the backlight to go low.
2. Video source output data switch from active video data to black image data (all visible pixel turn black); drive this for >2 frame times.
3. Set DS90C185 power down pin to PDB = GND.
4. Disable the video output of the video source.
5. Remove power from the LCD panel for lowest system power.

### Power Supply Filtering

The DS90C185 has several power supply pins at 1.8V. It is important that these pins all be connected and properly bypassed. Bypassing should consist of at least one 0.1µF capacitor placed on each pin, with an additional 4.7µF to 22µF capacitor placed on the PLL supply pin (VDDPLL). 0.01µF capacitors are typically recommended for each pin. Additional filtering including ferrite beads may be necessary for noisy systems. It is recommended to place a 0 resistor at the bypass capacitors that connect to each power pin to allow for additional filtering if needed. A large bulk capacitor is recommended at the point of power entry. This is typically in the 50µF to 100µF range.

### Layout Guidelines

Circuit board layout and stack-up for the LVDS serializer devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. This practice is easier to implement in dense pcbs with many layers and may not be practical in simpler boards. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 uF to 0.1 uF. Tantalum capacitors may be in the 2.2 uF to 10 uF range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with vias on both ends of the capacitor.

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A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20-30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the LVDS lines to prevent coupling from the LVCMOS lines to the LVDS lines. Closely coupled differential lines of 100 Ohms are typically recommended for LVDS interconnect. The closely coupled lines help to ensure that coupled noise will appear as common mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

Information on the WQFN package is provided in Application Note: AN-1187 (SNOA401).

### LVDS Interconnect Guidlines

See AN-1108 (SNLA008) and AN-905 (SNLA035) for full details.

- Use 100Ω coupled differential pairs
- Use differential connectors when above 500Mbps
- Minimize skew within the pair
- Use the S/2S/3S rule in spacings
  - S = space between the pairs
  - 2S = space between pairs
  - 3S = space to LVCMOS signals
- Place ground vias next to signal vias when changing between layers
- When a signal changes reference planes, place a bypass cap and vias between the new and old reference plane

For more tips and detailed suggestions regarding high speed board layout principles, please consult the LVDS Owner's Manual at: http://www.ti.com/lvds


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## REVISION HISTORY

**June 08, 2012**

- Fixed typo in Figure 12 for bits D14 and D15
- Fixed typo in Pin Descriptions for VODSEL. VODSEL = 0 reduced swing and VODSEL = 1 normal LVDS swing now match Functional Description explanation

**February 2013**

- Changed layout of National Data Sheet to TI format

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DS90C185SQ/NOPB | ACTIVE | WQFN | NJV | 48 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -10 to 70 | 90C185SQ | Samples |
| DS90C185SQE/NOPB | ACTIVE | WQFN | NJV | 48 | 250 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -10 to 70 | 90C185SQ | Samples |
| DS90C185SQX/NOPB | ACTIVE | WQFN | NJV | 48 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -10 to 70 | 90C185SQ | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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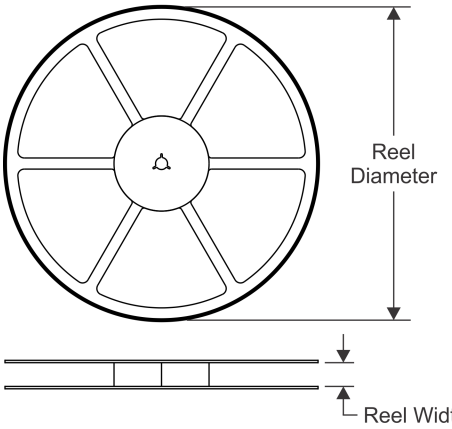
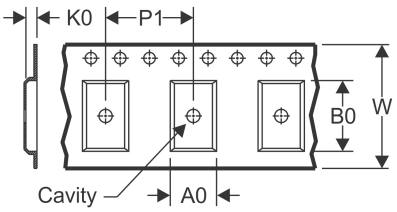
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

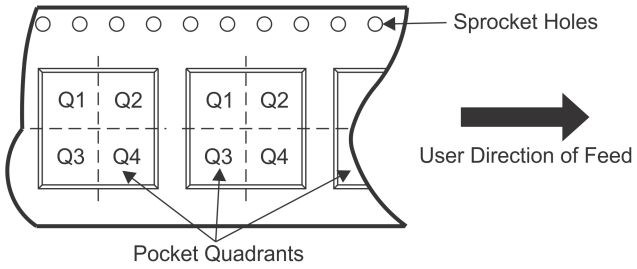



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

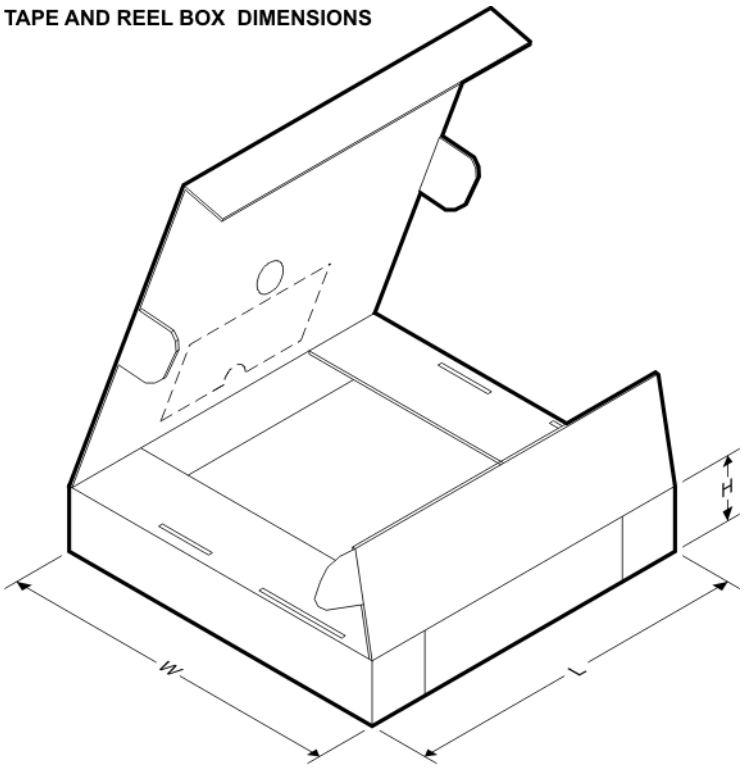
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DS90C185SQ/NOPB | WQFN | NJV | 48 | 1000 | 330.0 | 16.4 | 6.3 | 6.3 | 1.5 | 12.0 | 16.0 | Q1 |
| DS90C185SQE/NOPB | WQFN | NJV | 48 | 250 | 178.0 | 16.4 | 6.3 | 6.3 | 1.5 | 12.0 | 16.0 | Q1 |
| DS90C185SQX/NOPB | WQFN | NJV | 48 | 2500 | 330.0 | 16.4 | 6.3 | 6.3 | 1.5 | 12.0 | 16.0 | Q1 |

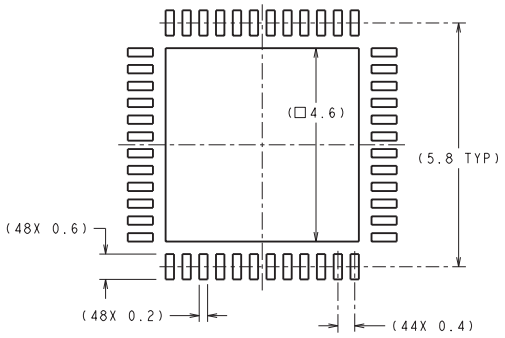
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

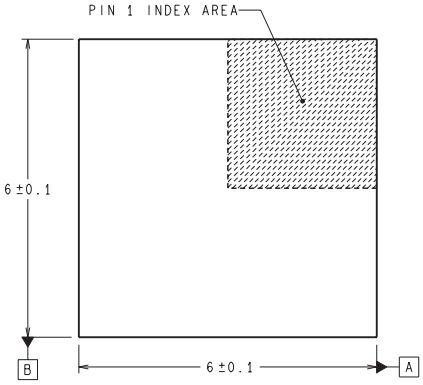
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| DS90C185SQ/NOPB | WQFN | NJV | 48 | 1000 | 367.0 | 367.0 | 35.0 |
| DS90C185SQE/NOPB | WQFN | NJV | 48 | 250 | 210.0 | 185.0 | 35.0 |
| DS90C185SQX/NOPB | WQFN | NJV | 48 | 2500 | 367.0 | 367.0 | 35.0 |

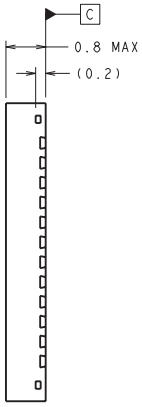
# NJV0048A

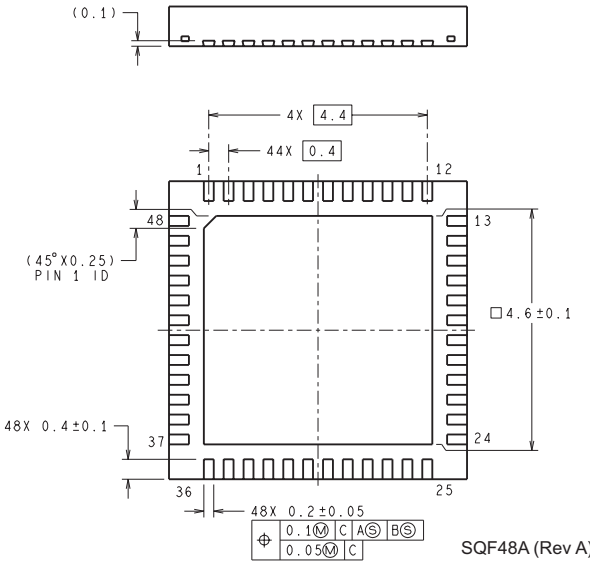



RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

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