

LOW QUIESCENT CURRENT BACK TO BACK MOSFET DRIVER

Features

- Very low quiescent current on and off state
- Back to back configuration
- Boost converter with integrated diode
- Standard level gate voltage
- Under voltage lockout with diagnostic
- Wide operating voltage 3-36V
- Lead-Free, Halogen Free, RoHS compliant

Product Summary

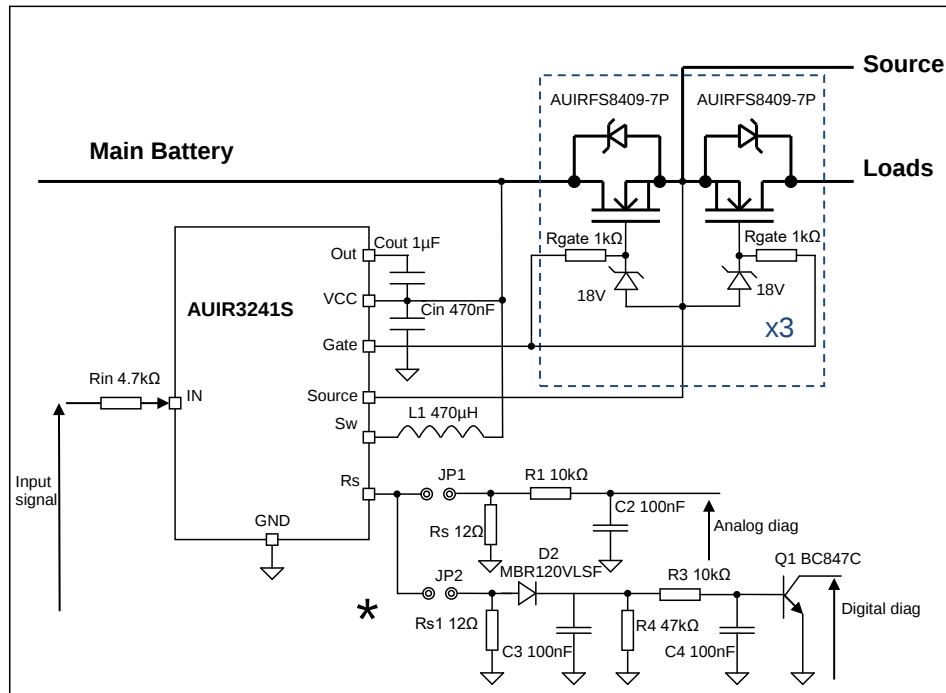
Operating voltage 3-36V
Vgate 11.5V min.
I_{qcc} On 50μA max.
I_{qcc} Off 50μA max.

Description

The AUIR3241S is a high side Mosfet driver for back to back topology targeting back to back switch. It features a very low quiescent current both on and off state. The AUIR3241S is a combination of a boost DC/DC converter using an external inductor and a gate driver. It drives standard level Mosfet even at low battery voltage. On the AUIR3241S, the input controls the gate voltage. The AUIR3241S integrates an under voltage lock out protection to prevent to drive the Mosfet in linear mode.



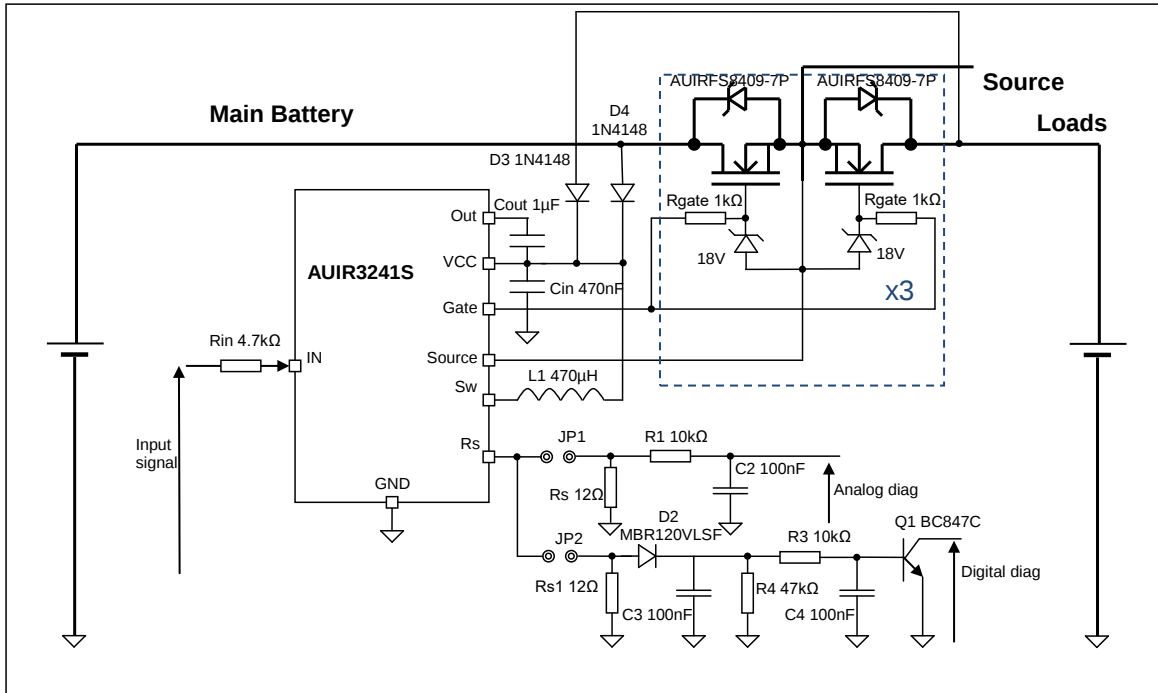
Typical Connection – Back to Back



*Don't connect jumper to JP1 and JP2 in the same time.

Dual battery information

For dual battery application, AUIR3241S can be supply by the “Main Battery” side or “Loads” side. Two diodes (D3 & D4) have to be connected between batteries and Vcc pinout:



On the Demoboard, D4 is shorted and D3 is not connected.

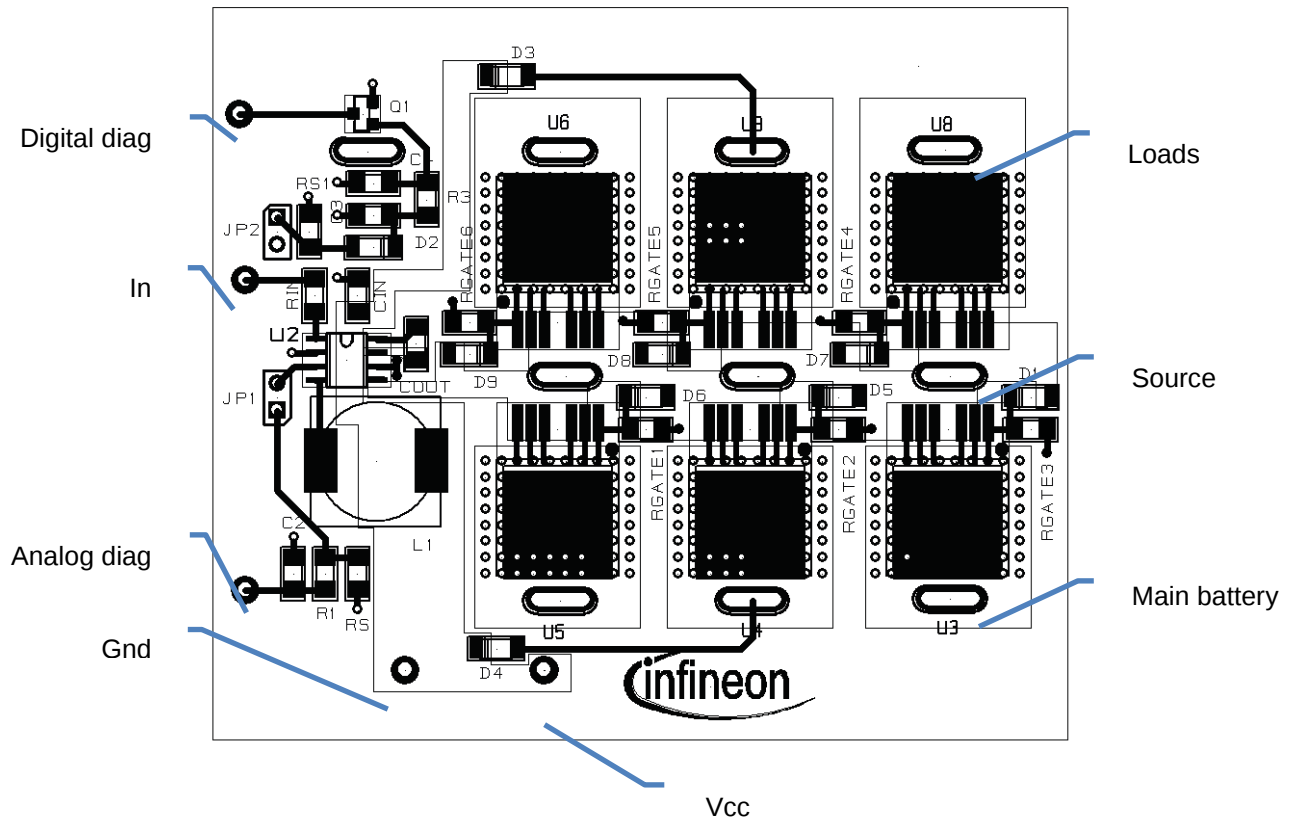
Turn on



Turn on with a Gate-Source resistor: $R_{gs} = 100\Omega$



Component implementation (only top layer):

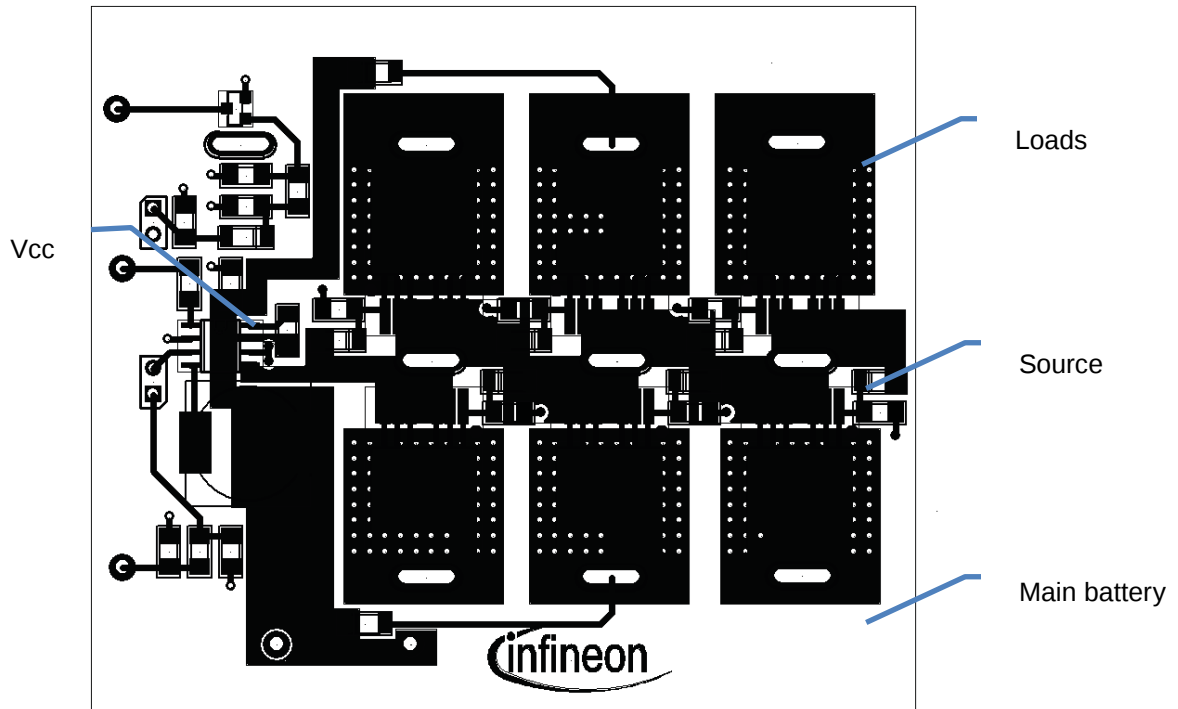


Bill of material:

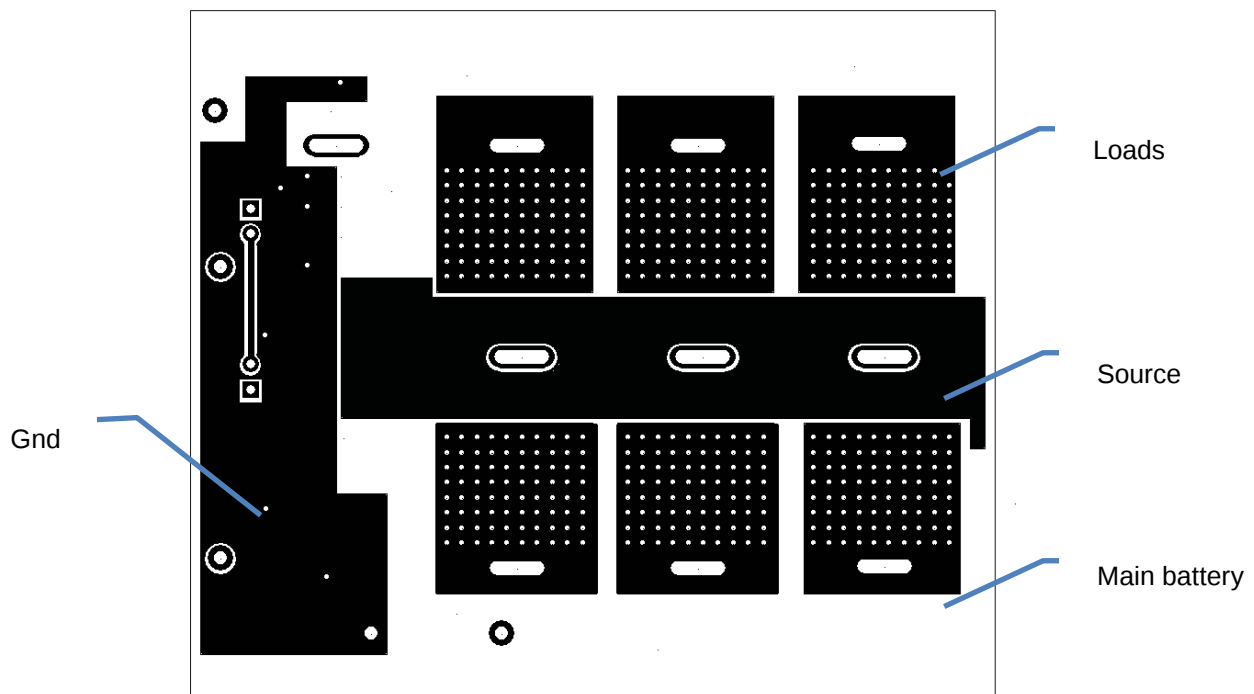
Reference	Value	Description
Cin	470nF 50V	Power supply capacitor
C2,C3,C4	100nF, 25V	Filter capacitor
D1,D5,D6,D7,D8,D9	18V	MMSZ5248BT1G Zener diode protection
D3, D4	1N4148	Schottky diode
D2	MBR120VLSFT1G	Schottky diode
JP1,JP2	Jumper	-
L1	470μH	B82462G4474M
Q1	BC847CE6327	Bipolar transistor
Rin	4.7kΩ	-
Rgate1, Rgate2, Rgate3, Rgate4, Rgate5, Rgate6	1kΩ	-
RS, RS1	12Ω 1%	-
R1,R3	10kΩ	-
R4	47kΩ	
TP1,TP2,TP3,TP4,TP5	Test point	Input/Output test point
U2	AUIR3241	Driver
U3,U4,U5,U6,U8,U9	AUIRFS8409	N-MOSFET
Cout	1μF 25V	Power supply capacitor

PCB Layout:

Top layer:



Bottom layer:



Revision History

Revision	Date	Notes/Changes
A1	November 30, 2015	Initial document
A2	December 10, 2015	BOM modification
A3	December 28, 2015	Update digital diagnostic schematic
A4	April 26, 2016	Add measure and labels updated