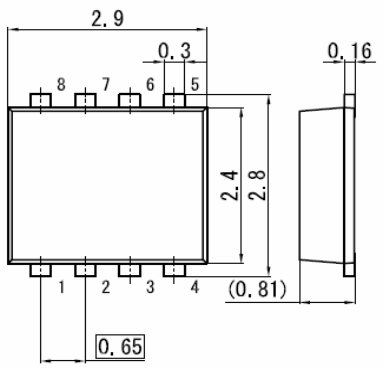
MTMC8E2A0LBF

Dual N-channel MOSFET

For lithium-ion secondary battery protection circuit

Unit: mm



1. Source(FET1) 5. Darin(FET1,2)
2. Gate(FET1) 6. Darin(FET1,2)
3. Source(FET2) 7. Darin(FET1,2)
4. Gate(FET2) 8. Darin(FET1,2)

Panasonic	WMini8-F1
JEITA	SC-115
Code	-

■ Features

- Low drain-source ON resistance:RDS(on)typ. = 15 mΩ (VGS = 4.5 V)
- Built-in gate resistor
- Halogen-free / RoHS compliant
  (EU RoHS / UL-94 V-0 / MSL:Level 1 compliant)

■ Marking Symbol: 4B

■ Packaging

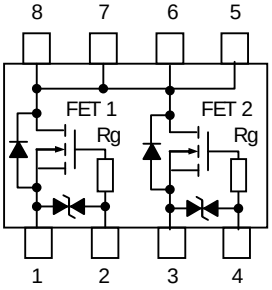
MTMC8E2A0LBF Embossed type (Thermo-compression sealing):
3 000 pcs / reel (standard)

■ Absolute Maximum Ratings Ta = 25 °C

Parameter		Symbol	Rating	Unit
FET1 FET2	Drain-source Voltage	VDS	20	V
	Gate-source Voltage	VGS	±12	V
	Drain Current	ID	7.0	A
	Peak Drain Current	IDp	42	A
Overall	Total Power Dissipation	PD1 *1	1.0	W
		PD2 *1,*2	1.2	
		PD3 *3	0.4	
	Channel Temperature Range	Tch	150	°C
	Storage Temperature	Tstg	-55 to +150	°C

Note: *1 Glass epoxy board: 25.4 mm × 25.4 mm × 0.8 mm Copper foil
of the drain portion should have a area of 300 mm^2 or more
PD absolute maximum rating Non-heat sink: 400 mW
*2 t = 10 s
*3 Non-heat sink

Internal Connection



Pin Name

1. Source(FET1) 5. Darin(FET1,2)
2. Gate(FET1) 6. Darin(FET1,2)
3. Source(FET2) 7. Darin(FET1,2)
4. Gate(FET2) 8. Darin(FET1,2)

Resistance Value	Rg	1	kΩ

■ Electrical Characteristics Ta = 25 °C ± 3 °C

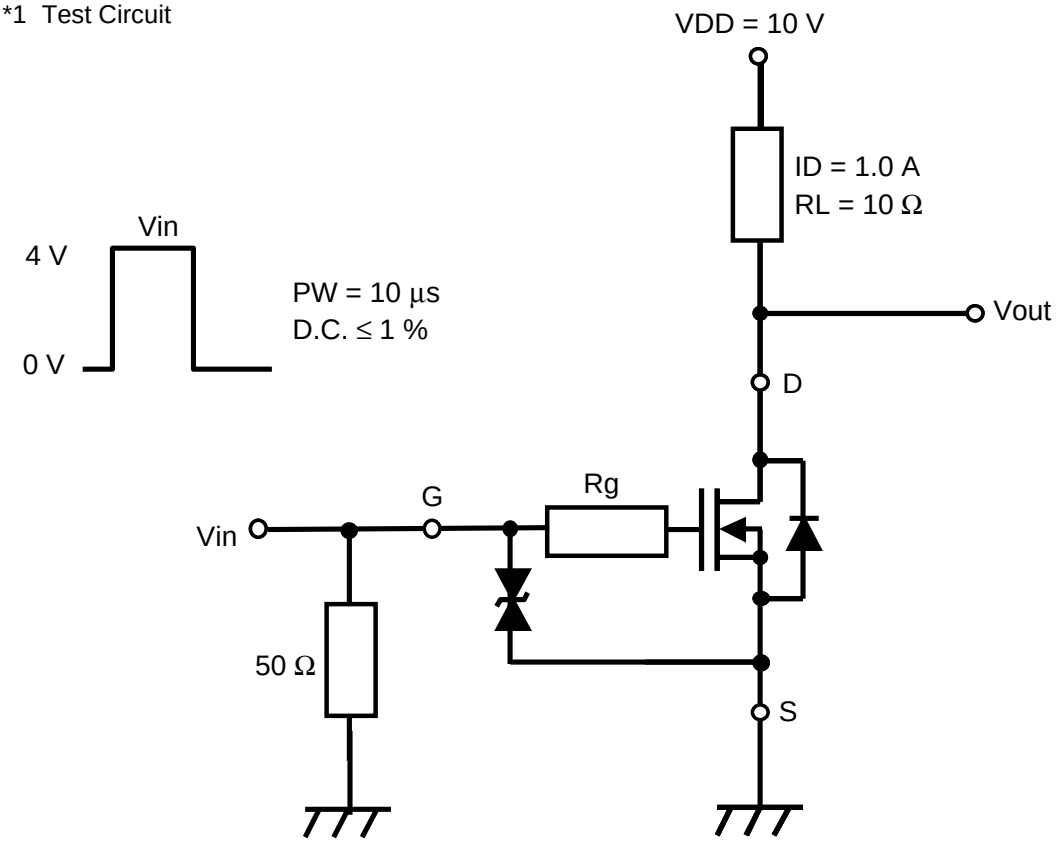
FET1,FET2

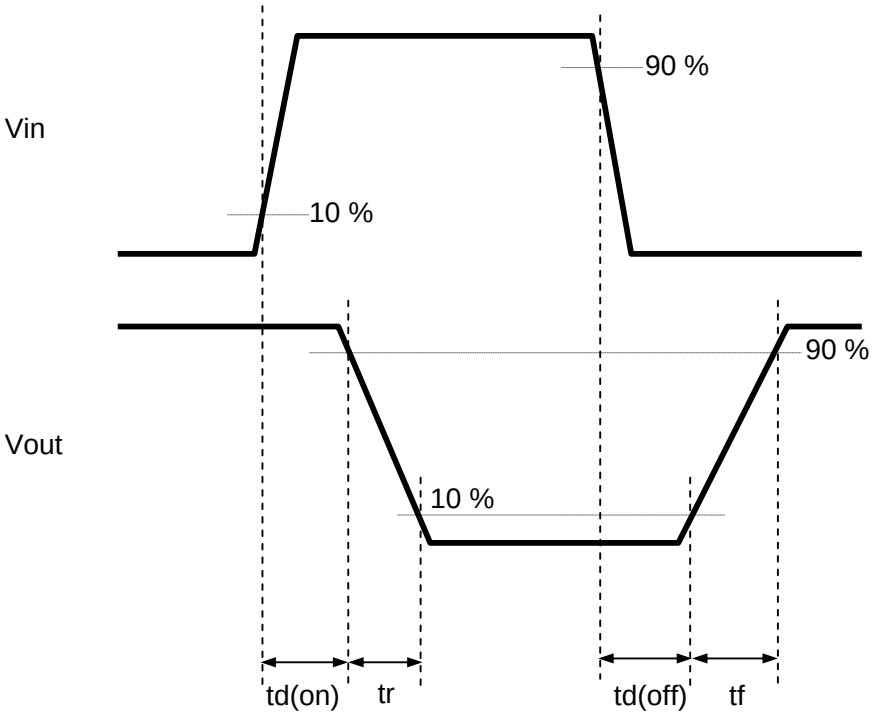
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source Breakdown Voltage	VDSS	ID = 1.0 mA, VGS = 0 V	20			V
Zero Gate Voltage Drain Current	IDSS	VDS = 20 V, VGS = 0 V			1.0	μA
Gate-source Leakage Current	IGSS	VGS = ±8.0 V, VDS = 0 V			±10	μA
Gate-source Threshold Voltage	Vth	ID = 1.0 mA, VDS = 10 V	0.40	0.85	1.30	V
Drain-source On-state Resistance	RDS(on)1	ID = 2.0 A, VGS = 4.5 V		15	21	mΩ
	RDS(on)2	ID = 2.0 A, VGS = 3.7 V		18	25	
	RDS(on)3	ID = 2.0 A, VGS = 2.5 V		22	33	
Forward transfer admittance	|Yfs|	ID = 1.0 A, VDS = -10 V	3.0			S
Input Capacitance	Ciss	VDS = 10 V, VGS = 0 V, f = 1 MHz		1 450		pF
Output Capacitance	Coss			100		
Reverse Transfer Capacitance	Crss			90		
Turn-on Delay Time *1	td(on)	VDD = 10 V, VGS = 0 to 4 V, ID = 1.0 A		0.33		μs
Rise Time *1	tr			0.70		
Turn-off Delay Time *1	td(off)	VDD = 10 V, VGS = 4 to 0 V, ID = 1.0 A		4.0		μs
Fall Time *1	tf			2.0		

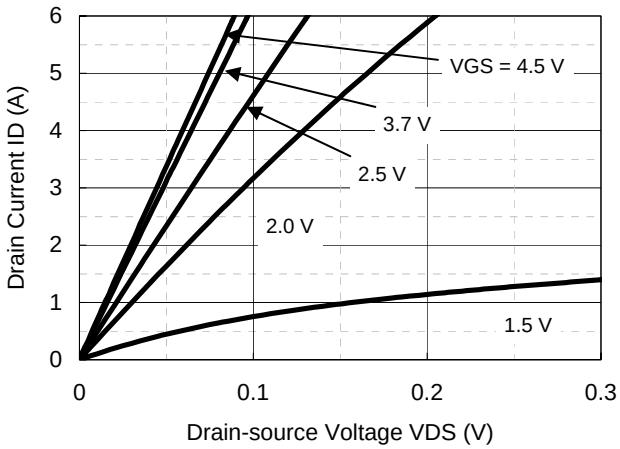
Note: Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

*1 See Test Circuit.

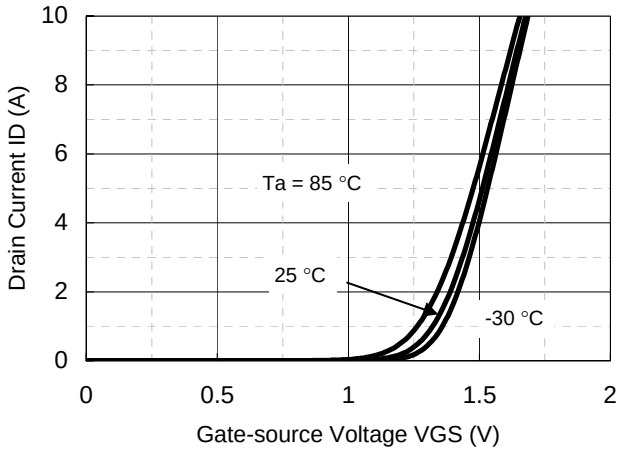
*1 Test Circuit



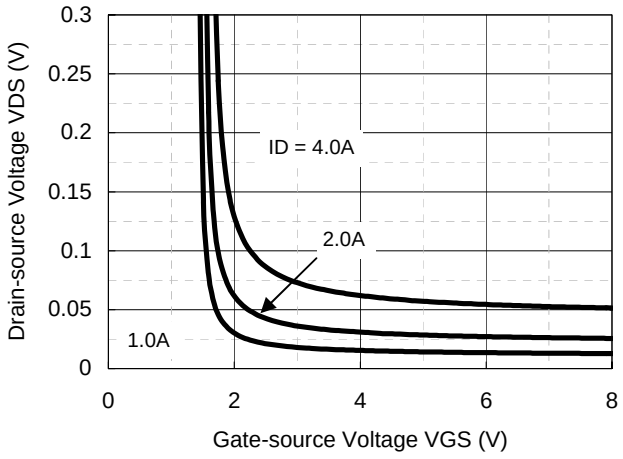




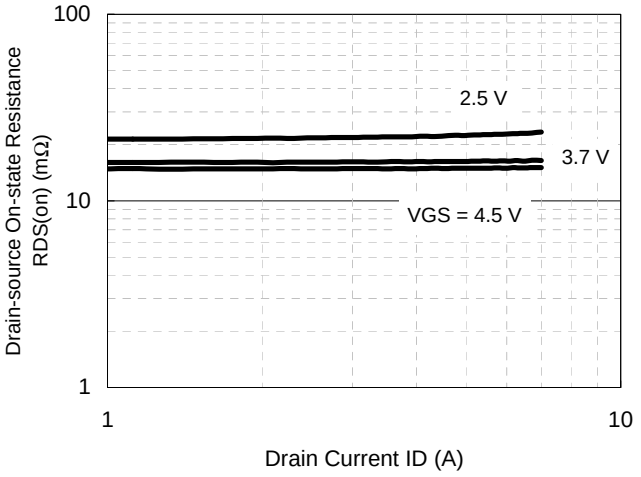
ID - VDS



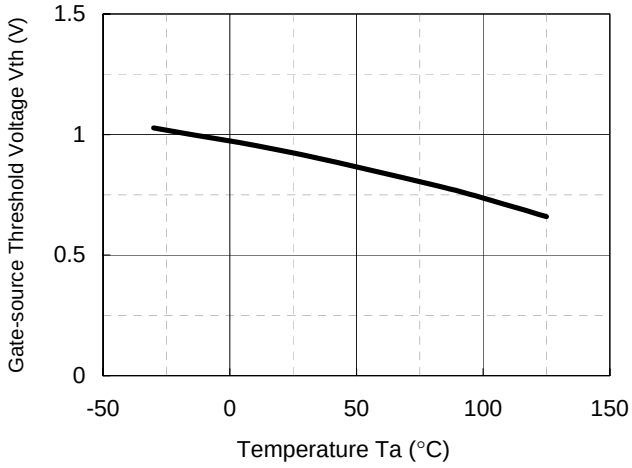
ID - VGS



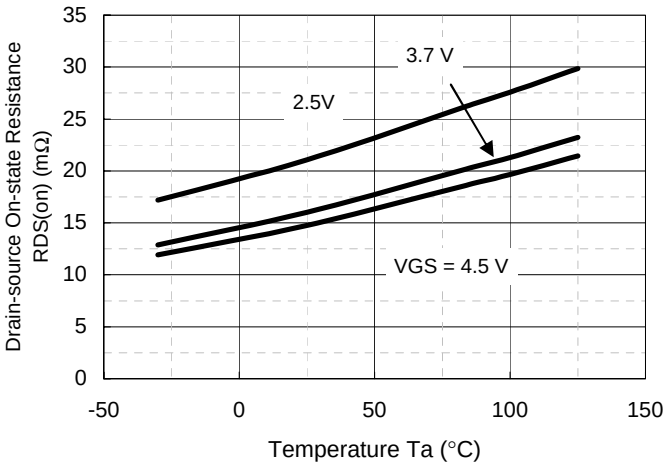
VDS - VGS



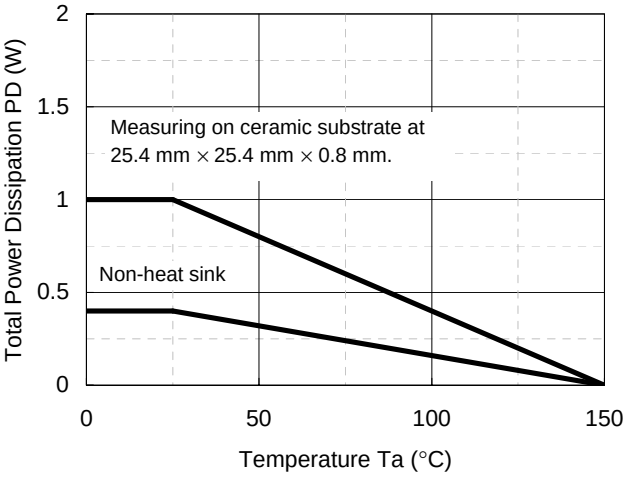
RDS(on) - ID



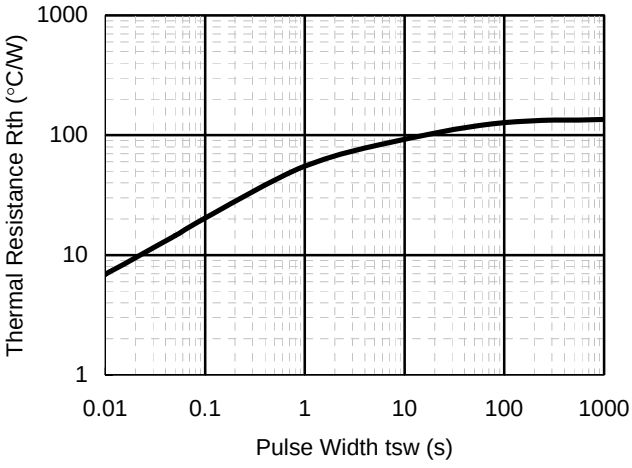
Vth - Ta



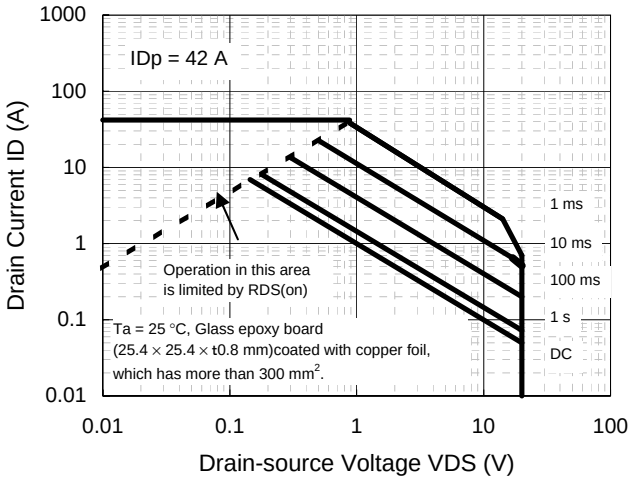
RDS(on) - Ta



PD - Ta



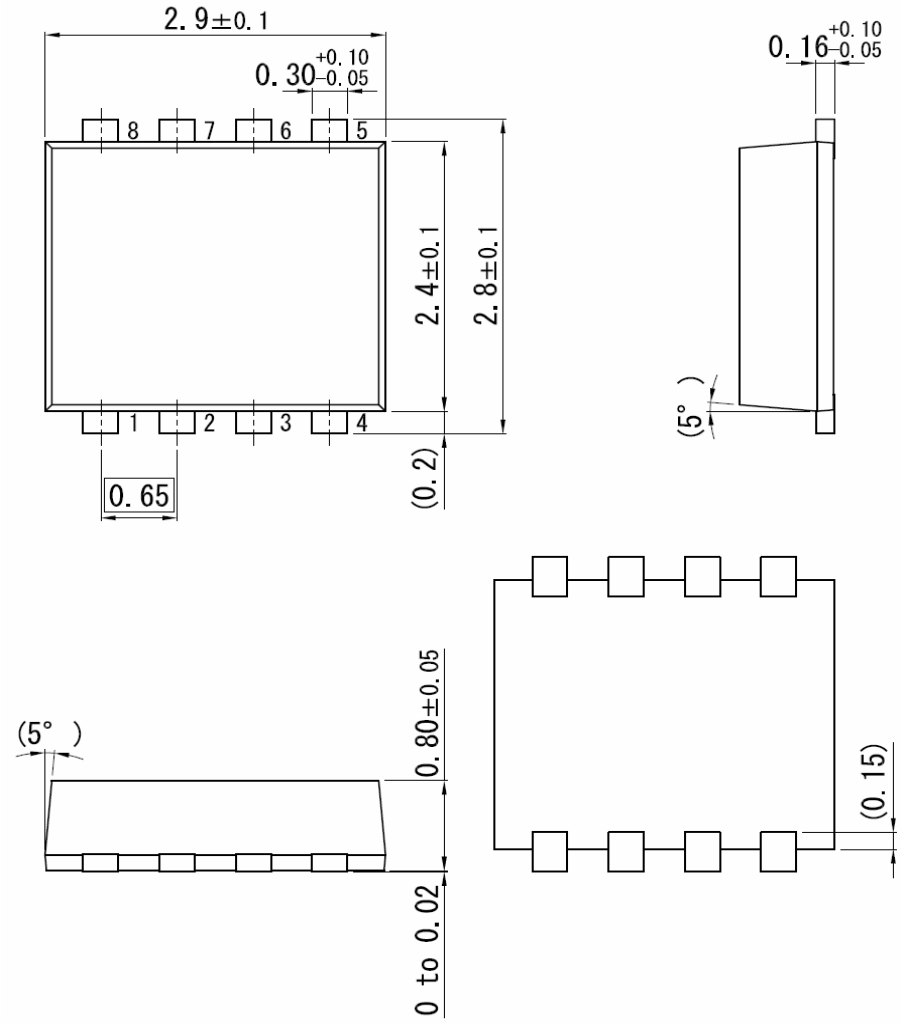
Rth -tsw



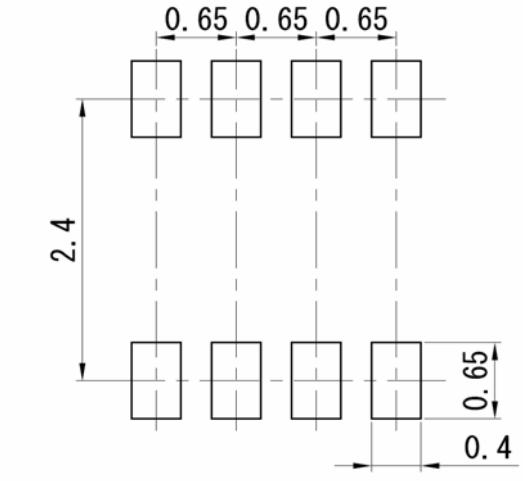
Safe Operating Area

WMini8-F1

Unit: mm



■ Land Pattern (Reference) (Unit: mm)



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