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October 2016

FAN7191_F085
High-Current, High and Low Side Gate Drive IC

Features

- Floating Channel for Bootstrap Operation to +600V
- 4.5A Sourcing and 4.5A Sinking Current Driving Capability
- Common-Mode dV/dt Noise Cancelling Circuit
- Built-in Under-Voltage Lockout for Both Channels
- Matched Propagation Delay for Both Channels
- 3.3V and 5V Input Logic Compatible
- Output In-phase with Input
- Qualified to AEC Q100

Applications

- Advanced Fuel Injection Systems
- Automotive high voltage DC-DC converters
- Starter/Alternator
- Electric Power Steering
- Motor Control (fans, pumps, compressors)
- MOSFET and IGBT driver applications

Description

The FAN7191_F085 is a monolithic high- and low-side gate-drive IC, which can drive high speed MOSFETs and IGBTs that operate up to +600V. It has a buffered output stage with all NMOS transistors designed for high pulse driving capability and minimum cross-conduction.

Fairchild's high-voltage process and common-mode noise canceling technique provide stable operation of high-drivers under high dV/dt noise circumstances. An advanced level-shift circuit allows high-side gate driver operation up to V_S = -9.8V (typical) for V_{BS} = 15V.

The UVLO circuit prevents malfunction when V_{DD} and V_{BS} are lower than the specified threshold voltage.

The high current and low output voltage drop features make this device suitable for controlling direct injection actuators and for use in many automotive DC-DC converter and motor control applications.

8-SOP

Figure 1. Package Options

Ordering Information

Part Number	Operating Temperature Range	Package	Eco Status	Packing Method
FAN7191MX_F085	-40°C to +125°C	8-SOP	RoHS	Tape & Reel

For Fairchild's definition of "green" Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

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Typical Application Circuit

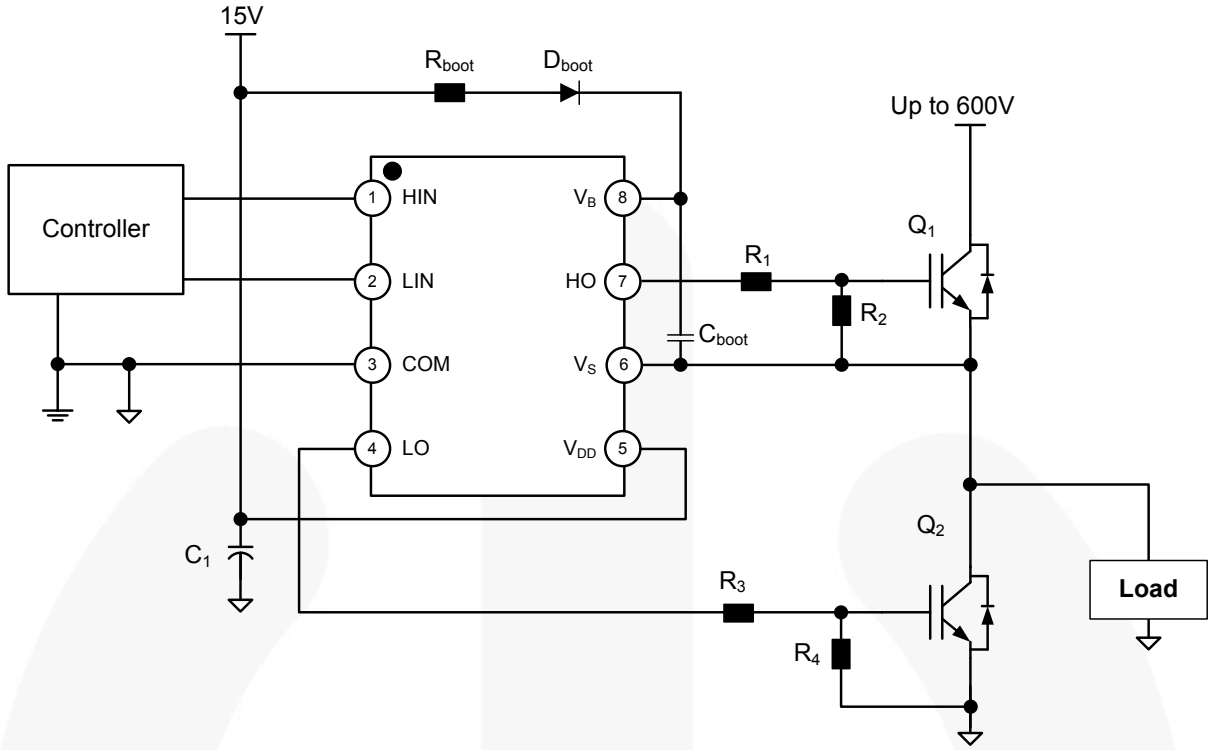

Figure 2. Half-Bridge Application Circuit (8-SOP)

Internal Block Diagram

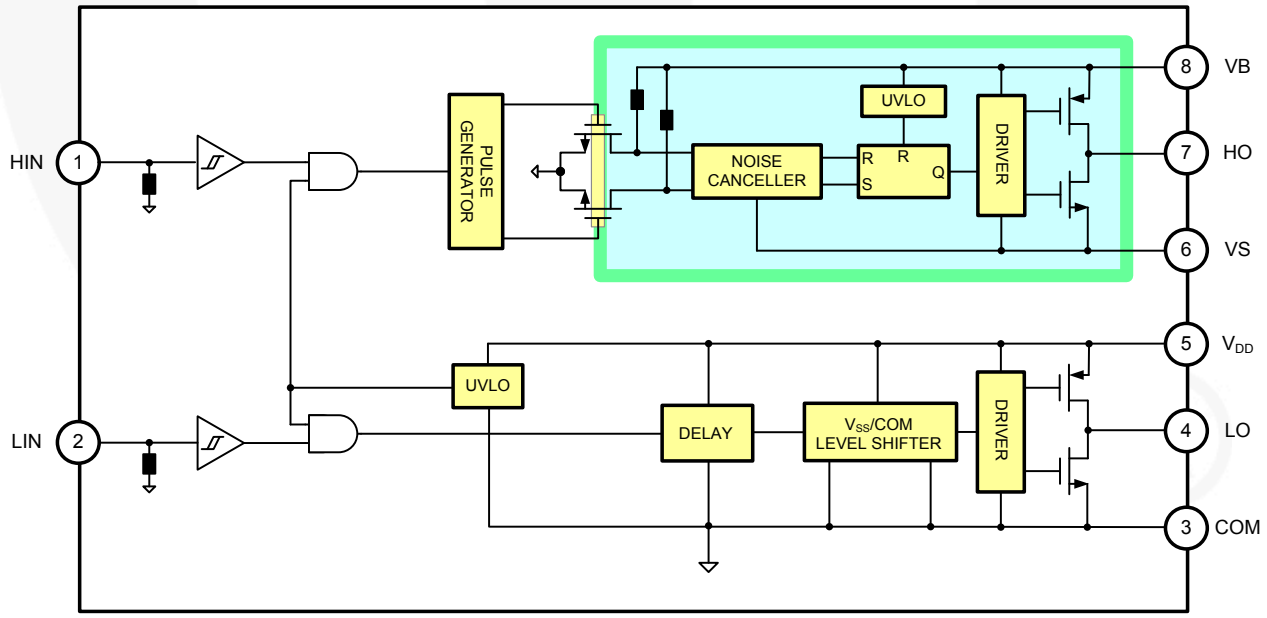

Figure 3. Functional Block Diagram (8-SOP)

Pin Assignment

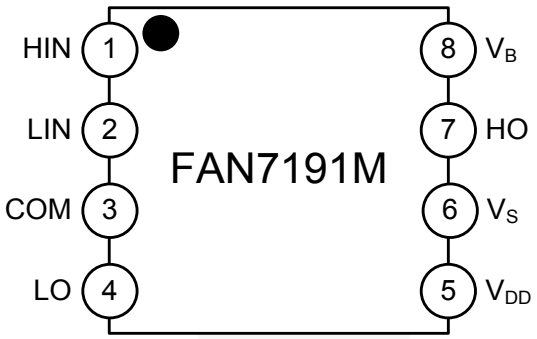

Figure 4. Pin Assignments (Top View)

Pin Definitions

8-Pin	Name	Description
1	HIN	Logic Input for High-Side Gate Driver Output
2	LIN	Logic Input for Low-Side Gate Driver Output
3	COM	Low-side Driver Return
4	LO	Low-Side Driver Output
5	V_{DD}	Low-Side and Logic Power Supply Voltage
6	V_S	High-Side Floating Supply Return
7	HO	High-Side Driver Output
8	V_B	High-Side Floating Supply

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

TA = 25°C, unless otherwise specified. V_B, V_{DD} and V_{IN} are referenced to COM for FAN7191M (8-SOP).

Symbol	Parameter		Min.	Max.	Unit
V_S	High-side offset voltage VS		VB-25	VB+0.3	V
V_B	High-side floating supply voltage VB		-0.3	625	V
V_{HO}	High-side floating output voltage		VS-0.3	VB+0.3	V
V_{DD}	Low-side and logic-fixed supply voltage		-0.3	25	V
V_{IN}	Logic Input voltage (HIN, LIN, EN)		-0.3	VDD+0.3	V
V_{LO}	Low-Side Output Voltage LO		COM-0.3	VDD+0.3	V
t_{pulse}	Minimum Pulse Width[4]		80		ns
$d_{VS/dt}$	Allowable offset voltage slew rate			50	V/ns
P_D[1][2][3]	Power dissipation	8-SOP		0.625	W
θ_{JA}	Thermal Resistance, junction-to-ambient	8-SOP		200	°C/W
T_J	Junction temperature			+150	°C
T_S	Storage temperature		-55	+150	°C
ESD	Electrostatic Discharge Capability	Human Body Model, ANSI/ESDA/JEDEC JS-001-2012		3000	V
		Charged Device Model, JESD22-C101		2000	

Notes:

1. Mounted on 76.2 x 114.3 x 1.6mm PCB (FR-4 glass epoxy material).
2. Refer to the following standards:
   JESD51-2: Integral circuits thermal test method environmental conditions – natural convection
   JESD51-3: Low effective thermal conductivity test board for leaded surface mount packages
3. Do not exceed P_D under any circumstances.
4. Minimum input pulse which is guaranteed to produce an output pulse.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings. V_{DD} is referenced to COM for FAN7191M (8-SOP).

Symbol	Parameter	Min.	Max.	Unit
V_B	High-side floating supply voltage	V_S+10	V_S+22	V
V_S	High-side Floating Supply Offset Voltage	6-V_{DD}	600	V
V_{HO}	High-side Output Voltage	V_S	V_B	V
V_{DD}	Low-side and Logic Supply voltage	10	22	V
V_{LO}	Low-side output voltage	COM	V_{DD}	V
V_{IN}	Logic input voltage (HIN, LIN)	COM	V_{DD}	V
COM	Power Ground	V_{SS}-0.5	V_{SS}+0.5	V
T_A	Ambient Temperature	-40	+125	°C

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Electrical Characteristics

V_{BIAS} (V_{DD}, V_{BS}) = 15.0V, V_S = COM, T_A = 25°C, unless otherwise specified. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to COM and are applicable to the respective input signals HIN and LIN. The V_O and I_O parameters are referenced to COM. V_S and GND and are applicable to the respective outputs HO and LO.

Symbol	Characteristic	Condition	Min.	Typ.	Max.	Unit
POWER SUPPLY SECTION (V_{DD} and V_{BS})						
V_{DDUV+} V_{BSUV+}	V_{DD} and V_{BS} Supply Under-Voltage Positive-going Threshold		7.8	8.8	9.8	V
V_{DDUV-} V_{BSUV-}	V_{DD} and V_{BS} Supply Under-Voltage Negative Going Threshold		7.2	8.3	9.1	
V_{DDHYS}	V_{DD} supply under-voltage lockout hysteresis			0.5		
I_{LK}	Offset Supply Leakage Current	V_B = V_S = 600V			50	μA
I_{QBS}	Quiescent V_{BS} Supply Current	V_{IN} = 0V or 5V		45	110	
I_{QDD}	Quiescent V_{DD} Supply Current	V_{IN} = 0V or 5V		75	150	
I_{PBS}	Operating V_{BS} Supply Current	f_{IN} = 20kHz, rms value		400	800	μA
I_{PDD}	Operating V_{DD} Supply Current	f_{IN} = 20kHz, rms value		400	800	
LOGIC INPUT SECTION (HIN, LIN, EN)						
V_{IH}	Logic “1” Input Voltage		2.5			V
V_{IL}	Logic “0” Input Voltage				1.2	
I_{IN+}	Logic “1” Input Bias Current (HIN/LIN)	V_{IN} = 5V		25	50	μA
I_{IN-}	Logic “0” Input Bias Current (HIN/LIN)	V_{IN} = 0V		1.0	2.0	
R_{IN}	Input Pull-down Resistance		100	200		kΩ
GATE DRIVER OUTPUT SECTION (HO, LO)						
V_{OH}	High-level Output Voltage, V_{BIAS}-V_O	No Load			1.35	V
V_{OL}	Low-level Output Voltage, V_O	No Load			35	mV
I_{O+}	Output HIGH, Short-circuit Pulsed Current	V_O=0V, V_{IN}=5V with PW<10μs	3.5	4.5		A
I_{O-}	Output LOW Short-circuit Pulsed Current	V_O=15V, V_{IN}=0V with PW<10μs	3.5	4.5		
V_S	Allowable Negative V_S Pin Voltage for HIN Signal Propagation to HO			-9.8	-7.0	V

Note:
5. This parameter guaranteed by design.

Dynamic Electrical Characteristics

V_{BIAS} (V_{DD}, V_{BS}) = 15.0V, V_S = COM = 0V, T_A = 25°C, C_{LOAD}=1000pF unless otherwise specified.

Symbol	Characteristic	Condition	Min.	Typ.	Max.	Unit
t_{on}	Turn-on Propagation Delay	V_S=0V		140	200	ns
t_{off}	Turn-off Propagation Delay	V_S=0V		140	200	ns
MT	Delay Matching				55	ns
t_r	Turn-off Rise Time			25	50	ns
t_f	Turn-off Fall Time			25	50	ns

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Typical Characteristics

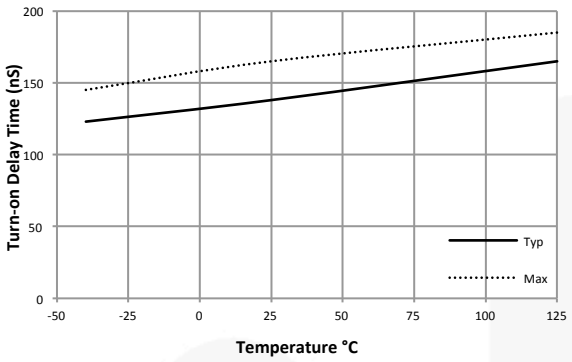

Figure 7. Turn-on Propagation Delay vs. Temperature

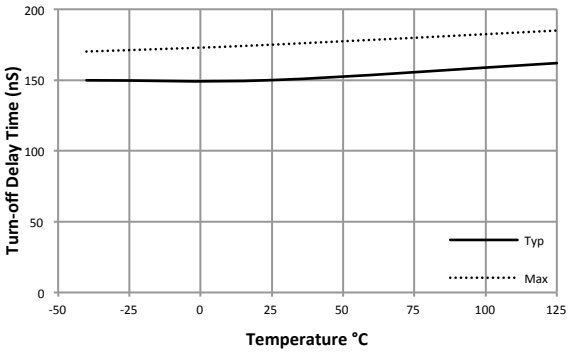

Figure 8. Turn-off Propagation Delay vs. Temperature

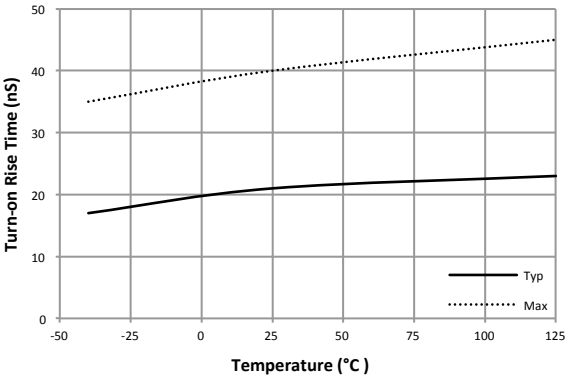

Figure 9. Turn-on Rise Time vs. Temperature

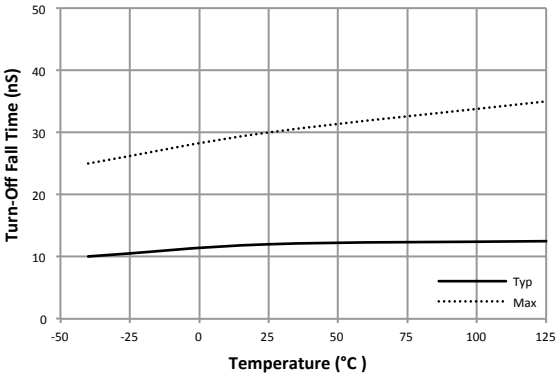

Figure 10. Turn-off Fall Time vs. Temperature

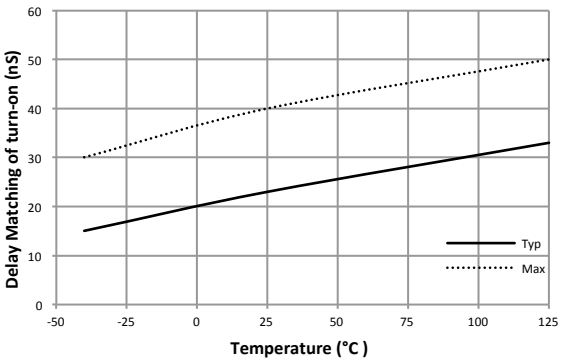

Figure 11. Turn-on Delay Matching vs. Temperature

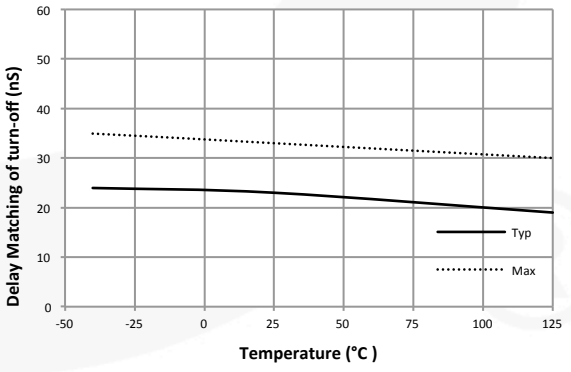

Figure 12. Turn-off Delay Matching vs. Temperature

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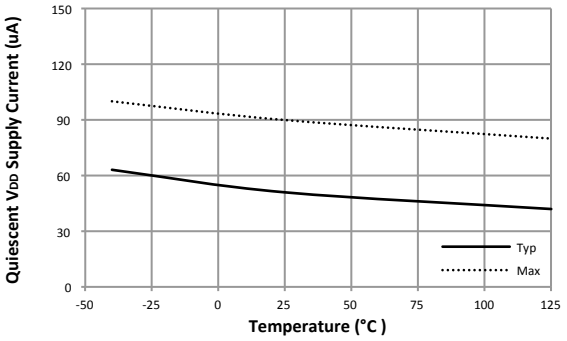

Figure 13. Quiescent V_{DD} Supply Current vs. Temperature

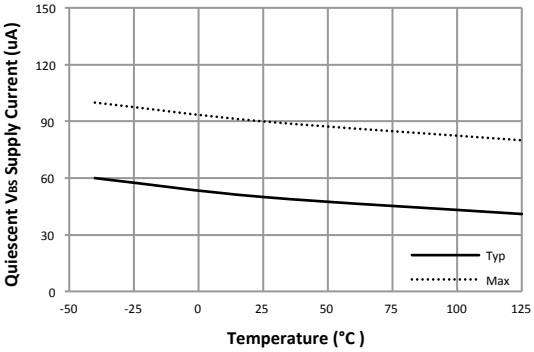

Figure 14. Quiescent V_{BS} Supply Current vs. Temperature

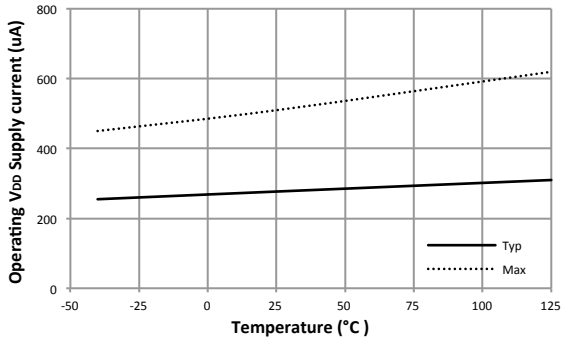

Figure 15. Operating V_{DD} Supply Current vs. Temperature

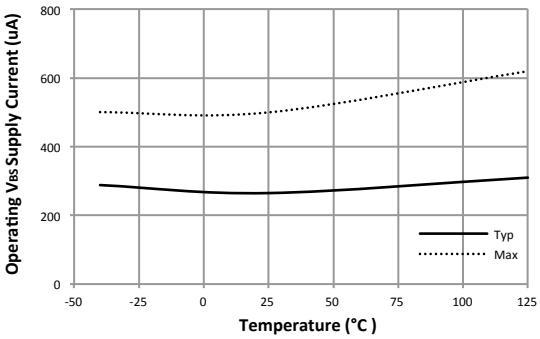

Figure 16. Operating V_{BS} Supply Current vs. Temperature

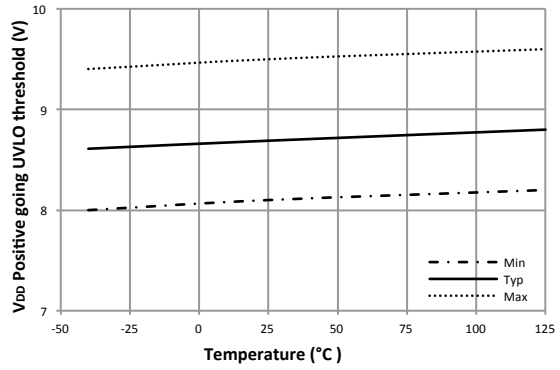

Figure 17. V_{DD} UVLO+ vs. Temperature

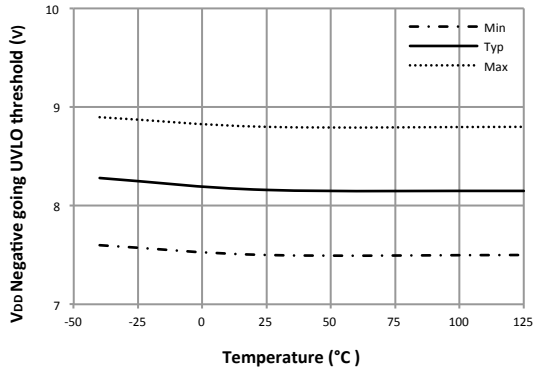

Figure 18. V_{DD} UVLO- vs. Temperature

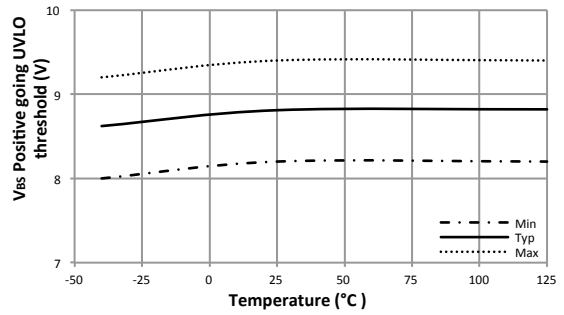

Figure 19. V_{BS} UVLO+ vs. Temperature

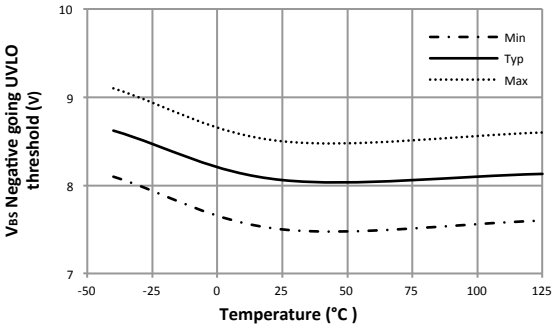

Figure 20. V_{BS} UVLO- vs. Temperature

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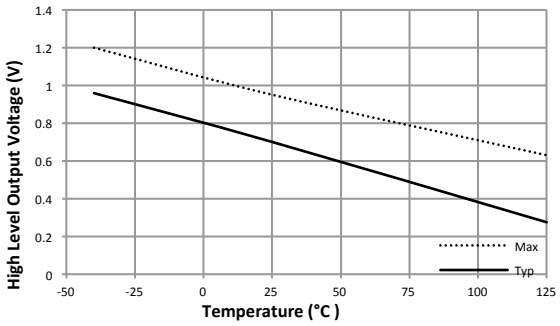

Figure 21. High-Level Output Voltage vs. Temperature

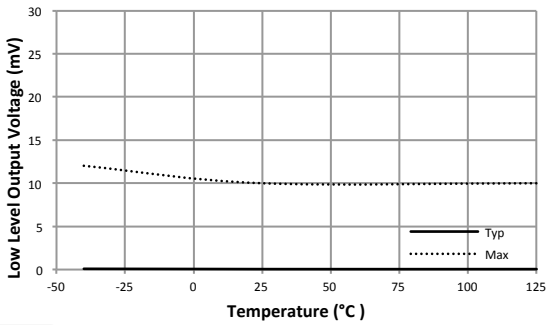

Figure 22. Low-Level Output Voltage vs. Temperature

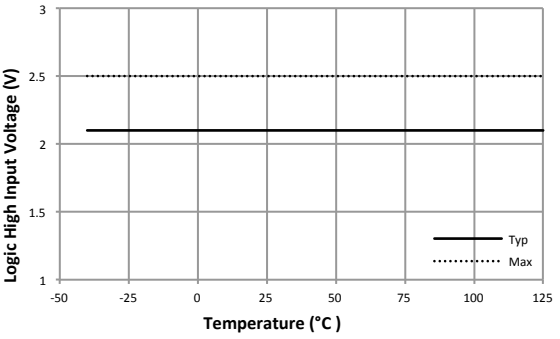

Figure 23. Logic High Input Voltage vs. Temperature

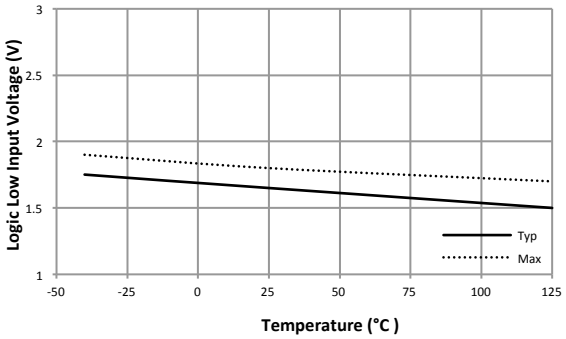

Figure 24. Logic Low Input Voltage vs. Temperature

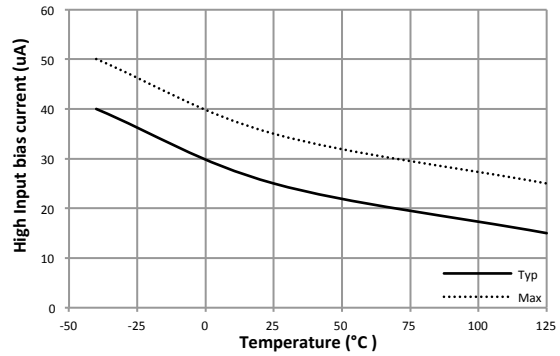

Figure 25. Logic “1” Input Bias Current vs. Temperature

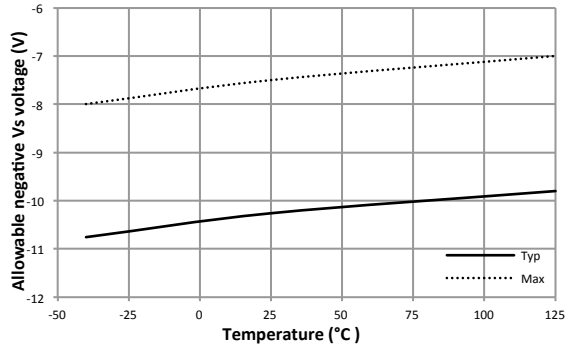

Figure 26. Allowable Negative V_S Voltage vs. Temperature

Switching Time Definitions

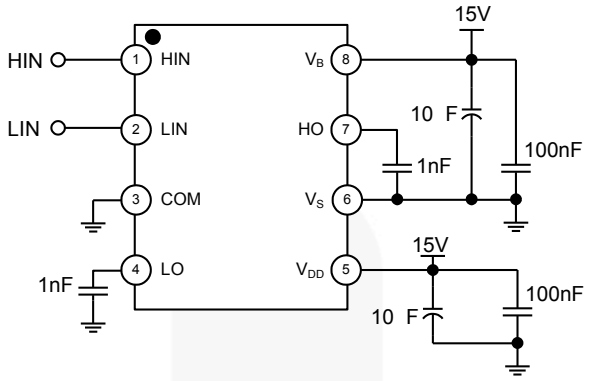

Figure 27. Switching Time Test Circuit (8-SOP)

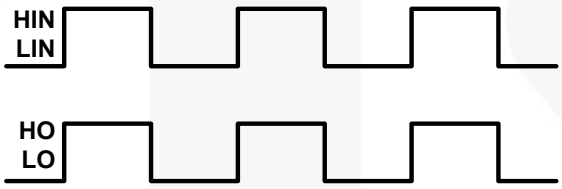

Figure 28. Input/Output Timing Diagram

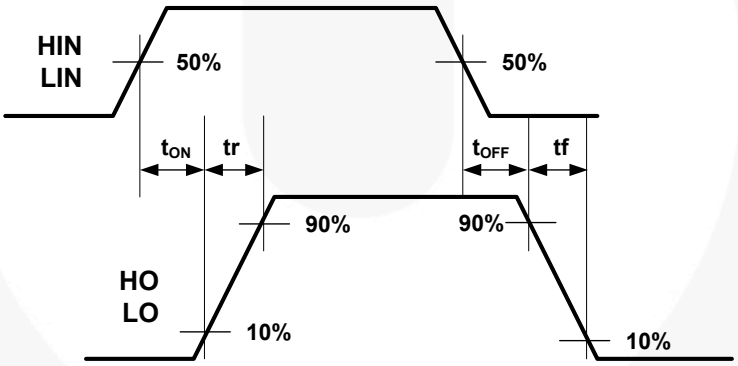

Figure 29. Switching Time Waveform Definitions

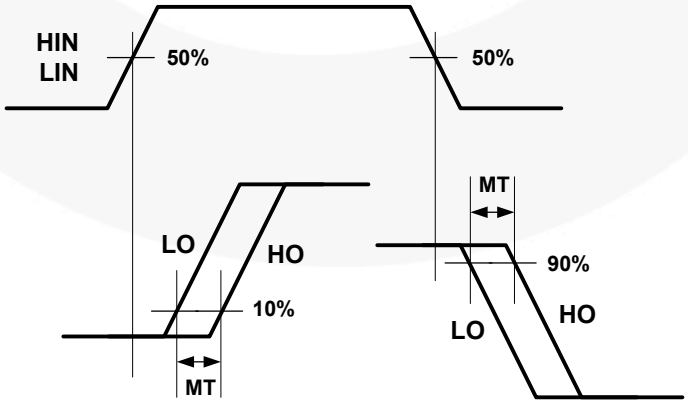

Figure 30. Delay Matching Waveform Definition

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Package Dimensions

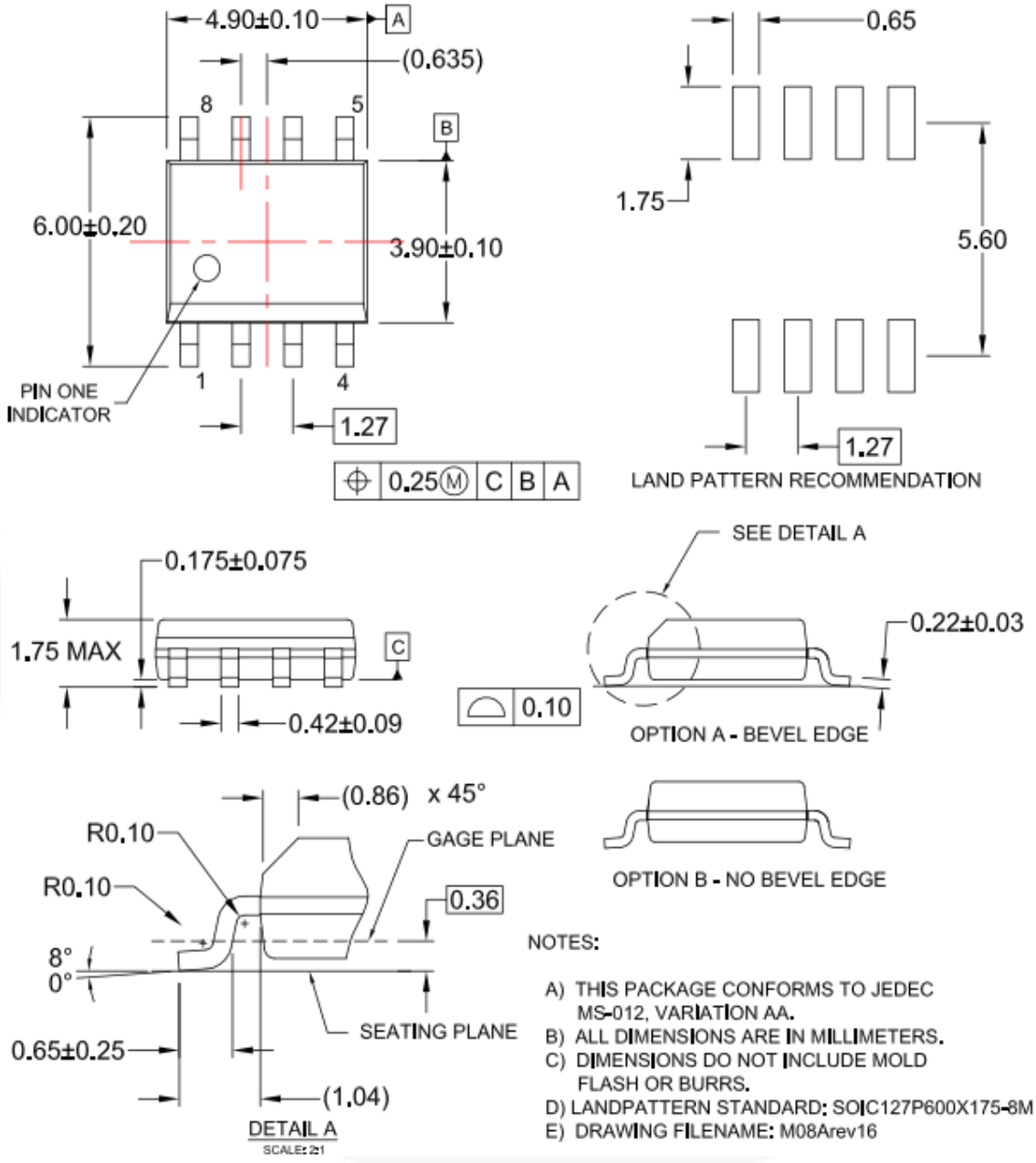

Figure 31. 8-Lead, Small Outline Package (SOP)

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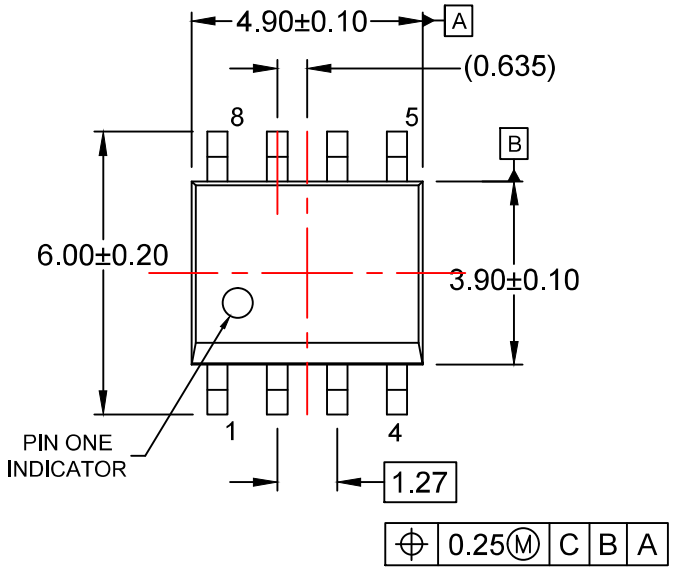
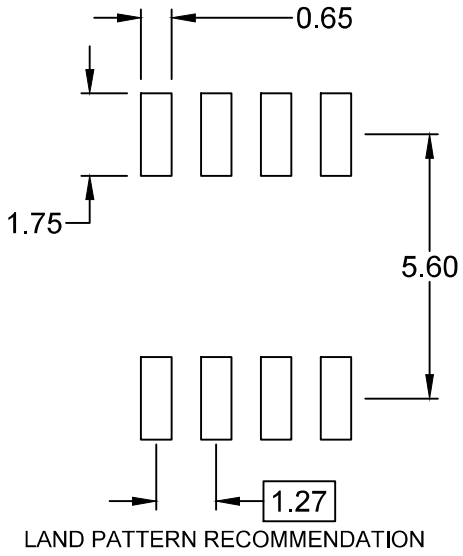
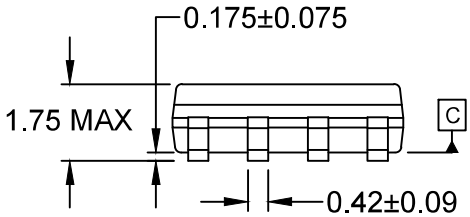
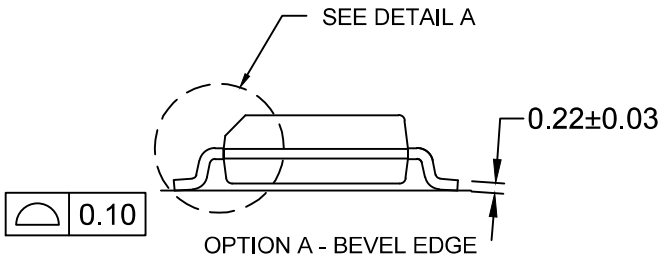


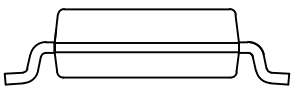


LAND PATTERN RECOMMENDATION

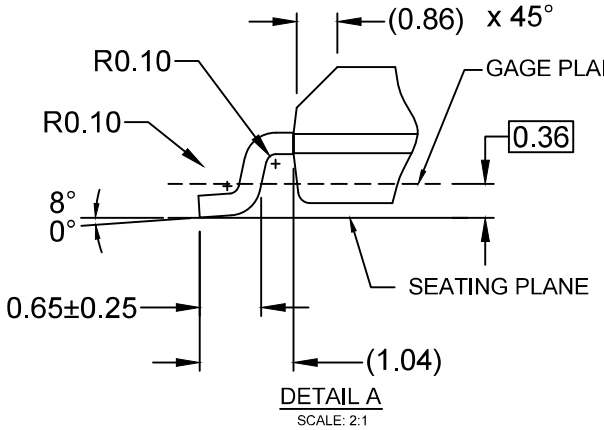




OPTION A - BEVEL EDGE



OPTION B - NO BEVEL EDGE



DETAIL A
SCALE: 2:1

NOTES:

A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M
E) DRAWING FILENAME: M08Arev16

FAIRCHILD.

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