

## N-channel 650 V, 0.075 $\Omega$ typ., 22.5 A MDmesh™ M5 Power MOSFET in a PowerFLAT™ 8x8 HV package

Datasheet - production data

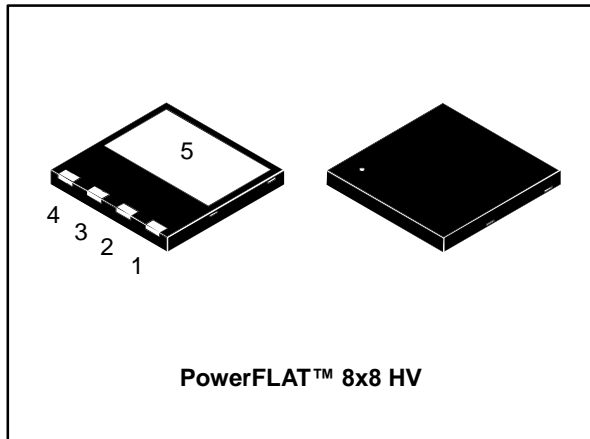
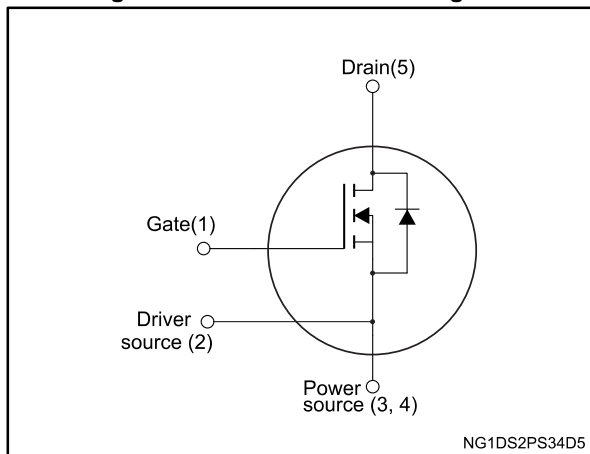


Figure 1: Internal schematic diagram



### Features

Order code	$V_{DS}$ @ $T_{Jmax.}$	$R_{DS(on)}$ max.	$I_D$	$P_{TOT}$
STL45N65M5	710 V	0.086 $\Omega$	22.5 A	160 W

- Extremely low  $R_{DS(on)}$
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET based on the MDmesh™ M5 innovative vertical process technology combined with the well-known PowerMESH™ horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STL45N65M5	45N65M5	PowerFLAT™ 8x8 HV	Tape and reel

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# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	650	V
$V_{GS}$	Gate-source voltage	±25	V
$I_D^{(1)}$	Drain current (continuous) at $T_{case} = 25\text{ °C}$	22.5	A
	Drain current (continuous) at $T_{case} = 100\text{ °C}$	18	
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	90	A
$P_{TOT}^{(1)}$	Total dissipation at $T_{case} = 25\text{ °C}$	160	W
$I_D^{(3)}$	Drain current (continuous) at $T_{amb} = 25\text{ °C}$	3.8	A
	Drain current (continuous) at $T_{amb} = 100\text{ °C}$	2.4	
$P_{TOT}^{(3)}$	Total dissipation at $T_{amb} = 25\text{ °C}$	2.8	W
$dv/dt^{(4)}$	Peak diode recovery voltage slope	15	V/ns
$T_{stg}$	Storage temperature	-55 to 150	°C
$T_j$	Operating junction temperature		

**Notes:**

- (1) The value is rated according to  $R_{thj-case}$  and limited by package.
- (2) Pulse width limited by safe operating area.
- (3) When mounted on a 1-inch<sup>2</sup> FR-4, 2oz Cu board.
- (4)  $I_{SD} \leq 22.5\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DD} = 400\text{ V}$ ,  $V_{DS(peak)} < V_{(BR)DSS}$ .

**Table 3: Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.78	°C/W
$R_{thj-amb}^{(1)}$	Thermal resistance junction-ambient	45	

**Notes:**

- (1) When mounted on a 1-inch<sup>2</sup> FR-4, 2oz Cu board.

**Table 4: Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}^{(1)}$	Avalanche current, repetitive or not repetitive	8	A
$E_{AS}^{(2)}$	Single pulse avalanche energy	810	mJ

**Notes:**

- (1) Pulse width limited by  $T_{jmax}$ .
- (2) starting  $T_j = 25\text{ °C}$ ,  $I_D = I_{AR}$ ,  $V_{DD} = 50\text{ V}$ .

## 2 Electrical characteristics

( $T_{\text{case}} = 25\text{ °C}$  unless otherwise specified)

**Table 5: Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$ , $I_{\text{D}} = 1\text{ mA}$	650			V
$I_{\text{DSS}}$	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$ , $V_{\text{DS}} = 650\text{ V}$			1	$\mu\text{A}$
		$V_{\text{GS}} = 0\text{ V}$ , $V_{\text{DS}} = 650\text{ V}$ , $T_{\text{case}} = 125\text{ °C}$			100	$\mu\text{A}$
$I_{\text{GSS}}$	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$ , $V_{\text{GS}} = \pm 25\text{ V}$			$\pm 100$	nA
$V_{\text{GS}(\text{th})}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$ , $I_{\text{D}} = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{\text{DS}(\text{on})}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$ , $I_{\text{D}} = 14.5\text{ A}$		0.075	0.086	$\Omega$

**Table 6: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{\text{ISS}}$	Input capacitance	$V_{\text{DS}} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{\text{GS}} = 0\text{ V}$	-	3470	-	pF
$C_{\text{OSS}}$	Output capacitance		-	82	-	
$C_{\text{RSS}}$	Reverse transfer capacitance		-	7	-	
$C_{\text{o(er)}^{(1)}}$	Equivalent output capacitance energy related	$V_{\text{GS}} = 0\text{ V}$ , $V_{\text{DS}} = 0\text{ to }520\text{ V}$	-	79	-	pF
$C_{\text{o(tr)}^{(2)}}$	Equivalent output capacitance time related		-	280	-	
$R_{\text{G}}$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_{\text{D}} = 0\text{ A}$	-	2	-	$\Omega$
$Q_{\text{g}}$	Total gate charge	$V_{\text{DD}} = 520\text{ V}$ , $I_{\text{D}} = 17.5\text{ A}$ , $V_{\text{GS}} = 10\text{ V}$ (see <a href="#">Figure 16: "Gate charge test circuit"</a> )	-	82	-	nC
$Q_{\text{gs}}$	Gate-source charge		-	18.5	-	
$Q_{\text{gd}}$	Gate-drain charge		-	35	-	

**Notes:**

(1) Energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{\text{OSS}}$  when  $V_{\text{DS}}$  increases from 0 to 80%  $V_{\text{DSS}}$

(2) Time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{\text{OSS}}$  when  $V_{\text{DS}}$  increases from 0 to 80%  $V_{\text{DSS}}$

**Table 7: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d(v)}}$	Voltage delay time	$V_{\text{DD}} = 400\text{ V}$ , $I_{\text{D}} = 22.5\text{ A}$ $R_{\text{G}} = 4.7\text{ }\Omega$ , $V_{\text{GS}} = 10\text{ V}$ (see <a href="#">Figure 20: "Switching time waveform"</a> )	-	79.5	-	ns
$t_{\text{r(v)}}$	Voltage rise time		-	11	-	
$t_{\text{f(i)}}$	Current fall time		-	9.3	-	
$t_{\text{c(off)}}$	Crossing time		-	16	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		22.5	A
$I_{SDM}^{(1)(2)}$	Source-drain current (pulsed)		-		90	A
$V_{SD}^{(3)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 22.5\text{ A}$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 22.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 100\text{ V}$ (see <a href="#">Figure 17</a> : " <i>Test circuit for inductive load switching and diode recovery times</i> ")	-	346		ns
$Q_{rr}$	Reverse recovery charge		-	6		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	35		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 22.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 100\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 17</a> : " <i>Test circuit for inductive load switching and diode recovery times</i> ")	-	432		ns
$Q_{rr}$	Reverse recovery charge		-	8.4		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	39		A

**Notes:**

- (1) The value is rated according to  $R_{thj-case}$  and limited by package.  
(2) Pulse width is limited by safe operating area.  
(3) Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

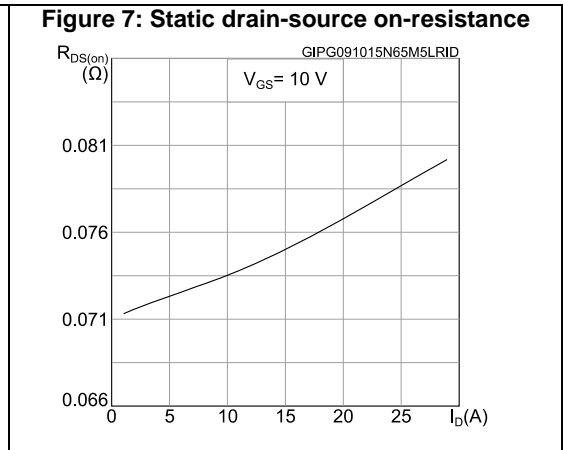
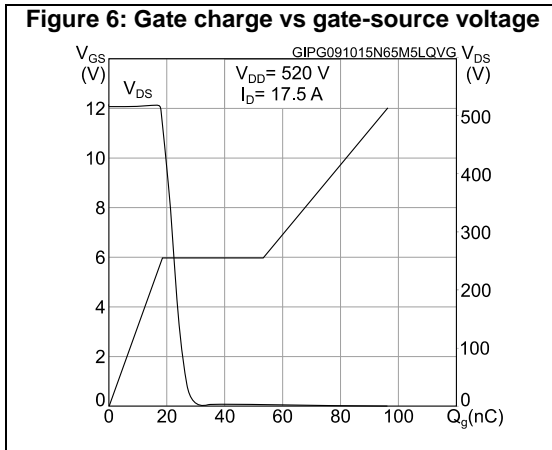
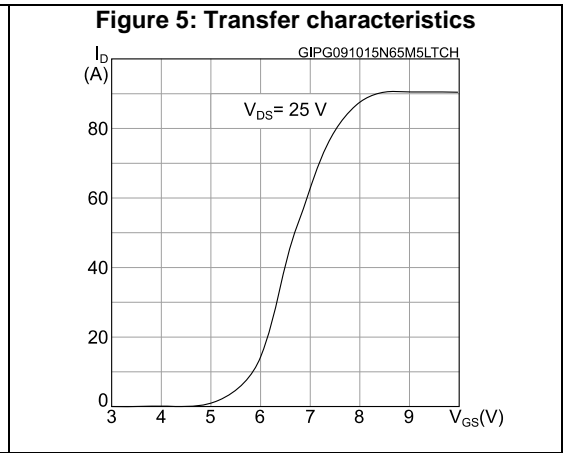
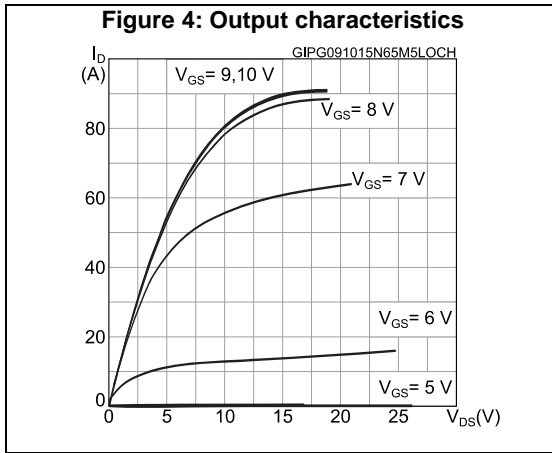
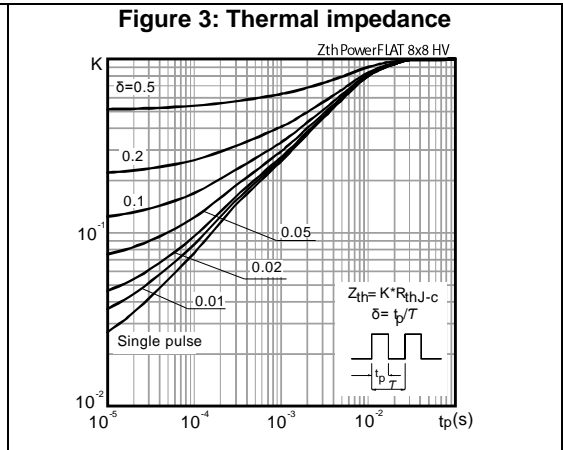
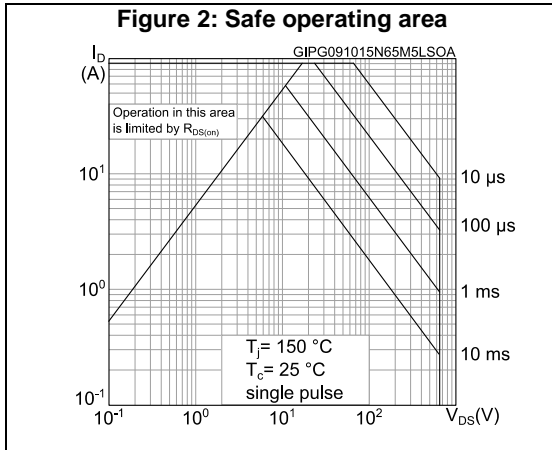


Figure 8: Capacitance variations

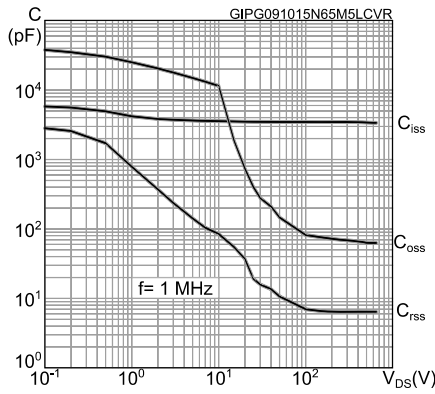


Figure 9: Output capacitance stored energy

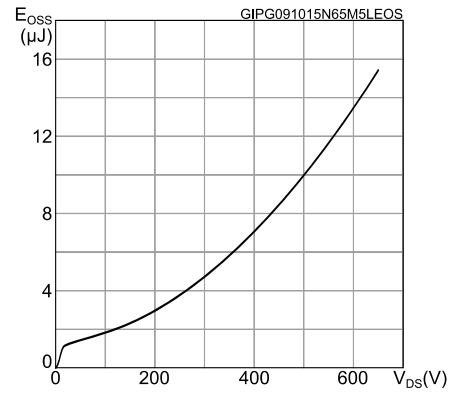


Figure 10: Normalized gate threshold voltage vs temperature

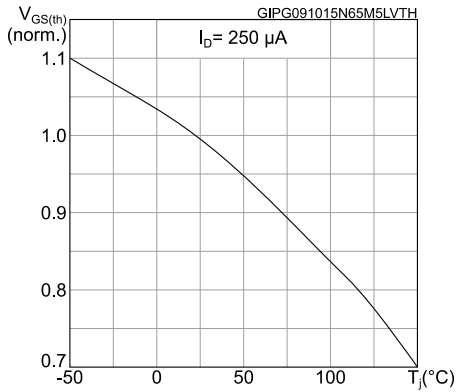


Figure 11: Normalized on-resistance vs. temperature

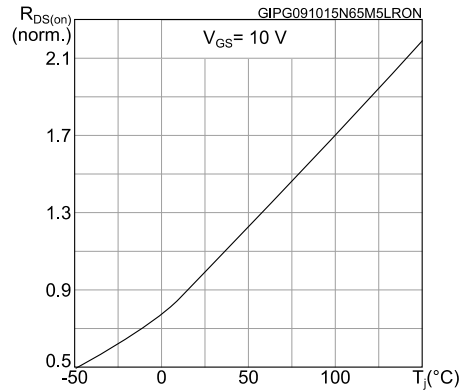


Figure 12: Drain-source diode forward characteristics

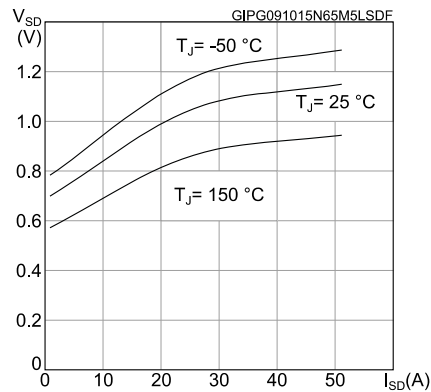


Figure 13: Normalized V(BR)DSS vs temperature

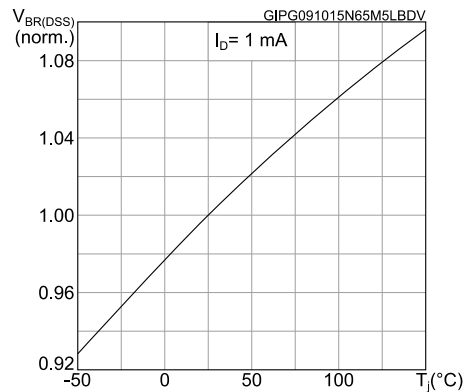
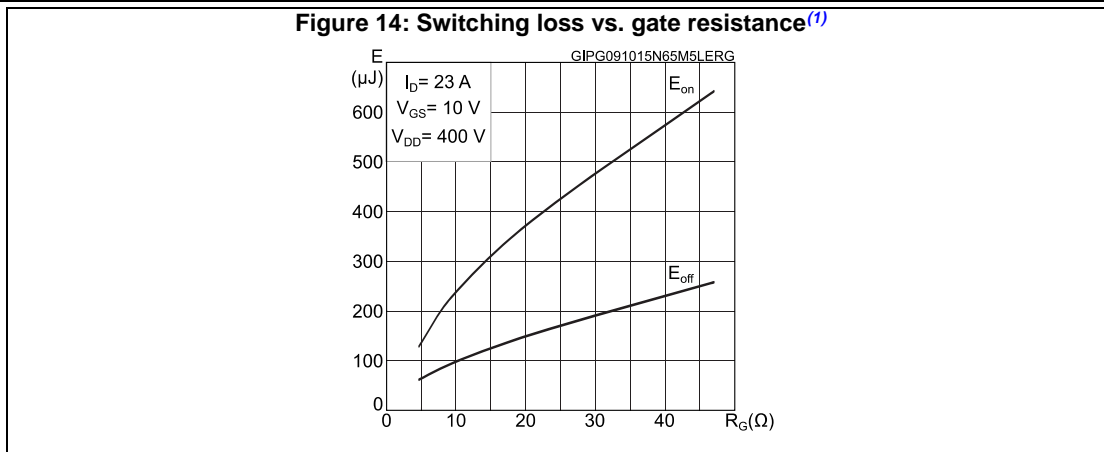


Figure 14: Switching loss vs. gate resistance<sup>(1)</sup>

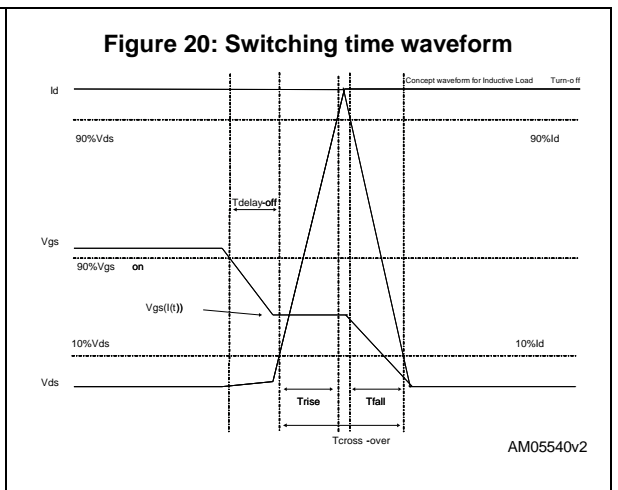
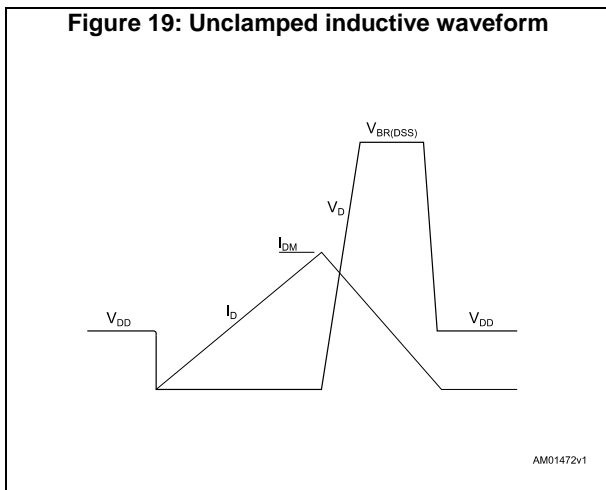
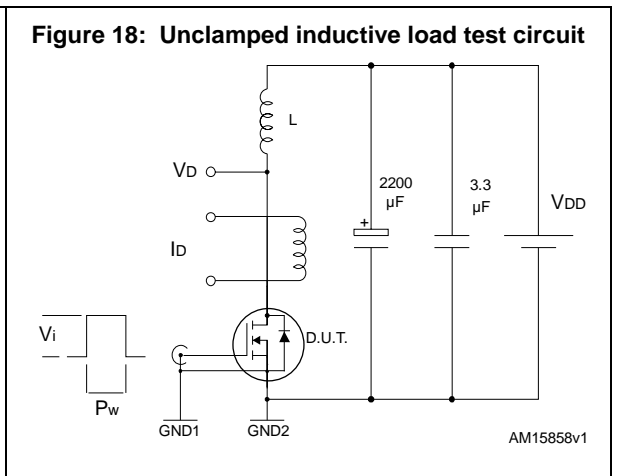
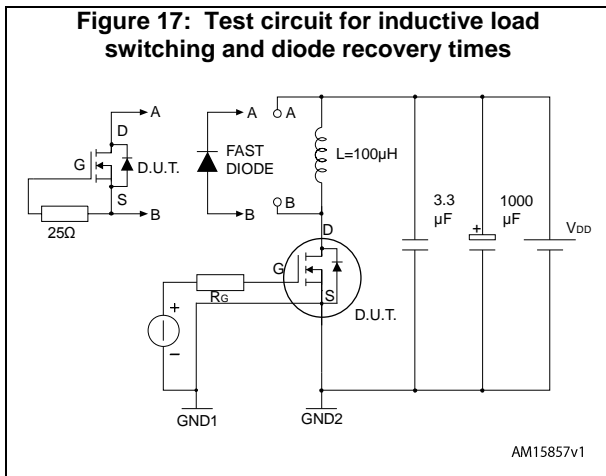
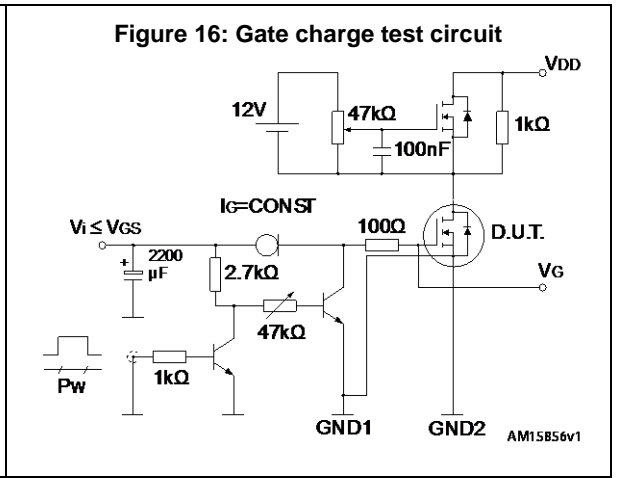
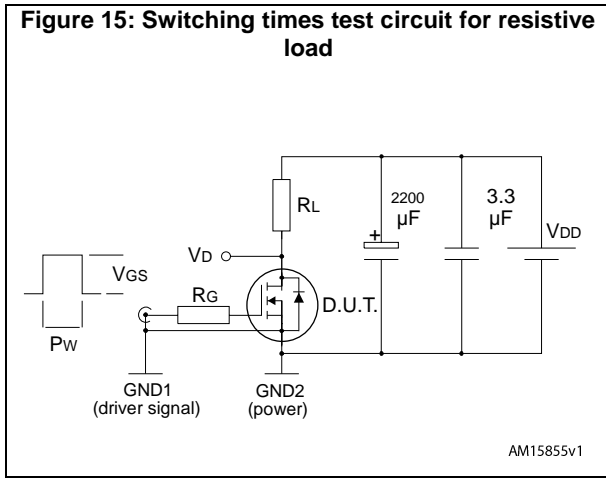


**Notes:**

<sup>(1)</sup>E<sub>on</sub> including reverse recovery of a SiC diode



### 3 Test circuits



## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 PowerFLAT 8x8 HV package information

Figure 21: PowerFLAT™ 8x8 HV package outline

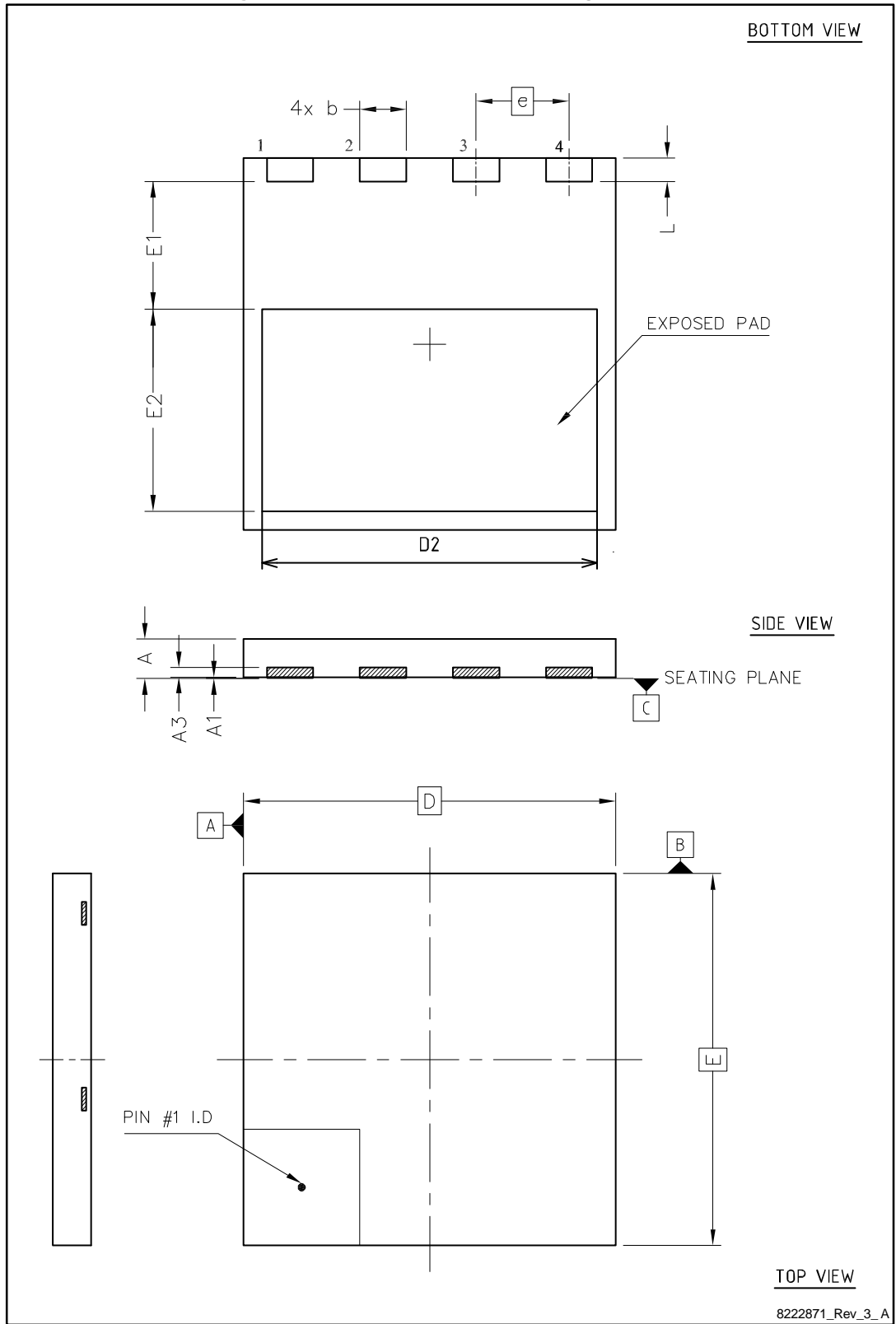
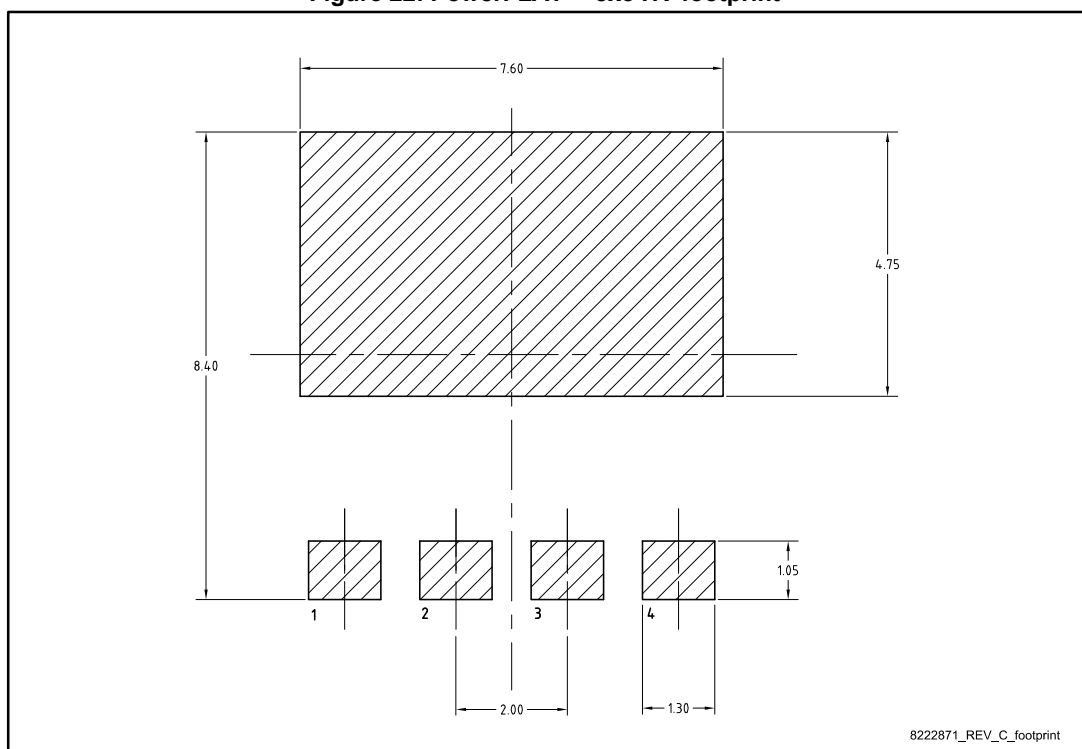


Table 9: PowerFLAT™ 8x8 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.75	0.85	0.95
A1	0.00		0.05
A3	0.10	0.20	0.30
b	0.90	1.00	1.10
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	7.10	7.20	7.30
E1	2.65	2.75	2.85
E2	4.25	4.35	4.45
e		2.00	
L	0.40	0.50	0.60

Figure 22: PowerFLAT™ 8x8 HV footprint



All dimensions are in millimeters.

### 4.2 PowerFLAT 8x8 HV packing information

Figure 23: PowerFLAT™ 8x8 HV tape

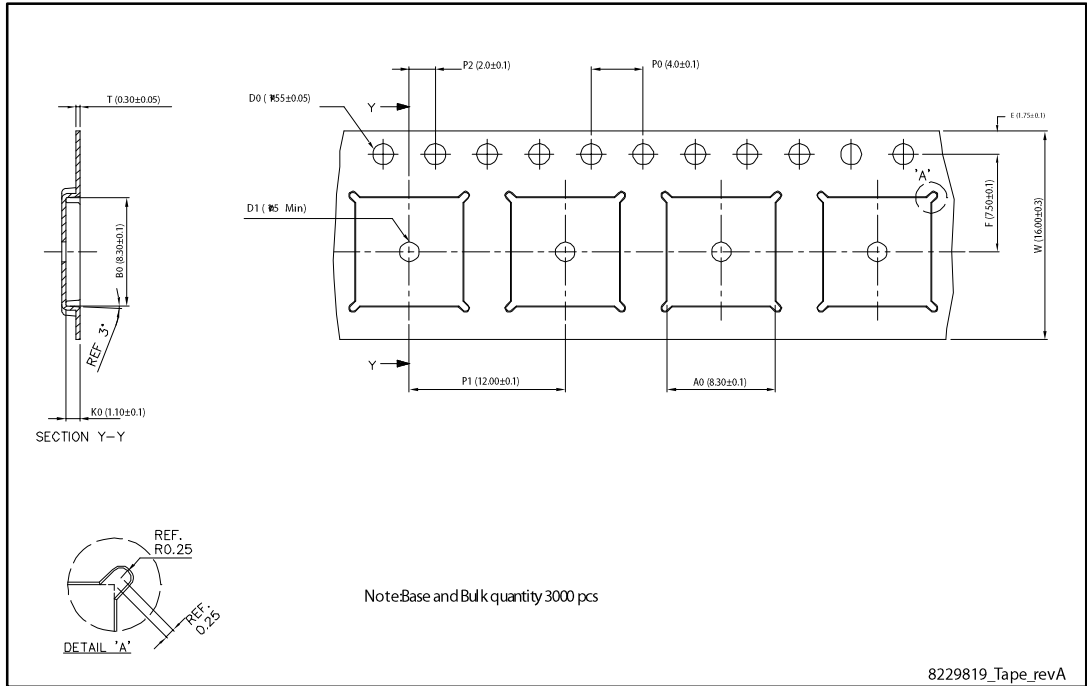


Figure 24: PowerFLAT™ 8x8 HV package orientation in carrier tape

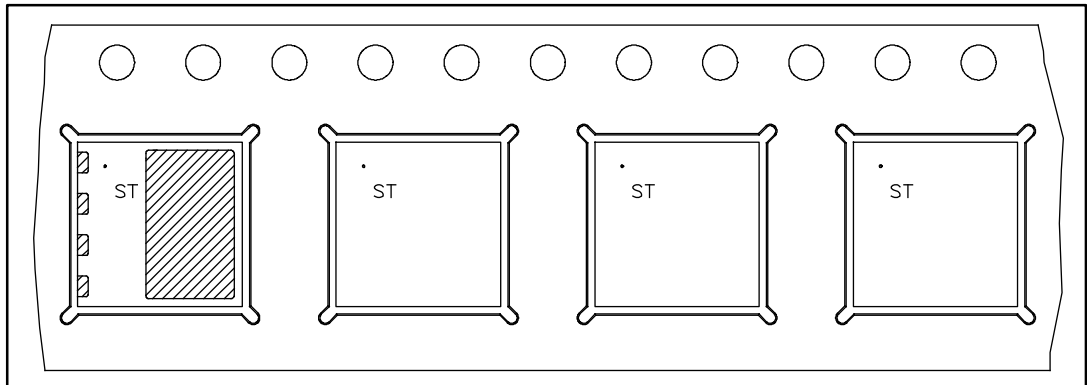
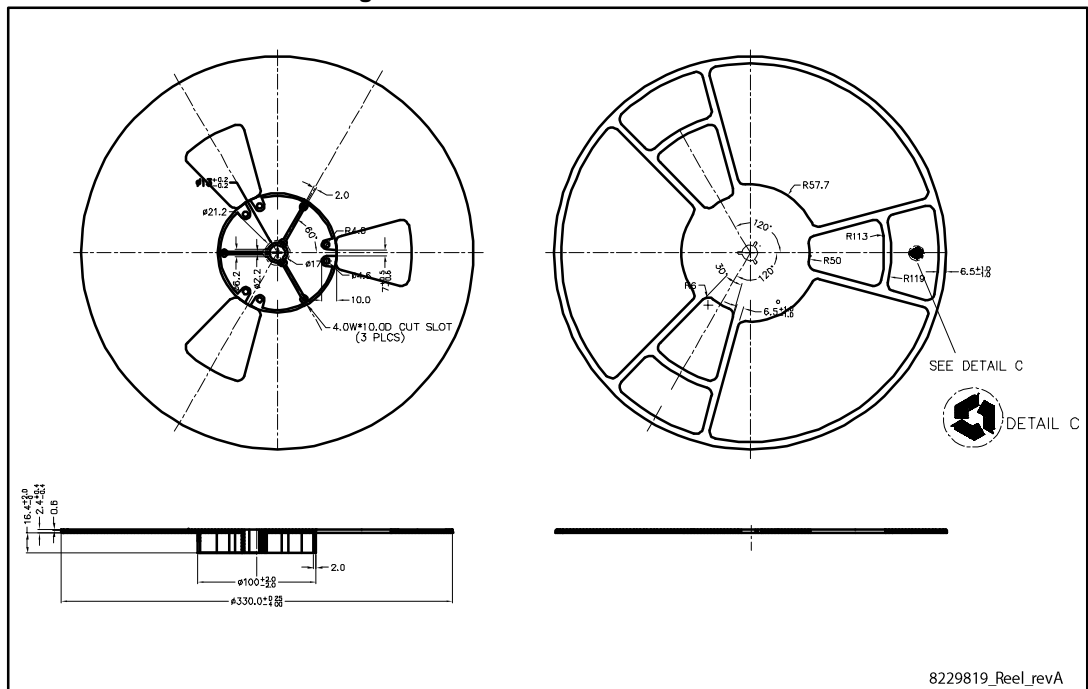


Figure 25: PowerFLAT™ 8x8 HV reel



## 5 Revision history

**Table 10: Document revision history**

Date	Revision	Changes
20-Sep-2012	1	First release.
09-Oct-2015	2	Text and formatting changes throughout document Datasheet status changed from preliminary to production data In section Electrical ratings: - added table Avalanche characteristics In section Electrical characteristics: - renamed table Static (was On /off states) Updated section Test circuits Updated and renamed section Package information (was Package mechanical data)

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