Middle Power Class-D Speaker Amplifier Series

20W+20W
Class D Speaker Amplifier for Digital Input

BD28620MUV

General Description

BD28620MUV is a Class D Speaker Amplifier designed for Flat-panel TVs in particular for space-saving and low-power consumption. This IC delivers an output power of 20W+20W. This IC employs state-of-the-art Bipolar, CMOS, and DMOS (BCD) process technology. With this technology, the IC can achieve high efficiency. In addition, the IC is packaged in a compact back-surface heat-sink type power package to achieve low power consumption and low heat generation and to eliminate need for external heat-sink. With this package, total output power is only 34W as compared to 40W total output power of package with external heat-sink This product satisfies all needs for drastic downsizing, low-profile structures and powerful high quality playback of sound systems.

Features

- 1 Digital Audio Interface
  I^2S format
  SDATA: 16 / 20 / 24bit
  LRCLK (f_S): 32kHz / 44.1kHz / 48kHz
  BCLK: 64f_S (fixed)
  MCLK: 256f_S / 512f_S Automatic Identification)
- Low supply current at RESET mode.
- Output Feedback Circuitry which prevents decrease of sound quality caused by change of power supply voltage, achieves low noise and low distortion, eliminates need for large electrolytic-capacitors
- Variable Gain (17dB / 20dB / 26dB)
- Wide power supply voltage range (8.5V to 24V)
- High efficiency, low heat
- Pop noise prevention at power supply ON/OFF
- Soft Muting Technology
- High reliability design by built-in protection circuits
  - High temperature protection
  - Under voltage protection
  - Output short protection
  - Output DC voltage protection
  - Clock stop protection (MCLK, BCLK, LRCLK)
- Small package (VQFN024V4040)

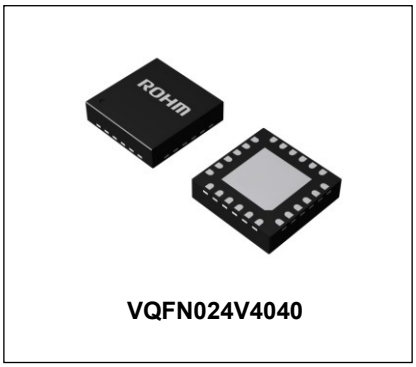
Applications

- Flat Panel TVs (LCD, Plasma)
- Home Audio (Sound Bar)
- Amusement Equipment
- Electronic Music Equipment
- Desktop PC, etc.

Key Specifications

- Supply Voltage: 8.5V to 24V
- Speaker Output Power: 17W+17W (Typ)
  (V_{CC}=18V, R_L=8Ω, Power Limit=OFF)
- Total Harmonic Distortion: 0.08% (Typ) @P_O=1W
  (V_{CC}=12V, R_L=8Ω, Power Limit=10W)
- Crosstalk: 90dB (Typ)
- PSRR: 60dB (Typ)
- Output Noise Voltage: 150μV_{rms} (Typ)
- Standby Current: 33μA (Typ)
- Operating Temperature Range: -25°C to +85°C

Package	W(Typ) x D(Typ) x H(Max)
VQFN024V4040	4.00mm x 4.00mm x 1.00mm



VQFN024V4040

Typical Application Circuit

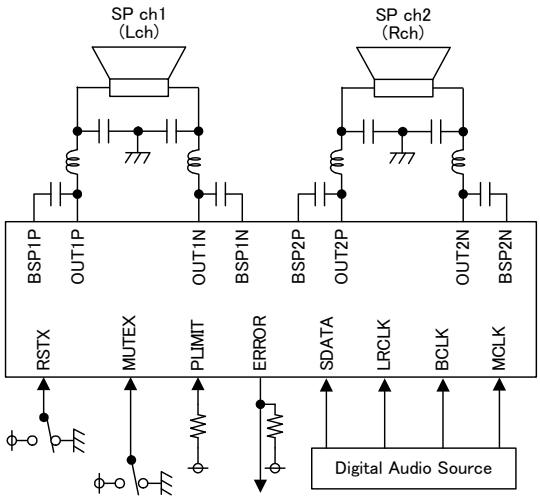


Figure 1. Typical Application Circuit

Pin Configuration

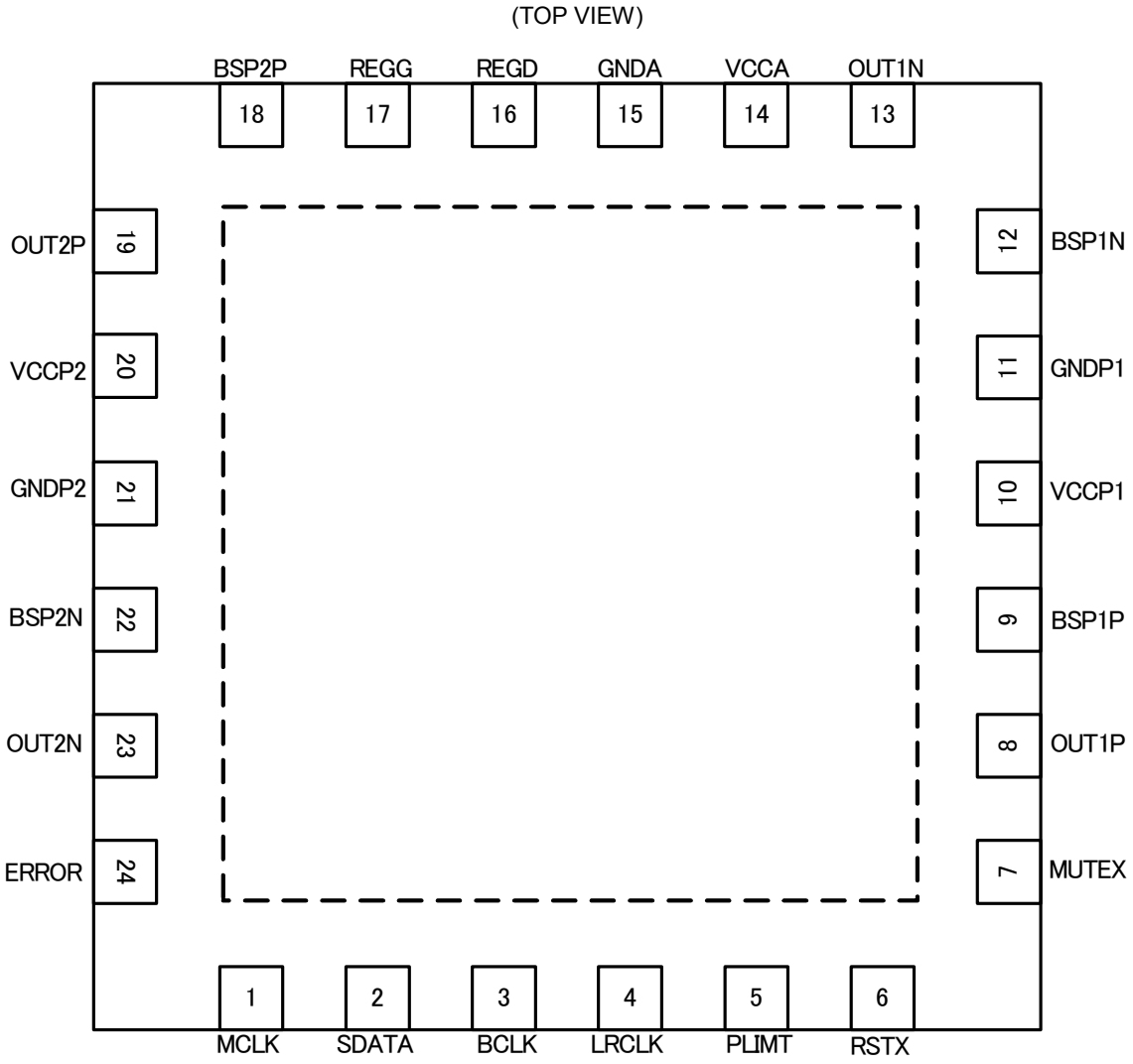
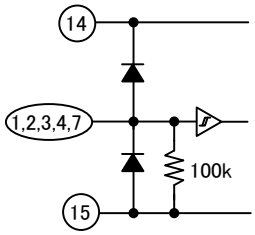
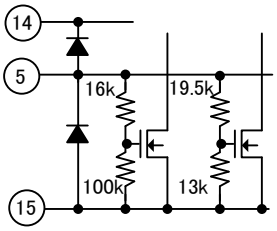
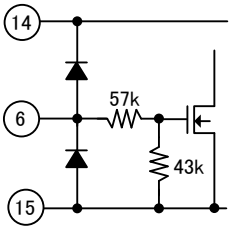
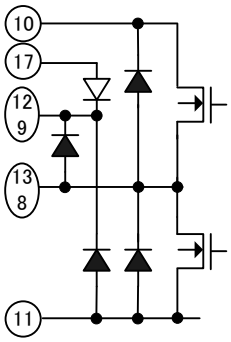
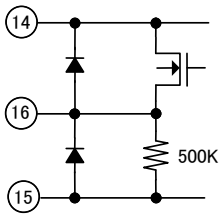
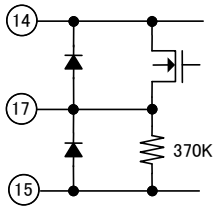
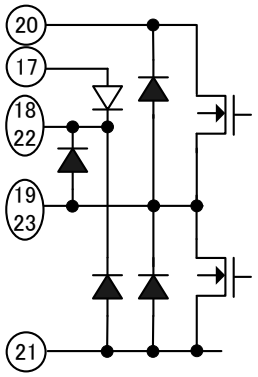
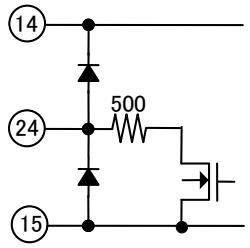


Figure 2. Pin Configuration

Pin Descriptions, I/O Equivalent Circuits (Provided pin voltages are typical values)

Pin No.	Pin Name	Pin Voltage	Pin Descriptions	Internal Equivalent Circuit
1 2 3 4	MCLK SDATA BCLK LRCLK	0V	Digital sound signal input pin	
7	MUTEX		Speaker output mute control pin H: Mute OFF L: Mute ON	
5	PLIMT	0V	Gain setting pin	
6	RSTX	0V	Reset pin H: Reset OFF L: Reset ON	
8	OUT1P	V_{CC} to 0V	Output pin of Ch1 positive PWM signal Please connect to output LPF. *If this pin is shorted to GND, the IC may be broken.	
9	BSP1P	-	Boot-strap pin of Ch1 positive PWM signal Please connect a capacitor.	
10	VCCP1	-	Power supply pin for Ch1 PWM signal Please connect a capacitor.	
11	GNP1	0V	GND pin for Ch1 PWM signal	
12	BSP1N	-	Boot-strap pin of Ch1 negative PWM signal Please connect a capacitor.	
13	OUT1N	V_{CC} to 0V	Output pin of Ch1 negative PWM signal Please connect to output LPF. *If this pin is shorted to GND, the IC may be broken.	
14	VCCA	V_{CC}	Power supply pin for Analog signal Please connect a capacitor.	–
15	GNDA	0V	GND pin for Analog signal	–
16	REGD	5.0V	Internal power supply pin for Digital circuit Please connect a capacitor. *The REGD terminal of BD28620MUV should not be used as external supply. Therefore, don't connect anything except for the capacitor for stabilization.	

Pin Descriptions, I/O Equivalent Circuits – continued (Provided pin voltages are typical values)

Pin No.	Pin Name	Pin Voltage	Pint Descriptions	Internal Equivalent Circuit
17	REGG	5.7V	Internal power supply pin for Gate driver Please connect a capacitor. *The REGG terminal of BD28620MUV should not be used as external supply. Therefore, don't connect anything except for the capacitor for stabilization.	
18	BSP2P	-	Boot-strap pin of Ch2 positive PWM signal Please connect a capacitor.	
19	OUT2P	V_{CC} to 0V	Output pin of Ch2 positive PWM signal Please connect to output LPF. *If this pin is shorted to GND, the IC may be broken.	
20	VCCP2	V_{CC}	Power supply pin for Ch2 PWM signal Please connect a capacitor.	
21	GNDP2	0V	GND pin for Ch2 PWM signal	
22	BSP2N	-	Boot-strap pin of Ch2 negative PWM signal Please connect a capacitor.	
23	OUT2N	V_{CC} to 0V	Output pin of Ch2 negative PWM signal Please connect to output LPF. *If this pin is shorted to GND, the IC may be broken.	
24	ERROR	-	Error flag pin Please connect pull-up resistor. H: Normal L: Error *An error flag is outputted when Output Short Protection, DC Voltage Protection in the speaker, and High Temperature Protection are operated. This flag shows IC condition during operation.	

The numerical value of internal equivalent circuit is typical value, not guaranteed value.

Block Diagram

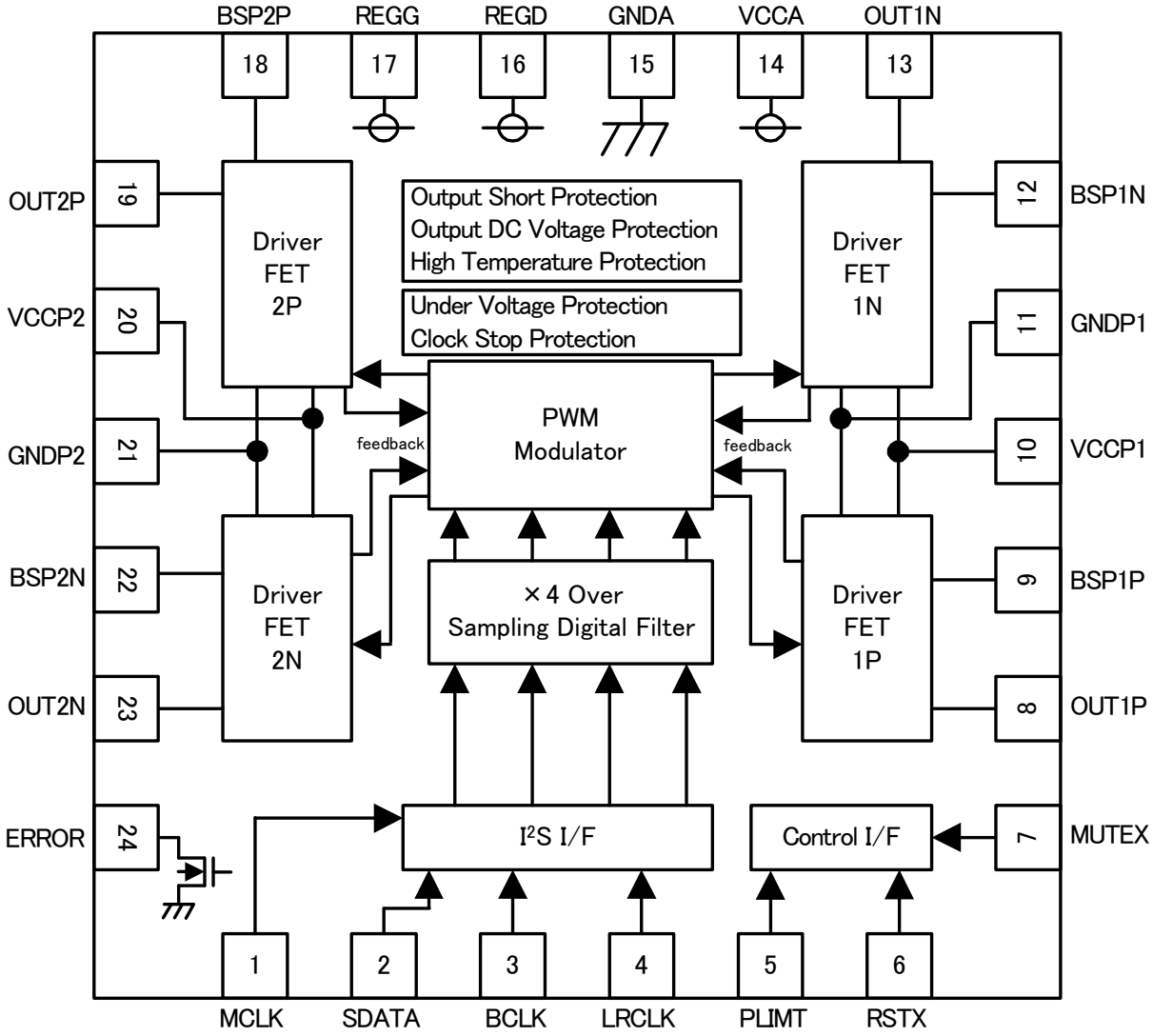


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Limit	Unit	Conditions
Supply Voltage (Note 1) (Note 2)	V_{CCMAX}	-0.3 to 29	V	Pin10, 14, 20
Power Dissipation	Pd	2.21 (Note 3)	W	
		3.56 (Note 4)		
Input Voltage (Note 1)	V_{IN}	-0.3 to 3.7	V	Pin1 to 7
Terminal Voltage 1 (Note 1)	V_{PIN1}	-0.3 to 7	V	Pin16, 17
Terminal Voltage 2 (Note 1) (Note 5)	V_{PIN2}	-0.3 to V_{CC}	V	Pin8, 13, 19, 23
Terminal Voltage 3 (Note 1)	V_{PIN3}	-0.3 to V_{CC}+7	V	Pin9, 12, 18, 22
Open-drain Terminal Voltage (Note 1)	V_{ERR}	-0.3 to V_{CCMAX}	V	Pin24
Operating Temperature Range	Topr	-25 to +85	°C	
Storage Temperature Range	Tstg	-55 to +150	°C	
Maximum Junction Temperature	Tjmax	+150	°C	

(Note 1) Voltage that can be applied with reference to GND (Pin11, 15, 21).
(Note 2) Pd and Tjmax=150°C must not be exceeded.
(Note 3) 74.2mm×74.2mm×1.6mm, FR4, 4-layer glass epoxy board
(Top and bottom layer back copper foil size: 10.29mm^2, 2nd and 3rd layer back copper foil size: 5505mm^2)
Derate by 17.7mW/°C when operating above Ta=25°C. The board is provided with thermal via.
(Note 4) 74.2mm×74.2mm×1.6mm, FR4, 4-layer glass epoxy board
(Top and bottom layer back copper foil size: 5505mm^2)
Derate by 28.5mW/°C when operating above Ta=25°C. The board is provided with thermal via.
(Note 5) The chip should be used within AC peak limits at all conditions. Overshoot should be ≦29V with reference to GND.
Undershoot should be ≦10nsec and ≦29V with reference to V_{CC}. (Please refer to the following figure.)

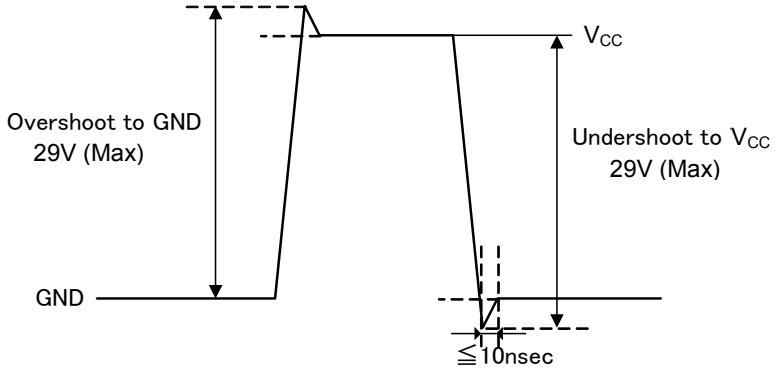


Figure 4.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions

Parameter	Symbol	Limit	Unit	Conditions
Supply Voltage (Note 1) (Note 2)	V_{CC}	8.5 to 24	V	Pin10, 14, 20
Minimum Load Impedance (Note 6)	R_L	6.4	Ω	21V < V_{CC} ≤ 24V
		4.8		14V < V_{CC} ≤ 21V
		3.6		V_{CC} ≤14V

(Note 6) Pd should not be exceeded.

Electrical Characteristics

(Unless otherwise specified, Ta=25°C, V_{CC}=18V, f=1kHz, R_L=8Ω, RSTX=3.3V, MUTEX=3.3V, PLIMT= Pull up(27kΩ), f_S=48kHz, MCLK=256f_S, Output LC filter: L=10μH, C=0.68μF, Snubber circuit: C=680pF, R=5.6Ω)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Total Circuit						
Circuit Current (Reset Mode)	I_{CC1}	-	33	200	μA	No load, RSTX=0V, MUTEX=0V
Circuit Current (Mute Mode)	I_{CC2}	-	15	25	mA	No load, RSTX=3.3V, MUTEX=0V
Circuit Current (Active Mode)	I_{CC3}	-	40	80	mA	No load, RSTX=3.3V, MUTEX=3.3V, Without Snubber circuit
Open-drain Terminal Low Level Voltage	V_{ERR}	-	-	0.8	V	I_O=0.5mA
Regulator Output Voltage 1	V_{REGG}	4.6	5.7	6.5	V	RSTX=3.3V, MUTEX=3.3V
Regulator Output Voltage 2	V_{REGD}	4.2	5.0	5.7	V	RSTX=3.3V, MUTEX=3.3V
High level Input Voltage	V_{IH}	2.2	-	3.3	V	Pin1 to 7
Low level Input Voltage	V_{IL}	0	-	0.8	V	Pin1 to 7
Input Current1 (Input Pull-down Terminal)	I_{IH}	27.5	33	42	μA	V_{IN} = 3.3V, Pin1 to 4, 6 to 7
Input Current2 (Input Pull-down Terminal)	I_{IH2}	90	120	160	μA	V_{IN} = 3.3V, Pin5
Speaker Parts						
Maximum Output Power 1(Note 7)	P_{O1}	-	15	-	W	V_{CC}=16V, THD+N=10%, PLIMT=H
Maximum Output Power 2(Note 7)	P_{O2}	10	12.5	-	W	V_{CC}=16V, THD+N<10%, PLIMT=Pull up(27kΩ)
Maximum Output Power 3(Note 7)	P_{O3}	5	6.3	-	W	V_{CC}=16V, THD+N<10%, PLIMT=L
Voltage Gain1(Note 7)	G_{V26}	25	26	27	dB	P_O=1W, PLIMT=H
Voltage Gain2(Note 7)	G_{V20}	19	20	21	dB	P_O=1W, PLIMT=Pull up(27kΩ)
Voltage Gain3(Note 7)	G_{V17}	16	17	18	dB	P_O=1W, PLIMT=L
Total Harmonic Distortion1(Note 7)	THD_1	-	0.08	-	%	V_{CC}=12V, Po=1W BW=20 to 20kHz (AES17) PLIMT=Pull up(27kΩ)
Crosstalk (Note 7)	CT	60	90	-	dB	P_O=1W, BW=IHF-A, PLIMT=Pull up(27kΩ)
PSRR (Note 7)	PSRR	-	60	-	dB	V_{ripple}=1V_{rms}, f=1kHz, PLIMT=Pull up(27kΩ)
Output Noise Voltage (Note 7)	V_{NO}	-	150	250	μV_{rms}	-∞dBFS, BW=IHF-A, PLIMT=Pull up(27kΩ)
PWM (Pulse Width Modulation) Frequency	f_{PWM}	-	512	-	kHz	f_S=32kHz
		-	705.6	-	kHz	f_S=44.1kHz
		-	768	-	kHz	f_S=48kHz

(Note 7) The rated values of items above indicate average performances of the device, which largely depend on circuit layouts, components, and power supplies. The reference values are those applicable to the device and components directly installed on a board specified by ROHM during testing.

Typical Performance Curves (1/11)

(Unless otherwise specified, Ta=25°C, V_{CC}=18V, f=1kHz, R_L=8Ω, RSTX=3.3V, MUTEX=3.3V, f_S=48kHz, MCLK=256f_S, PLIMIT=H, Snubber circuit: C=680pF, R=5.6Ω, ROHM 4-layer Board)

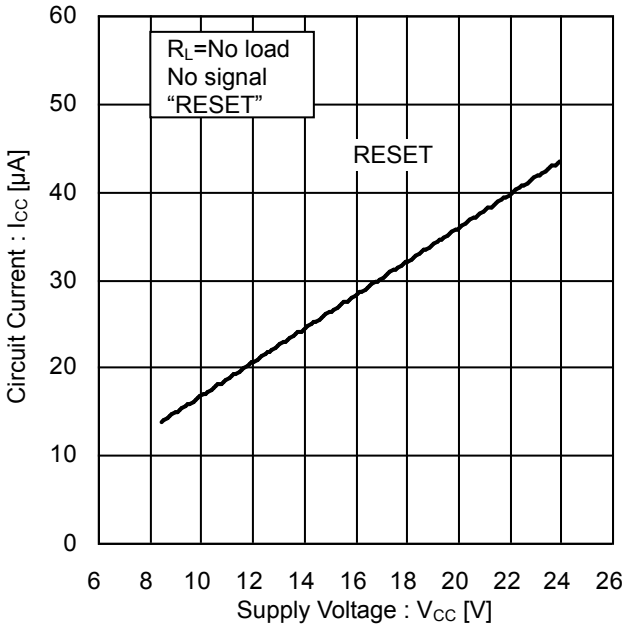


Figure 5. Circuit Current vs Supply Voltage (RESET)

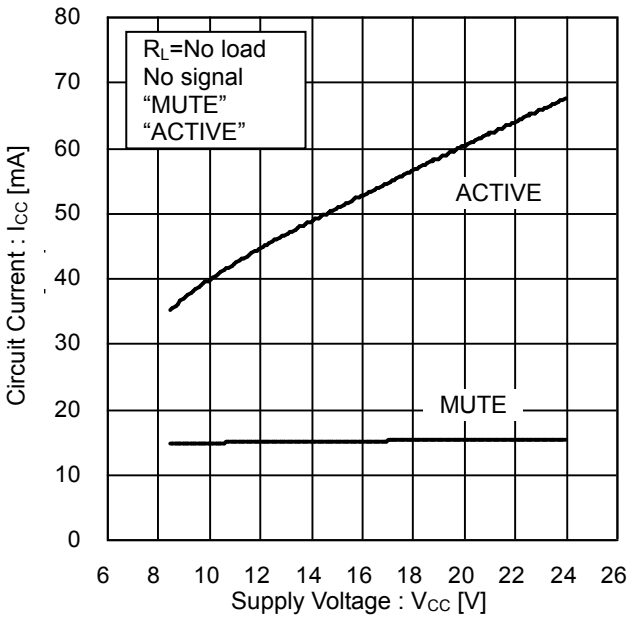


Figure 6. Circuit Current vs Supply Voltage (MUTE, ACTIVE)

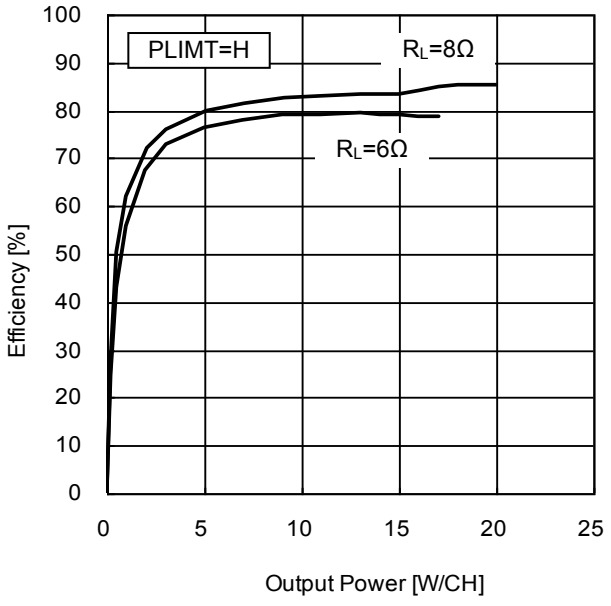


Figure 7. Efficiency vs Output Power (8Ω, 6Ω)

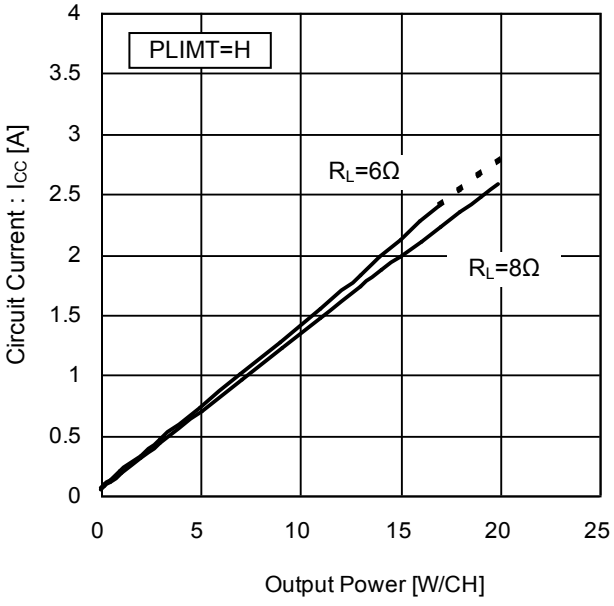


Figure 8. Circuit Current vs Output Power (8Ω, 6Ω)

※ Dotted line means power dissipation is exceeded.

Typical Performance Curves – continued (2/11)

(Unless otherwise specified, Ta=25°C, V_{CC}=18V, f=1kHz, R_L=8Ω, RSTX=3.3V, MUTEX=3.3V, f_S=48kHz, MCLK=256f_S, PLIMIT=Pull up(27kΩ), Snubber circuit: C=680pF, R=5.6Ω, ROHM 4-layer Board)

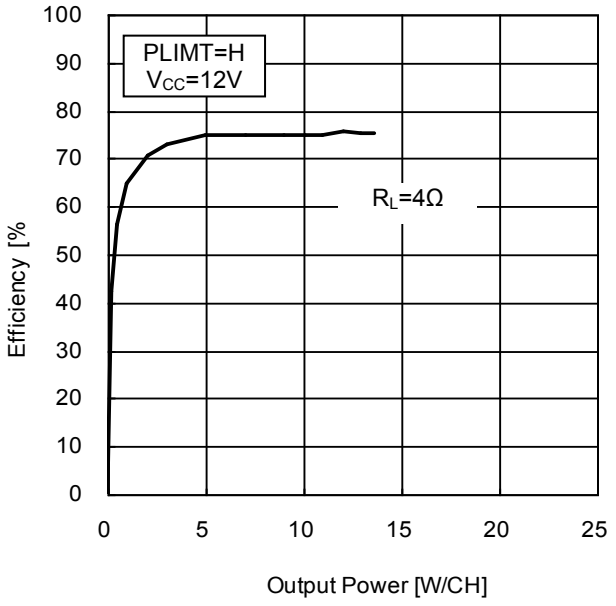


Figure 9. Efficiency vs Output Power (4Ω)

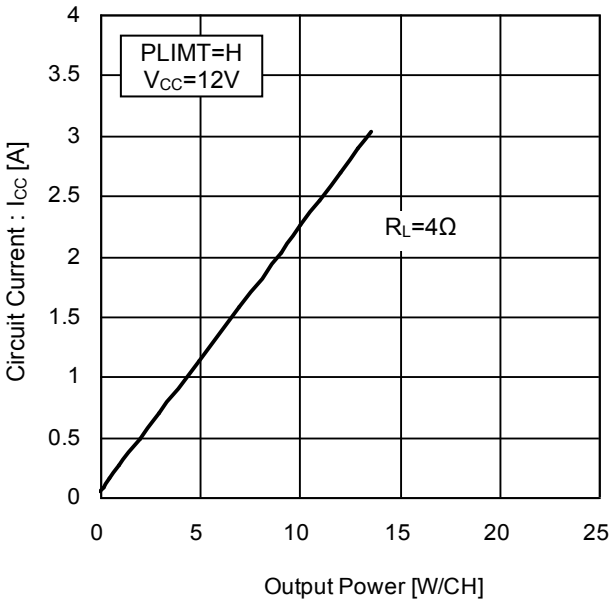


Figure 10. Circuit Current vs Output Power (4Ω)

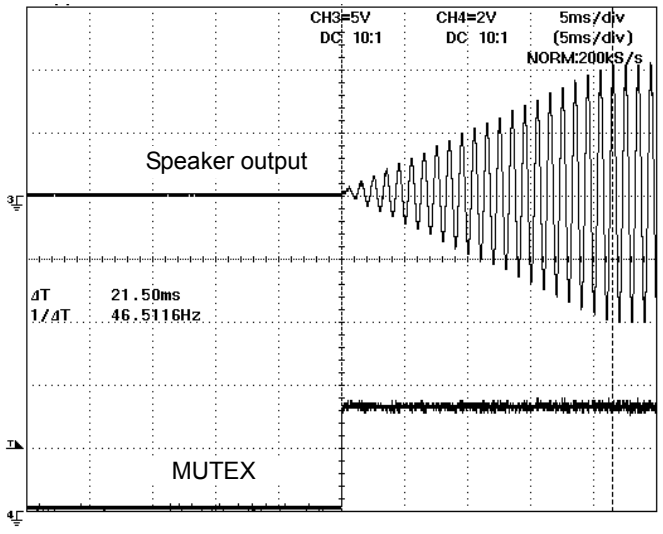


Figure 11. Waveform of Soft Start

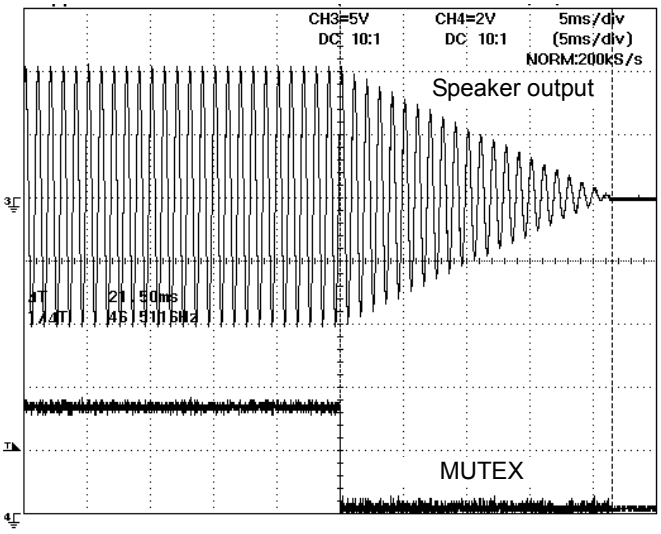


Figure 12. Waveform of Soft Mute

Typical Performance Curves - continued (3/11)

(Unless otherwise specified, Ta=25°C, V_{CC}=18V, f=1kHz, R_L=8Ω, RSTX=3.3V, MUTEX=3.3V, f_S=48kHz, MCLK=256f_S, PLIMIT=H, Snubber circuit: C=680pF, R=5.6Ω, ROHM 4-layer Board)

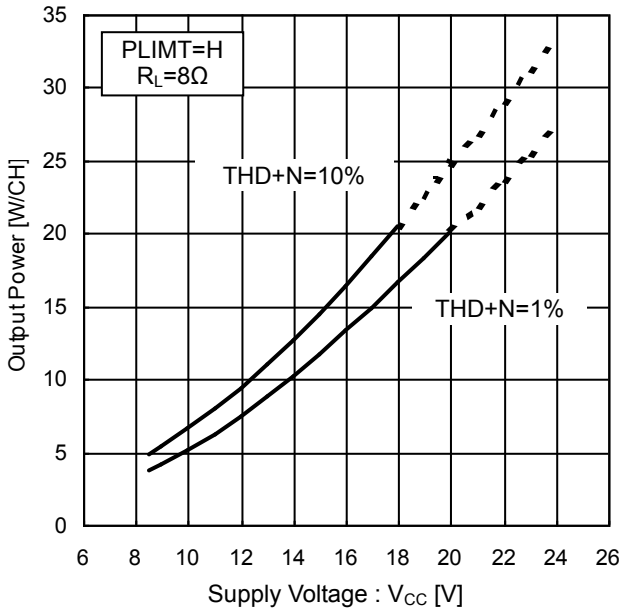


Figure 13. Output Power vs Supply Voltage (8Ω)

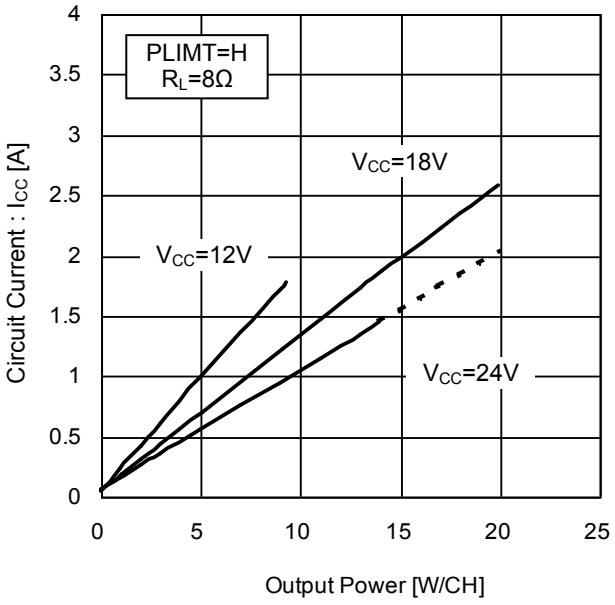


Figure 14. Circuit Current vs Output Power (8Ω)

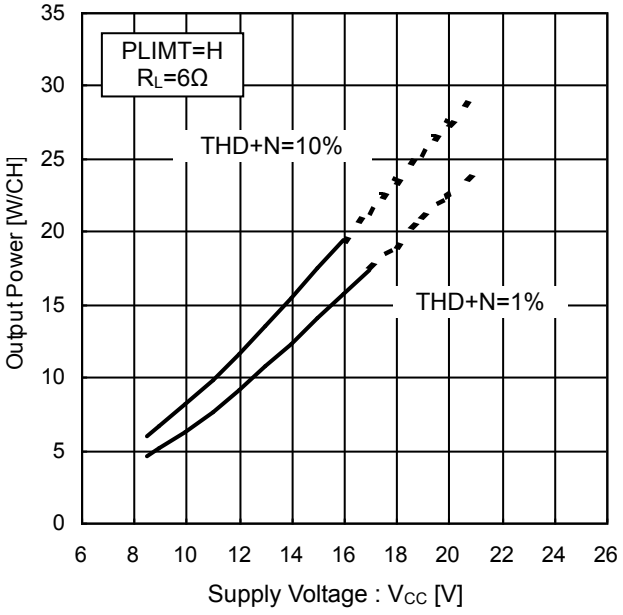


Figure 15. Output Power vs Supply Voltage (6Ω)

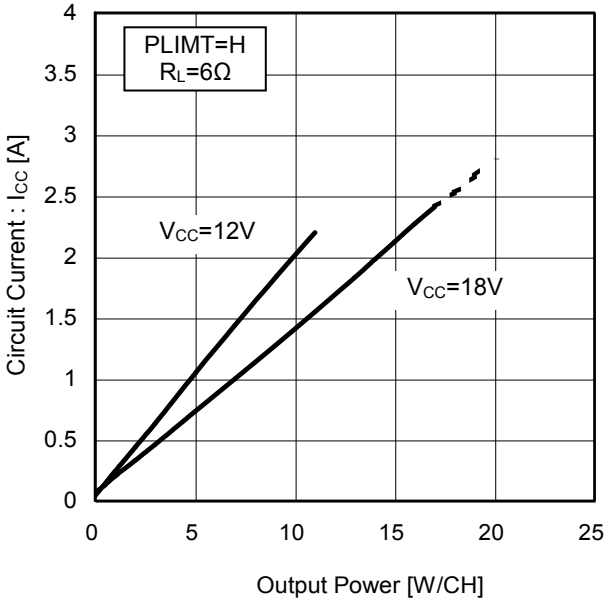


Figure 16. Circuit Current vs Output Power (6Ω)

※ Dotted line means power dissipation is exceeded.

Typical Performance Curves - continued (4/11)

(Unless otherwise specified, Ta=25°C, V_{CC}=18V, f=1kHz, R_L=8Ω, RSTX=3.3V, MUTEX=3.3V, f_S=48kHz, MCLK=256f_S, PLIMIT=Pull up(27kΩ), Snubber circuit: C=680pF, R=5.6Ω, ROHM 4-layer Board)

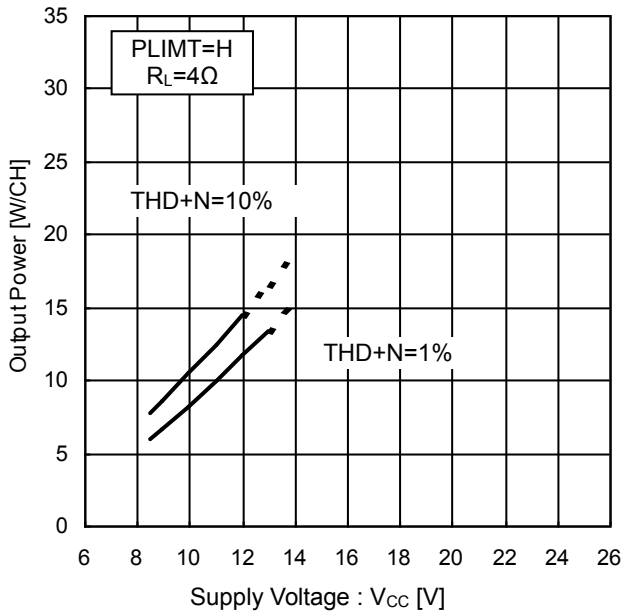


Figure 17. Output Power vs Supply Voltage (4Ω)

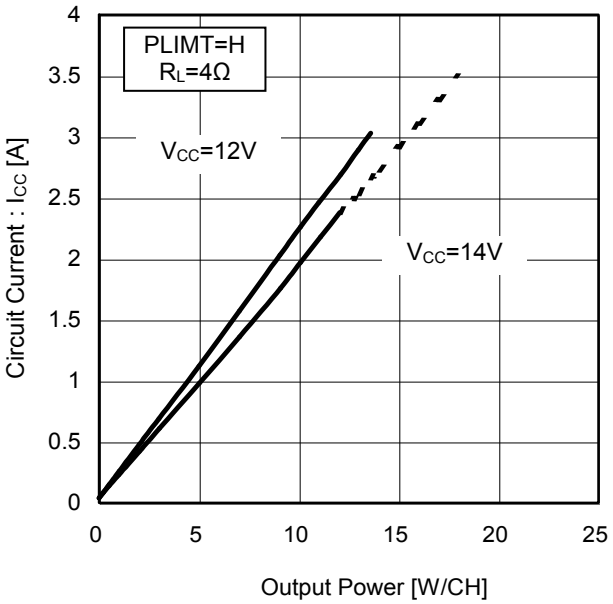


Figure 18. Circuit Current vs Output Power (4Ω)

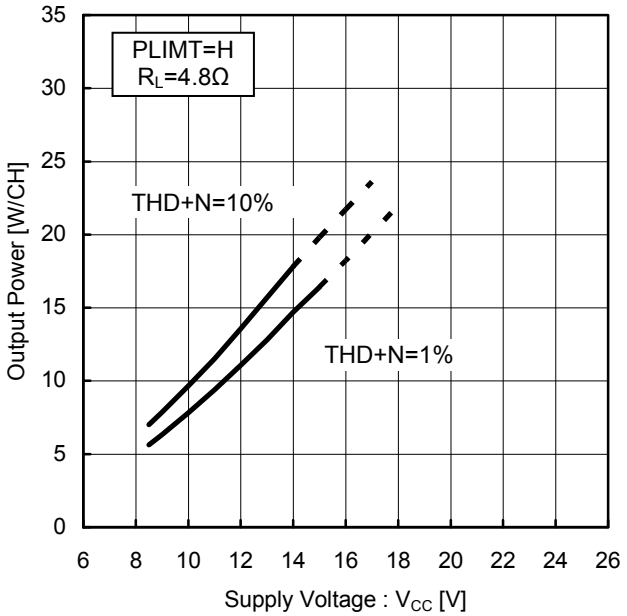


Figure 19. Output Power vs Supply Voltage (4.8Ω)

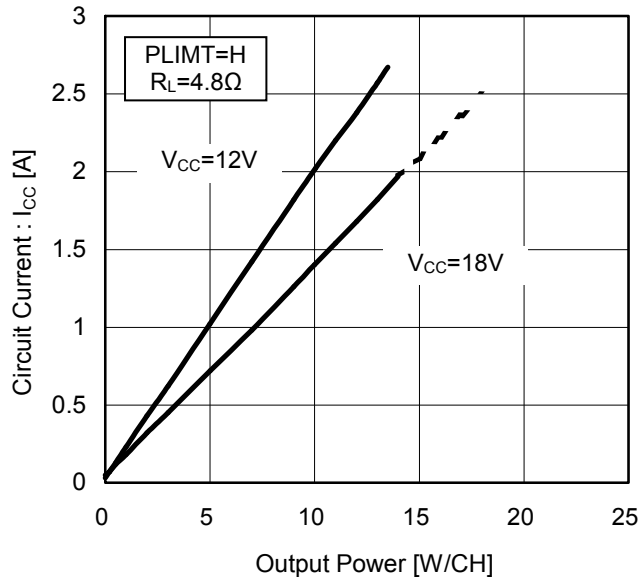


Figure 20. Circuit Current vs Output Power (4.8Ω)

※ Dotted line means power dissipation is exceeded.

Typical Performance Curves - continued (5/11)

(Unless otherwise specified, Ta=25°C, V_{CC}=18V, f=1kHz, R_L=8Ω, RSTX=3.3V, MUTEX=3.3V, f_S=48kHz, MCLK=256f_S, PLIMIT=Pull up(27kΩ), Snubber circuit: C=680pF, R=5.6Ω, ROHM 4-layer Board)

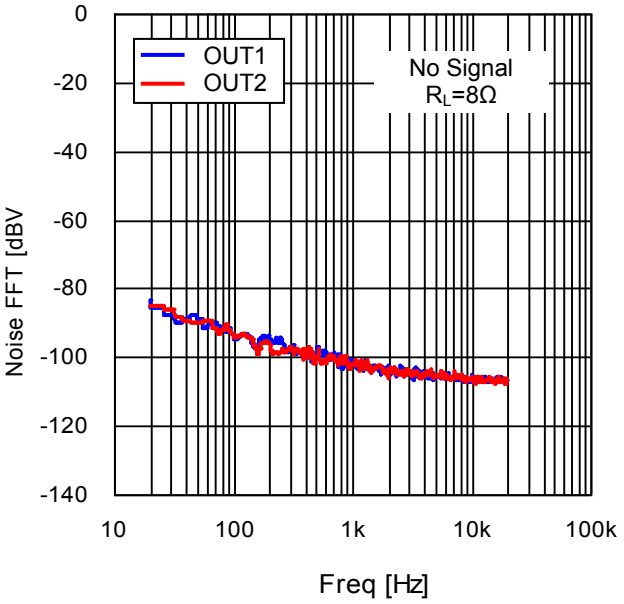


Figure 21. FFT of output noise voltage

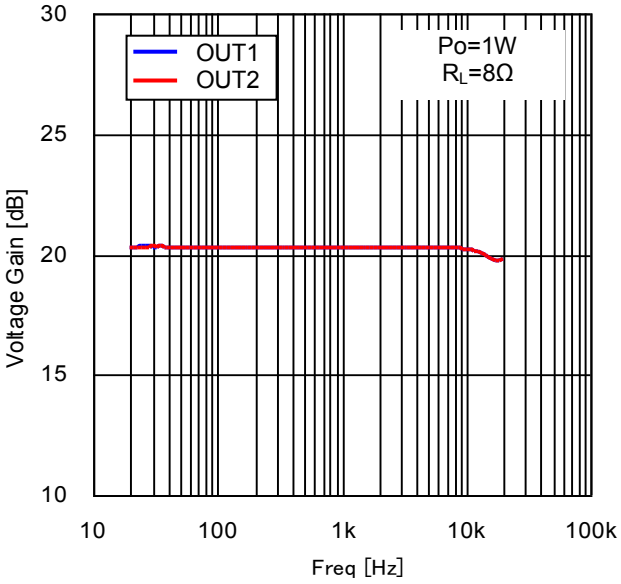


Figure 22. Voltage Gain vs Freq (8Ω)

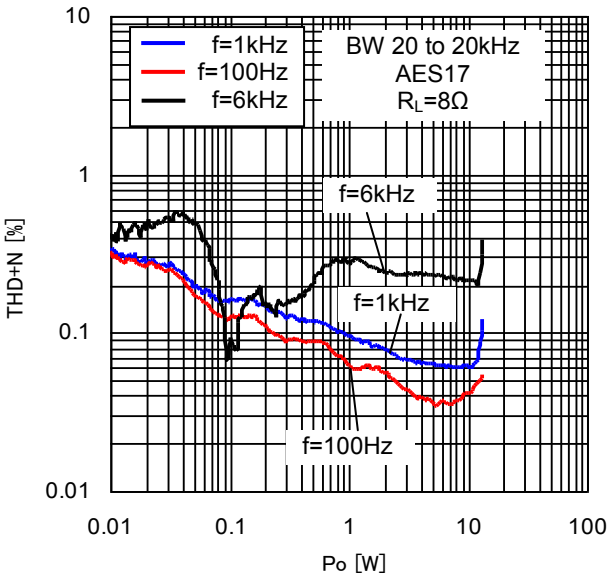


Figure 23. THD+N vs P_O (8Ω)

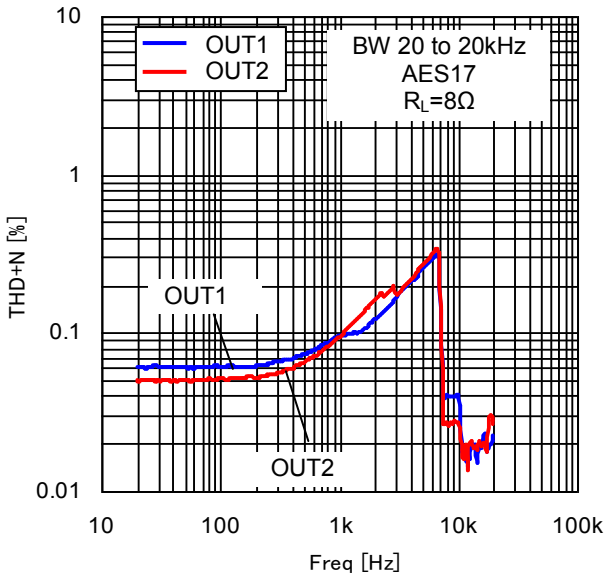


Figure 24. THD+N vs Freq (8Ω)

Typical Performance Curves - continued (6/11)

(Unless otherwise specified, Ta=25°C, V_{CC}=18V, f=1kHz, R_L= 8Ω/6Ω, RSTX=3.3V, MUTEX=3.3V, f_S=48kHz, MCLK=256f_S, PLIMIT=Pull up(27kΩ), Snubber circuit: C=680pF, R=5.6Ω, ROHM 4-layer Board)

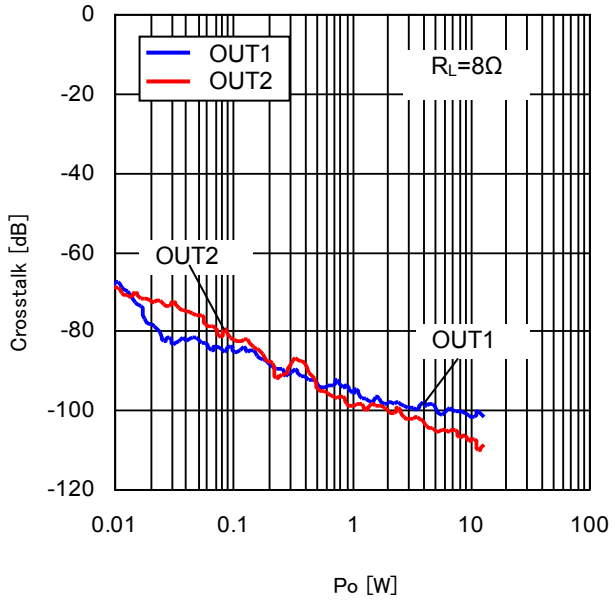


Figure 25. Crosstalk vs P_O (8Ω)

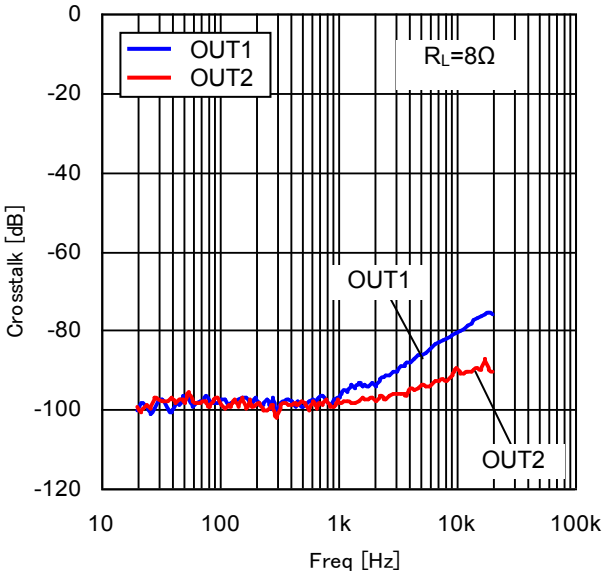


Figure 26. Crosstalk vs Freq (8Ω)

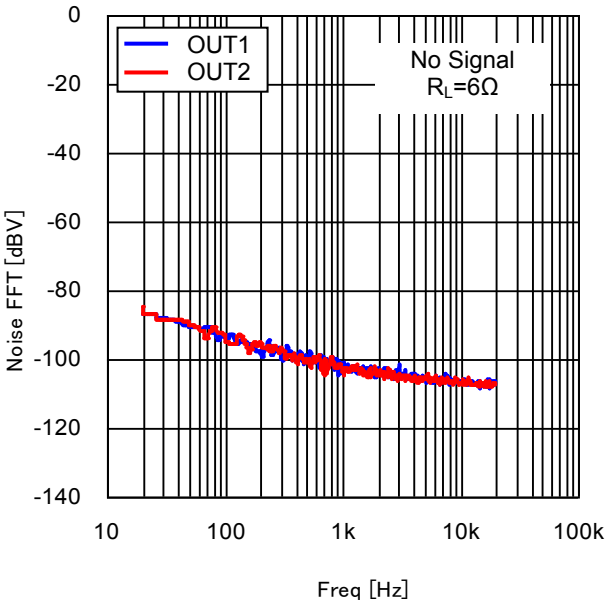


Figure 27. FFT of output noise voltage (6Ω)

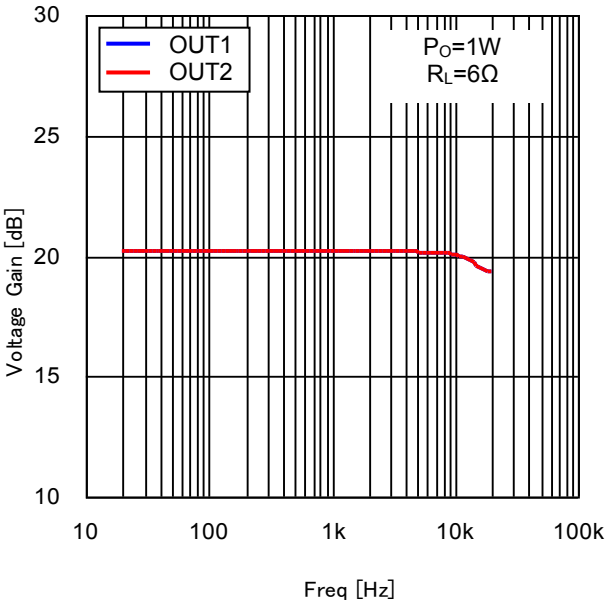


Figure 28. Voltage Gain vs Freq (6Ω)

Typical Performance Curves – continued (7/11)

(Unless otherwise specified, Ta=25°C, V_{CC}=18V, f=1kHz, R_L=6Ω, RSTX=3.3V, MUTEX=3.3V, f_S=48kHz, MCLK=256f_S, PLIMIT=Pull up(27kΩ), Snubber circuit: C=680pF, R=5.6Ω, ROHM 4-layer Board)

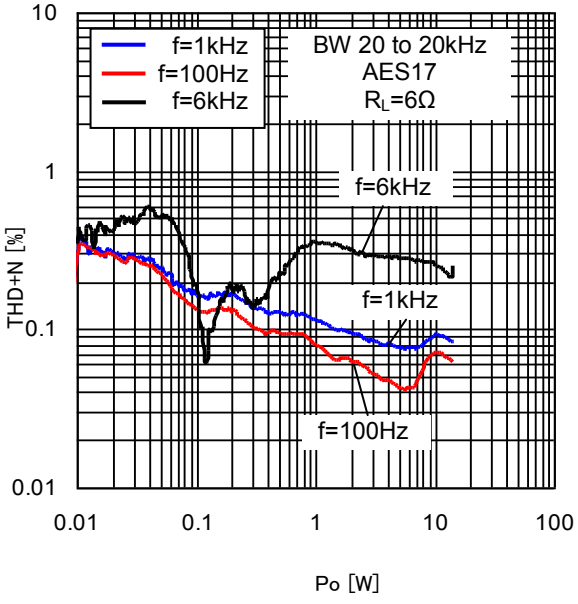


Figure 29. THD+N vs P_O (6Ω)

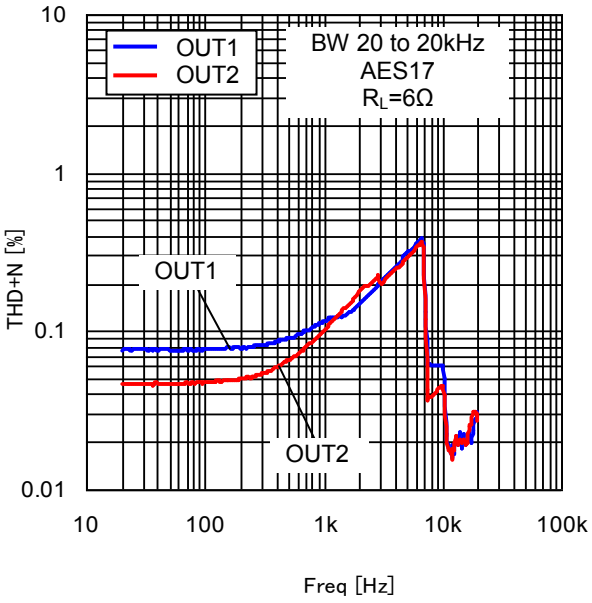


Figure 30. THD+N vs Freq (6Ω)

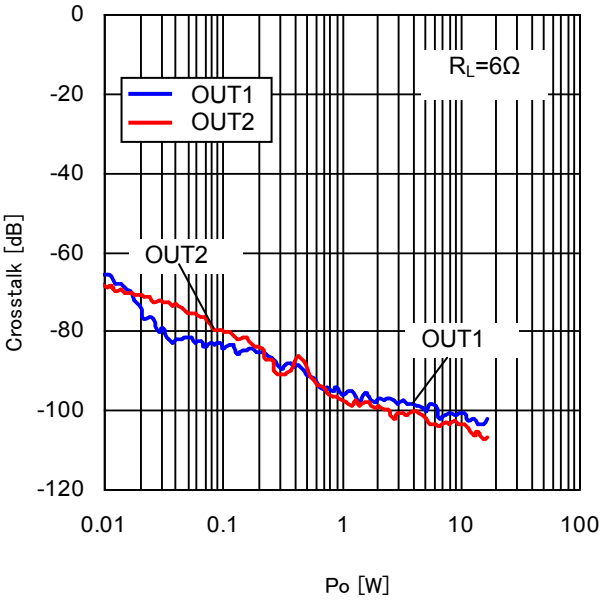


Figure 31. Crosstalk vs P_O (6Ω)

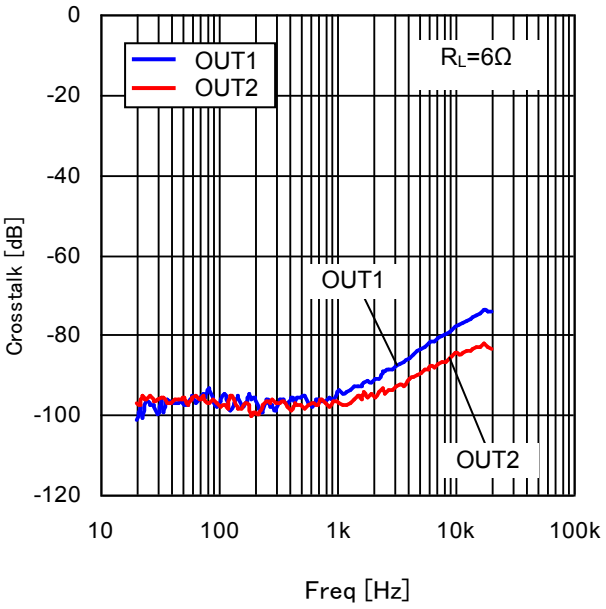


Figure 32. Crosstalk vs Freq (6Ω)

Typical Performance Curves – continued (8/11)

(Unless otherwise specified, Ta=25°C, V_{CC}=12V, f=1kHz, R_L=4Ω, RSTX=3.3V, MUTEX=3.3V, f_S=48kHz, MCLK=256f_S, PLIMIT=Pull up(27kΩ), Snubber circuit: C=680pF, R=5.6Ω, ROHM 4-layer Board)

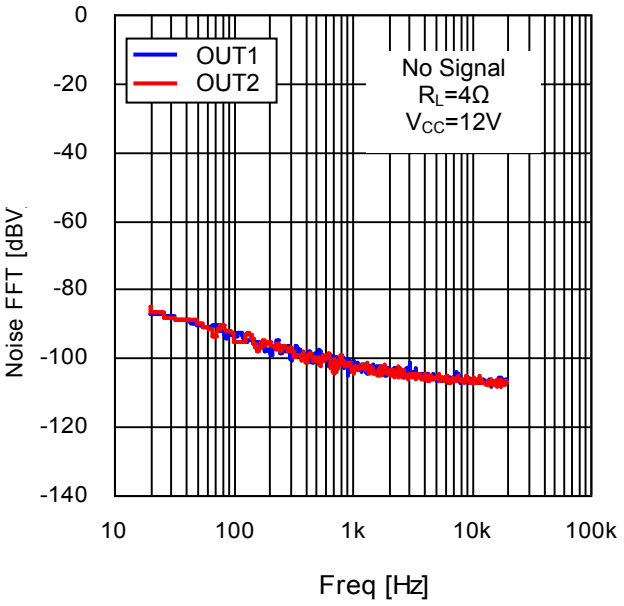


Figure 33. FFT of output noise voltage (4Ω)

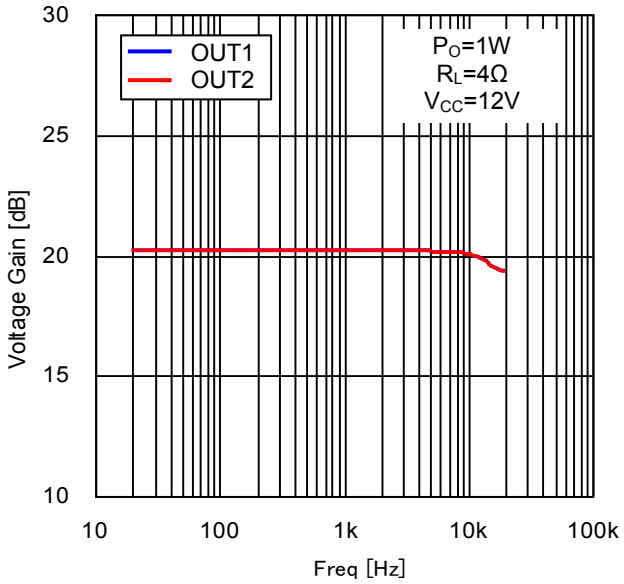


Figure 34. Voltage Gain vs Freq (4Ω)

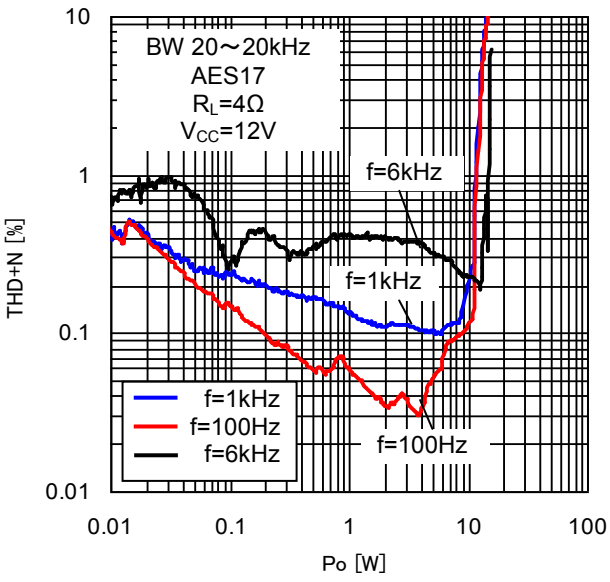


Figure 35. THD+N vs P_O (4Ω)

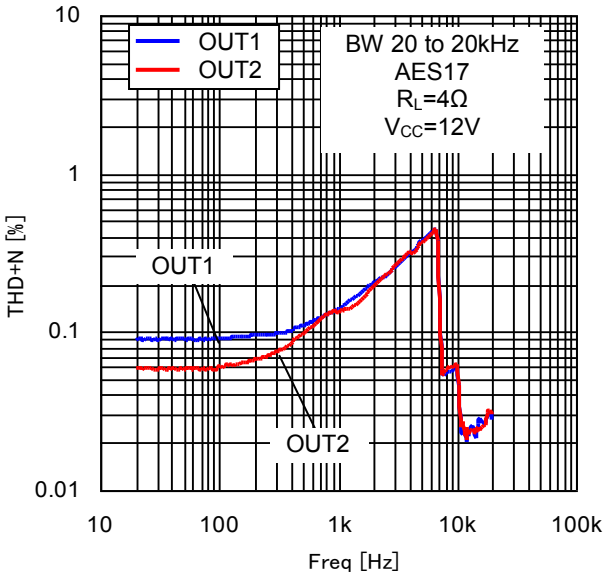


Figure 36. THD+N vs Freq (4Ω)

Typical Performance Curves - continued (9/11)

(Unless otherwise specified, Ta=25°C, V_{CC}=18V, f=1kHz, R_L= 4Ω/4.8Ω, RSTX=3.3V, MUTEX=3.3V, f_S=48kHz, MCLK=256f_S, PLIMIT=Pull up(27kΩ), Snubber circuit: C=680pF, R=5.6Ω, ROHM 4-layer Board)

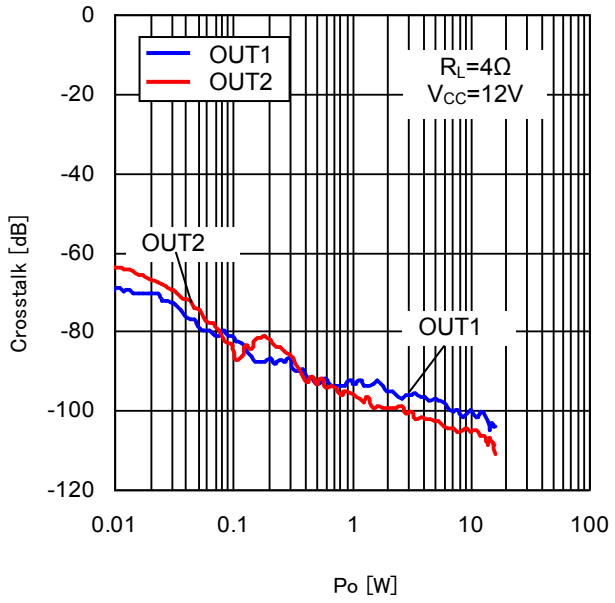


Figure 37. Crosstalk vs P_O (4Ω)

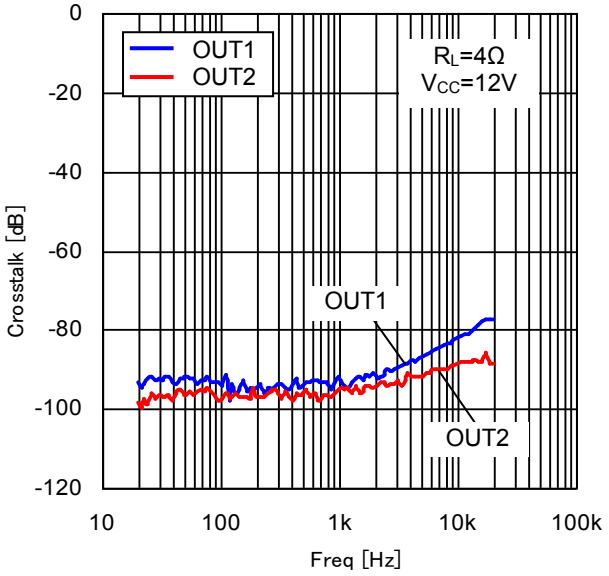


Figure 38. Crosstalk vs Freq (4Ω)

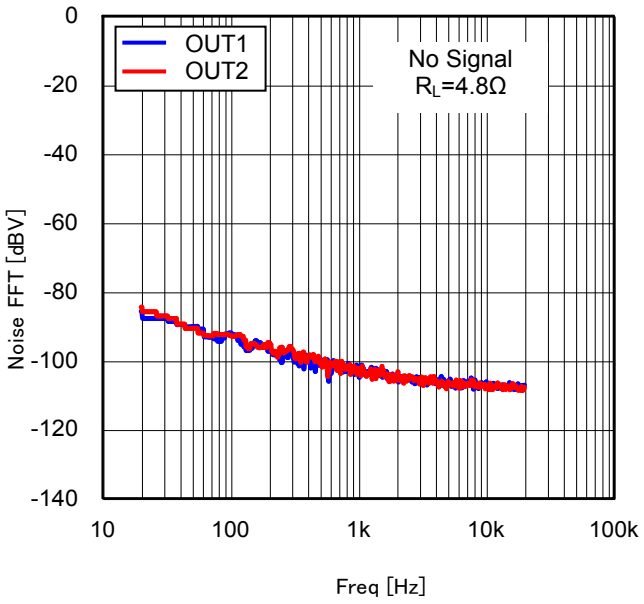


Figure 39. FFT of output noise voltage (4.8Ω)

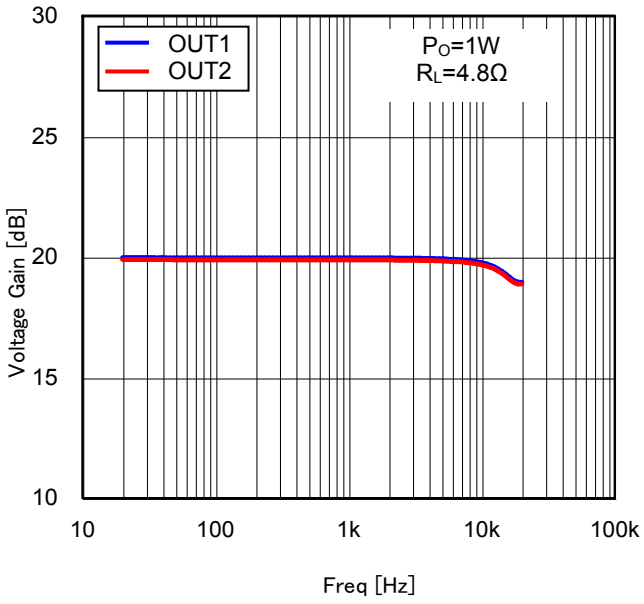


Figure 40. Voltage Gain vs Freq (4.8Ω)

Typical Performance Curves – continued (10/11)

(Unless otherwise specified, Ta=25°C, V_{CC}=18V, f=1kHz, R_L=4.8Ω, RSTX=3.3V, MUTEX=3.3V, f_S=48kHz, MCLK=256f_S, PLIMIT=Pull up(27kΩ), Snubber circuit: C=680pF, R=5.6Ω, ROHM 4-layer Board)

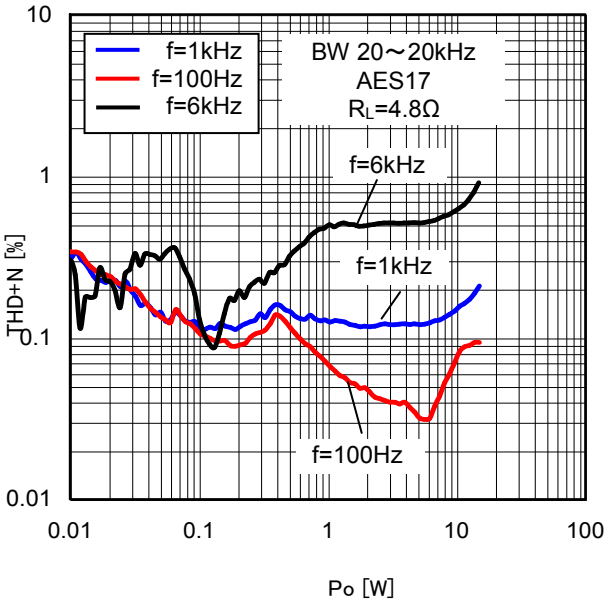


Figure 41. THD+N vs P_O (4.8Ω)

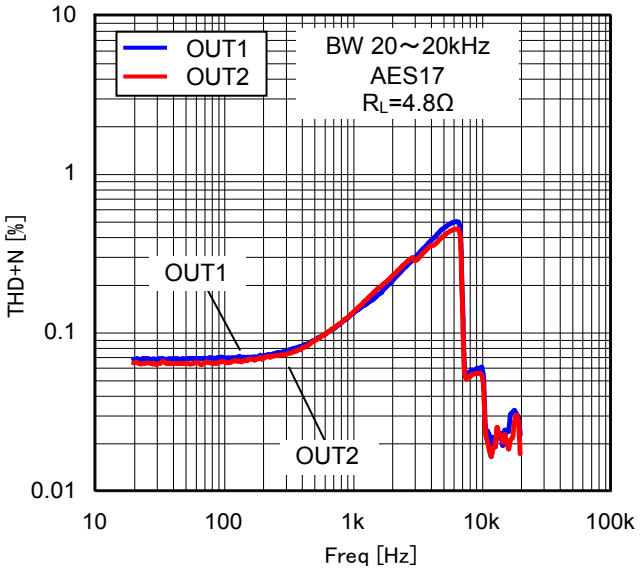


Figure 42. THD+N vs Freq (4.8Ω)

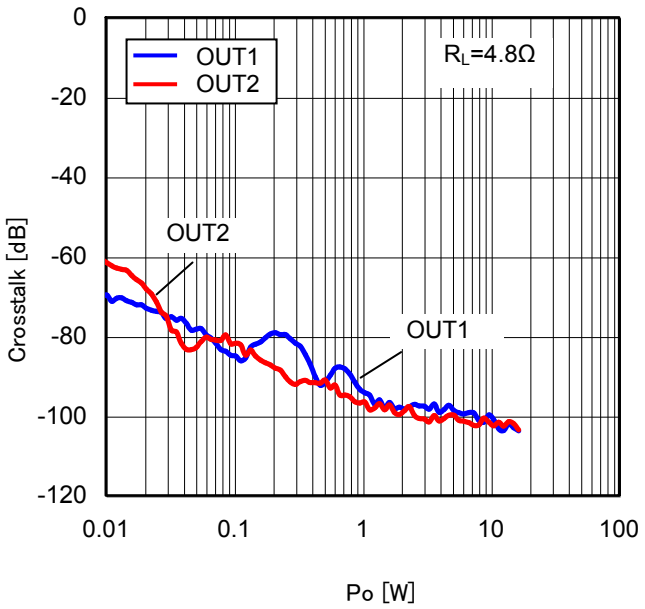


Figure 43. Crosstalk vs P_O (4.8Ω)

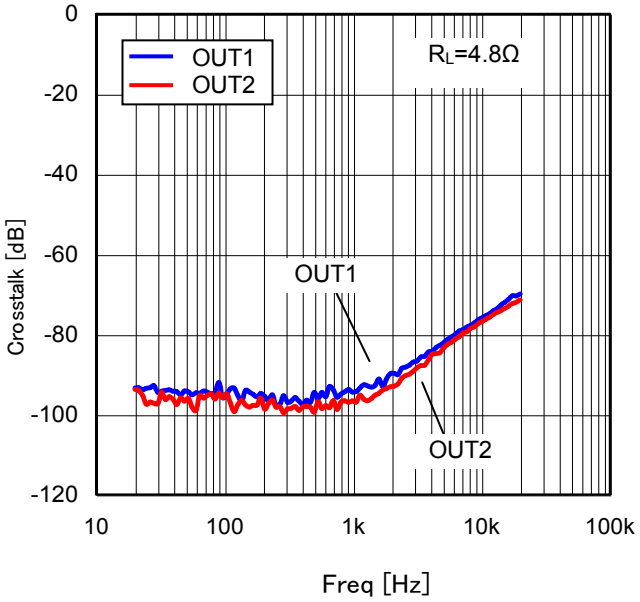


Figure 44. Crosstalk vs Freq (4.8Ω)

Typical Performance Curves – continued (11/11)

(Unless otherwise specified, Ta=25°C, V_{CC}=18V, f=1kHz, R_L=8Ω/6Ω, RSTX=3.3V, MUTEX=3.3V, f_S=48kHz, MCLK=256f_S, Snubber circuit: C=680pF, R=5.6Ω, ROHM 4-layer Board)

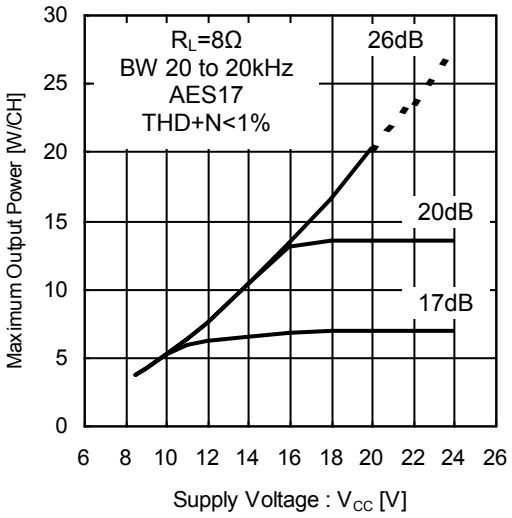


Figure 45. Supply Voltage vs Maximum Output Power (8Ω)

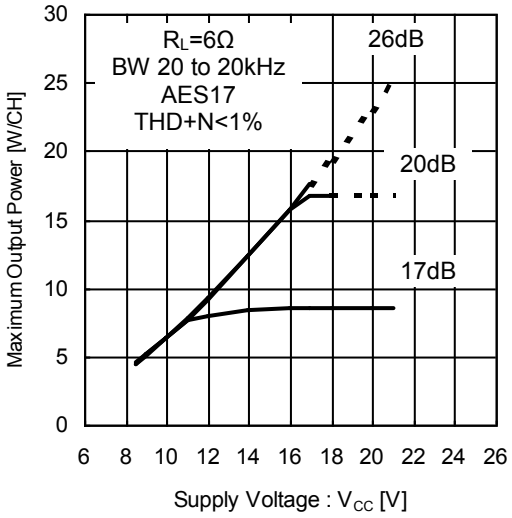


Figure 46. Supply Voltage vs Maximum Output Power (6Ω)

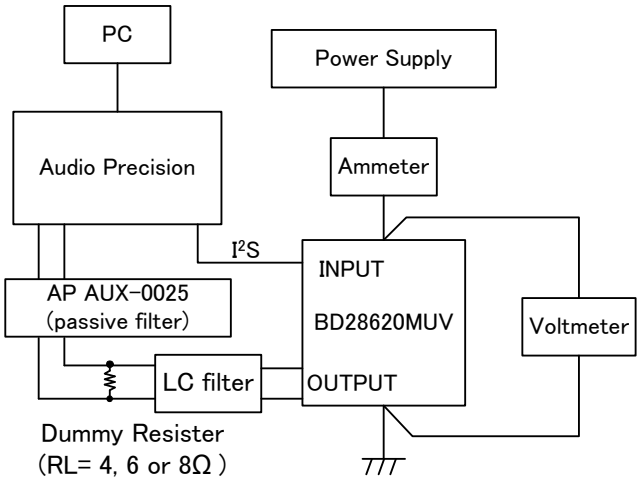


Figure 47. Audio Characteristics Measurement Environment

※ Dotted line means power dissipation is exceeded.

Timing Chart

1. Power Supply Start-up Sequence

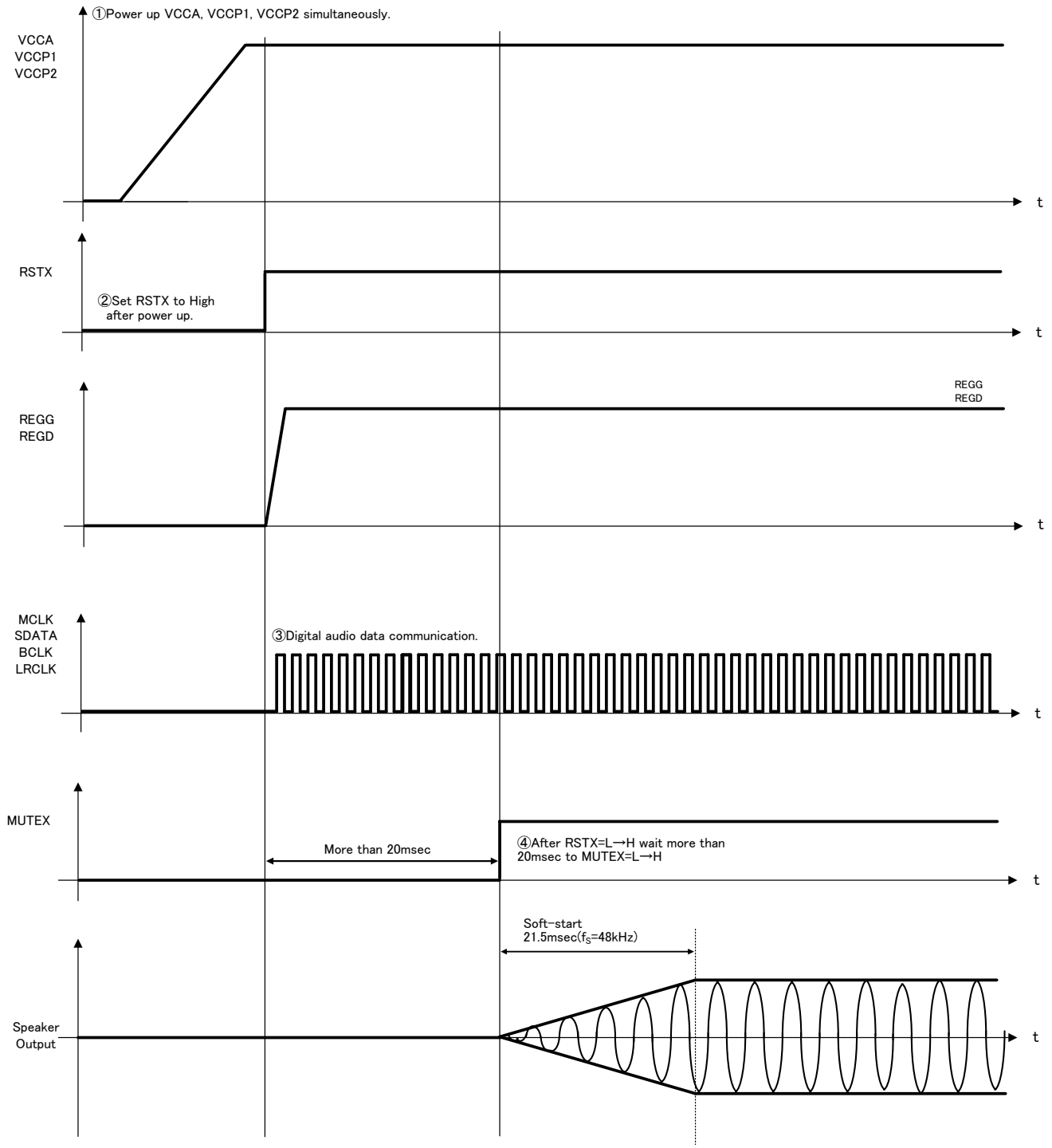


Figure 48. Power Supply Start-up Sequence

Caution: To eliminate pop noise when power supply is turned ON, RSTX and MUTEX should always be set Low. And also, all power supply terminals should start up together.

Order of ② and ③ can be interchanged

2. Power Supply Shutdown Sequence

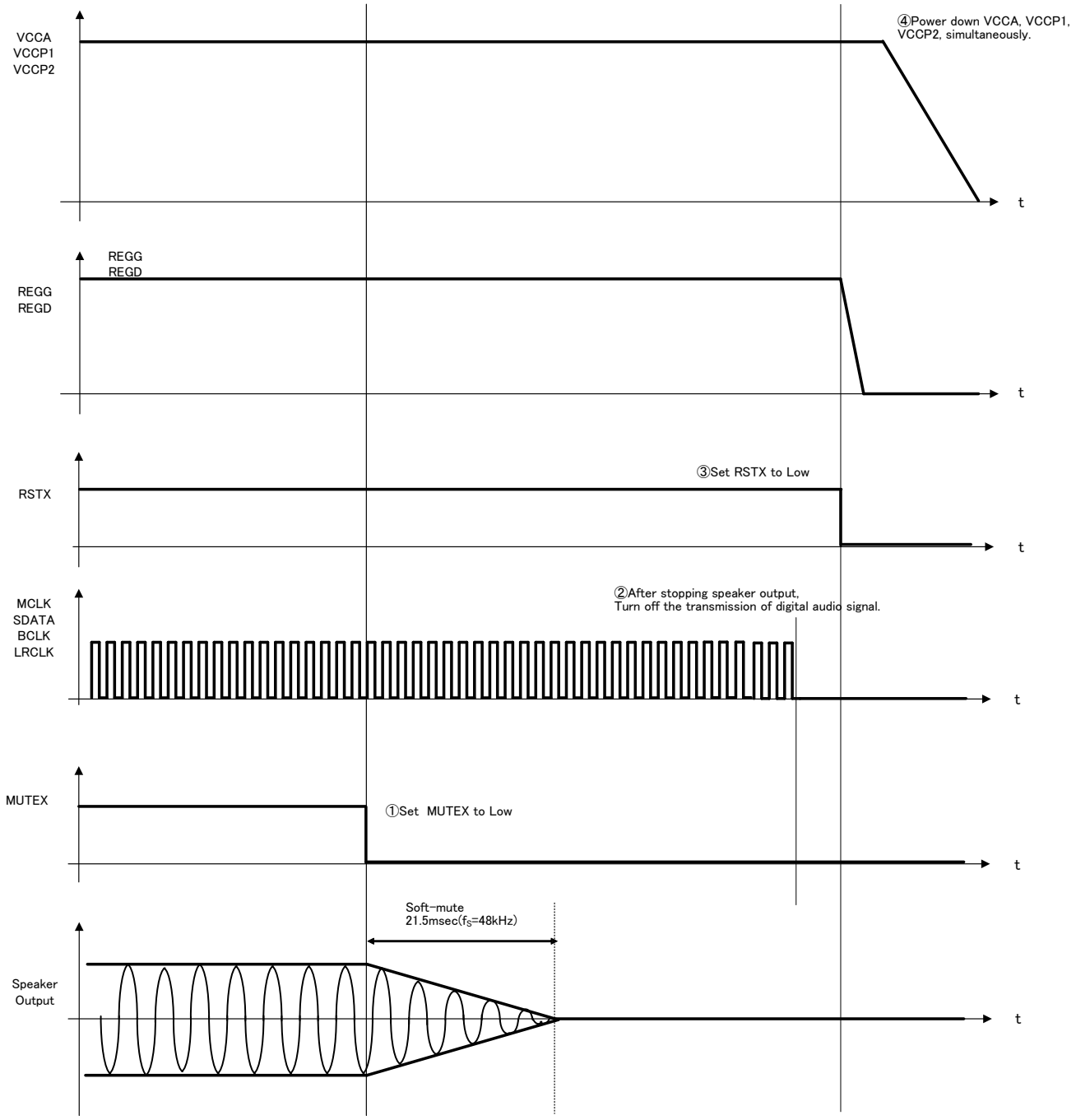


Figure 49. Power Supply Shutdown Sequence

Caution: To eliminate pop noise when power supply is turned OFF, RSTX and MUTEX should always be set Low first. And also, all power supply terminals should shut down together.

Order of ② and ③ can be interchanged

3. About Changing Audio Signal

Output PWM frequency is sixteen times the sampling frequency "f_S".
Therefore, output PWM frequency will also become unstable if MCLK becomes unstable when switching channel or switching input. During unstable period, LC resonance may occur and short protection function may work.

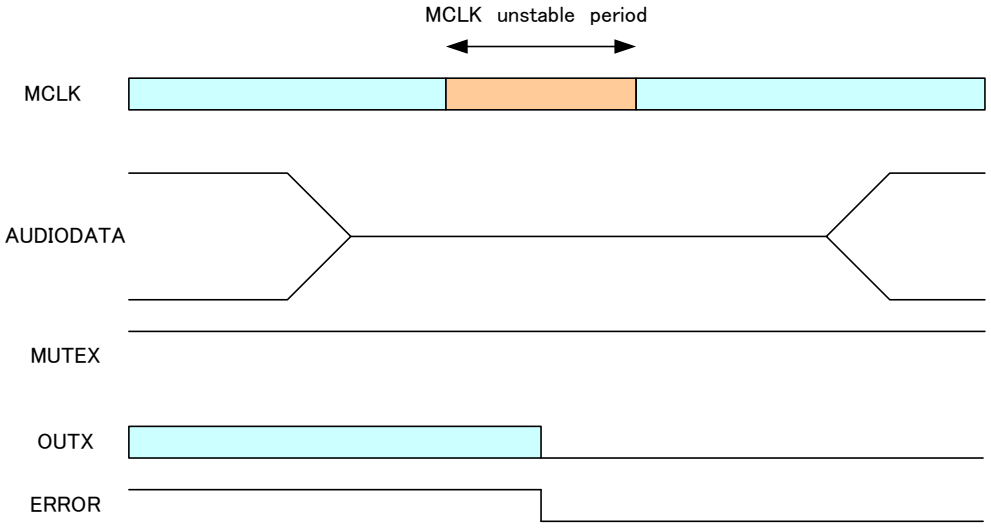


Figure 50. Action at MCLK Unstable 1

To prevent "MCLK unstable condition", please obey the following process.

(1) Mute "AUDIODATA" from scaler IC. (A)
(2) After muting "AUDIODATA" (B), set MUTEX=L (C).
(3) After MCLK goes to stable state, set MUTEX=H (D).
(4) Release mute "AUDIODATA" (E).

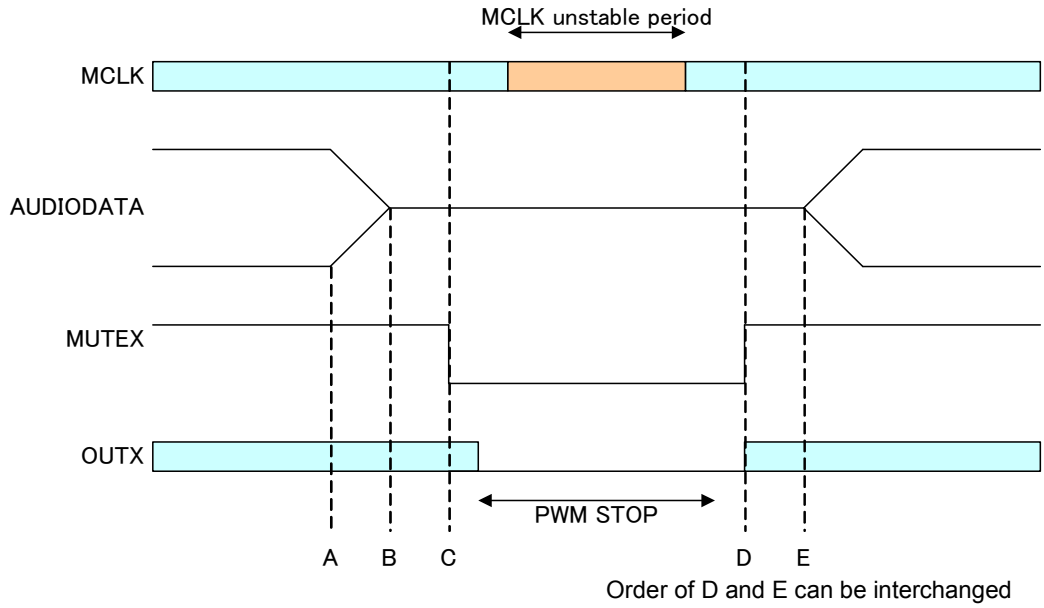


Figure 51. Action at MCLK Unstable 2

Especially, if the “twice and more frequency compared with normality” is entered, for some timing, the impure data is set to the IC’s internal resistor and it generates noises continuously.
In case the “twice and more frequency compared with normality” is entered, please follow the timing chart bellow and add a reset sequence.
(Please release reset after MCLK(BCLK) becomes stable, then release mute of BD28620MUV.)

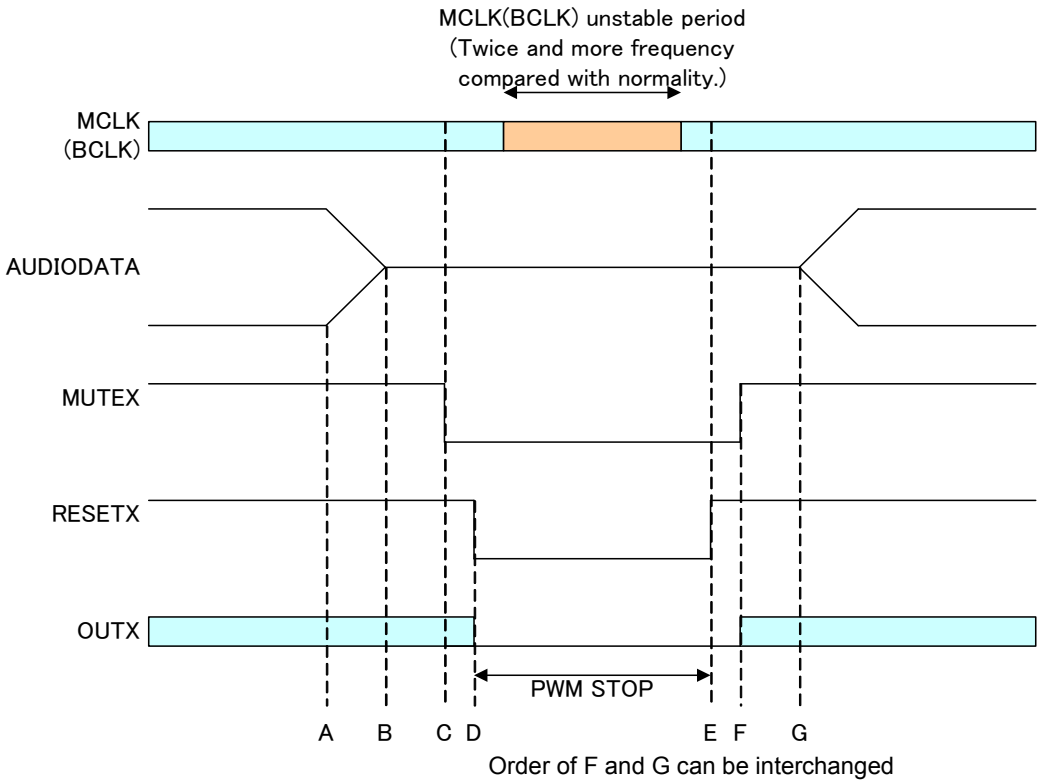


Figure 52. Action at MCLK Unstable 3

4. Recovery Sequence from the Instantaneous Power Supply Interruption

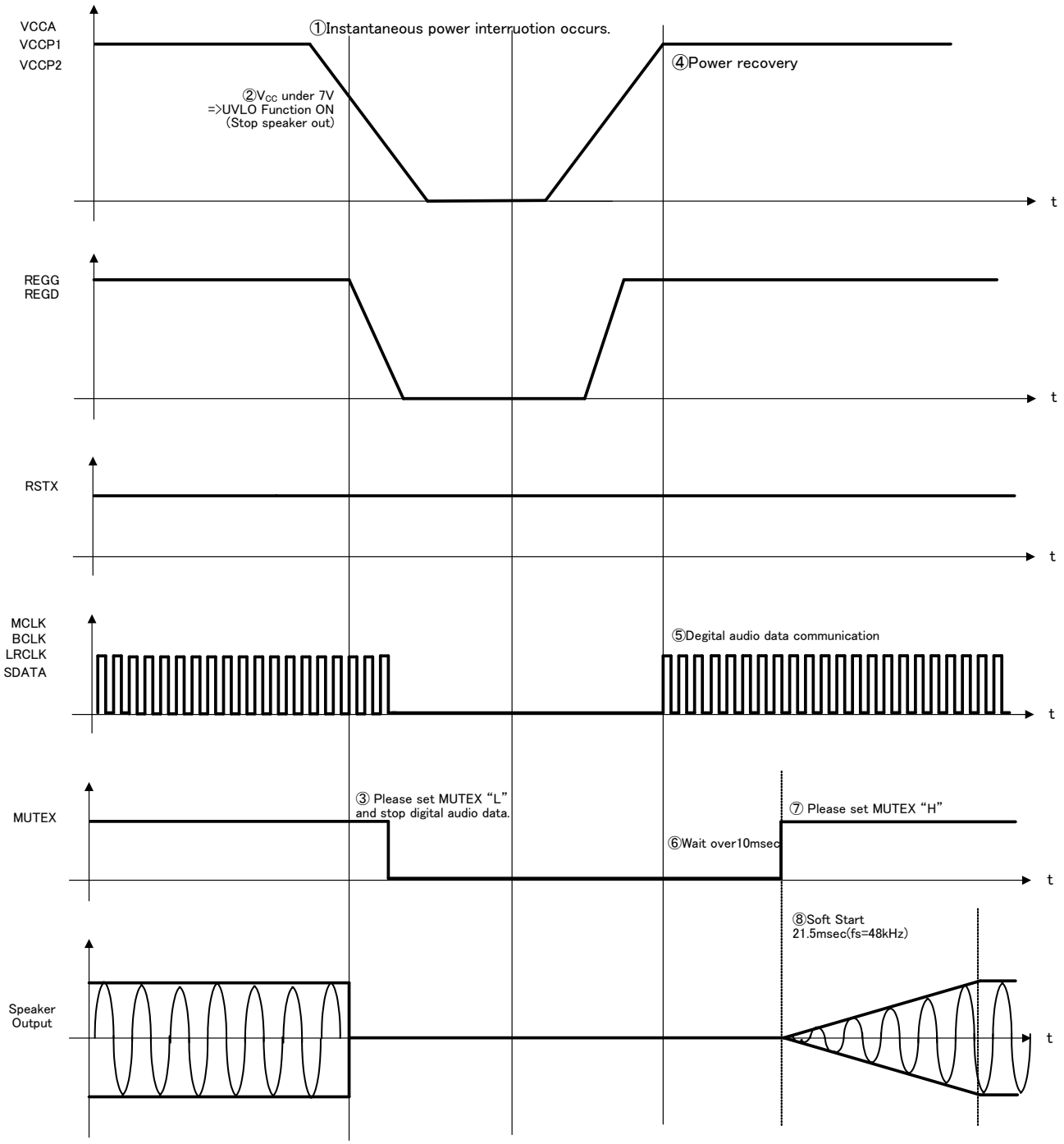


Figure 53. Instantaneous Power Interruption Recovery Sequence

Application Information

1. About digital audio input

(1) Input digital audio signal sampling frequency (f_S)

PWM frequency, Soft-start time, Soft-mute time, and the detection time of the DC voltage protection in the speaker depend on the sampling frequency (f_S) of the digital audio input.

Sampling Frequency of the Digital Audio Input (f_S)	PWM Frequency (f_{PWM})	Soft-start / Soft-mute Time	DC Voltage Protection in the Speaker Detection Time
32kHz	512kHz	32msec	1.02sec
44.1kHz	705.6kHz	23msec	0.74sec
48kHz	768kHz	21.5msec	0.68sec

(2) Format of digital audio input

MCLK: System Clock input signal

It will input LRCLK, BCLK, SDATA that synchronizes with this clock. MCLK frequency is 256 times the sampling frequency ($256f_S$) or 512 times the sampling frequency ($512f_S$).

LRCLK: L/R Clock input signal

It corresponds to 32kHz/44.1kHz/48kHz clock (f_S) which are same to the sampling frequency (f_S). The audio data of left and right channel for one sample is input to this section.

BCLK: Bit Clock input signal

It is used to latch data per bit using 64 times the sampling frequency ($64f_S$).

SDATA: Data input signal

It is amplitude data. The data length is different according to the resolution of the input digital audio data. It corresponds to 16/ 20/ 24 bits.

(3) I^2S Data Format

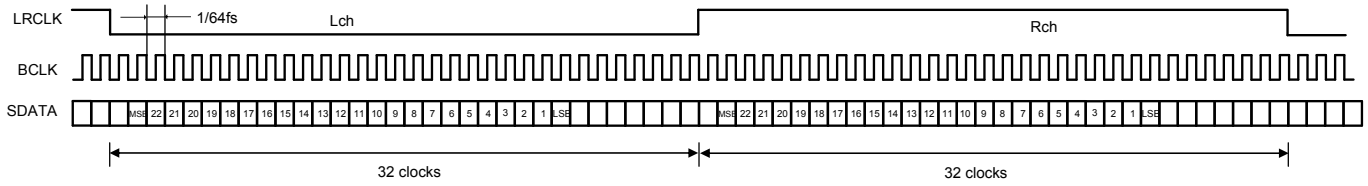


Figure 54. I2S Data Format 64fs, 24bit Data

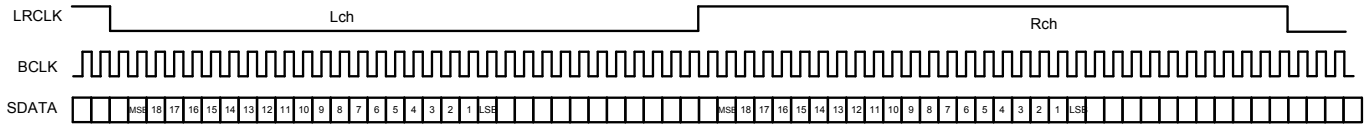


Figure 55. I2S Data Format 64fs, 20bit Data

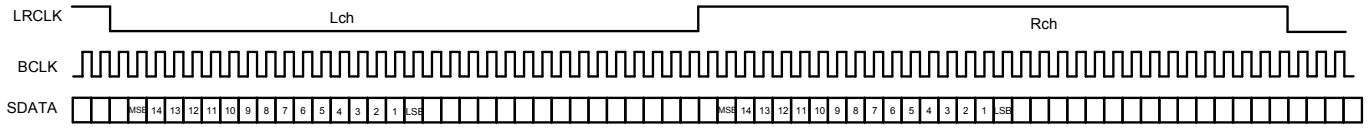


Figure 56. I2S Data Format 64fs, 16bit Data

The Low section of LRCLK becomes Lch and the High section of LRCLK becomes Rch.
After changing LRCLK, second bit becomes MSB.

(4) Audio Interface Format and Timing
Recommended timing and operating condition (MCLK, BCLK, LRCLK and SDATA)

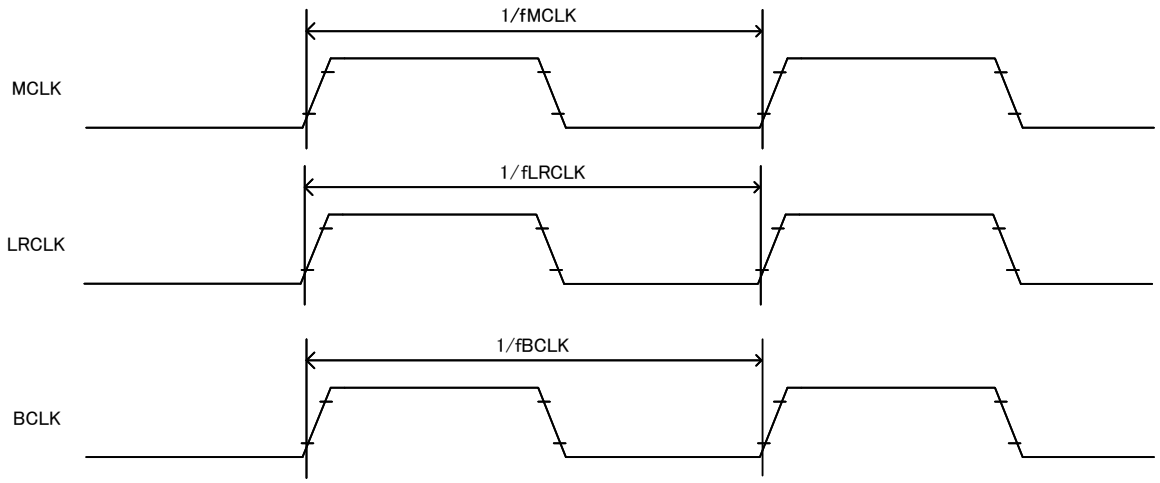


Figure 57. Clock Timing

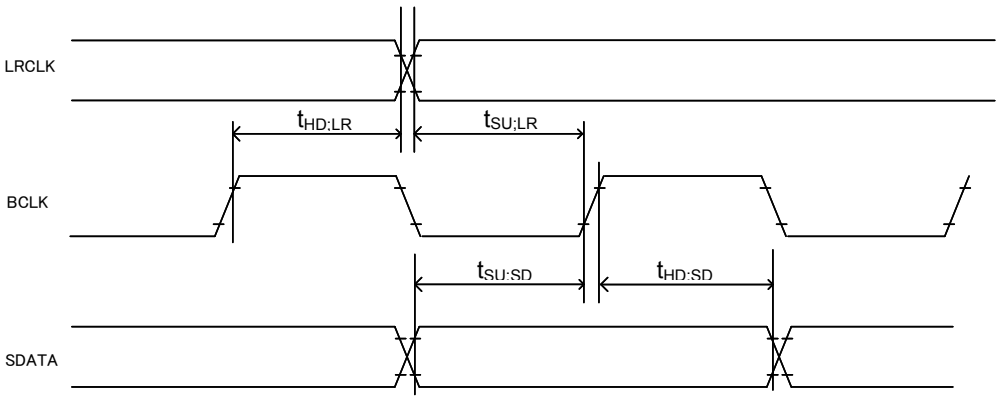


Figure 50 Audio Interface Timing

No.	Parameter	Symbol	Limit				Unit
			MCLK=256f_S		MCLK=512f_S		
			Min	Max	Min	Max	
1	MCLK Frequency(Note 8-1)	f_{MCLK}	8.192 ±10%	12.288 ±10%	16.384 ±10%	24.576 ±10%	MHz
2	LRCLK Frequency(Note 8-1)	f_{LRCLK}	32 ±10%	48 ±10%	32 ±10%	48 ±10%	kHz
3	BCLK Frequency(Note 8-1)	f_{BCLK}	2.048 ±10%	3.072 ±10%	2.048 ±10%	3.072 ±10%	MHz
4	Setup Time, LRCLK (Note 8-2)	$t_{SU;LR}$	20	–	20	–	ns
5	Hold Time, LRCLK (Note 8-2)	$t_{HD;LR}$	20	–	20	–	ns
6	Setup Time, SDATA	$t_{SU;SD}$	20	–	20	–	ns
7	Hold Time, SDATA	$t_{HD;SD}$	20	–	20	–	ns
8	MCLK, DUTY	d_{MCLK}	40	60	40	60	%
9	LRCLK, DUTY	d_{LRCLK}	40	60	40	60	%
10	BCLK, DUTY	d_{BCLK}	40	60	40	60	%

(Note 8-1) Must be synchronized with BCLK, LRCK
(Note 8-2) This regulation is to keep rising edge of LRCK and rising edge of BCLK from overlapping.

2. Terminal Setting

(1) RSTX Pin, MUTEX Pin Function

Condition	RSTX	MUTEX	Normal		Error Detection	
			Output (OUT1P, 1N, 2P, 2N)	ERROR	Output (OUT1P, 1N, 2P, 2N)	ERROR
"RESET"(Note 9)	L	L/H	High-Z_Low(Note 10) (Reset mode)	H	High-Z_Low (Reset mode)	H
"MUTE"	H	L	High-Z_Low (MUTE_ON)	H	High-Z_Low (MUTE_ON)	L
"ACTIVE"	H	H	Active (MUTE_OFF)	H	High-Z_Low (MUTE_ON)	L

(Note 9) If RSTX is set Low, internal registers (I^2S / I/F part, ×8 over sampling digital filter part, latch circuit when detecting ERROR) are initialized.
(Note 10) This means that all power transistors are OFF and output terminals are pulled down by 40kΩ (Typ).

(2) PLIMT Pin Function

PLIMT terminal sets the gain. Gain setting limits maximum output power.
PLIMT setting depends on the value of speaker load, because maximum output power depends on speaker load.
Set PLIMT after setting MUTE to L. Pop noise may be occur if PLIMT is set while MUTE=H.

PLIMT	Gain Setting (BTL)	Power Limit
L	17dB	Min 5 W (at 8Ω)
Pull-up (3.3V) to 27kΩ(1/10W, J(±5%))	20dB	Min 10 W (at 8Ω)
H	26dB	OFF

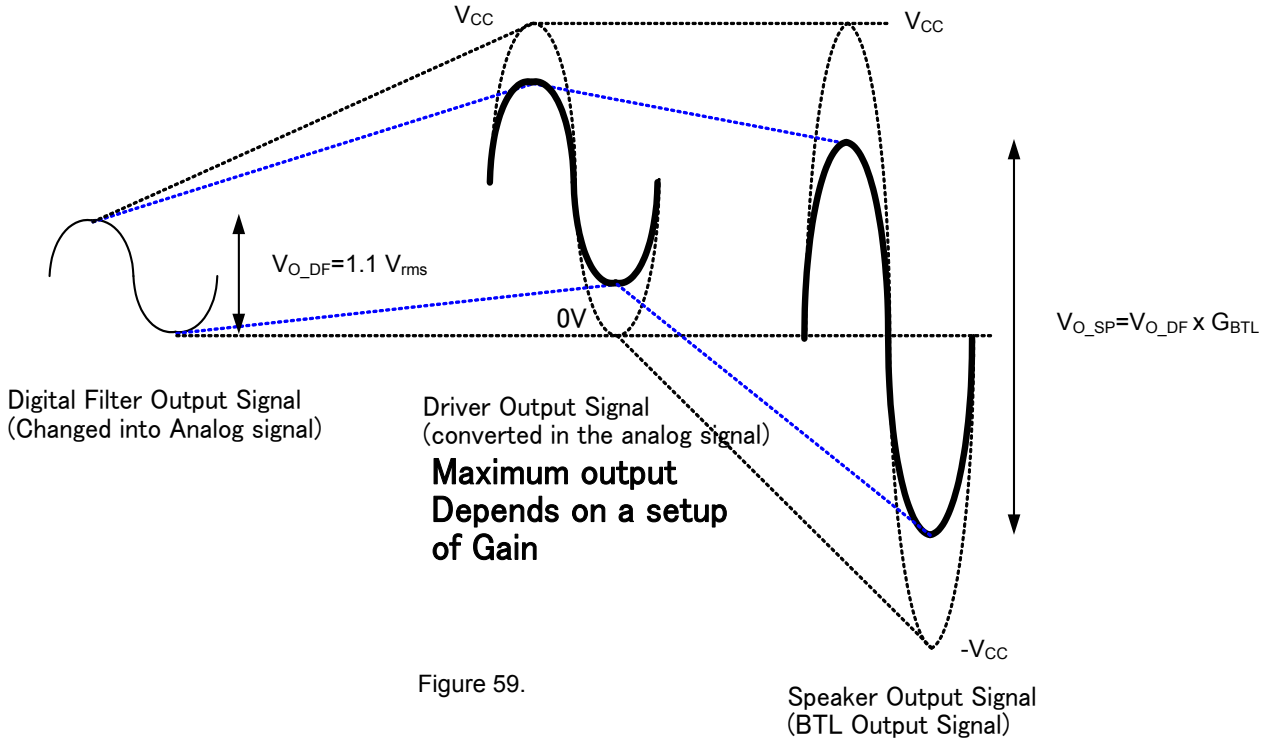


Figure 59.

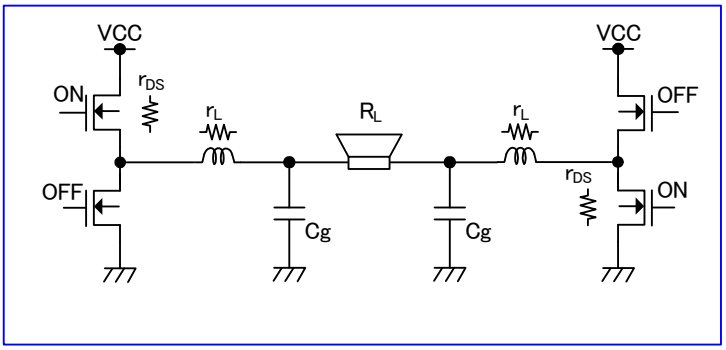


Figure 60. Schematic of Output Equivalent

$$V_{O\_SP} = V_{O\_DSP} \times 10^{\left(\frac{G_{BTL}}{20}\right)} \times \frac{R_L}{2(r_{DS} + r_{DC}) + R_L}$$

$$P_{O(THD=1\%)} = \frac{\left[\left(10^{\frac{V_{IN}}{20}}\right) \times 10^{\left(\frac{G_{BTL}}{20}\right)} \times \frac{R_L}{2(r_{DS} + r_{DC}) + R_L}\right]^2}{R_L}$$

where:
V_{IN} is the I^2S input level [dBFS]
G_{BTL} is the gain setting [dB]
R_L is the load resistance [Ω]
r_{DS} is the resistance of FET [Ω]
(Typ=0.23Ω)
r_{DC} is the DC resistance of inductor [Ω]

3. About the Protection Function

Protection Function	Detecting & Releasing Condition		PWM Output	ERROR Output
Output Short Protection	Detecting condition	Detecting current = 7A (Typ) /4.3A (Min. Tj=85℃) 3.7A (Min. Tj=150℃)	High-Z_Low (Latch)	L (Latch)
DC Voltage Protection in the Speaker	Detecting condition	At speaker output, impressed DC voltage over 0.68sec (f_S=48kHz) Over 3.5V (power limit OFF) Over 1.75V (power limit 10W) Over 1.225V (power limit 5W)	High-Z_Low (Latch)	L (Latch)
High Temperature Protection	Detecting condition	Chip temperature above 150°C (Typ)	High-Z_Low	L
	Releasing condition	Chip temperature below 120°C (Typ)	Normal operation	
Under Voltage Protection	Detecting condition	Power supply voltage below 7V (Typ)	High-Z_Low	H
	Releasing condition	Power supply voltage above 7.5V (Typ)	Normal operation	
Clock Stop Protection	Detecting condition	No change in MCLK for more than 1μsec (Typ) or	High-Z_Low	H
		No change in BCLK for more than 1μsec (Typ) or		
		No change in LRCLK for more than 21μsec (at f_S=48kHz.).		
	Releasing condition	Normal input to MCLK, BCLK and LRCLK.	Normal operation	

(Note) The ERROR pin is Nch open-drain output.
(Note) Once an IC is latched, the circuit is not released automatically even after the detecting status is removed.

Procedure ① or ② is needed for recovery.
①MUTEX terminal is turned Low (holding time at Low = 10msec(Min)) then turned back to High again.
②Power supply is turned on again after dropping to V_{CC}<3V(10msec (Min) holding) in which the internal power ON reset circuit activates.

(Note) Please remove the DC component in SoC and DSP IC of the preceding paragraph of this IC so that DC voltage protection feature not to aim at does not operate.
The Low pass filter function for the DC component removal is not to this product.

(1) Output Short Protection (Short to Power Supply)

This IC has PWM output short protection circuit that stops the PWM output when the Speaker output (after LC-filter) is short-circuited to the power supply due to wrong condition.

Detecting condition - It will detect when MUTEX pin is set High and the current that flows in the PWM output pin becomes 7A(Typ) or more. The PWM output instantaneously enters the state of High-Z_Low if detected, and the IC is latched.

Releasing method - ①After MUTEX terminal is turned Low (holding time at Low = 10msec(Min)) then turned back to High again.
② Power supply is turned on again after dropping to V_{CC}<3V(10msec (Min) holding) in which the internal power ON reset circuit activates.

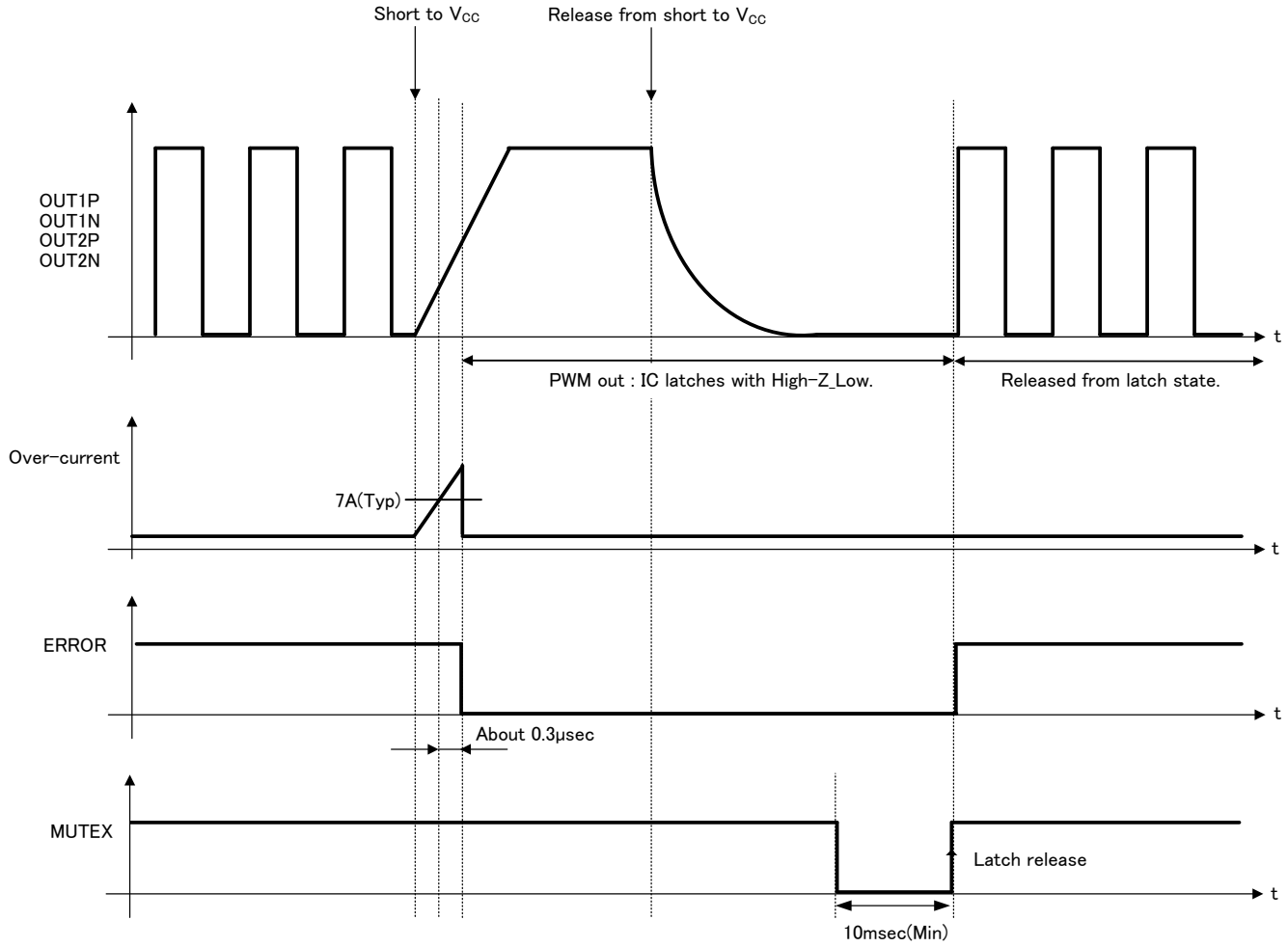


Figure 61. Output Short Protection (Short to Power Supply) Sequence

(2) Output Short Protection (Short to GND)

This IC has PWM output short protection circuit that stops the PWM output when the Speaker output (after LC-filter) is short-circuited to GND due to wrong condition.

Detecting condition - It will detect when MUTEX pin is set High and the current that flows in the PWM output terminal becomes 7A(Typ) or more. The PWM output instantaneously enters the state of High-Z_Low if detected, and the IC is latched.

Releasing method - ① After MUTEX terminal is turned Low (holding time at Low = 10msec(Min)) then turned back to High again.
② Power supply is turned on again after dropping to V_{CC}<3V(10msec (Min) holding) in which the internal power ON reset circuit activates.

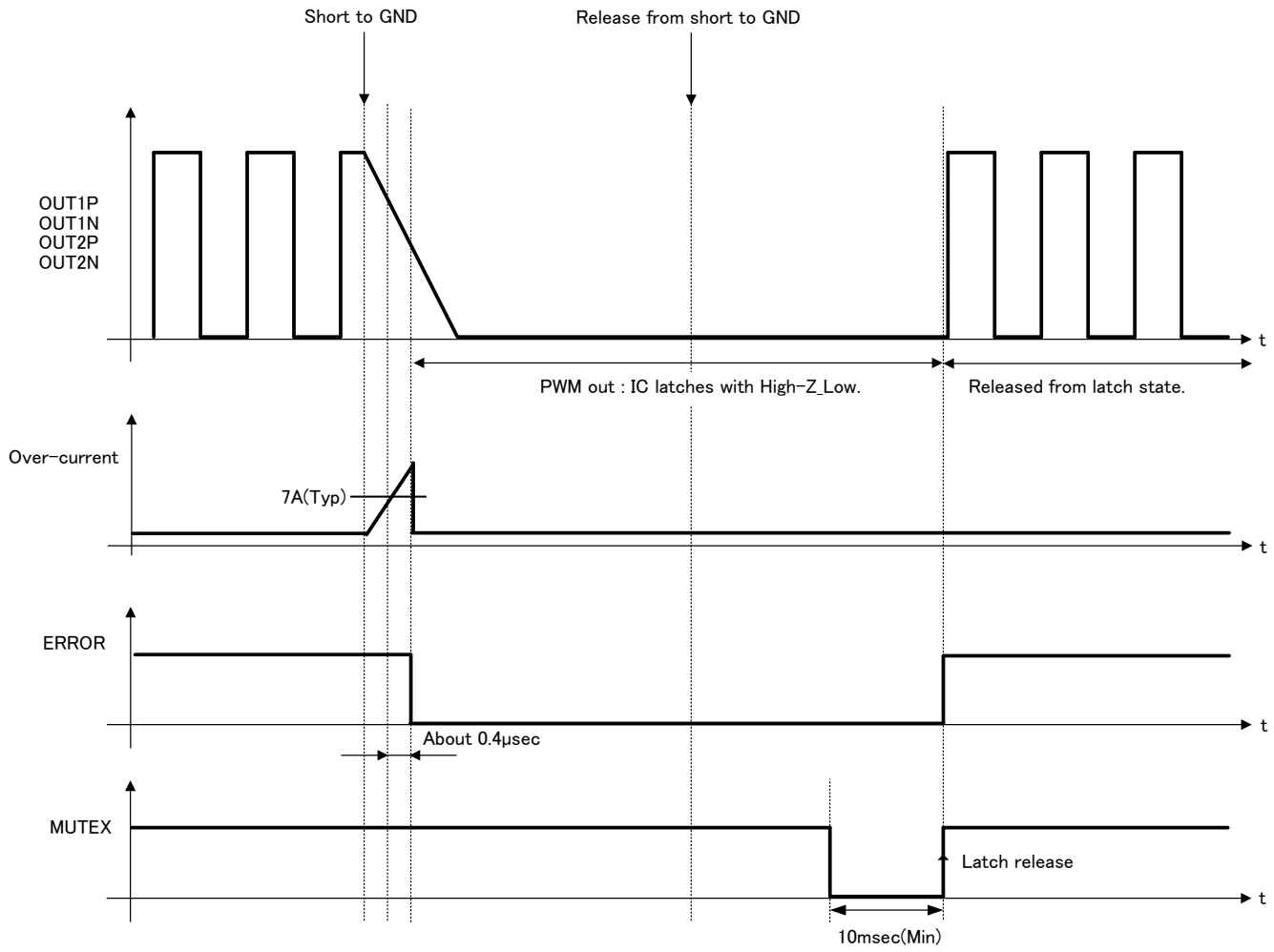


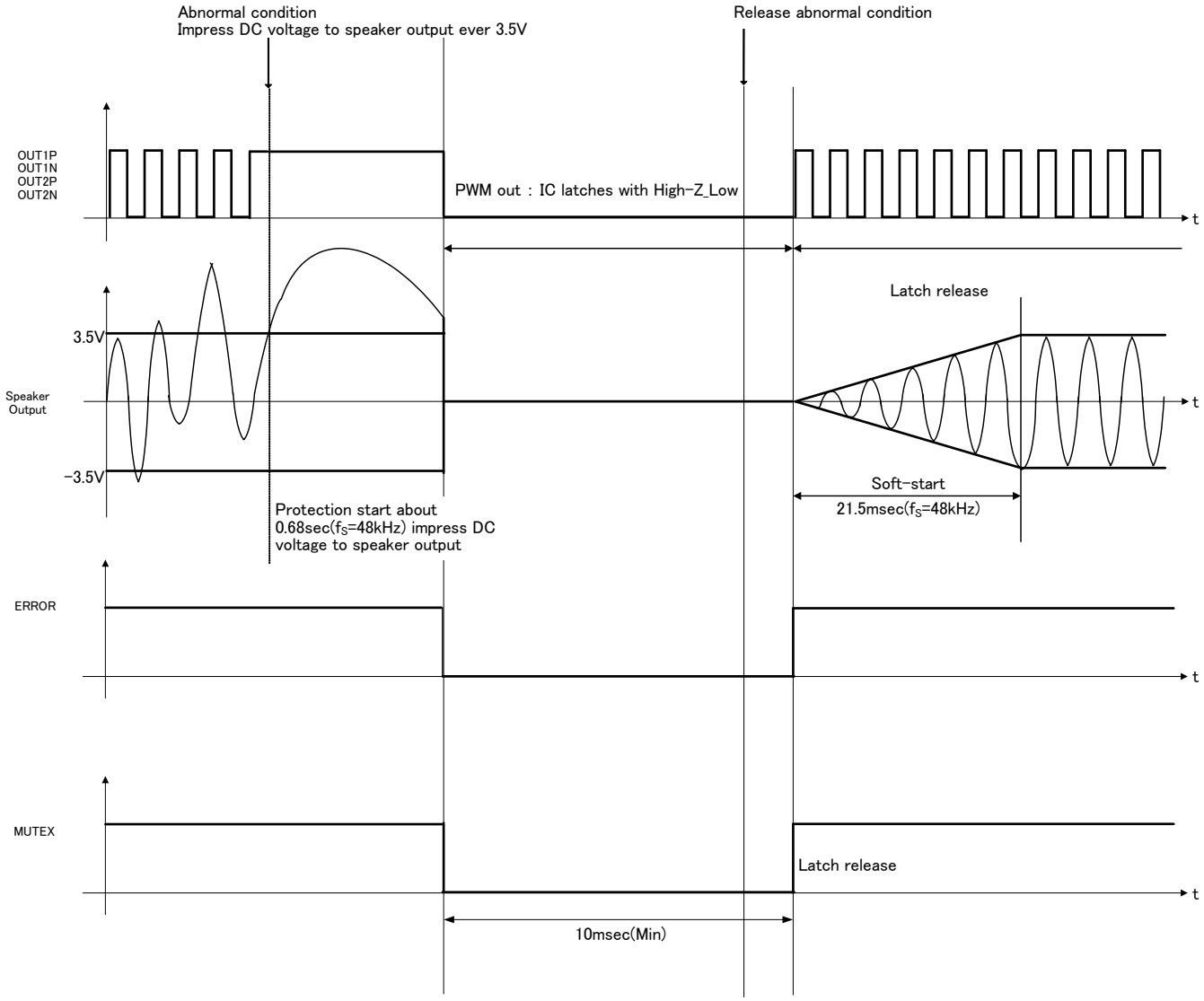
Figure 62. Output Short Protection (Short to GND) Sequence

(3) DC Voltage Protection

When DC voltage is applied to the speaker due to wrong condition, this IC has protection circuit where the speaker is protected from destruction.

Detecting condition - It will detect when MUTEX pin is set High and speaker output is more than 3.5V (TYP, Power Limit OFF setting), 1.75V (TYP, Power Limit 10W setting), 1.225V (TYP, Power Limit 5W setting), 0.68sec(f_S=48kHz) or above. Once detected, the PWM output instantaneously enters the state of High-Z_Low, and the IC is latched.

Releasing method - ①After MUTEX terminal is turned Low (holding time at Low = 10msec(Min)) then turned back to High again.
② Power supply is turned on again after dropping to V_{CC}<3V(10msec (Min) holding) in which the internal power ON reset circuit activates.



(Power Limit OFF settings)

Figure 63. DC Voltage Protection Sequence

(4) High Temperature Protection

This IC has high temperature protection circuit that prevents thermal runaway when the temperature of the chip exceeds Tjmax=150°C.

Detecting condition - It will detect when MUTEX pin is set High and the temperature of the chip becomes 150°C (Typ) or more. Speaker output turns MUTE immediately when high temperature protection is detected.

Releasing condition - It will release when MUTEX pin is set High and the temperature of the chip becomes 120°C (Typ) or less. The speaker output is outputted through a soft-start when released. (Auto recovery)

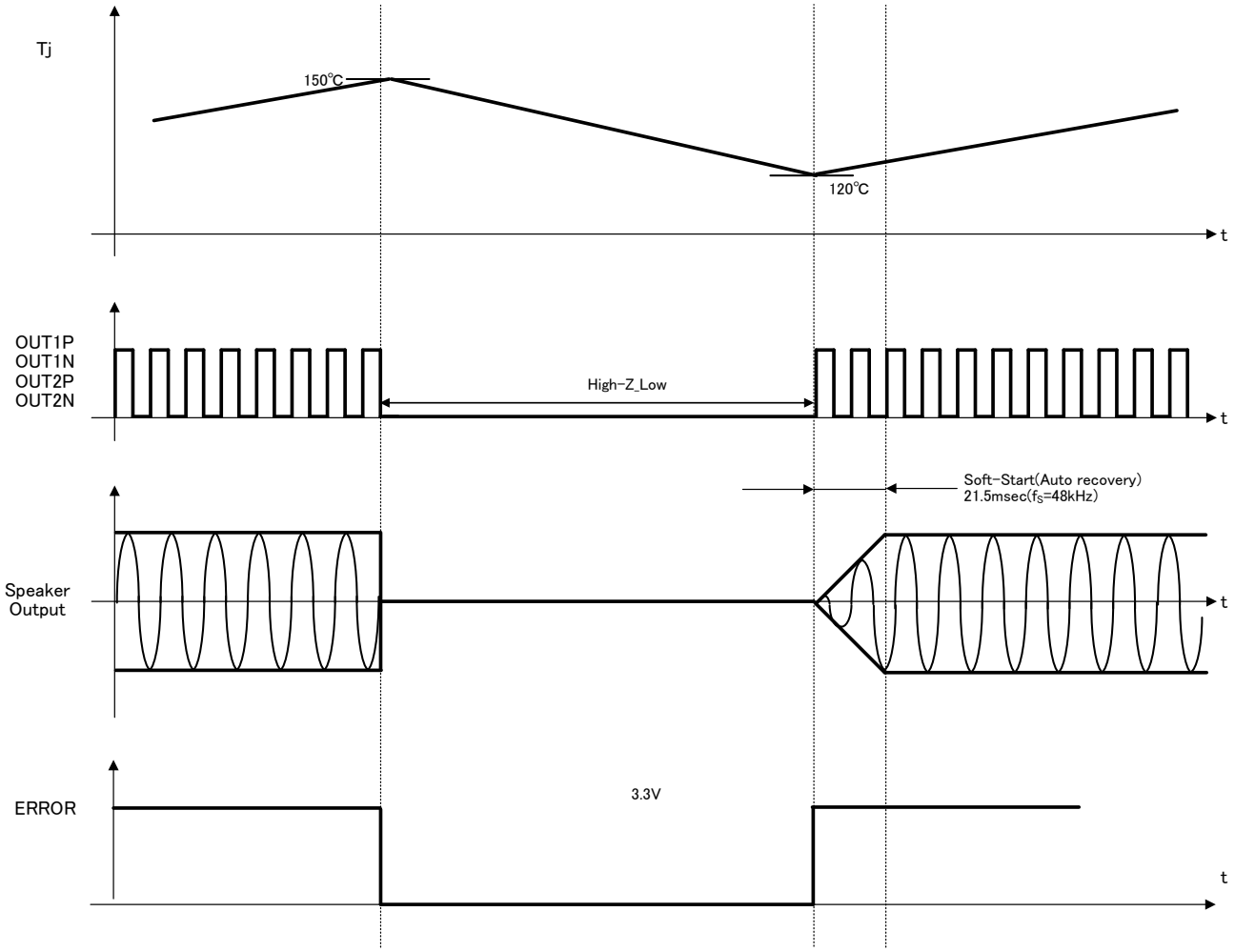


Figure 64. High Temperature Protection Sequence

(5) Under Voltage Protection

This IC has under voltage protection circuit that mutes the speaker output mute once it detects extreme drop of the power supply voltage.

Detecting condition - It will detect when MUTEX pin is set High and the power supply voltage becomes lower than 7V(Typ). Speaker output turns MUTE immediately when under voltage protection is detected.

Releasing condition - It will release when MUTEX pin is set High and the power supply voltage becomes more than 7.5V (Typ). The speaker output is outputted through a soft-start when released. (Auto recovery)

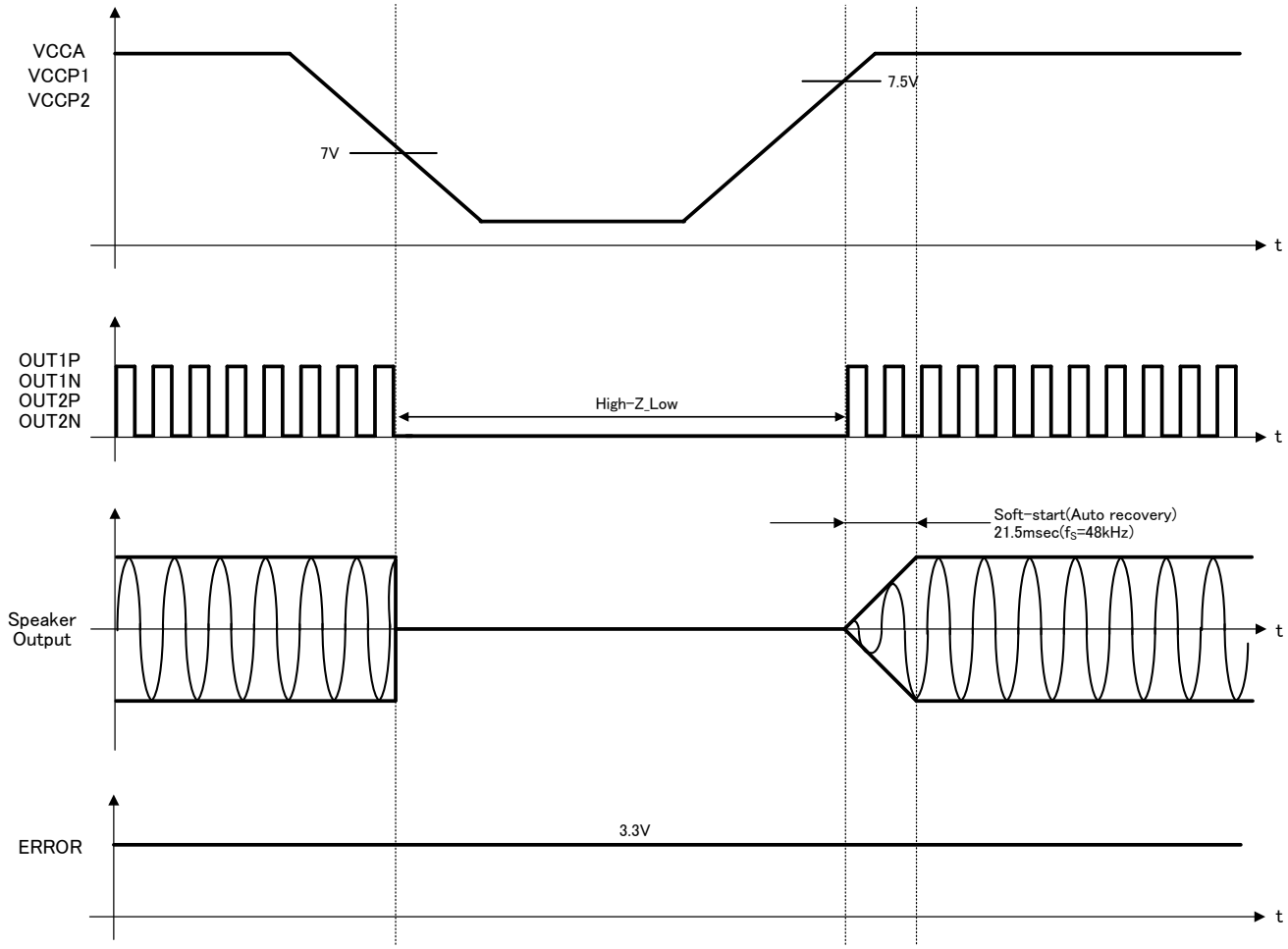


Figure 65. Under Voltage Protection Sequence

(6) Clock Stop Protection (MCLK)

This IC has clock stop protection circuit that mutes the speaker output when the MCLK signal of the digital audio input stops.

Detecting condition - It will detect when MUTEX pin is set High and the MCLK signal stops for about 1µsec or more. Speaker output turns MUTE immediately when clock stop protection is detected.

Releasing condition - It will release when MUTEX pin is set High and the MCLK signal returns to the normal clock operation. The speaker output is outputted through a soft-start when released. (Auto recovery)

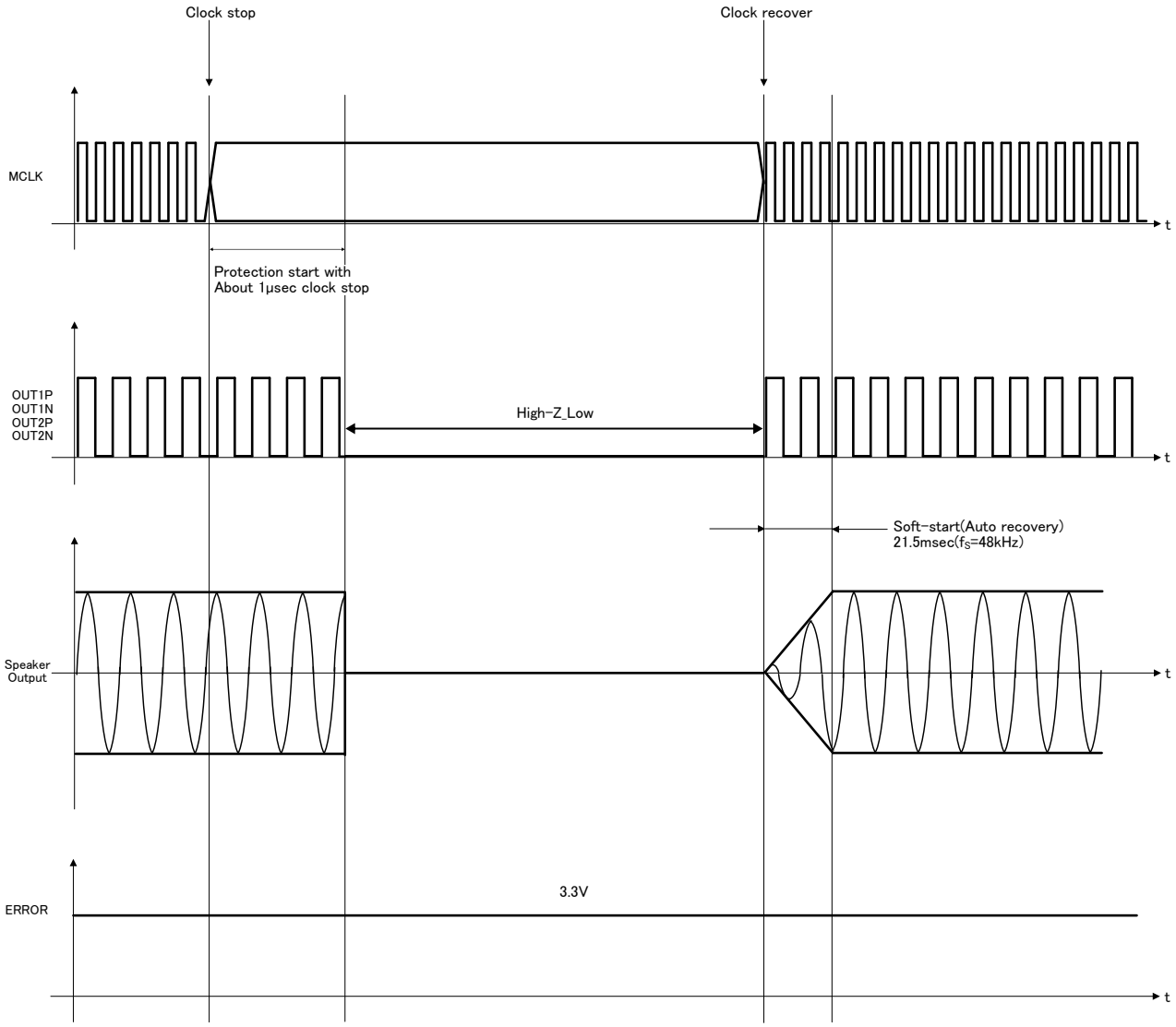


Figure 66. Clock Stop Protection (MCLK) Sequence

(7) Clock Stop Protection (BCLK)

This IC has clock stop protection circuit that mutes the speaker output when the BCLK signal of the digital audio input stops.

Detecting condition - It will detect when MUTEX pin is set High and the BCLK signal stops for about 1µsec or more. Speaker output turns MUTE immediately when clock stop protection is detected.

Releasing condition - It will release when MUTEX pin is set High and the BCLK signal returns to the normal clock operation. The speaker output is outputted through a soft-start when released. (Auto recovery)

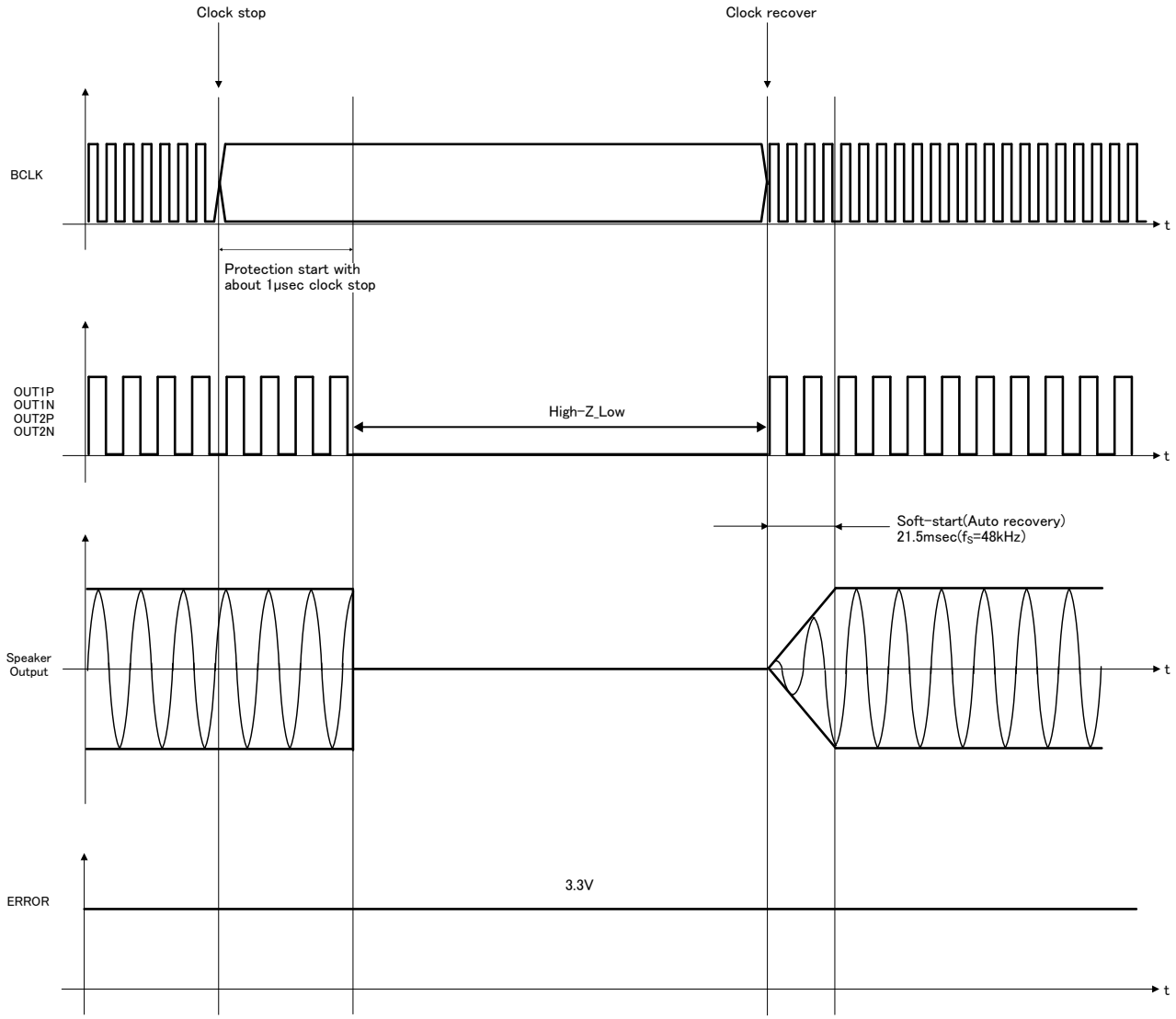


Figure 67. Clock Stop Protection (BCLK) Sequence

(8) Clock Stop Protection (LRCLK)

This IC has clock stop protection circuit that mutes the speaker output when the LRCLK signal of the digital audio input stops.

Detecting condition - It will detect when MUTEX pin is set High and the LRCLK signal stops for about 21µsec (at f_S=48kHz) or more. Speaker output turns MUTE immediately when clock stop protection is detected.

Releasing condition - It will release when MUTEX pin is set High and the LRCLK signal returns to the normal clock operation. The speaker output is outputted through a soft-start when released. (Auto recovery)

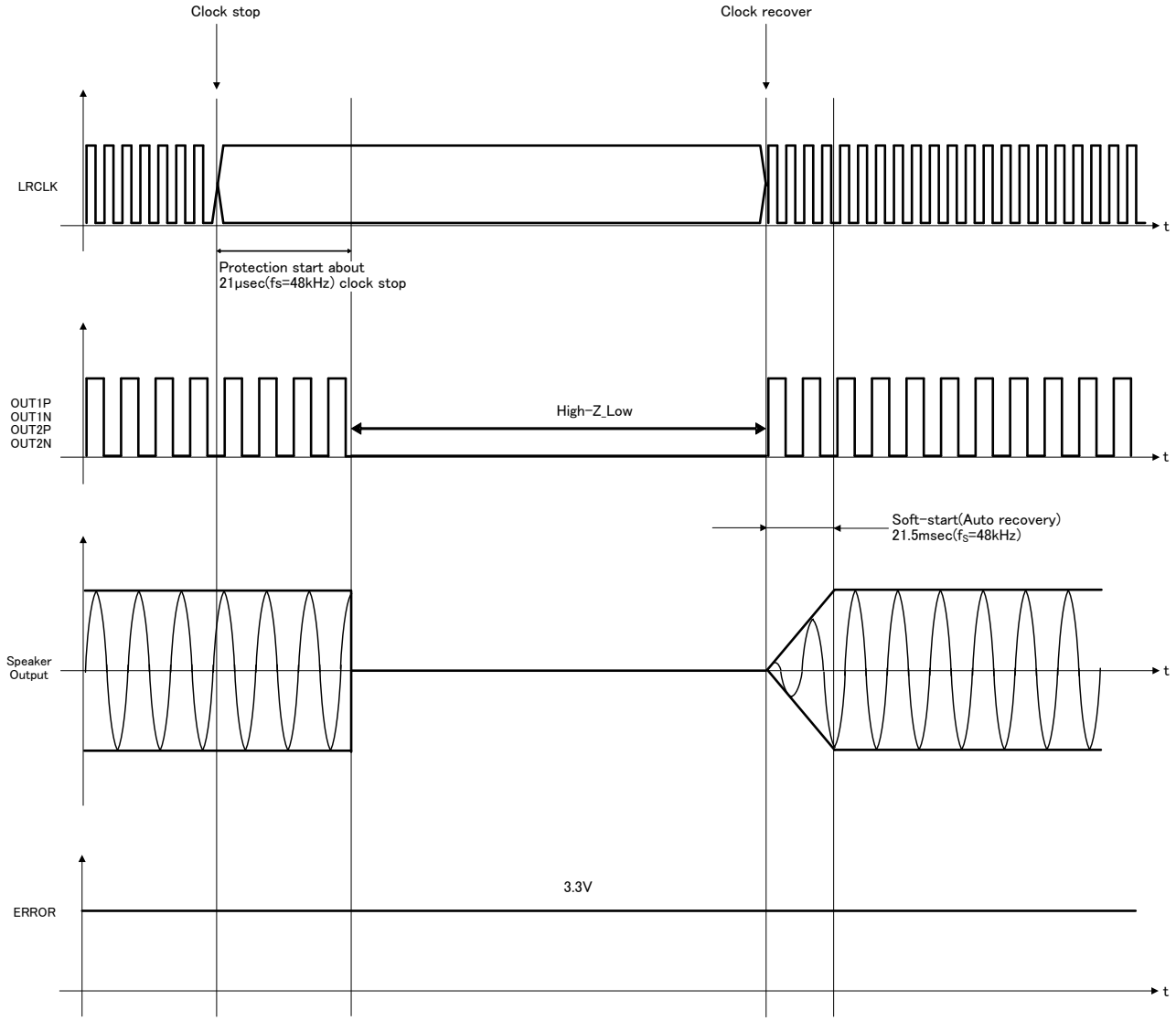


Figure 68. Clock Stop Protection (LRCLK) Sequence

4. Application Circuit Example

Stereo BTL Output, R_L=8Ω/6Ω

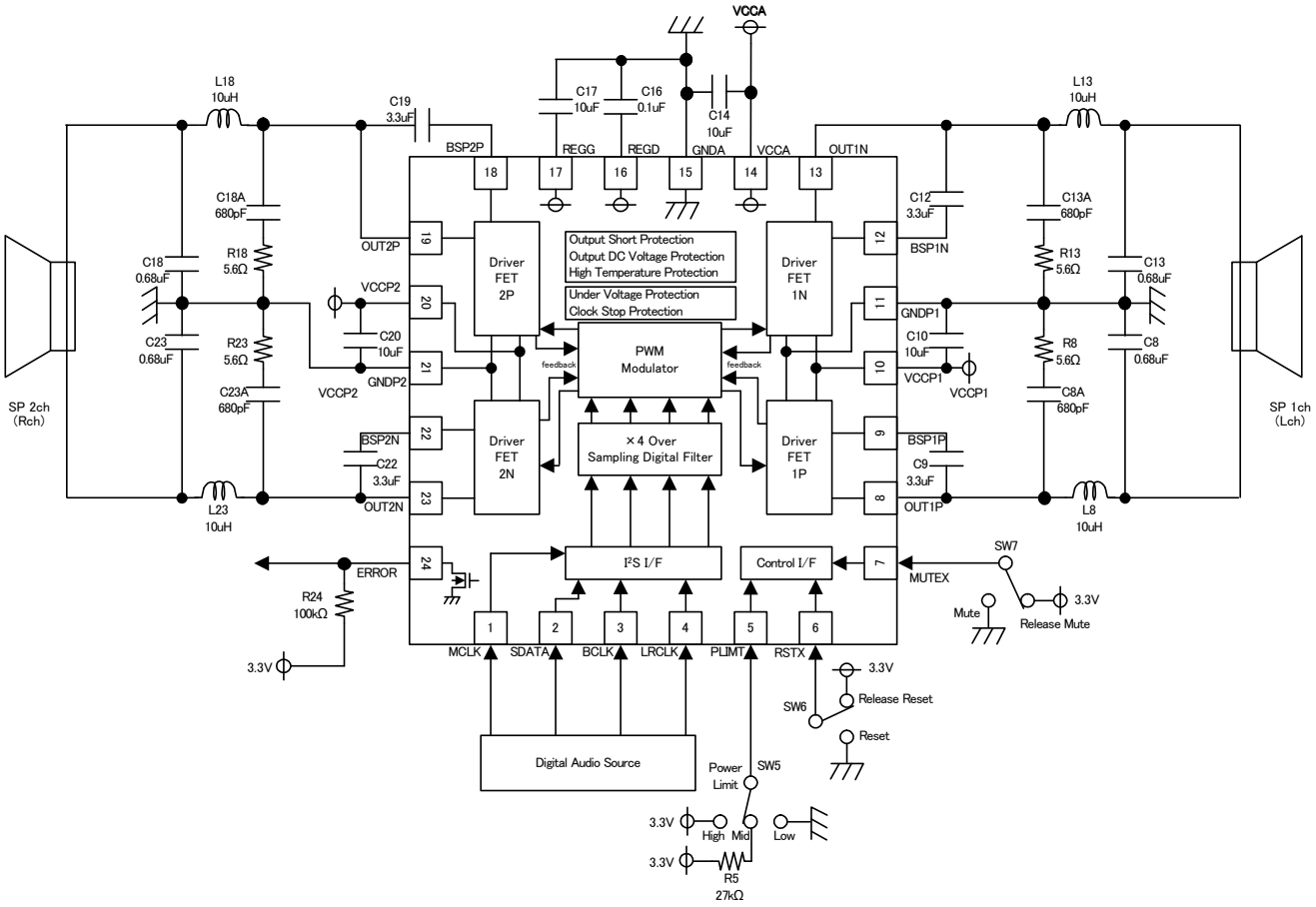


Figure 69. Application Circuit

Caution1: If the impedance characteristics of the speakers at high-frequency range increase rapidly, the IC might not have stable operation in the resonance frequency range of the LC filter. Therefore, consider adding damping-circuit, etc., depending on the impedance of the speaker.

Caution2: Though this IC has a short protection function, when short to VCC or GND after the LC filter, over current occurs during short protection function operation. Be careful about over/undershoot which exceeds the maximum standard ratings because back electromotive force of the inductor will occur which sometimes leads to IC destruction.

5. About Using BD28620MUV ICs for 2.1ch or 2.2ch audio

Be careful when using two BD28620MUVs at the same time for 2.1ch or 2.2ch audio.

BD28620MUV doesn't have the function that synchronizes both PWM frequencies of the two BD28620MUVs. Beat noise may occur due to the difference between PWM frequencies.

Switching current flows to the GND of LC-Filter and only a small part to the speaker which lowers emission noise. When you have two BD28620MUVs used at the same time with synchronized PWM output, there is common impedance in the GND of the filter. The GND electric potential becomes higher which also causes noise to become higher. The GND of the filter is shorted at one point when you use two BD28620MUVs at the same time.

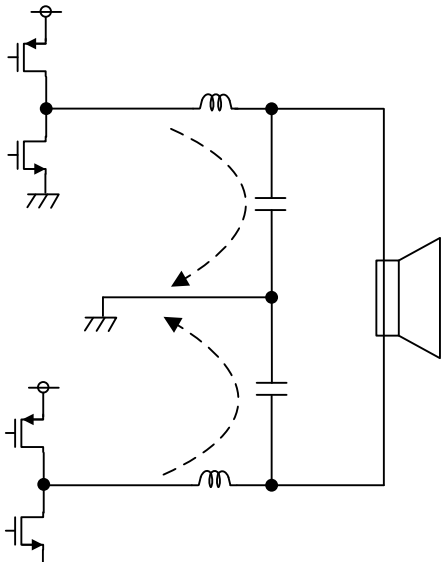


Figure 70. Output LC Filter

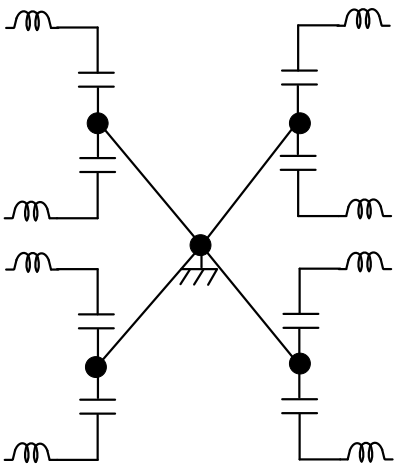


Figure 71. Circuit Using Two ICs to 2.1ch or 2.2ch audio

6. Selecting External Components

(1) Output LC Filter Circuit

An output filter is required to eliminate radio-frequency components exceeding the audio-frequency region supplied to a load (speaker). Because this IC uses sampling clock frequencies from 512kHz (f_S=32kHz) to 768kHz (f_S=48kHz) in the output PWM signals, the high-frequency components must be appropriately removed.

This section takes an example of an LC type LPF shown below, in which coil L and capacitor C compose a differential filter with an attenuation property of -12dB/oct. A large part of switching currents flow to capacitor C, and only a small part of the currents flow to speaker RL. This filter reduces unwanted emission this way. In addition, coil L and capacitor C compose a filter against in-phase components, reducing unwanted emission further.

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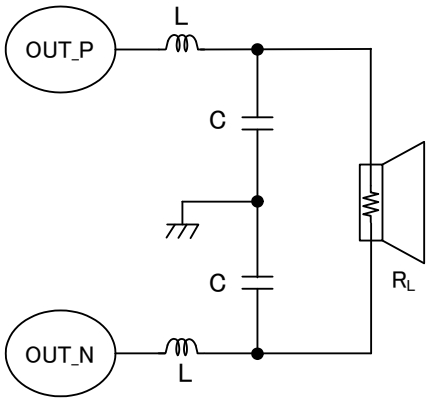


Figure 72. Output LC Filter

The following shows output LC filter constants with typical load impedances.

R_L	L	C
4Ω	10μH	1μF
6Ω, 8Ω	10μH	0.68μF

Use inductors with low ESR and with sufficient margin of allowable currents. Power loss will increase if inductors with high ESR are used.
Select a closed magnetic circuit type product in normal cases to prevent emission noise.
Use capacitors with low equivalent series resistance, and good impedance characteristics at high frequency ranges (100kHz or higher). Also, select an item with sufficient voltage rating because massive amount of high-frequency current flow is expected.

(2) Snubber circuit constant
When overshoot/undershoot of PWM Output exceeds absolute maximum rating, or when overshoot/undershoot of PWM output negatively affects EMC, or when ringing deteriorates the audio characteristic of the PWM output, snubber circuit is used as shown below.

(a) Measure the spike resonance frequency "f_1" of PWM output waveform (when rising) by using FET probe at the OUT terminal. (Figure 73)
Shorten GND lead of FET probe and monitor as near as possible to output pin.

(b) Measure the resonance frequency "f_2" of the spike as the snubber-circuit R value equals 0Ω
(capacitor "C" is connected to GND)
Adjust the value of the capacitor "C" until it becomes ($2 \times f_2 = f_1$)
The value of "C" that becomes ($2xf_2=f_1$) is 3 times of the parasitic capacity "C_p" that a spike is formed. ($C=3C_p$)

(c) Parasitic inductance "L_p" is calculated using the next formula.

$$L_p = \frac{1}{(2\pi f_1)^2 C_p}$$

(d) The character impedance Z of resonance is calculated from the parasitic capacity "C_p" and the parasitic inductance L_p using the next formula.

$$Z = \sqrt{\frac{L_p}{C_p}}$$

(e) Set snubber circuit "R" same as the character impedance "Z".
Set snubber circuit "C" 4 to 10 times of the parasitic capacity "C_p".
If "C" is set larger than $10C_p$, switching current will possibly increase.

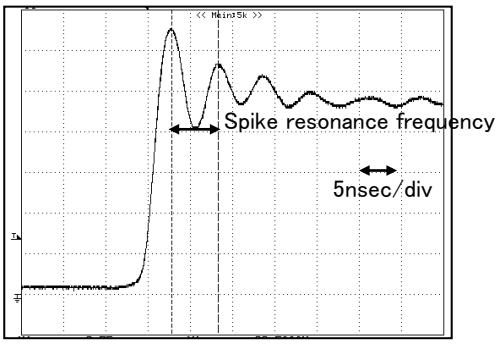


Figure 73. PWM Output Waveform
(Measure of Spike Resonance Frequency)

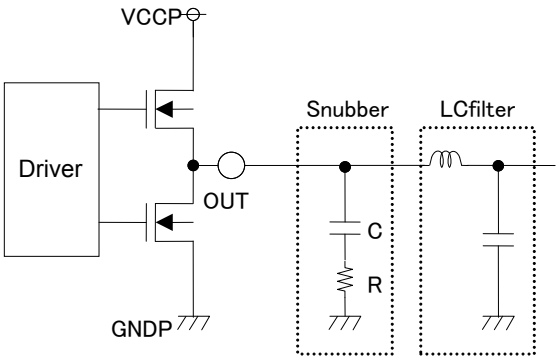


Figure74. Snubber Schematic

The following table shows ROHM recommended value of "Snubber filter constants" when using ROHM 4 layer board.

R_L	C	R
4Ω	680pF to 1200pF ,50V B(±10%)	5.6Ω,1/10W J(±5%)
6Ω	680pF to 1200pF ,50V B(±10%)	5.6Ω,1/10W J(±5%)
8Ω	680pF to 1200pF ,50V B(±10%)	5.6Ω,1/10W J(±5%)

Power Dissipation

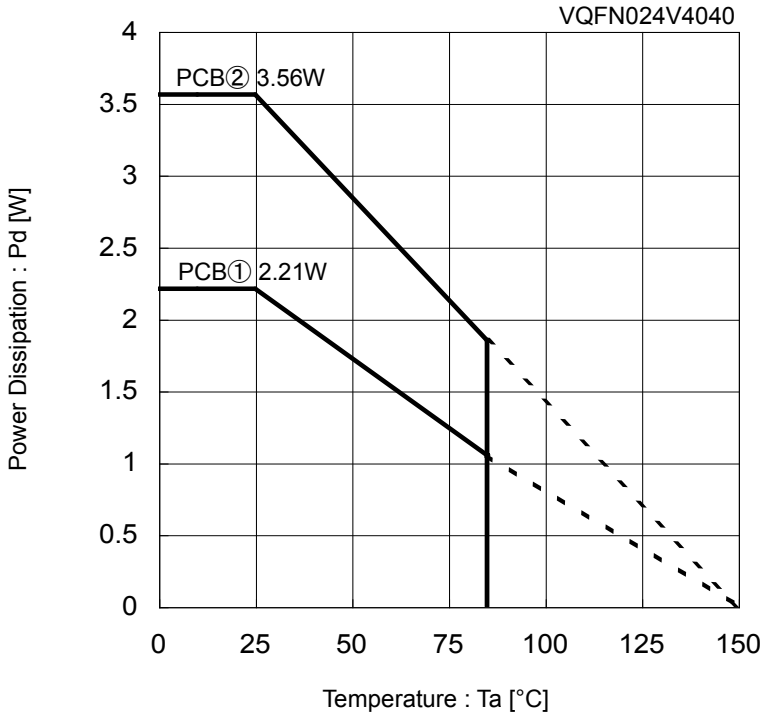


Figure 75. Power Dissipation Curve

Measuring instrument : TH-156 (Shibukawa Kuwano Electrical Instruments Co., Ltd.)
Measuring conditions : Installation on ROHM's board
Board size : 74.2mm x 74.2mm x 1.6mm (with thermal via on board)
Material：FR4
・The board and exposed heat sink on the back of package are connected by soldering.

PCB①：4- layer board (Top and bottom layer back copper foil size: 10.29mm2, 2nd and 3rd layer back copper foil size: 5505mm2), θja = 56.6°C/W
PCB②：4-layer board（back copper foil size: 5505mm2), θja = 35.1°C/W

Use a thermal design that has sufficient margin so as not to exceed allowable power dissipation (Pd) in actual operating conditions. This IC exposes its frame of the backside of package. Note that this part is used to provide heat dissipation treatment to improve heat dissipation efficiency. Try to occupy as wide as possible heat dissipation pattern not only on the board surface but also the backside.

Class D speaker amplifier has high efficiency and low heat generation in comparison with conventional analog power amplifier. However, in case it is operated continuously by maximum output power, power dissipation (Pdiss) may exceed package dissipation. Please consider heat design that power dissipation (Pdiss) does not exceed package dissipation (Pd) in average power (Poav).

$$\text{Package dissipation : } Pd(W) = (Tjmax - Ta) / \theta ja$$
$$\text{Power dissipation : } Pdiss(W) = Poav \times (1/\eta - 1)$$

where:
Tjmax is the maximum junction temperature=150°C
Ta is the peripheral temperature[°C],
θja is the thermal resistance of package[°C/W],
Poav is the average power [W],
η is the efficiency

Operational Notes

1. Reverse Connection of Power Supply
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned OFF completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

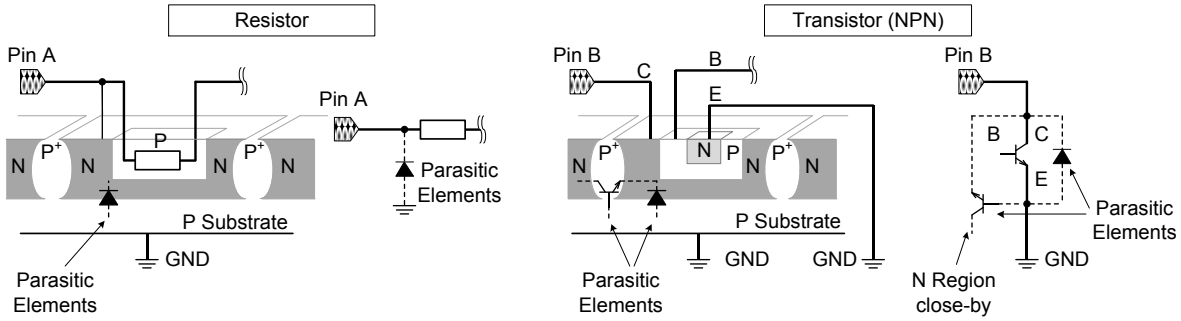


Figure 68. Example of Monolithic IC Structure

13. Ceramic Capacitor
When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

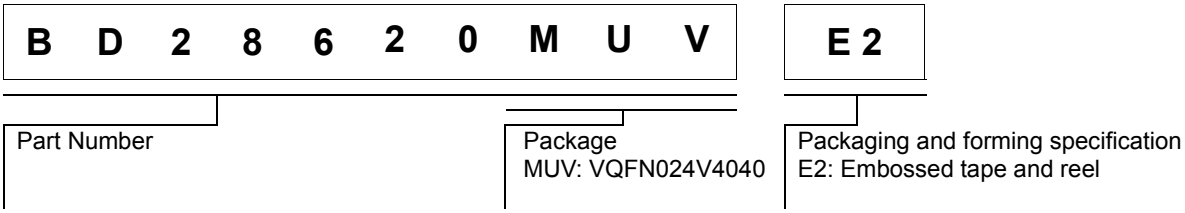
14. Area of Safe Operation (ASO)
Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.

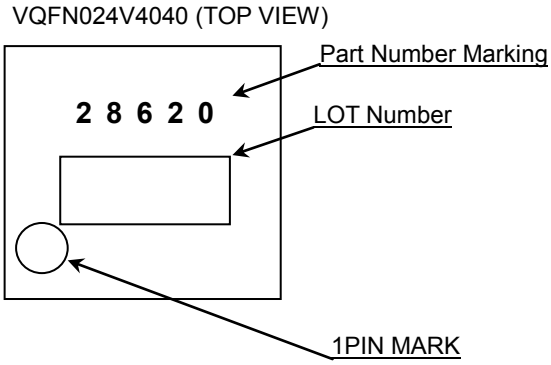
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over-Current Protection Circuit (OCP)
This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

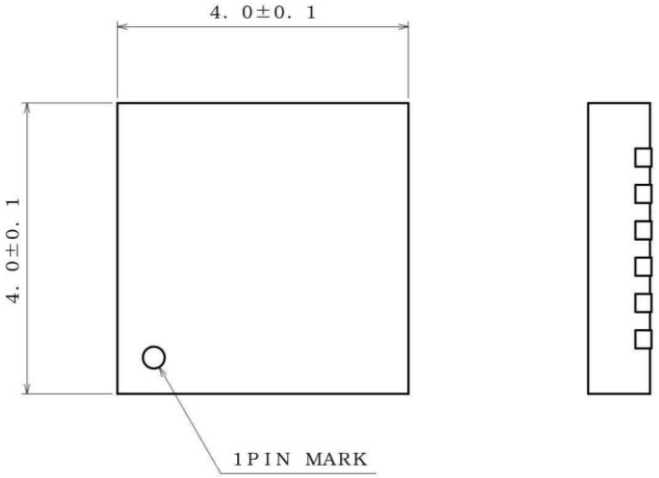


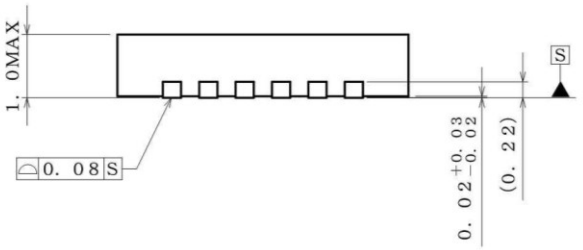
Marking Diagram

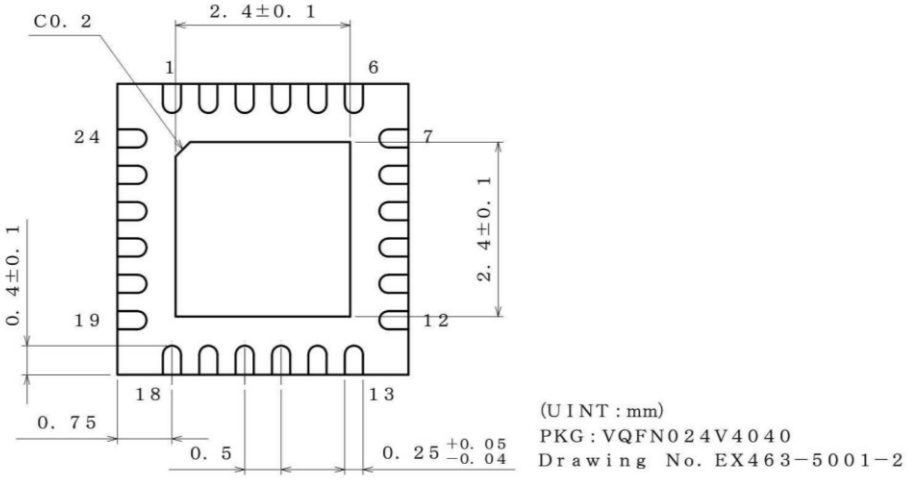


Physical Dimension, Tape and Reel Information

Package Name	VQFN024V4040

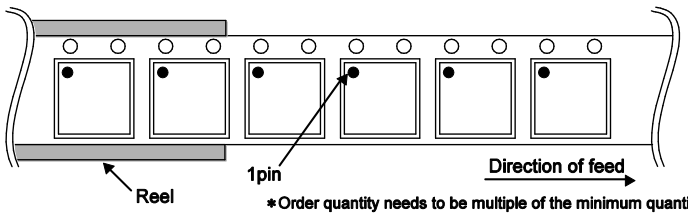






<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
2014/03/05	001	First version
2014/07/23	002	Modification of Minimum Load Impedance Function name changing ; Power limit function → Variable gain function Addition of MCLK Frequency spec. Addition of Output Short Protection Min. Value. Addition of Typical Performance Curves. (R_L=4.8Ω Condition)
2014/08/27	003	Power Supply Start-up Sequence ; Addition of caution. Power Supply Shutdown Sequence ; Addition of caution. About the Protection Function ; Addition of note.
2015/03/16	004	Electrical Characteristics ; Addition of TYP value of Maximum Output Power 2 and 3. Typical Performance Curves ; Modification of the condition. Addition of LRCLK and BCLK Frequency spec.

Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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