19-2083; Rev 0; 8/01

EVALUATION KIT AVAILABLE

16-Bit ADC, 200ksps, 5V Single-Supply with Reference

MAX1132/MAX1133

General Description

The MAX1132/MAX1133 are 200ksps, 16-bit ADCs. These serially interfaced ADCs connect directly to SPI™, QSPI™, and MICROWIRE™ devices without external logic. They combine an input scaling network, internal track/hold, clock, a +4.096V reference, and three general-purpose digital output pins (for external multiplexer or PGA control) in a 20-pin SSOP package. The excellent dynamic performance (SINAD ≥ 85dB), high-speed (200ksps), and low power (7.5mA) of these ADCs, make them ideal for applications such as industrial process control, instrumentation, and medical applications. The MAX1132 accepts input signals of 0 to +12V (unipolar) or ±12V (bipolar), while the MAX1133 accepts input signals of 0 to +4.096V (unipolar) or ±4.096V (bipolar). Operating from a single +4.75V to +5.25V analog supply and a +4.75V to +5.25V digital supply, power-down modes reduce current consumption to 1mA at 10ksps and further reduce supply current to less than 20µA at slower data rates. A serial strobe output (SSTRB) allows direct connection to the TMS320 family of digital signal processors. The MAX1132/MAX1133 user can select either the internal clock, or an external serial-interface clock for the ADC to perform analog-to-digital conversions.

The MAX1132/MAX1133 feature internal calibration circuitry to correct linearity and offset errors. On-demand calibration allows the user to optimize performance. Three user-programmable logic outputs are provided for the control of an 8-channel mux or a PGA.

Applications

Industrial Process Control

Industrial I/O Modules

Data-Acquisition Systems

Medical Instruments

Portable and Battery-Powered Equipment

Functional Diagram appears at end of data sheet.
Typical Application Circuit appears at end of data sheet.

SPI and QSPI are trademarks of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corp.

Features

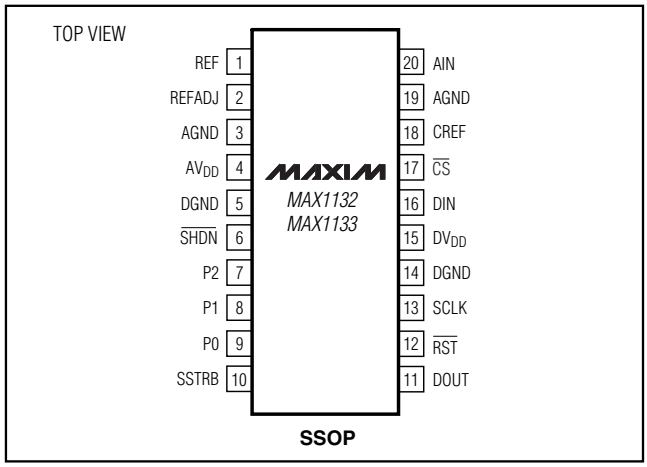
- **200ksps (Bipolar) and 150ksps (Unipolar) Sampling ADC**
- **16-Bits, No Missing Codes**
- **1.5LSB INL Guaranteed**
- **85dB (min) SINAD**
- **+5V Single-Supply Operation**
- **Low-Power Operation, 7.5mA (Unipolar Mode)**
- **2.5µA Shutdown Mode**
- **Software-Configurable Unipolar and Bipolar Input Ranges**
  - **0 to +12V and ±12V (MAX1132)**
  - **0 to +4.096V and ±4.096V (MAX1133)**
  - **Internal or External Reference**
- **Internal or External Clock**
- **SPI/QSPI/MICROWIRE-Compatible Serial Interface**
- **Three User-Programmable Logic Outputs**
- **Small 20-Pin SSOP Package**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX1132ACAP*	0°C to +70°C	20 SSOP	±1.5
MAX1132BCAP	0°C to +70°C	20 SSOP	±2.5

Ordering Information continued at end of data sheet.

Pin Configuration



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

16-Bit ADC, 200ksps, 5V Single-Supply with Reference

ABSOLUTE MAXIMUM RATINGS

AV_{DD} to AGND, DV_{DD} to DGND .....-0.3V to +6V
AGND to DGND.....-0.3V to +0.3V
AIN to AGND.....±16.5V
REFADJ, CREF, REF to AGND.....-0.3V to (AV_{DD} + 0.3V)
Digital Inputs to DGND.....-0.3V to +6V
Digital Outputs to DGND .....-0.3V to (DV_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
20-Pin SSOP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges
MAX113_CAP .....0°C to +70°C
MAX113_EAP.....-40°C to +85°C
Storage Temperature Range .....-60°C to +150°C
Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = DV_{DD} = +5V ±5%, f_{SCLK} = 4.8MHz, external clock (50% duty cycle), 24 clocks/conversion (200ksps), bipolar input, external V_{REF} = +4.096V, V_{REFADJ} = AV_{DD}, C_{REF} = 2.2µF, C_{CREF} = 1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)							
Resolution				16			Bits
Relative Accuracy (Note 2)	INL	Bipolar mode	MAX113_A			±1.5	LSB
			MAX113_B			±2.5	
No Missing Codes				16			Bits
Differential Nonlinearity	DNL	Bipolar mode	MAX113_A	-1		+1	LSB
			MAX113_B	-1		+1.75	
Transition Noise					0.77		LSB_{RMS}
Offset Error		Unipolar	MAX1132			±4	mV
			MAX1133			±2	
		Bipolar	MAX1132			±6	
			MAX1133			±5	
Gain Error (Note 3)		Unipolar				±0.2	%FSR
		Bipolar				±0.3	
Offset Drift (Bipolar and Unipolar)		Excluding reference drift			±1		ppm/°C
Gain Drift (Bipolar and Unipolar)		Excluding reference drift			±1		ppm/°C
DYNAMIC SPECIFICATIONS (5kHz sine-wave input, 200ksps, 4.8MHz clock, bipolar input mode. MAX1132: 24Vp-p. MAX1133: 8.192Vp-p)							
SINAD		f_{IN} = 5kHz		85			dB
		f_{IN} = 100kHz			85		
SNR		f_{IN} = 5kHz		87			dB
		f_{IN} = 100kHz			92		
THD		f_{IN} = 5kHz				-90	dB
		f_{IN} = 100kHz			-92		
SFDR		f_{IN} = 5kHz		92			dB
		f_{IN} = 100kHz			96		

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = +5V ±5%, f_{SCLK} = 4.8MHz, external clock (50% duty cycle), 24 clocks/conversion (200ksps), bipolar input, external V_{REF} = +4.096V, V_{REFADJ} = AV_{DD}, C_{REF} = 2.2µF, C_{CREF} = 1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG INPUT							
Input Range		MAX1132	Unipolar	0		12	V
			Bipolar	-12		12	
		MAX1133	Unipolar	0		4.096	
			Bipolar	-4.096		4.096	
Input Impedance		MAX1132	Unipolar	7.5	10.0		kΩ
			Bipolar	5.9	7.9		
		MAX1133	Unipolar	100	1000		
			Bipolar	3.4	4.5		
Input Capacitance					32		pF
CONVERSION RATE							
Internal Clock Frequency					4		MHz
Aperture Delay	t_{AD}				10		ns
Aperture Jitter	t_{AS}				50		ps
MODE 1 (24 External Clock Cycles per Conversion)							
External Clock Frequency	f_{SCLK}	Unipolar		0.1		3	MHz
		Bipolar		0.1		4.8	
Sample Rate	$f_S = f_{SCLK}/24$	Unipolar		4.17		125	ksps
		Bipolar		4.17		200	
Conversion Time (Note 4)	$t_{CONV+ACQ} = 24 / f_{SCLK}$	Unipolar		8		240	µs
		Bipolar		5		240	
MODE 2 (Internal Clock Mode)							
External Clock Frequency (Data Transfer Only)						8	MHz
Conversion Time		SSTRB low pulse width			4	6	µs
Acquisition Time		Unipolar		1.82			µs
		Bipolar		1.14			
MODE 3 (32 External Clock Cycles per Conversion)							
External Clock Frequency	f_{SCLK}	Unipolar or bipolar		0.1		4.8	MHz
Sample Rate	$f_S = f_{SCLK}/32$	Unipolar or bipolar		3.125		150	ksps
Conversion Time (Note 4)	$t_{CONV+ACQ} = 32 / f_{SCLK}$	Unipolar or bipolar		6.67		320	µs
INTERNAL REFERENCE							
Output Voltage	V_{REF}			4.056	4.096	4.136	V
REF Short-Circuit Current					24		mA
Output Tempco					±20		ppm/°C

16-Bit ADC, 200ksps, 5V Single-Supply with Reference

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = +5V ±5%, f_{SCLK} = 4.8MHz, external clock (50% duty cycle), 24 clocks/conversion (200ksps), bipolar input, external V_{REF} = +4.096V, V_{REFADJ} = AV_{DD}, C_{REF} = 2.2µF, C_{CREF} = 1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Capacitive Bypass at REF			0.47		10	µF
Maximum Capacitive Bypass at REFADJ				10		µF
REFADJ Output Voltage				4.096		V
REFADJ Input Range		For small adjustments from 4.096V		±100		mV
REFADJ Buffer Disable Threshold		To power-down the internal reference	AV_{DD} - 0.5V		AV_{DD} - 0.1V	V
Buffer Voltage Gain				1		V/V
EXTERNAL REFERENCE (Reference buffer disabled. Reference applied to REF)						
Input Range (Notes 5 and 6)			3.0	4.096	4.2	V
Input Current		V_{REF} = 4.096V, f_{SCLK} = 4.8MHz		250		µA
		V_{REF} = 4.096V, f_{SCLK} = 0		230		
		In power-down, f_{SCLK} = 0		0.1		
DIGITAL INPUTS						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Leakage	I_{IN}	V_{IN} = 0 or DV_{DD}			±1	µA
Input Hysteresis	V_{HYST}			0.2		V
Input Capacitance	C_{IN}			10		pF
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	I_{SOURCE} = 0.5mA	DV_{DD} - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 5mA			0.4	V
		I_{SINK} = 16mA			0.8	
Three-State Leakage Current	I_L	$\overline{CS}$ = DV_{DD}			±10	µA
Three-State Output Capacitance		$\overline{CS}$ = DV_{DD}		10		pF
POWER SUPPLIES						
Analog Supply (Note 7)	AV_{DD}		4.75	5	5.25	V
Digital Supply (Note 7)	DV_{DD}		4.75	5	5.25	V
Analog Supply Current	I_{ANALOG}	Unipolar mode		5	8	mA
		Bipolar mode		8.5	11	
		$\overline{SHDN}$ = 0, or software power-down mode		0.3	10	µA
Digital Supply Current	$I_{DIGITAL}$	Unipolar or bipolar mode		2.5	3.5	mA
		$\overline{SHDN}$ = 0, or software power-down mode		2.2	10	µA
Power-Supply Rejection Ratio (Note 8)	PSRR	AV_{DD} = DV_{DD} = 4.75V to 5.25V		72		dB

TIMING CHARACTERISTICS (Figures 5 and 6)

(AV_{DD} = DV_{DD} = +5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Acquisition Time	t_{ACQ}		1.14			µs
DIN to SCLK Setup	t_{DS}		50			ns
DIN to SCLK Hold	t_{DH}				0	ns
SCLK to DOUT Valid	t_{DO}				70	ns
$\overline{CS}$ Fall to DOUT Enable	t_{DV}	C_{LOAD} = 50pF			80	ns
$\overline{CS}$ Rise to DOUT Disable	t_{TR}	C_{LOAD} = 50pF			80	ns
$\overline{CS}$ to SCLK Rise Setup	t_{CSS}		100			ns
$\overline{CS}$ to SCLK Rise Hold	t_{CSH}		0			ns
SCLK High Pulse Width	t_{CH}		80			ns
SCLK Low Pulse Width	t_{CL}		80			ns
SCLK Fall to SSTRB	t_{SSTRB}	C_{LOAD} = 50pF			80	ns
$\overline{CS}$ Fall to SSTRB Enable	t_{SDV}	C_{LOAD} = 50pF, external clock mode			80	ns
$\overline{CS}$ Rise to SSTRB Disable	t_{STR}	C_{LOAD} = 50pF, external clock mode			80	ns
SSTRB Rise to SCLK Rise	t_{SCK}	Internal clock mode	0			ns
$\overline{RST}$ Pulse Width	t_{RS}		208			ns

Note 1: Tested at AV_{DD} = DV_{DD} = +5V, bipolar input mode.
Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the gain error and offset error have been nulled.
Note 3: Offset nulled.
Note 4: Conversion time is defined as the number of clock cycles multiplied by the clock period, clock has 50% duty cycle. Includes the acquisition time.
Note 5: ADC performance is limited by the converter's noise floor, typically 300µVp-p.
Note 6: When an external reference has a different voltage than the specified typical value, the full scale of the ADC will scale proportionally.
Note 7: Electrical characteristics are guaranteed from $AV_{DD(MIN)}$ = $DV_{DD(MIN)}$ to $AV_{DD(MAX)}$ = $DV_{DD(MAX)}$. For operations beyond this range, see the *Typical Operating Characteristics*. For guaranteed specifications beyond the limits, contact the factory.
Note 8: Defined as the change in positive full scale caused by a ±5% variation in the nominal supply voltage.

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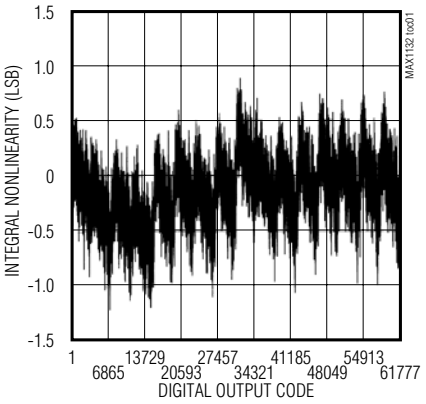
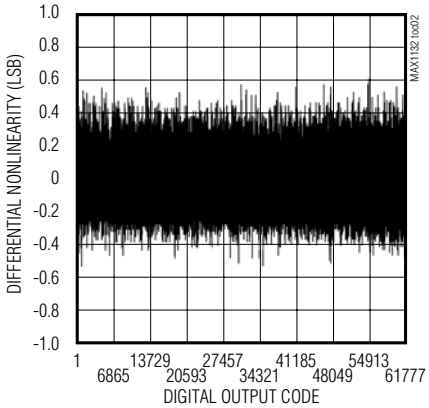
Typical Operating Characteristics

(MAX1132/MAX1133: AV_{DD} = DV_{DD} = +5V , f_{SCLK} = 4.8MHz, external clock (50% duty cycle), 24 clocks/conversion (200ksps), bipolar input, external REF = +4.096V, 0.22µF bypassing on REFADJ, 2.2µF on REF, 1µF on CREF, T_A = 25°C, unless otherwise noted.)

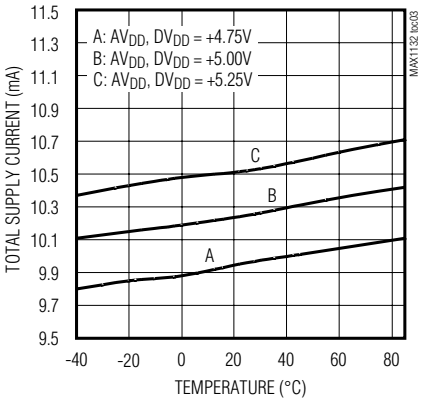
INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE



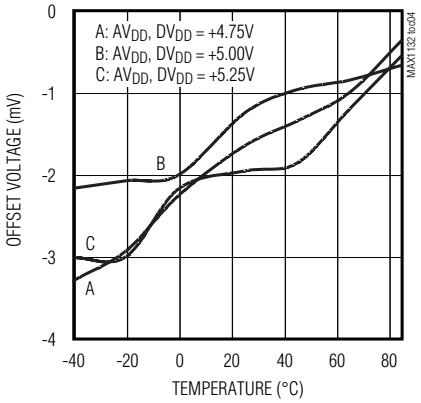
DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE



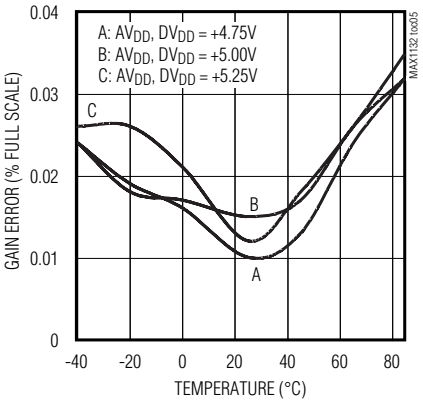
TOTAL SUPPLY CURRENT vs. TEMPERATURE



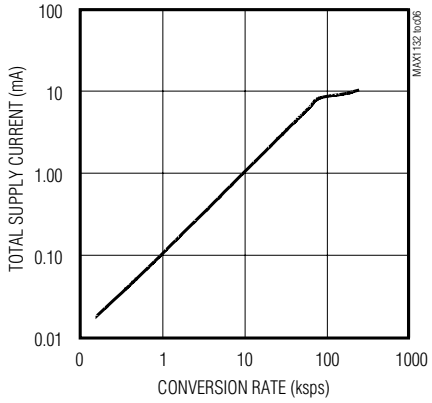
OFFSET VOLTAGE vs. TEMPERATURE



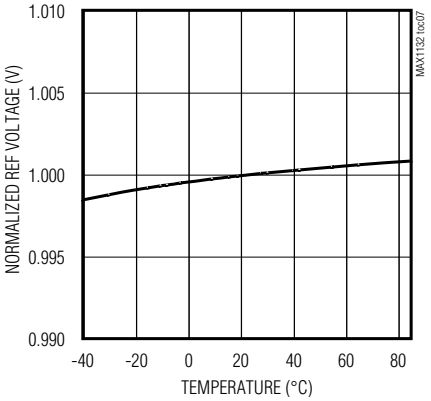
GAIN ERROR vs. TEMPERATURE



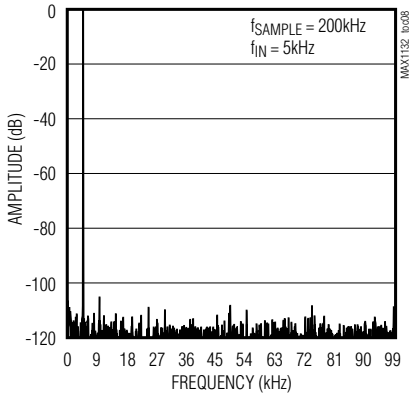
TOTAL SUPPLY CURRENT vs. CONVERSION RATE (USING SHUTDOWN)



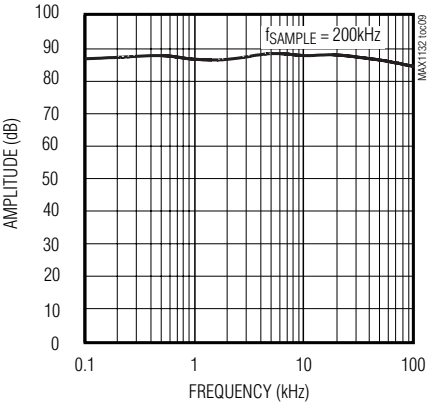
NORMALIZED REF VOLTAGE vs. TEMPERATURE



FFT PLOT

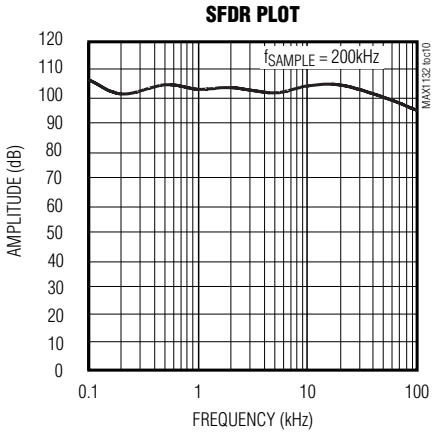


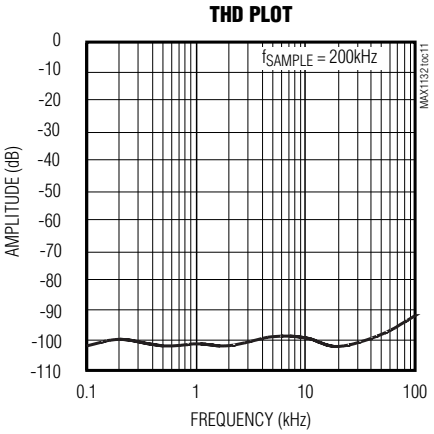
SINAD PLOT



Typical Operating Characteristics (continued)

(MAX1132/MAX1133: AV_{DD} = DV_{DD} = +5V , f_{SCLK} = 4.8MHz, external clock (50% duty cycle), 24 clocks/conversion (200ksps), bipolar input, external REF = +4.096V, 0.22µF bypassing on REFADJ, 2.2µF on REF, 1µF on CREF, T_A = 25°C, unless otherwise noted.)





Pin Description

PIN	NAME	FUNCTION
1	REF	Reference Buffer Output/ADC Reference Input. Reference voltage for analog-to-digital conversion. In internal reference mode, the reference buffer provides a +4.096V nominal output, externally adjustable at REFADJ. In external reference mode, disable the internal buffer by pulling REFADJ to AV_{DD}. Bypass to AGND with a 2.2µF capacitor when using the internal reference.
2	REFADJ	Bandgap Reference Output/Bandgap Reference Buffer Input. Bypass to AGND with 0.22µF. When using an external reference, connect REFADJ to AV_{DD} to disable the internal bandgap reference.
3	AGND	Analog Ground. This is the primary analog ground (Star Ground).
4	AV_{DD}	Analog Supply. 5V ±5%. Bypass AV_{DD} to AGND (pin 3) with a 0.1µF capacitor.
5	DGND	Digital Ground
6	$\overline{SHDN}$	Shutdown Control Input. Drive $\overline{SHDN}$ low to put the ADC in shutdown mode.
7	P2	User-Programmable Output 2
8	P1	User-Programmable Output 1
9	P0	User-Programmable Output 0
10	SSTRB	Serial Strobe Output. In internal clock mode, SSTRB goes low when the ADC begins a conversion and goes high when the conversion is finished. In external clock mode, SSTRB pulses high for one clock period before the MSB decision. It is high impedance when $\overline{CS}$ is high in external clock mode.
11	DOUT	Serial Data Output. MSB first, straight binary format for unipolar input, two's complement for bipolar input. Each bit is clocked out of DOUT at the falling edge of SCLK.
12	$\overline{RST}$	Reset Input. Drive $\overline{RST}$ low to put the device in the power-on default mode. See the *Power-On Reset* section.

16-Bit ADC, 200ksps, 5V Single-Supply with Reference

Pin Description (continued)

PIN	NAME	FUNCTION
13	SCLK	Serial Data Clock Input. Serial data on DIN is loaded on the rising edge of SCLK, and serial data is updated on DOUT on the falling edge of SCLK. In external clock mode, SCLK sets the conversion speed.
14	DGND	Digital Ground. Connect to pin 5.
15	DV_{DD}	Digital Supply. 5V ±5%. Bypass DV_{DD} to DGND (pin 14) with a 0.1µF capacitor.
16	DIN	Serial Data Input. Serial data on DIN is latched on the rising edge of SCLK.
17	$\overline{CS}$	Chip-Select Input. Drive $\overline{CS}$ low to enable the serial interface. When $\overline{CS}$ is high, DOUT is high impedance. In external clock mode, SSTRB is high impedance when $\overline{CS}$ is high.
18	CREF	Reference Buffer Bypass. Bypass CREF to AGND (pin 3) with 1µF.
19	AGND	Analog Ground. Connect pin 19 to pin 3.
20	AIN	Analog Input

Detailed Description

The MAX1132/MAX1133 analog-to-digital converters (ADCs) use a successive-approximation technique and input track/hold (T/H) circuitry to convert an analog signal to a 16-bit digital output. The MAX1132/MAX1133 easily interfaces to microprocessors (µPs). The data bits can be read either during the conversion in external clock mode or after the conversion in internal clock mode.

In addition to a 16-bit ADC, the MAX1132/MAX1133 include an input scaler, an internal digital microcontroller, calibration circuitry, an internal clock generator, and an internal bandgap reference. The input scaler for the MAX1132 enables conversion of input signals ranging from 0 to +12V (unipolar input) or ±12V (bipolar input). The MAX1133 accepts 0 to +4.096V (unipolar input) or ±4.096V (bipolar input). Input range selection is software controlled.

Calibration

To minimize linearity, offset, and gain errors, the MAX1132/MAX1133 have on-demand software calibration. Initiate calibration by writing a Control-Byte with bit M1 = 0, and bit M0 = 1 (see Table 1). Select internal or external clock for calibration by setting the INT/$\overline{EXT}$ bit in the Control Byte. Calibrate the MAX1132/MAX1133 with the clock used for performing conversions.

Offsets resulting from synchronous noise (such as the conversion clock) are canceled by the MAX1132/MAX1133's calibration circuitry. However, because the magnitude of the offset produced by a synchronous signal depends on the signal's shape, recalibration may be appropriate if the shape or relative timing of the clock or other digital signals change, as might occur if more than one clock signal or frequency is used.

Input Scaler

The MAX1132/MAX1133 have an input scaler which allows conversion of true bipolar input voltages while operating from a single +5V supply. The input scaler attenuates and shifts the input as necessary to map the external input range to the input range of the internal DAC. The MAX1132 analog input range is 0 to +12V (unipolar) or ±12V (bipolar). The MAX1133 analog input range is 0 to +4.096V (unipolar) or ±4.096V (bipolar). Unipolar and bipolar mode selection is configured with bit 6 of the serial Control Byte.

Figure 1 shows the equivalent input circuit of the MAX1132/MAX1133. The resistor network on the analog input provides ±16.5V fault protection. This circuit limits the current going into or out of the pin to less than 2mA. The overvoltage protection is active, even if the device is in a power-down mode, or if AV_{DD} = 0.

Digital Interface

The digital interface pins consist of $\overline{SHDN}$, $\overline{RST}$, SSTRB, DOUT, SCLK, DIN and $\overline{CS}$. Bringing $\overline{SHDN}$ low, places the MAX1132/MAX1133 in its 2.5µA shutdown mode. A logic low on $\overline{RST}$ halts the MAX1132/MAX1133 operation and returns the part to its power-on reset state.

In external clock mode, SSTRB is is low and pulses high for one clock cycle at the start of conversion. In internal clock mode, SSTRB goes low at the start of the conversion and goes high to indicate the conversion is finished.

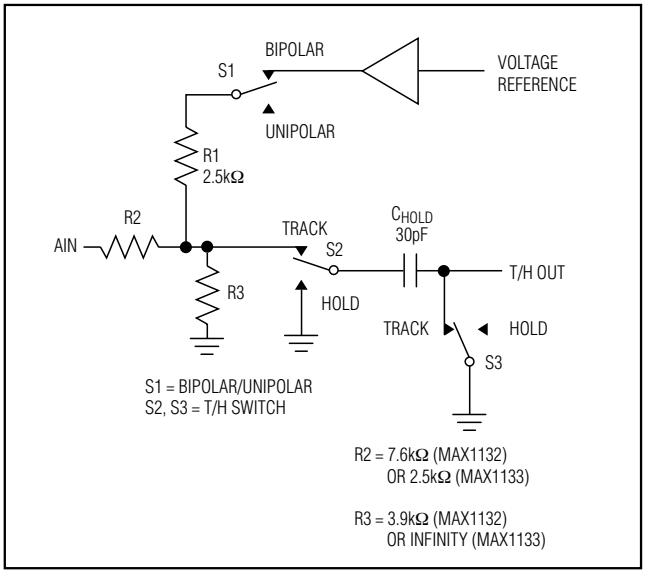


Figure 1. Equivalent Input Circuit

The DIN input accepts Control Byte data which is clocked in on each rising edge of SCLK. After $\overline{CS}$ goes low or after a conversion or calibration completes, the first logic "1" clocked into DIN is interpreted as the START bit, the MSB of the 8-bit Control Byte.

The SCLK input is the serial data transfer clock which clocks data in and out of the MAX1132/MAX1133. SCLK also drives the A/D conversion steps in external clock mode (see *Internal and External Clock Modes* section).

DOUT is the serial output of the conversion result. DOUT is updated on the falling edge of SCLK. DOUT is high-impedance when $\overline{CS}$ is high.

$\overline{CS}$ must be low for the MAX1132/MAX1133 to accept a Control Byte. The serial interface is disabled when $\overline{CS}$ is high.

User-Programmable Outputs

The MAX1132/MAX1133 have three user-programmable outputs, P0, P1 and P2. The power-on default state for the programmable outputs is zero. These are push-pull CMOS outputs suitable for driving a multiplexer, a PGA, or other signal preconditioning circuitry. The user-programmable outputs are controlled by bits 0, 1, and 2 of the Control Byte (Table 2).

The user-programmable outputs are set to zero during power-on reset (POR) or when $\overline{RST}$ goes low. During hardware or software shutdown P0, P1, and P2 are unchanged and remain low-impedance.

Starting a Conversion

Start a conversion by clocking a Control Byte into the device's internal shift register. With $\overline{CS}$ low, each rising edge on SCLK clocks a bit from DIN into the MAX1132/MAX1133's internal shift register. After $\overline{CS}$ goes low or after a conversion or calibration completes, the first arriving logic "1" is defined as the start bit of the Control Byte. Until this first start bit arrives, any number of logic "0" bits can be clocked into DIN with no effect. If at any time during acquisition or conversion, $\overline{CS}$ is brought high and then low again, the part is placed into a state where it can recognize a new start bit. If a new start bit occurs before the current conversion is complete, the conversion is aborted and a new acquisition is initiated.

Internal and External Clock Modes

The MAX1132/MAX1133 may use either the external serial clock or the internal clock to perform the successive-approximation conversion. In both clock modes, the external clock shifts data in and out of the MAX1132/MAX1133. Bit 5 (INT/$\overline{EXT}$) of the Control Byte programs the clock mode.

External Clock

In external clock mode, the external clock not only shifts data in and out, but it also drives the ADC conversion steps. In short acquisition mode, SSTRB pulses high for one clock period after the seventh falling edge of SCLK following the start bit. The MSB of the conversion is available at DOUT on the eighth falling edge of SCLK (Figure 2).

In long acquisition mode, when using external clock, SSTRB pulses high for one clock period after the fifteenth falling edge of SCLK following the start bit. The MSB of the conversion is available at DOUT on the sixteenth falling edge of SCLK (Figure 3).

In external clock mode, SSTRB is high-impedance when $\overline{CS}$ is high. In external clock mode, $\overline{CS}$ is normally held low during the entire conversion. If $\overline{CS}$ goes high during the conversion, SCLK is ignored until $\overline{CS}$ goes low. This allows external clock mode to be used with 8-bit bytes.

Internal Clock

In internal clock mode, the MAX1132/MAX1133 generates its own conversion clock. This frees the microprocessor from the burden of running the SAR conversion clock, and allows the conversion results to be read back at the processor's convenience, at any clock rate up to 8MHz.

SSTRB goes low at the start of the conversion and goes high when the conversion is complete. SSTRB will be

16-Bit ADC, 200ksps, 5V Single-Supply with Reference

Table 1. Control Byte Format

BIT	NAME	DESCRIPTION		
7 (MSB)	START	The first logic "1" bit, after $\overline{CS}$ goes low, defines the beginning of the Control Byte		
6	UNI/$\overline{BIP}$	1 = unipolar, 0 = bipolar. Selects unipolar or bipolar conversion mode. In unipolar mode, analog input signals from 0 to +12V (MAX1132) or 0 to V_{REF} (MAX1133) can be converted. In bipolar mode analog input signals from -12V to +12V (MAX1132) or -V_{REF} to +V_{REF} (MAX1133) can be converted.		
5	INT/$\overline{EXT}$	Selects the internal or external conversion clock. 1 = Internal, 0 = External.		
4	M1			
3	M0	**M1**	**M0**	**MODE**
		0	0	24 External clocks per conversion (short acquisition mode)
		0	1	Start Calibration. Starts internal calibration.
		1	0	Software power-down mode
		1	1	32 External clocks per conversion (long acquisition mode)
2 1 0(LSB)	P2 P1 P0	These three bits are stored in a port register and output to pins P2, P1, P0 for use in addressing a mux or PGA. These three bits are updated in the port register simultaneously when a new Control Byte is written.		

Table 2. User-Programmable Outputs

OUTPUT PIN	PROGRAMMED THROUGH CONTROL BYTE	POWER-ON OR $\overline{RST}$ DEFAULT	DESCRIPTION
P2	Bit 2	0	User-programmable outputs follow the state of the Control Byte's three LSBs and are updated simultaneously when a new Control Byte is written. Outputs are push-pull. In hardware and software shutdown, these outputs are unchanged and remain low-impedance.
P1	Bit 1	0	
P0	Bit 0	0	

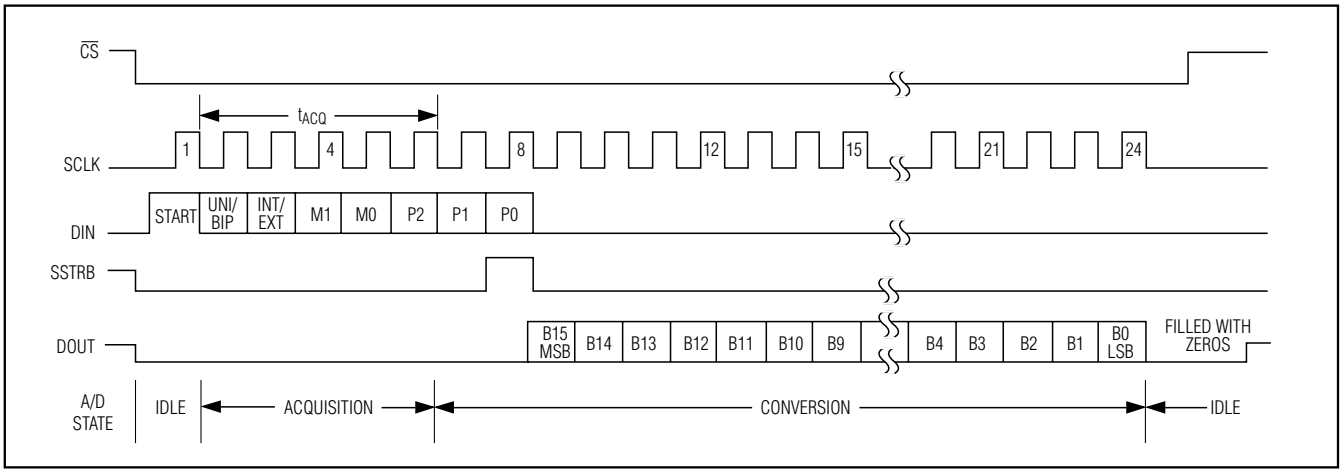


Figure 2. Short Acquisition Mode (24-Clock Cycles) External Clock, Bipolar Mode

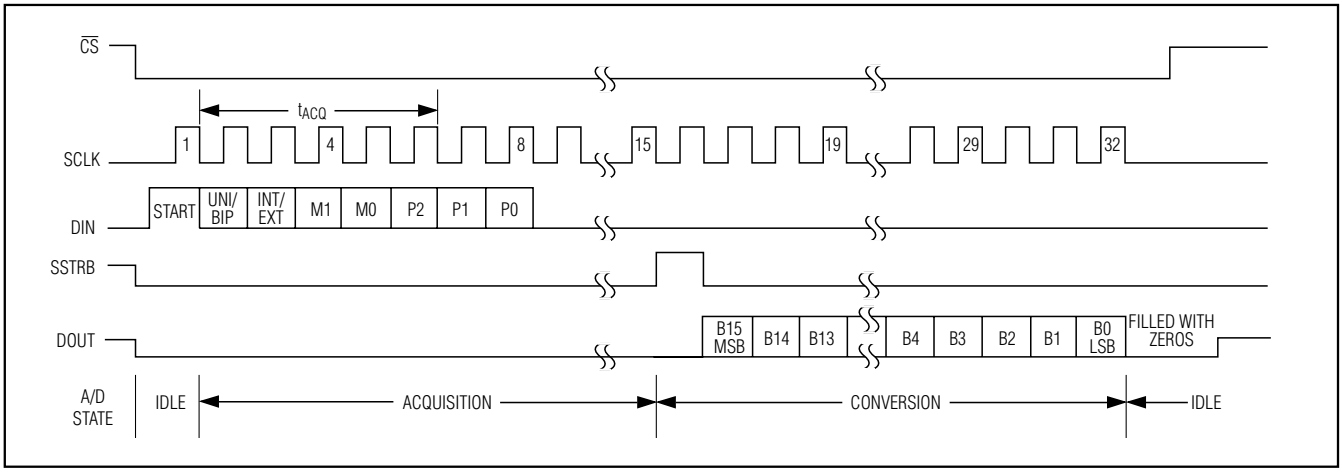


Figure 3. Long Acquisition Mode (32-Clock Cycles) External Clock, Bipolar Mode

low for a maximum of 6µs, during which time SCLK should remain low for best noise performance. An internal register stores data when the conversion is in progress. SCLK clocks the data out of the internal storage register at any time after the conversion is complete.

The MSB of the conversion is available at DOUT when SSTRB goes high. The subsequent 15 falling edges on SCLK shift the remaining bits out of the internal storage register (Figure 4). $\overline{CS}$ does not need to be held low once a conversion is started.

When internal clock mode is selected, SSTRB does not go into a high-impedance state when $\overline{CS}$ goes high. Figure 5 shows the SSTRB timing in internal clock mode. In internal clock mode, data can be shifted in to the MAX1132/MAX1133 at clock rates up to 4.8MHz, provided that the minimum acquisition time, t_{ACQ}, is kept above 1.14µs in bipolar mode and 1.82µs in unipolar mode. Data can be clocked out at 8MHz.

Output Data

The output data format is straight binary for unipolar conversions and two's complement in bipolar mode. In both modes the MSB is shifted out of the MAX1132/MAX1133 first.

Data Framing

The falling edge of $\overline{CS}$ does NOT start a conversion on the MAX1132/MAX1133. The first logic high clocked into DIN is interpreted as a start bit and defines the first bit of the Control Byte. A conversion starts on the falling edge of SCLK, after the seventh bit of the Control Byte (the P1 bit) is clocked into DIN. The start bit is defined as:

The first high bit clocked into DIN with $\overline{CS}$ low anytime the converter is idle, e.g., after AV_{DD} is applied, or as the first high bit clocked into DIN after $\overline{CS}$ is pulsed high, then low.

OR

If a falling edge on $\overline{CS}$ forces a start bit before the conversion or calibration is complete, then the current operation will be terminated and a new one started.

Applications Information

Power-On Reset

When power is first applied to the MAX1132/MAX1133 or if $\overline{RST}$ is pulsed low, the internal calibration registers are set to their default values. The user-programmable registers (P0, P1, and P2) are low, and the device is configured for bipolar mode with internal clocking.

Calibration

To compensate the MAX1132/MAX1133 for temperature drift and other variations, they should be periodically calibrated. After any change in ambient temperature more than 10°C the device should be recalibrated. A 100mV change in supply voltage or any change in the reference voltage should be followed by a calibration. Calibration corrects for errors in gain, offset, integral nonlinearity, and differential nonlinearity. The MAX1132/MAX1133 should be calibrated after power-up or the assertion of reset. Make sure the power supplies and the reference voltage have fully settled prior to initiating the calibration sequence.

Initiate calibration by setting M1 = 0 and M0 = 1 in the Control-Byte. In internal clock mode, SSTRB goes low at

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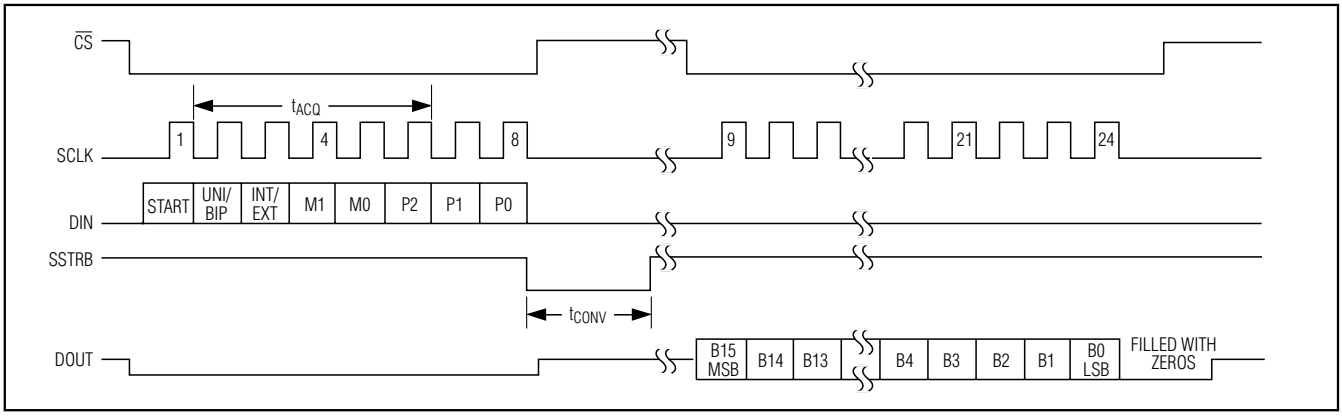

Figure 4. Internal Clock Mode Timing, Short Acquisition, Bipolar Mode

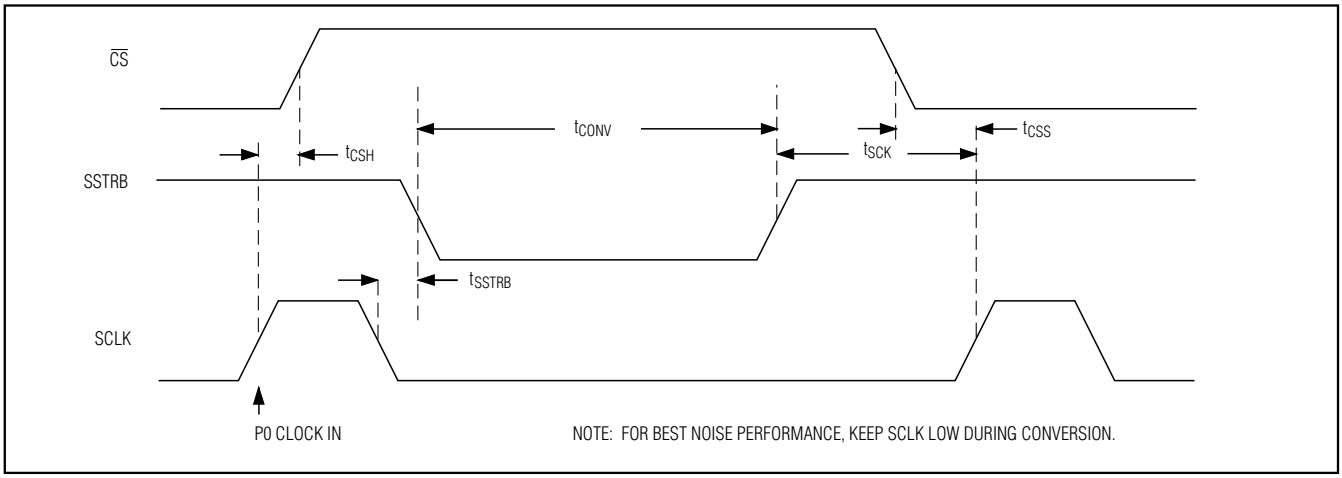

Figure 5. Internal Clock Mode SSTRB Detailed Timing

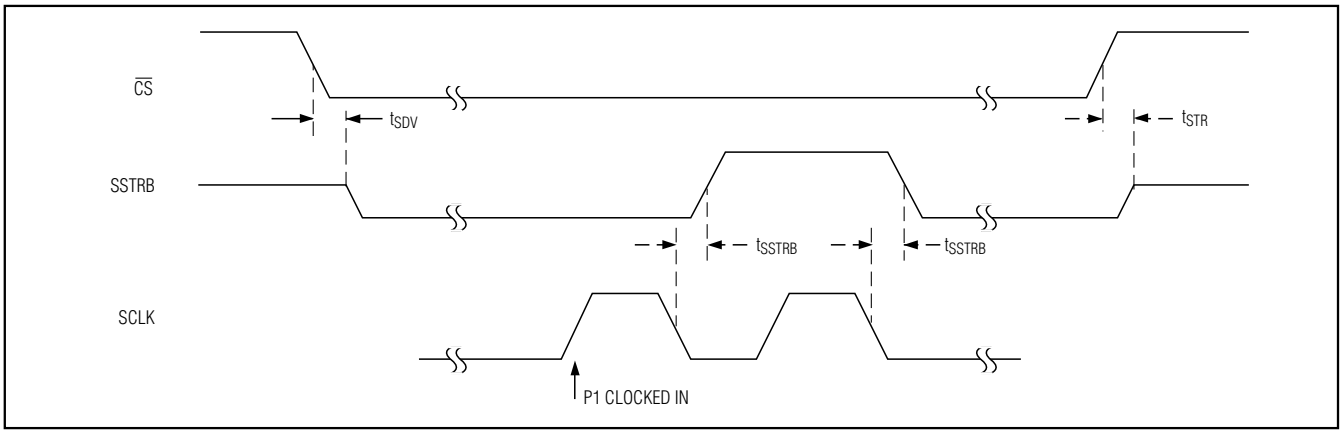

Figure 6. External Clock Mode SSTRB Detailed Timing

the beginning of calibration and goes high to signal the end of calibration, approximately 80,000 clock cycles later. In external clock mode, SSTRB goes high at the beginning of calibration and goes low to signal the end of calibration. Calibration should be performed in the same clock mode as will be used for conversions.

Reference

The MAX1132/MAX1133 can be used with an internal or external reference. An external reference can be connected directly at the REF pin or at the REFADJ pin. CREF is an internal reference node and must be bypassed with a 1µF capacitor when using either the internal or an external reference.

Internal Reference

When using the MAX1132/MAX1133's internal reference, place a 0.22µF ceramic capacitor from REFADJ to AGND and place a 2.2µF capacitor from REF to AGND. Fine adjustments can be made to the internal reference voltage by sinking or sourcing current at REFADJ. The input impedance of REFADJ is nominally 9kΩ. The internal reference voltage is adjustable to ±1.5% with the circuit of Figure 7.

External reference

An external reference can be placed at either the input (REFADJ) or the output (REF) of the MAX1132/MAX1133's internal buffer amplifier.

When connecting an external reference to REFADJ, the input impedance is typically 9kΩ. Using the buffered REFADJ input makes buffering of the external reference unnecessary, however, the internal buffer output must be bypassed at REF with a 2.2µF capacitor.

When connecting an external reference at REF, REFADJ must be connected to AV_{DD}. Then the input impedance at REF is a minimum of 164kΩ for DC currents. During conversion, an external reference at REF must deliver 250µA DC load current and have an output impedance of 10Ω or less. If the reference has a higher output impedance or is noisy, bypass it at the REF pin with a 4.7µF capacitor.

Analog Input

The MAX1132/MAX1133 use a capacitive DAC that provides an inherent track/hold function. Drive AIN with a source impedance less than 10Ω. Any signal conditioning circuitry must settle with 16-bit accuracy in less than 500ns. Limit the input bandwidth to less than half the sampling frequency to eliminate aliasing. The MAX1132/MAX1133 has a complex input impedance which varies from unipolar to bipolar mode (Figure 1).

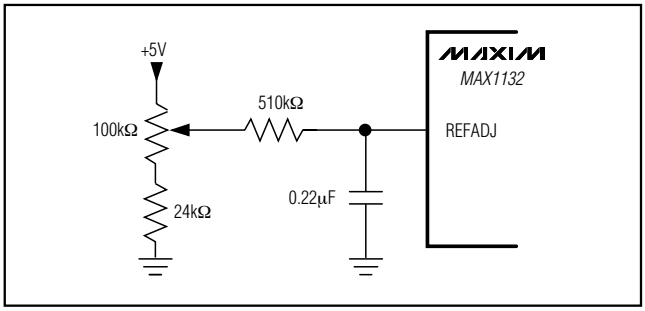

Figure 7. MAX1132 Reference-Adjust Circuit

Input Range

The analog input range in unipolar mode is 0 to +12V for the MAX1132, and 0 to +4.096V for the MAX1133. In bipolar mode, the analog input can be -12V to +12V for the MAX1132, and -4.096V to +4.096V for the MAX1133. Unipolar and bipolar mode is programmed with the UNI/$\overline{BIP}$ bit of the Control Byte. When using a reference other than the MAX1132/MAX1133's internal +4.096V reference, the full-scale input range will vary accordingly. The full-scale input range depends on the voltage at REF and the sampling mode selected (Tables 3 and 4).

Input Acquisition and Settling

Clocking in a Control Byte starts input acquisition. In bipolar mode the main capacitor array starts acquiring the input as soon as a start bit is recognized. If unipolar mode is selected by the second DIN bit, the part will immediately switch to unipolar sampling mode and acquire a sample.

Acquisition can be extended by eight clock cycles by setting M1 = 1, M0 = 1 (long acquisition mode). The sampling instant in short acquisition completes on the falling edge of the sixth clock cycle after the start bit (Figure 2).

Acquisition is 5.5 clock cycles in short acquisition mode and 13.5 clock cycles in long acquisition mode. Short acquisition mode is 24 clock cycles per conversion. Using the external clock to run the conversion process limits unipolar conversion speed to 125ksps instead of 200ksps in bipolar mode. The input resistance in unipolar mode is larger than that of bipolar mode (Figure1). The RC time constant in unipolar mode is larger than that of bipolar mode, reducing the maximum conversion rate in 24 external clock mode. Long acquisition mode with external clock allows both unipolar and bipolar sampling of 150ksps (4.8MHz/32 clock cycles) by adding eight extra clock cycles to the conversion.

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Table 3. Unipolar Full Scale and Zero Scale

PART	REFERENCE	ZERO SCALE	FULL SCALE
MAX1132	Internal	0	+12V
	External	0	+12(V_{REF}/4.096)
MAX1133	Internal	0	+4.096V
	External	0	+V_{REF}

Table 4. Bipolar Full Scale, Zero Scale, and Negative Scale

PART	REFERENCE	NEGATIVE FULL SCALE	ZERO SCALE	FULL SCALE
MAX1132	Internal	-12V	0	+12V
	External	-12(V_{REF}/4.096)	0	+12(V_{REF}/4.096)
MAX1133	Internal	-4.096V	0	+4.096V
	External	-V_{REF}	0	+V_{REF}

Most applications require an input buffer amplifier. If the input signal is multiplexed, the input channel should be switched immediately after acquistion, rather than near the end of or after a conversion. This allows more time for the input buffer amplifier to respond to a large step-change in input signal. The input amplifier must have a high enough slew-rate to complete the required output voltage change before the beginning of the acquisition time. At the beginning of acquisition, the capacitive DAC is connected to the amplifier output, causing some output disturbance. Ensure that the sampled voltage has settled to within the required limits before the end of the acquisition time. If the frequency of interest is low, AIN can be bypassed with a large enough capacitor to charge the capacitive DAC with very little change in voltage. However, for AC use, AIN must be driven by a wideband buffer (at least 10MHz), which must be stable with the DACs capacitive load (in parallel with any AIN bypass capacitor used) and also settle quickly (Figures 8 or 9).

Digital Noise

Digital noise can couple to AIN and REF. The conversion clock (SCLK) and other digital signals that are active during input acquisition contribute noise to the conversion result. If the noise signal is synchronous to the sampling interval, an effective input offset is produced. Asynchronous signals produce random noise on the input, whose high-frequency components may be aliased into the frequency band of interest. Minimize noise by presenting a low impedance (at the frequencies contained in the noise signal) at the inputs. This requires bypassing AIN to AGND, or buffering the input with an amplifier that has a small-signal bandwidth of several MHz, or preferably both. AIN has a bandwidth of about 4MHz.

Offsets resulting from synchronous noise (such as the conversion clock) are canceled by the MAX1132/MAX1133's calibration scheme. The magnitude of the offset produced by a synchronous signal depends on the signal's shape. Recalibration may be appropriate if the shape or relative timing of the clock or other digital signals change, as might occur if more than one clock signal or frequency is used.

Distortion

Avoid degrading dynamic performance by choosing an amplifier with distortion much less than the MAX1132/MAX1133's THD (-90dB) at frequencies of interest. If the chosen amplifier has insufficient common-mode rejection, which results in degraded THD performance, use the inverting configuration to eliminate errors from common-mode voltage. Low temperature-coefficient resistors reduce linearity errors caused by resistance changes due to self-heating. To reduce linearity errors due to finite amplifier gain, use an amplifier circuit with sufficient loop gain at the frequencies of interest.

DC Accuracy

If DC accuracy is important, choose a buffer with an offset much less than the MAX1132/MAX1133's maximum offset (±6mV), or whose offset can be trimmed while maintaining good stability over the required temperature range.

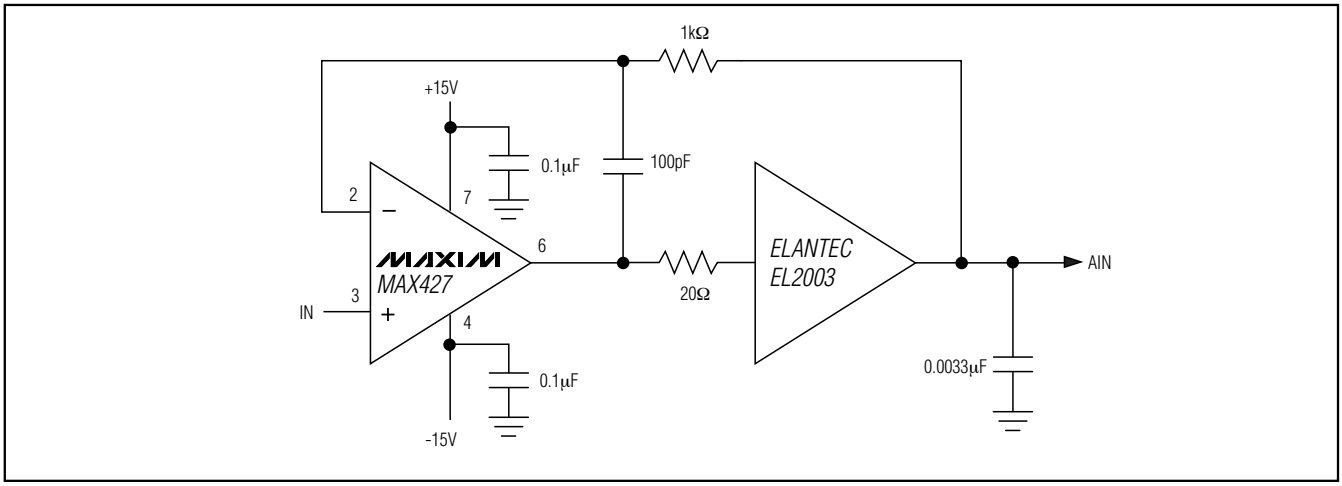


Figure 8. AIN Buffer for AC/DC Use

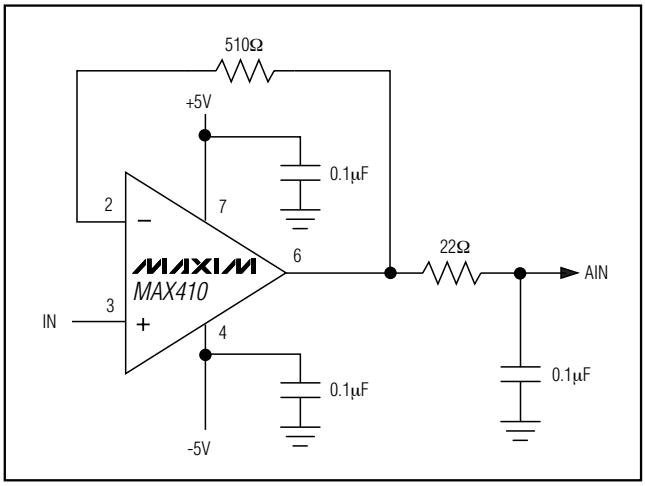


Figure 9. ±5V Buffer for AC/DC Use Has ±3.5V Swing

Operating Modes and Serial Interfaces

The MAX1132/MAX1133 are fully compatible with MICROWIRE and SPI/QSPI devices. MICROWIRE and SPI/QSPI both transmit a byte and receive a byte at the same time. The simplest software interface requires only three 8-bit transfers to perform a conversion (one 8-bit transfer to configure the ADC, and two more 8-bit transfers to clock out the 16-bit conversion result).

Short Acquisition Mode (24 SCLK)

Configure short acquisition by setting M1 = 0 and M0 = 0. In short acquisition mode, the acquisition time is 5.5 clock cycles. The total period is 24 clock cycles per conversion.

Mode 2 Long Acquisition Mode (32 SCLK)

Configure long acquisition by setting M1 = 1 and M0 = 1. In long acquisition mode, the acquisition time is 13.5 clock cycles. The total period is 32 clock cycles per conversion.

Calibration Mode

A calibration is initiated through the serial interface by setting M1 = 0, M0 = 1. Calibration can be done in either internal or external clock mode, though it is desirable that the part be calibrated in the same mode in which it will be used to do conversions. The part will remain in calibration mode for approximately 80,000 clock cycles unless the calibration is aborted. Calibration is halted if $\overline{RST}$ or $\overline{SHDN}$ goes low, or if a valid start condition occurs.

Software Shutdown

A software power-down is initiated by setting M1 = 1, M0 = 0. After the conversion completes, the part shuts down. It reawakens upon receiving a new start bit. Conversions initiated with M1 = 1 and M0 = 0 (shutdown) use the acquisition mode selected for the previous conversion.

Shutdown Mode

The MAX1132/MAX1133 may be shut down by pulling $\overline{SHDN}$ low or by asserting software shutdown. In addition to lowering power dissipation to 13µW, considerable power can be saved by shutting down the converter for short periods (duration will be affected by REF startup time with internal reference) between conversions. There is no need to perform a calibration after the converter has been shut down, unless the time in

shutdown is long enough that the supply voltage or ambient temperature may have changed.

Supplies, Layout, Grounding and Bypassing

For best system performance, use separate analog and digital ground planes. The two ground planes should be tied together at the MAX1132/MAX1133. Use pins 3 and 14 as the primary AGND and DGND, respectively. If the analog and digital supplies come from the same source, isolate the digital supply from the analog with a low value resistor (10Ω).

The MAX1132/MAX1133 are not sensitive to the order of AV_{DD} and DV_{DD} sequencing. Either supply can be present in the absence of the other. Do not apply an external reference voltage until after both AV_{DD} and DV_{DD} are present.

Be sure that digital return currents do not pass through the analog ground. All return current paths must be low-impedance. A 5mA current flowing through a PC board ground trace impedance of only 0.05Ω creates an error voltage of about 250µV, or about 2LSBs error with a ±4V full-scale system. The board layout should ensure as much as possible that digital and analog signal lines are kept separate. Do not run analog and digital lines parallel to one another. If you must cross one with the other, do so at right angles.

The ADC is sensitive to high-frequency noise on the AV_{DD} power supply. Bypass this supply to the analog ground plane with 0.1µF. If the main supply is not adequately bypassed, add an additional 1µF or 10µF low-ESR capacitor in parallel with the primary bypass capacitor.

Transfer Function

Figures 10 and 11 show the MAX1132/MAX1133's transfer functions. In unipolar mode, the output data is binary format and in bipolar mode it is two's complement.

Definitions

Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. INL for the MAX1132/MAX1133 is measured using the end-point method.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step-width and the ideal value of 1LSB. A DNL error specification of less than 1LSB guarantees no missing codes and a monotonic transfer function.

Aperture Jitter

Aperture jitter (t_{AJ}) is the sample-to-sample variation in the time between the samples.

Aperture Delay

Aperture delay (t_{AD}) is the time between the falling edge of the sampling clock and the instant when an actual sample is taken.

Signal-to-Noise Ratio

For a waveform perfectly reconstructed from digital samples, signal-to-noise ratio (SNR) is the ratio of full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical, minimum analog-to-digital noise is caused by quantization error only and results directly from the ADCs resolution (N bits):

$$SNR = (6.02 \times N + 1.76)dB$$

In reality, there are other noise sources besides quantization noise, including thermal noise, reference noise, clock jitter, etc. Therefore, SNR is calculated by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion

Signal-to-Noise Plus Distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to the RMS equivalent of all other ADC output signals:

$$SINAD\ (dB) = 20 \times \log (Signal_{RMS}/Noise_{RMS})$$

Effective Number of Bits

Effective number of bits (ENOB) indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADCs error consists of quantization noise only. With an input range equal to the full-scale range of the ADC, calculate the effective number of bits as follows:

$$ENOB = (SINAD - 1.76) / 6.02$$

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log \left[\sqrt{\left(V_2^2 + V_3^2 + V_4^2 + V_5^2 \right)} / V_1 \right]$$

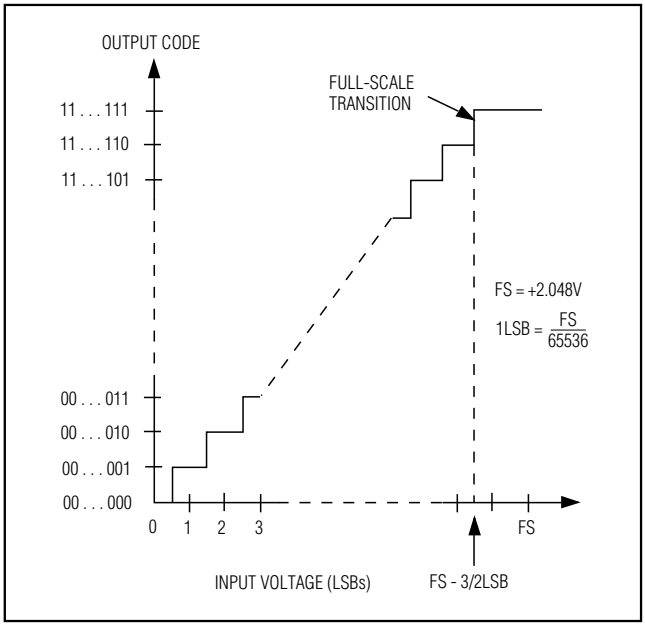


Figure 10. MAX1135 Unipolar Transfer Function, 2.048V = Full Scale

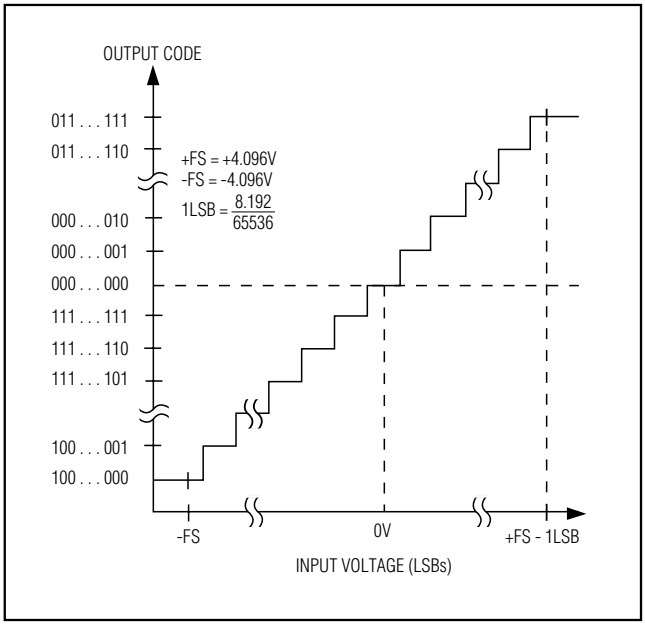


Figure 11. MAX1133 Bipolar Transfer Function, 4.096V = Full Scale

where V_1 is the fundamental amplitude, and V_2 through V_5 are the amplitudes of the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of RMS amplitude of the fundamental (maximum signal component), to the RMS value of the next largest distortion component.

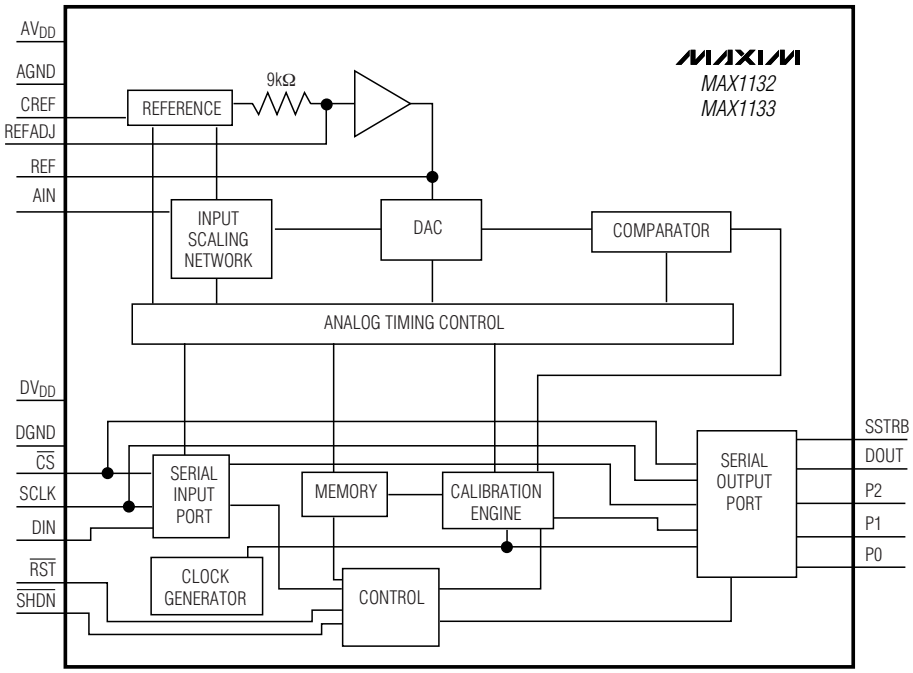
Chip Information

TRANSISTOR COUNT: 21,807

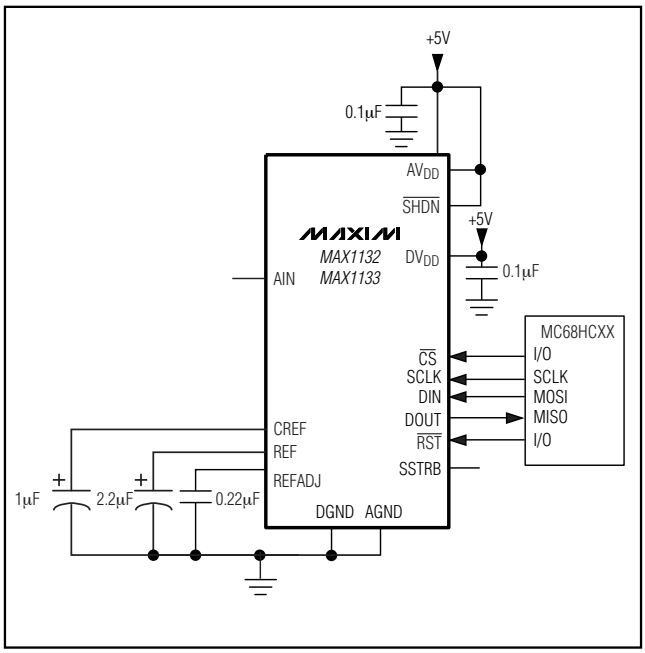
PROCESS: BiCMOS

16-Bit ADC, 200ksps, 5V Single-Supply with Reference

Functional Diagram



Typical Application Circuit



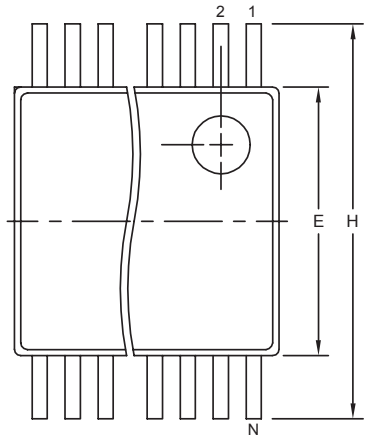
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX1132AEAP*	-40°C to +85°C	20 SSOP	±1.5
MAX1132BEAP	-40°C to +85°C	20 SSOP	±2.5
MAX1133ACAP*	0°C to +70°C	20 SSOP	±1.5
MAX1133BCAP	0°C to +70°C	20 SSOP	±2.5
MAX1133AEAP*	-40°C to +85°C	20 SSOP	±1.5
MAX1133BEAP	-40°C to +85°C	20 SSOP	±2.5

*Future product

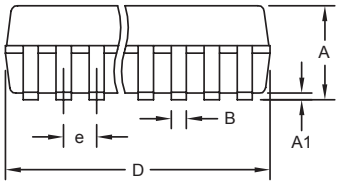
Package Information

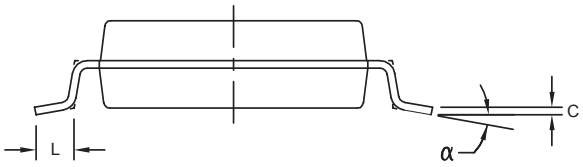
SSOP EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.212	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0∞	8∞	0∞	8∞

	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	N
D	0.239	0.249	6.07	6.33	14L
D	0.239	0.249	6.07	6.33	16L
D	0.278	0.289	7.07	7.33	20L
D	0.317	0.328	8.07	8.33	24L
D	0.397	0.407	10.07	10.33	28L





NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO150.
5. LEADS TO BE COPLANAR WITHIN 0.10 MM.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, SSOP, 5.3 MM

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	21-0056	C	1/1

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