FAIRCHILD SEMICONDUCTOR®

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FIN1049
LVDS Dual-Line Driver with Dual-Line Receiver

Features

- Greater than 400 Mbps Data Rate
- 3.3 V Power Supply Operation
- Low Power Dissipation
- Fail-Safe Protection for Open-Circuit Conditions
- Meets or Exceeds TIA/EIA-644-A LVDS Standard
- 16-pin TSSOP Package Saves Space
- Flow-Through Pinout Simplifies PCB Layout
- Enable/Disable for all Outputs
- Industrial Operating Temperature Range: -40°C to +85°C

Description

This dual driver-receiver is designed for high-speed interconnects utilizing Low Voltage Differential Signaling (LVDS) technology. The driver accepts LVTTL inputs and translates them to LVDS outputs. The receiver accepts LVDS inputs and translates them to LVTTL outputs. The LVDS levels have a typical differential output swing of 350 mV, which provides for low EMI at ultra-low power dissipation even at high frequencies. The FIN1049 can accept LVPECL inputs for translating from LVPECL to LVDS. The En and Enb inputs are AND-ed together to enable / disable the outputs. The enables are common to all four outputs. A single-line driver and single-line receiver function is also available in the FIN1019.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FIN1049MTCX	-40 to +85°C	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide	Tape and Reel

Pin Configuration

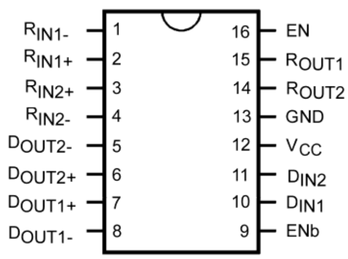


Figure 1. Pin Configuration

Functional Diagram

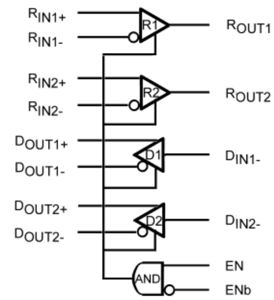


Figure 2. Functional Diagram

Pin Definitions

Pin #	Name	Description
2, 3	R_{IN1+}, R_{IN2+}	Non-Inverting LVDS Inputs
1, 4	R_{IN1-}, R_{IN2-}	Inverting LVDS Inputs
7, 6	D_{OUT1+}, D_{OUT2+}	Non-Inverting Driver Outputs
8, 5	D_{OUT1-}, D_{OUT2-}	Inverting Driver Outputs
16, 9	EN, ENb	Driver Enable Pins for All Outputs
15, 14	R_{OUT1}, R_{OUT2}	LVTTL Output Pins for R_{OUT1} and R_{OUT2}
10, 11	D_{IN1}, D_{IN2}	LVTTL Input Pins for D_{IN1} and D_{IN2}
12	V_{CC}	Power Supply (3.3 V)
13	GND	Ground

Function Table

Inputs		Outputs (LVTTL)		Inputs (LVDS)[1]		Outputs (LVDS)	
EN	**ENb**	**R_{OUT1}**	**R_{OUT2}**	**R_{INn+}**	**R_{INn-}**	**D_{OUTn+}**	**D_{OUTn-}**
H	L	ON	ON			ON	ON
H	H	Z	Z			Z	Z
L	H	Z	Z			Z	Z
L	L	Z	Z			Z	Z
H	L	H	H	Open Current Fail-Safe Condition			

Legend:

H=HIGH Logic Level

L=LOW Logic Level or OPEN

X=Don't Care

Z=High Impedance

Note:

1. Any unused receiver Inputs should be left open.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	-0.5	+4.6	V
V_{IN}	LVDS DC Input Voltage	-0.5	+4.6	V
V_{OUT}	LVDS DC Output Voltage	-0.5	+4.6	V
I_{OSD}	Driver Short-Circuit Current (Continuous)	10		mA
T_{STG}	Storage Temperature Range	-65	+150	°C
T_J	Max Junction Temperature		+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)		+260	°C
ESD	Human Body Model, JESD22-A114		≥ 7000	V
	Machine Model, JESD22-A115		≥ 250	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.6	V
$\|V_{ID}\|$	Magnitude of Differential Voltage	100	V_{CC}	mV
T_A	Operating Temperature	-40	+85	°C

DC Electrical Characteristics

Over-supply voltage and operating temperature ranges, unless otherwise specified. All typical values are at T_A=25°C and with V_{CC}=3.3 V.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
LVDS Input DC Specifications (R_{IN1+}, R_{IN1-}, R_{IN2+}, R_{IN2-}) *See Figure 3 and Table 1*						
V_{TH}	Differential Input Threshold HIGH	V_{CM}=1.2 V, 0.05 V, 2.35 V		0	35	mV
V_{TL}	Differential Input Threshold LOW		-100	0		mV
V_{IC}	Common Mode Voltage Range	V_{ID}=100 mV, V_{CC}=3.3 V	V_{ID}/2		V_{CC} - (V_{ID}/2)	V
I_{IN}	Input Current	V_{CC}=0 V or 3.6 V, V_{IN}=0 V or 2.8 V			±20	mA
CMOS/ LVTTL Input DC Specifications (EN, ENb, D_{IN1}, D_{IN2})						
V_{IH}	Input High Voltage (LVTTL)		2.0		V_{CC}	V
V_{IL}	Input Low Voltage (LVTTL)		GND		0.8	V
I_{IN}	Input Current (EN, ENb, D_{IN1}, D_{IN2}, R_{INx+}, R_{INx-})	V_{IN}=0 V or V_{CC}			±20	µA
V_{IK}	Input Clamp Voltage	V_{IK}=-18 mA	-1.5	-0.7		V
LVDS Output DC Specifications (D_{OUT1+}, D_{OUT1-}, D_{OUT2+}, D_{OUT2-})						
V_{OD}	Output Differential Voltage	*See Figure 4*	250	350	450	mV
ΔV_{OD}	V_{OD} Magnitude Change from	R_L=100 Ω			35	mV
	Differential LOW-to-HIGH	Driver Enabled				
V_{OS}	Offset Voltage	*See Figure 4*	1.125	1.250	1.375	V
ΔV_{OS}	Offset Magnitude Change from Differential LOW-to-HIGH				25	mV
I_{OS}	Short-Circuit Output Current	D_{OUT+}=0V & D_{OUT-}=0 V, Driver Enabled			-9	mA
I_{OSD}		V_{OD}=0 V, Driver Enabled			-9	mA
I_{OFF}	Power-Off Input or Output Current	V_{CC}=0 V, V_{OUT}=0 V or V_{CC}			±20	mA
I_{OZD}	Disabled Output Leakage Current	Driver Disabled, D_{OUT+}=0 V or V_{CC} or D_{OUT-}=0V or V_{CC}			±10	mA
CMOS/LVTTL Output DC Specifications (R_{OUT1}, R_{OUT2})						
V_{OH}	Output High Voltage	I_{OH}=-2 mA, V_{ID}=200 mV	2.7			V
V_{OL}	Output Low Voltage	I_{OL}=2 mA, V_{ID}=200 mV			0.25	V
I_{OZ}	Disabled Output Leakage Current	Driver Disabled, R_{OUTn}=0 V or V_{CC}			±10	mA
I_{CC}	Power Supply Current[(2)]	Drivers Enabled, Any Valid Input Condition			25	mA
I_{CCZ}	Power Supply Current	Drivers Disabled			10	mA
C_{IND}	Input Capacitance	LVDS Input		3.0		pF
C_{OUT}	Output Capacitance	LVDS Output		4.0		pF
C_{INT}	Input Capacitance	LVTTL Input		3.5		pF

Note:

2. Both driver and receiver inputs are static. All LVDS outputs have 100 Ω load. None of the outputs have any lumped capacitive load.

AC Electrical Characteristics

Over-supply voltage and operating temperature ranges, unless otherwise specified. All typical values are at T_A=25°C and with V_{CC}=3.3 V.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Switching Characteristics - LVDS Outputs						
t_{PLHD}	Differential Propagation Delay LOW-to-HIGH	*See Figure 5, Figure 6*			2	ns
t_{PHLD}	Differential Propagation Delay HIGH-to-LOW				2	ns
t_{TLHD}	Differential Output Rise Time (20% to 80%)		0.2		1.0	ns
t_{THLD}	Differential Output Fall Time (80% to 20%)		0.2		1.0	ns
$t_{SK(P)}$	Pulse Skew $\|t_{PLH} - t_{PHL}\|$				0.35	ns
$t_{SK(LH)}$, $t_{SK(HL)}$	Channel-to-Channel Skew[3]				0.35	ns
$t_{SK(PP)}$	Part-to-Part Skew[4]				1	ns
t_{PZHD}	Differential Output Enable Time, Z-to-HIGH	*See Figure 7, Figure 8*			6	ns
t_{PZLD}	Differential Output Enable Time, A-to-LOW				6	ns
t_{PHZD}	Differential Output Disable Time, HIGH-to-Z				3	ns
t_{PLZD}	Differential Output Disable Time, LOW-to-Z				3	ns
f_{MAXD}	Maximum Frequency[5]	*See Figure 5*	200			MHz
Switching Characteristics - LVTTL Outputs						
t_{PHL}	Propagation Delay HIGH-to-LOW	Measured from 20% to 80% Signal	0.5	1.0	3.5	ns
t_{PLH}	Propagation Delay LOW-to-HIGH	V_{ID}=200 mV	0.5	1.0	3.5	ns
t_{SK1}	Pulse Skew	Distributed Load	0	35	400	ps
t_{SK2}	Channel-to-Channel Skew	C_L=15 pF and 50 Ω	0	50	500	ps
t_{SK3}	Part-to-Part Skew	R_L=1 kΩ	0		1	ns
t_{LHR}	Transition Time LOW-to-HIGH	V_{OS}=1.2 V	0.10	0.25	1.40	ns
t_{HLR}	Transition Time HIGH-to-LOW	*See Figure 9, Figure 10*	0.10	0.18	1.40	ns
t_{PHZ}	Disable Time HIGH-to-Z	*See Figure 11, Figure 12*	2.2	4.5	8.0	ns
t_{PLZ}	Disable Time LOW-to-Z		1.3	3.5	8.0	ns
t_{PZH}	Enable Time Z-to-HIGH		1.8	3.0	7.0	ns
t_{PZL}	Enable Time Z-to-LOW		0.9	1.4	7.0	ns
f_{MAXT}	Maximum Frequency[6]	*See Figure 9*	200			MHz

Notes:

3. $t_{SK(LH)}$, $t_{SK(HL)}$ is the skew between specified outputs of a single device when the outputs have identical loads and are switching in the same direction.
4. $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices switching in the same direction (either LOW-to-HIGH or HIGH-to-LOW) when both devices operate with the same supply voltage, same temperature, and have identical test circuits.
5. f_{MAXD} generator input conditions: t_r=t_f < 1 ns (10% to 90%), 50% duty cycle, 0 V to 3 V. Output criteria: duty cycle=45% / 55%, V_{OD} > 250 mV, all channels switch.
6. f_{MAXT} generator input conditions: t_r=t_f < 1 ns (10% to 90%), 50% duty cycle, V_{ID}=200 mV, V_{CM}=1.2 V. Output criteria: duty cycle=45% / 55%, V_{OH} > 2.7 V. V_{OL} < 0.25 V, all channels switching.

Required Specifications and Test Diagrams

Notes:

7. Electrostatic Discharge Capability: Human Body Model and Machine Model ESD should be measured using MIL-STD-883C method 3015.7 standard.
8. Latch-up immunity should be tested to the EIA/JEDEC Standard Number 78 (EIA/JESD78).

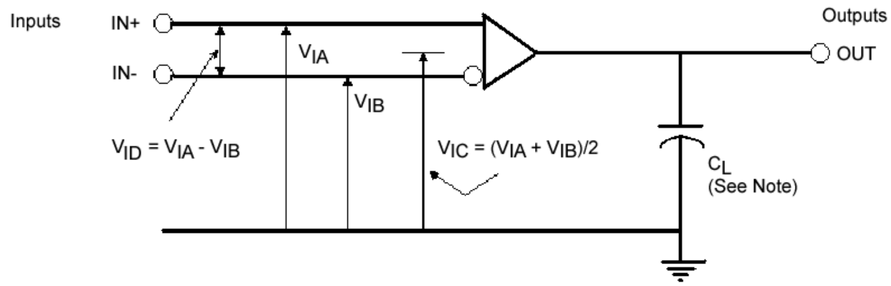


Figure 3. Differential Receiver Voltage Definitions Test Circuit

Note:

9. C_L=15 pF, includes all probe and jig capacitances.

Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages

Applied Voltages (V)		Resulting Differential Input Voltage (mV)	Resulting Common Mode Input Voltage (V)
V_{IA}	**V_{IB}**	**V_{ID}**	**V_{IC}**
1.25	1.15	100	1.2
1.15	1.25	-100	1.2
V_{CC}	V_{CC} - 0.1	100	V_{CC} - 0.05
V_{CC} - 0.1	V_{CC}	-100	V_{CC} - 0.05
0.1	0.0	100	0.05
0.0	0.1	-100	0.05
1.75	0.65	1100	1.2
0.65	1.75	-1100	1.2
V_{CC}	V_{CC} - 1.1	1100	V_{CC} - 0.55
V_{CC} - 1.1	V_{CC}	-1100	V_{CC} - 0.55
1.1	0.0	1100	0.55
0.0	1.1	-1100	0.55

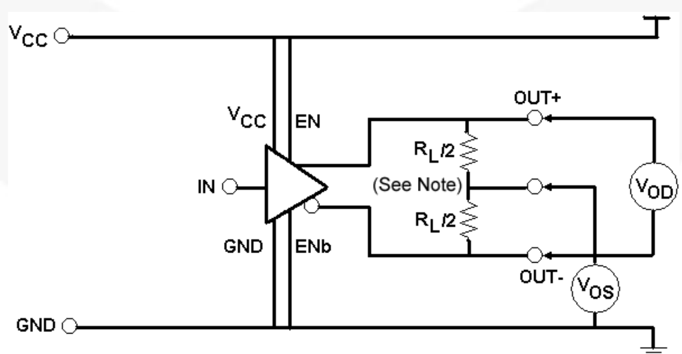


Figure 4. LVDS Output Circuit for DC Test

Note:

10. R_L=100 Ω.

Required Specifications and Test Diagrams (Continued)

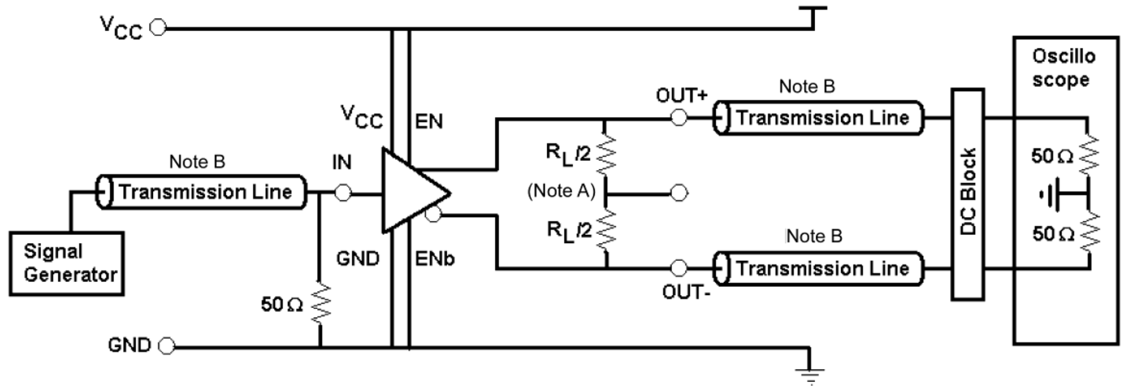


Figure 5. LVDS Output Propagation Delay and Transition Time Test Circuit

Notes:

11. A: R_L=100 Ω.
12. B: Z_O=50 Ω and C_T=15 pF distributed.

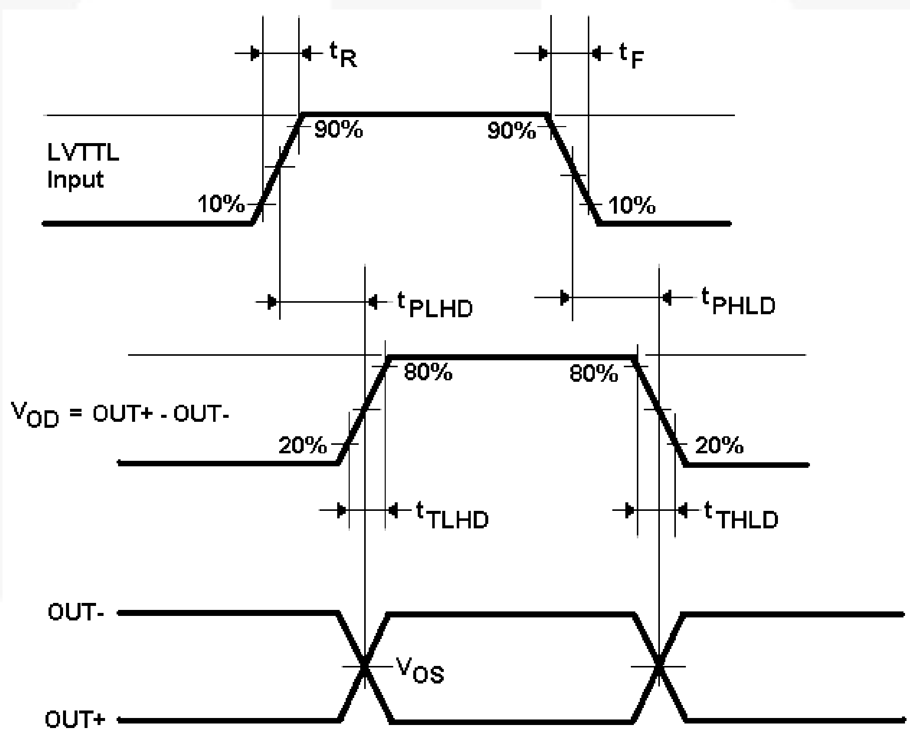


Figure 6. LVTTL Input to LVDS Output AC Waveform

Required Specifications and Test Diagrams (Continued)

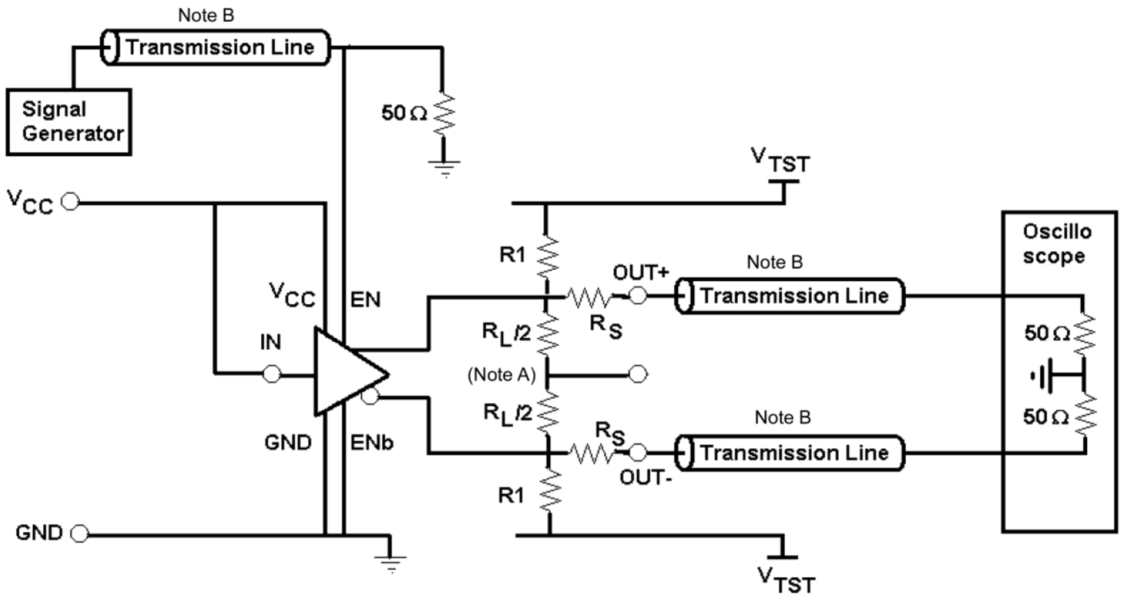


Figure 7. LVDS Output Enable / Disable Delay Test Circuit

Notes:

13. A: R_L=100 Ω.
14. B: Z_O=50 Ω and C_T=15 pF distributed.
15. R1=1000 Ω, R_S=950 Ω.
16. V_{TST}=2.4 V.

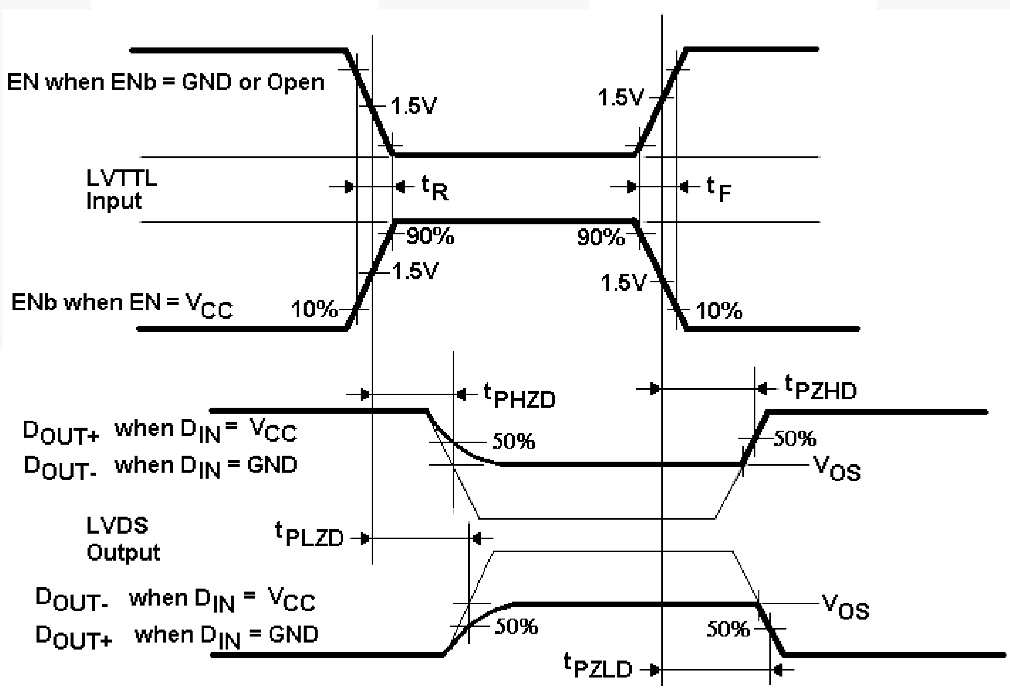


Figure 8. LVDS Output Enable / Disable Timing Waveforms

Required Specifications and Test Diagrams (Continued)

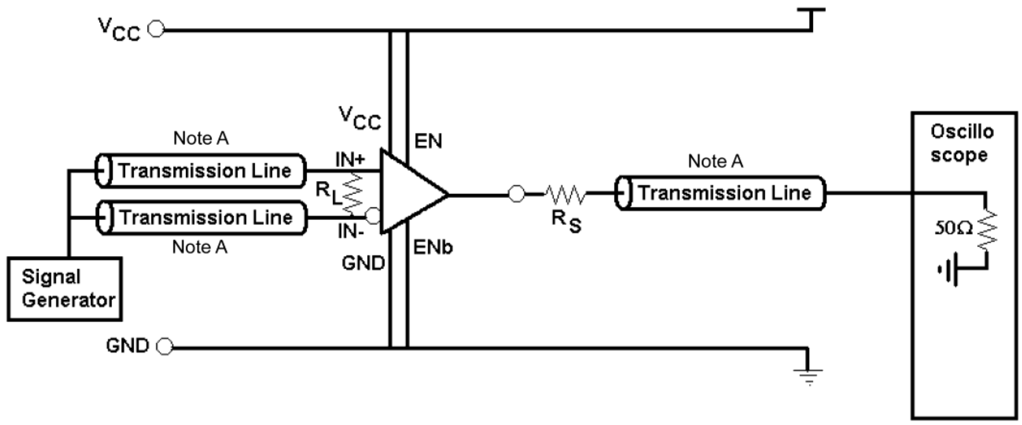


Figure 9. LVTTL Output Propagation Delay and Transition Time Test Circuit

Notes:

17. A: Z_O=50 Ω and C_T=15 pF distributed.
18. R_L=100 Ω and R_S=950 Ω.

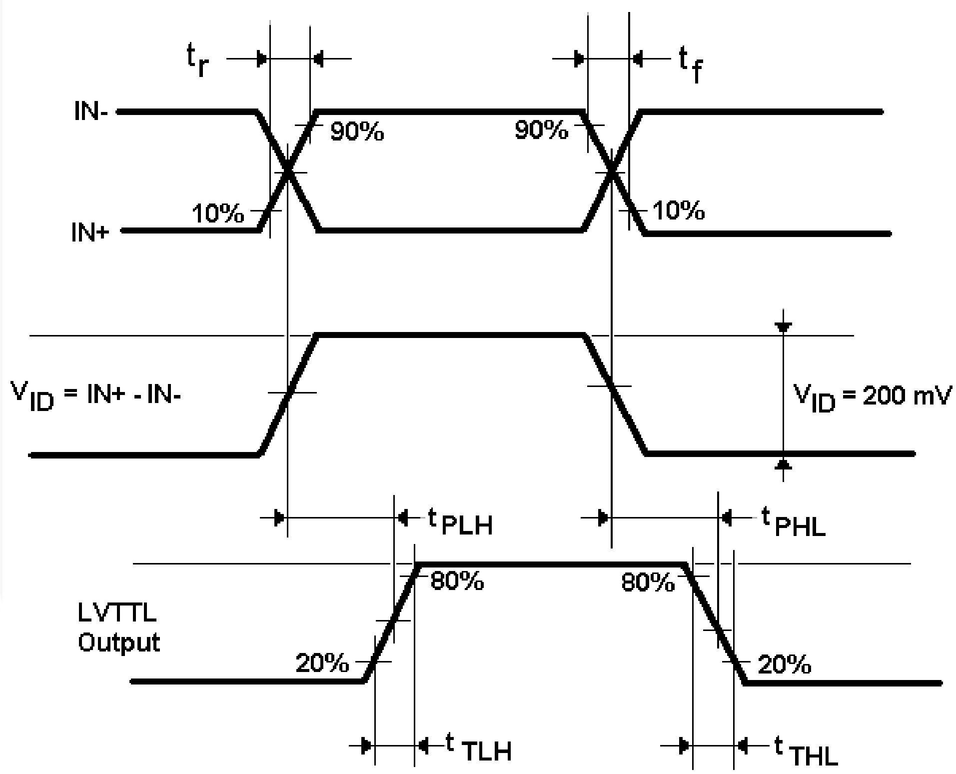


Figure 10. LVDS Input to LVTTL Output Propagation Delay and Transition Time Waveforms

Required Specifications and Test Diagrams (Continued)

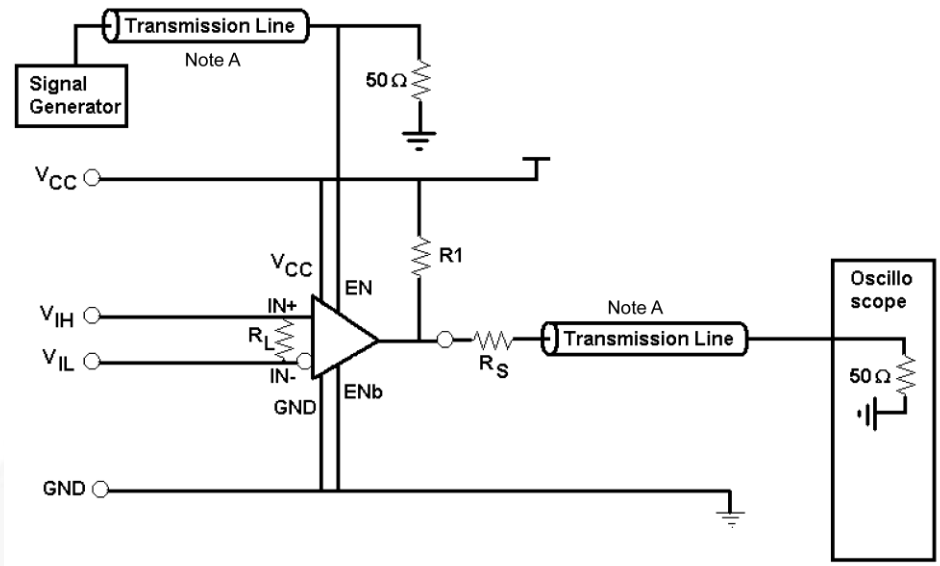


Figure 11.LVTTL Output Enable / Disable Test Circuit

Notes:

19. A: Z_O=50 Ω and C_T=15 pF distributed.
20. R_L=100 Ω, R1=1000 Ω, and R_S=950 Ω.

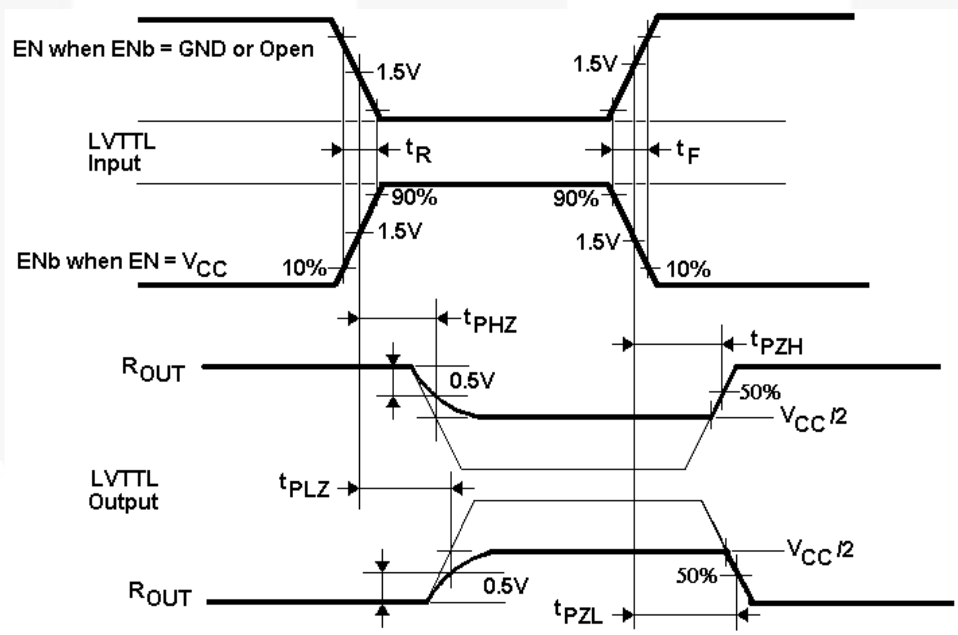
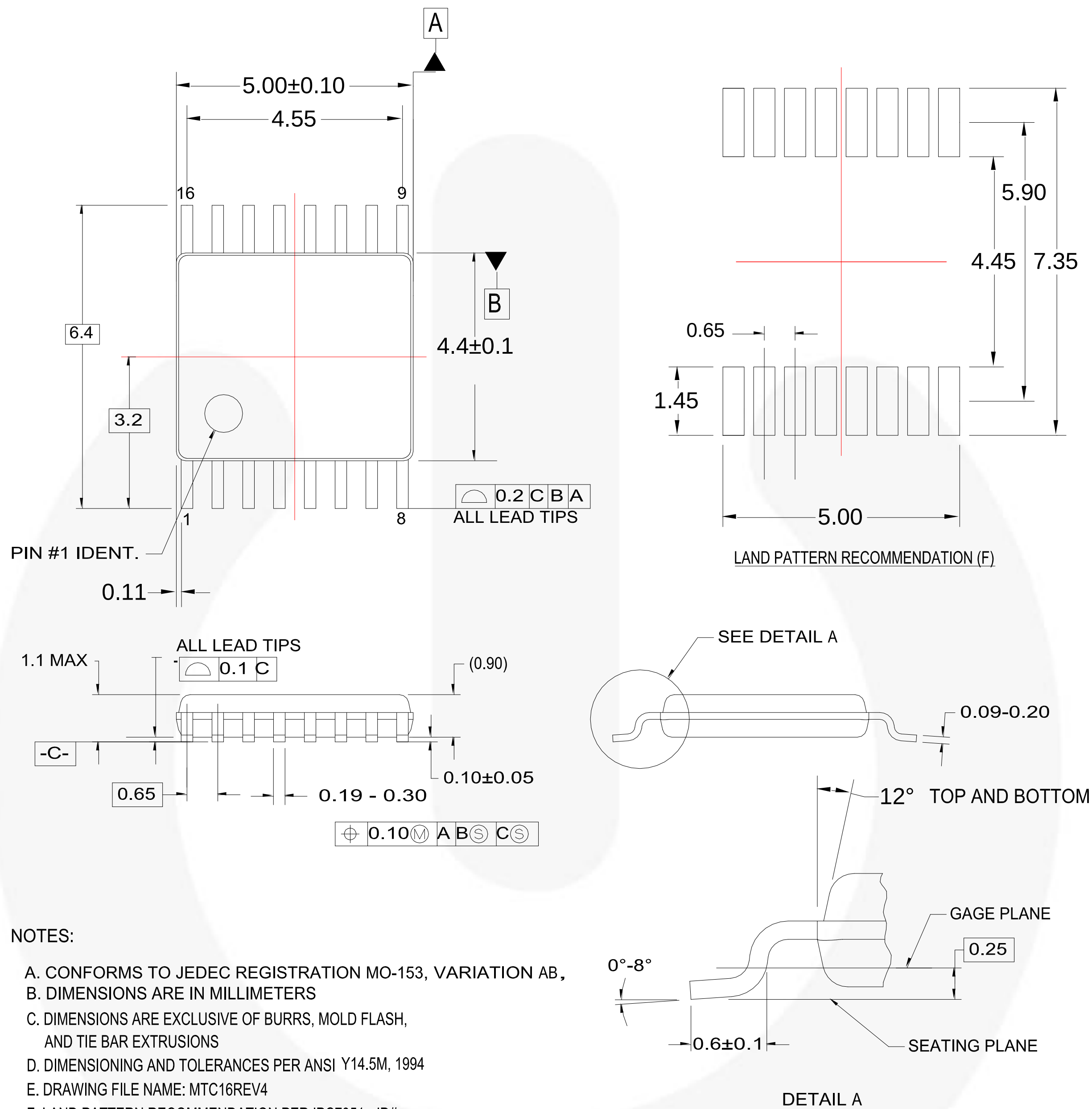


Figure 12.LVTTL Output Enable / Disable Timing Waveforms

Physical Dimensions



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB,
B. DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1994
E. DRAWING FILE NAME: MTC16REV4
F. LAND PATTERN RECOMMENDATION PER IPC7351 - ID# TSOP65P640X110-16N

MTC16rev4

Figure 13.16-Lead, Thin-Shrink Small-Outline Package (TSSOP), JEDEC MO-153, 4.4 mm Wide

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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