EVAL_3KW_DB_PFC_C7

High efficiency 3 kW bridgeless dual boost PFC evaluation board

90 kHz digital control design based on
650 V CoolMOS™ C7 in TO-247 4pin

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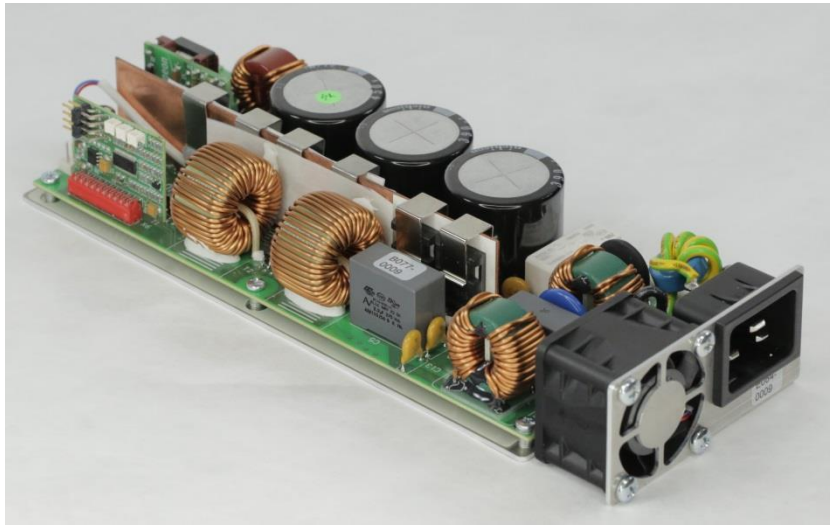
General

Description:

› The **"EVAL_3kW_DB_PFC_C7"** evaluation board shows how to design a high power density 3 kW 90 kHz bridgeless dual boost power factor correction (PFC) boost converter working in continuous conduction mode (CCM). For this purpose the following technologies have been used: power MOSFET 650 V CoolMOS™ C7 technology (IPZ65R045C7 and IPW65R045C7), CoolSiC™ Schottky diode 650 V G5 (IDH06G65C5), EiceDRIVER™ 1EDI isolated gate driver IC (1EDI60N12AF) and EiceDRIVER™ 2EDN non-isolated gate driver IC (2EDN7524F), XMC1300 microcontroller (XMC1302-T038X0200 AB), linear voltage regulator (TLF4949) and quasi-resonant CoolSET™ (ICE2QR4780Z).



Summary of features:

› Output voltage: 400 V_{DC}
› Output current: 7.5 A
› Efficiency: >98% from 20% load, V_{in} = 230 V_{DC}
› Switching frequency: 90 kHz

The following variant is available:

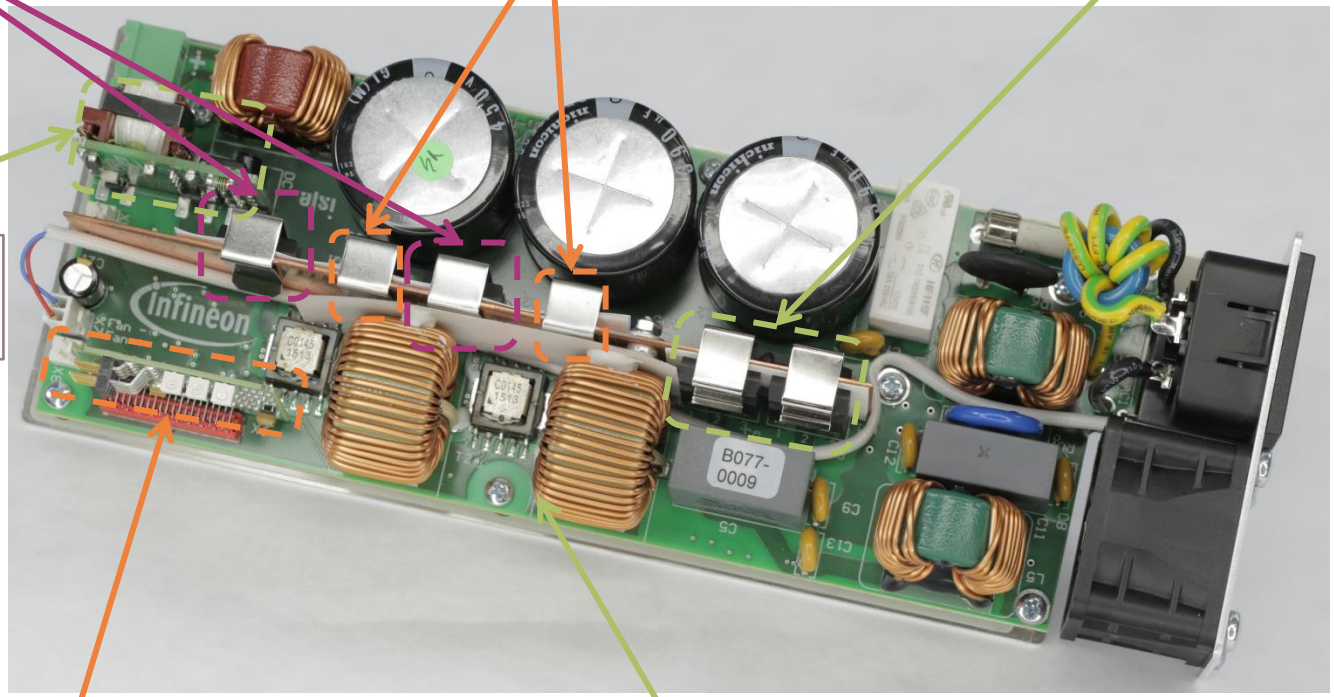
› **EVAL_3KW_DB_PFC_C7**: 3 kW 90 kHz PFC version with 650 V CoolMOS™ C7 (IPZ65R045C7)

High efficiency 3 kW bridgeless dual boost PFC demo board

Power MOSFETs
CoolMOS™ IPZ65R045C7
CoolMOS™ IPZ60R037P7 (optional)

Silicon Carbide diode
CoolSiC™ 650 V G5 IDH16G65C5
CoolSiC™ 650 V G5 IDH16G65C6 (optional)

Power MOSFETs
CoolMOS™ IPW65R045C7

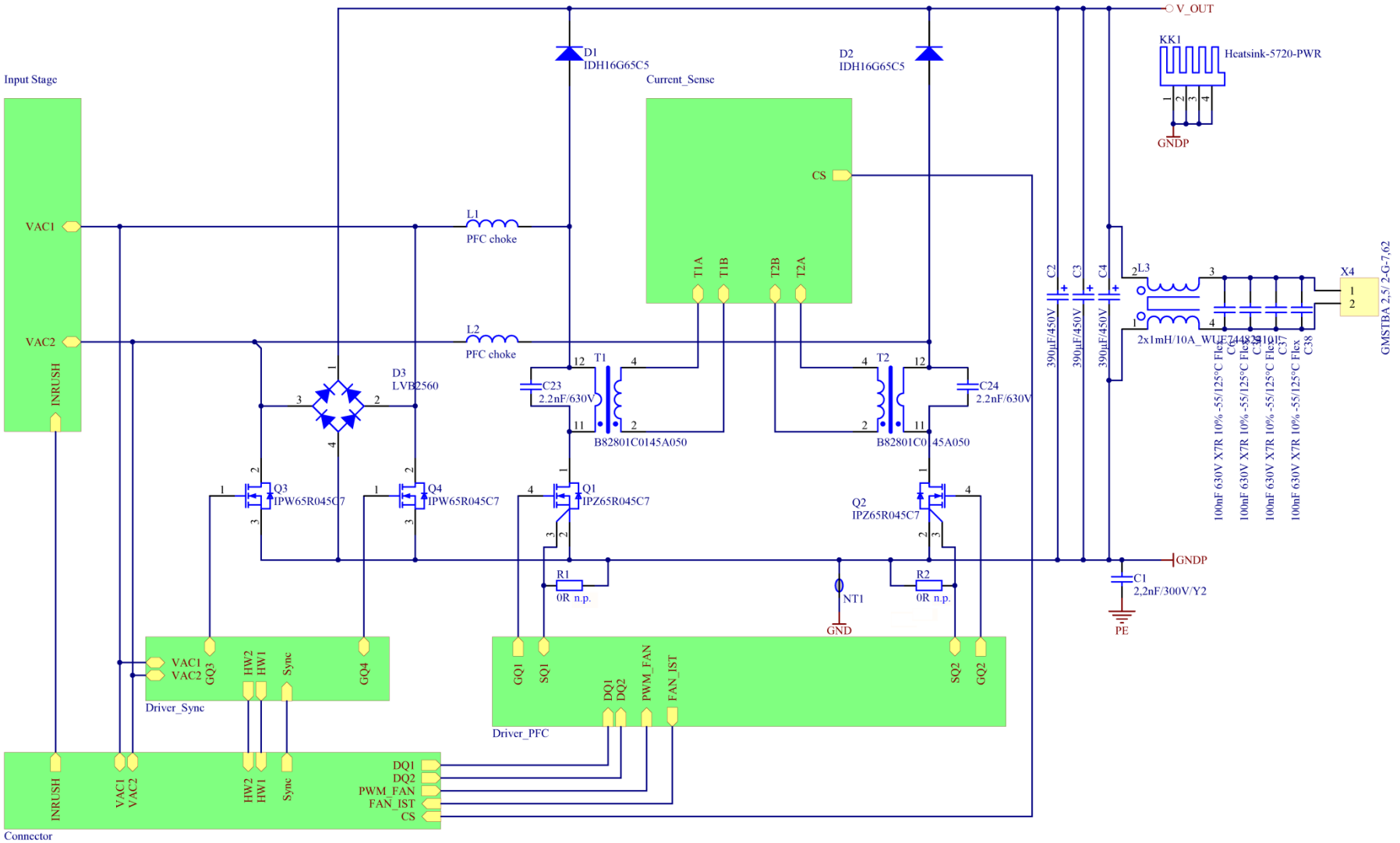


PWM controller
CoolSET™ ICE2QR4780Z

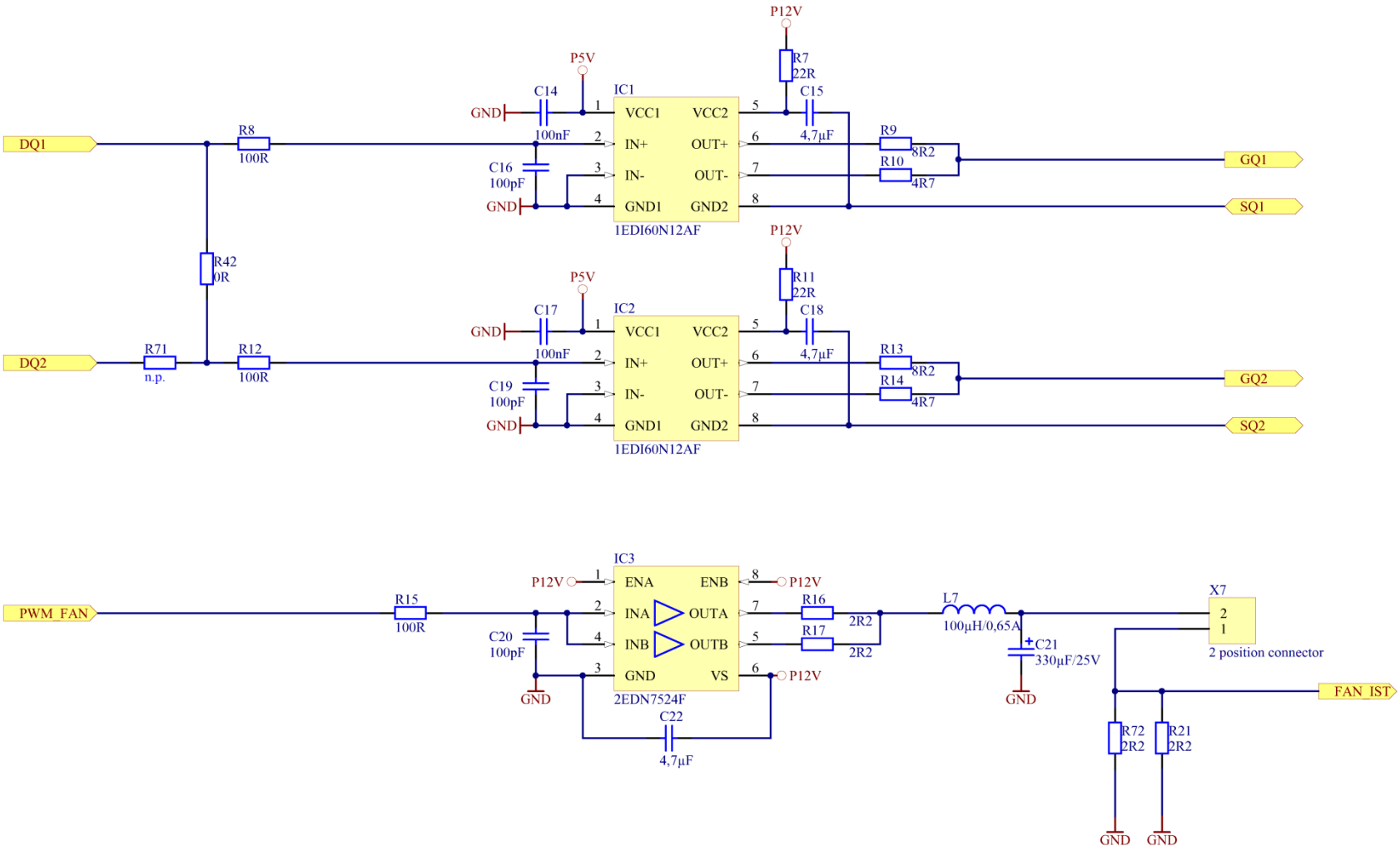
Microcontroller XMC1300
digital
XMC1302-T038X0200 AB
Linear voltage regulator TLF4949

EiceDRIVER™
1EDI60N12AF
2EDN7524F

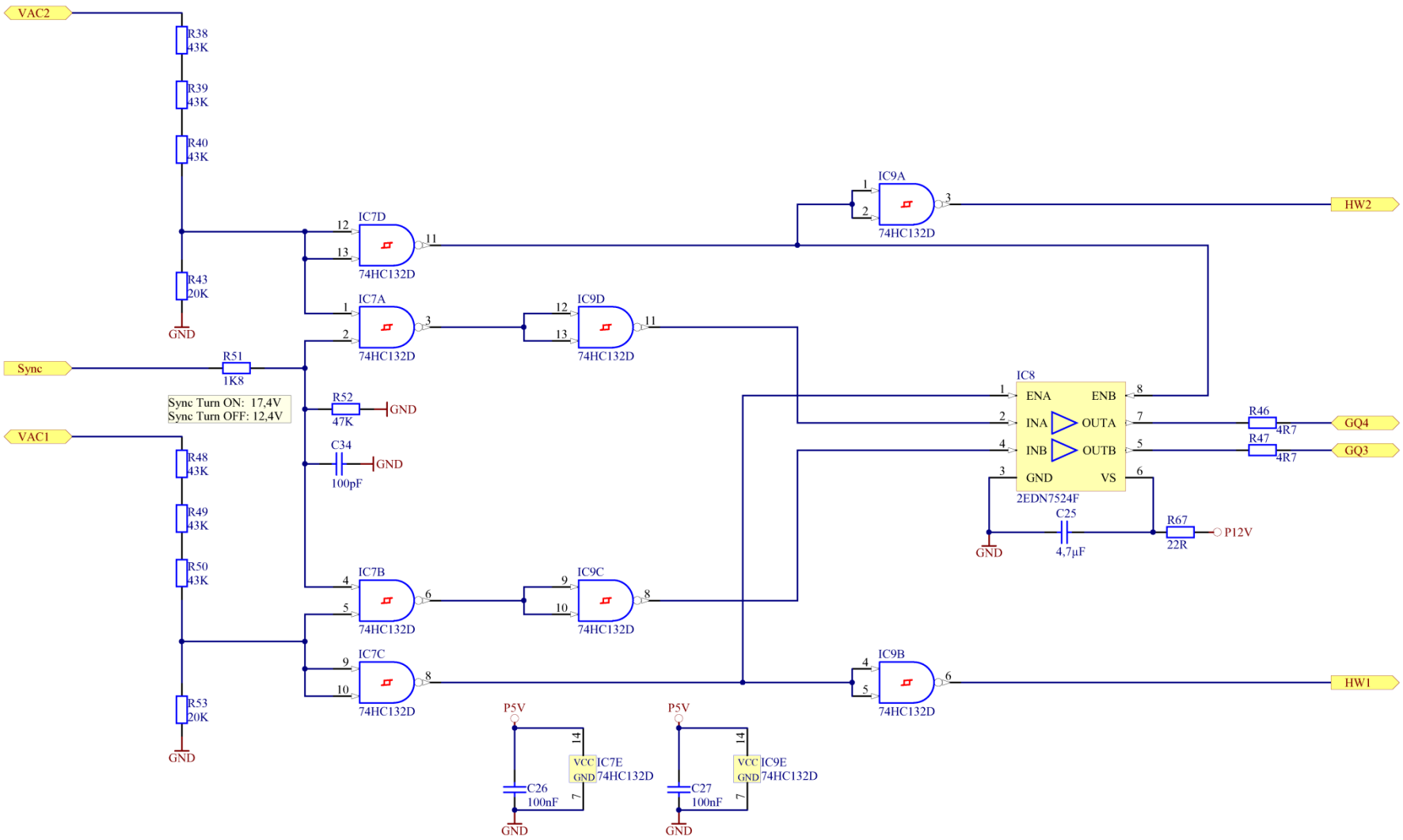
Power stage schematic



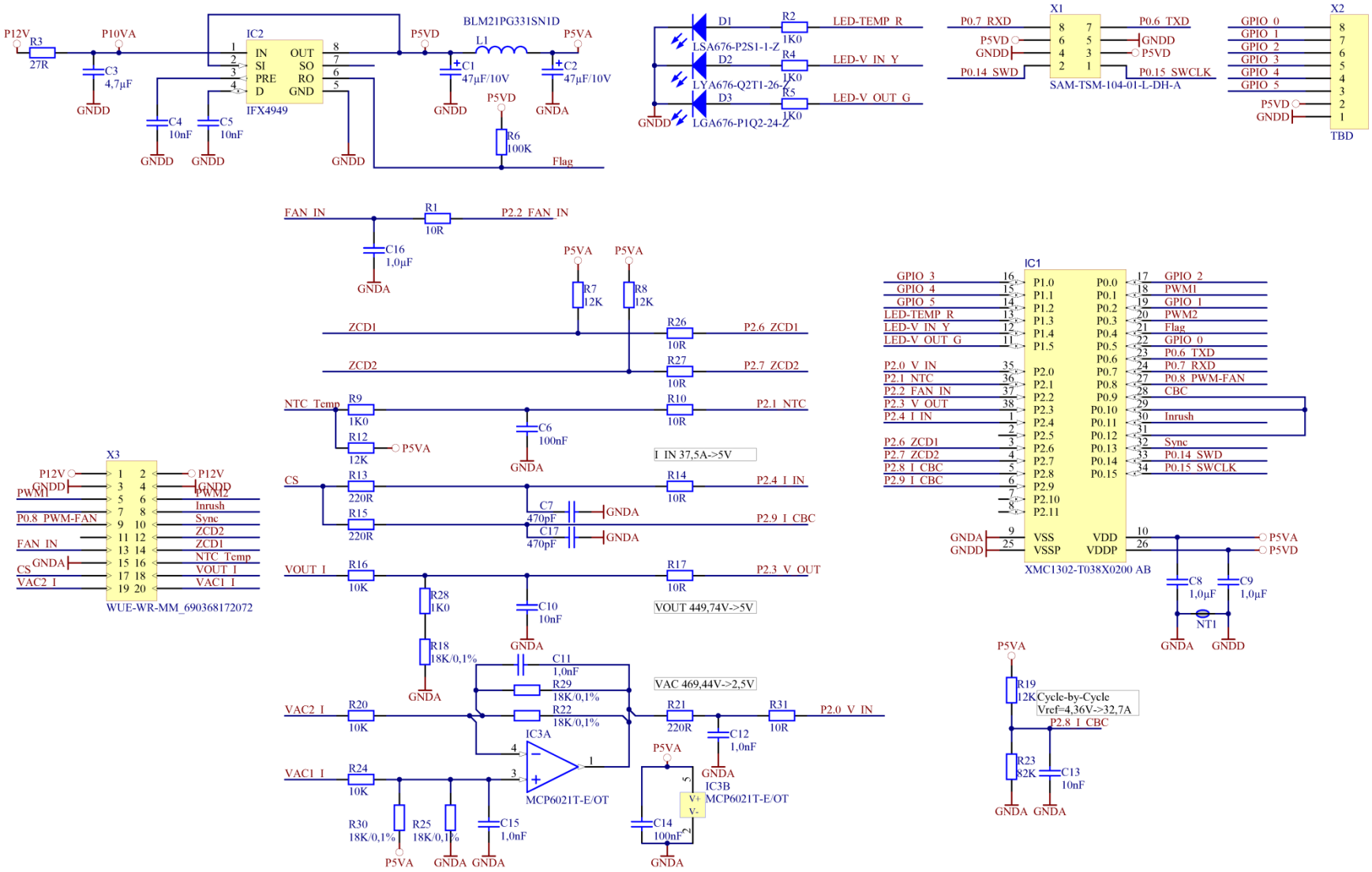
PFC MOSFETs gate drivers schematic



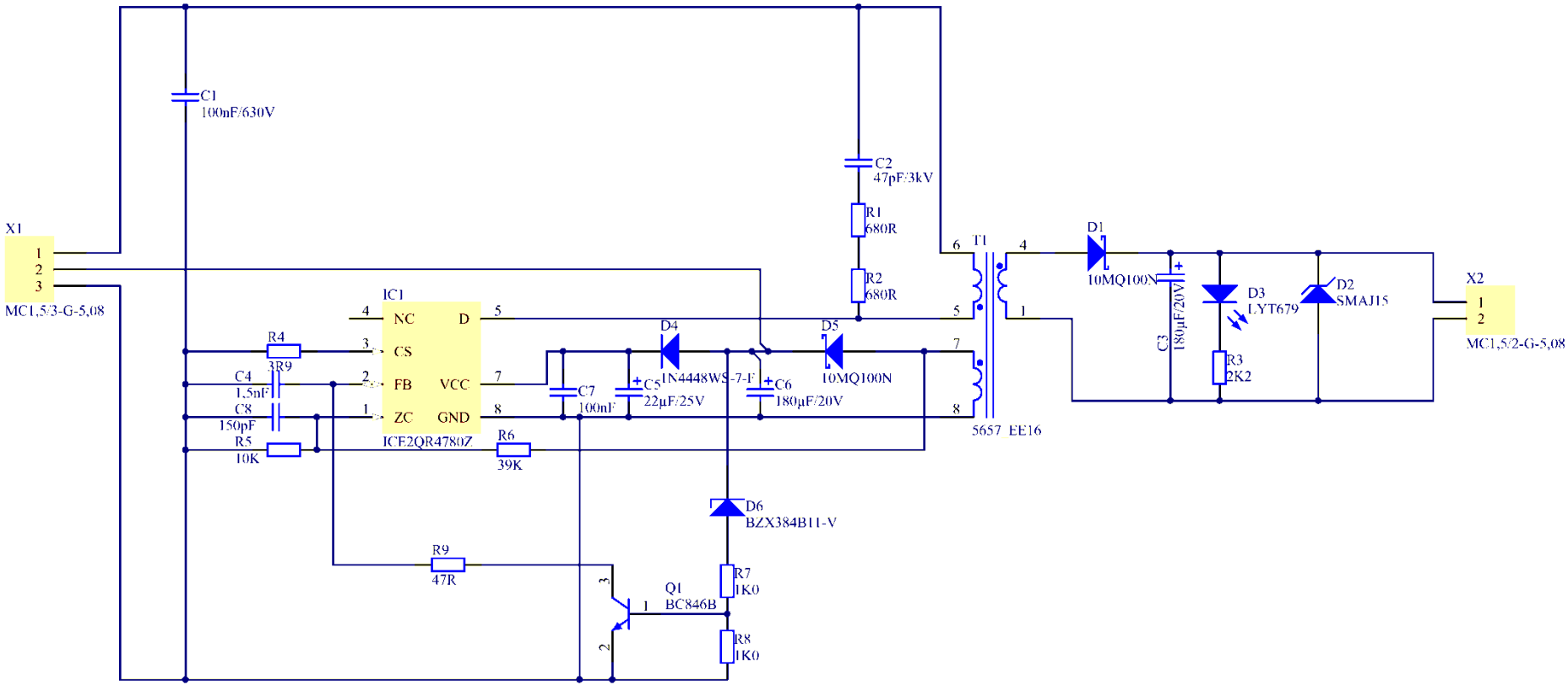
Active rectification MOSFETs control circuitry and gate driver schematics



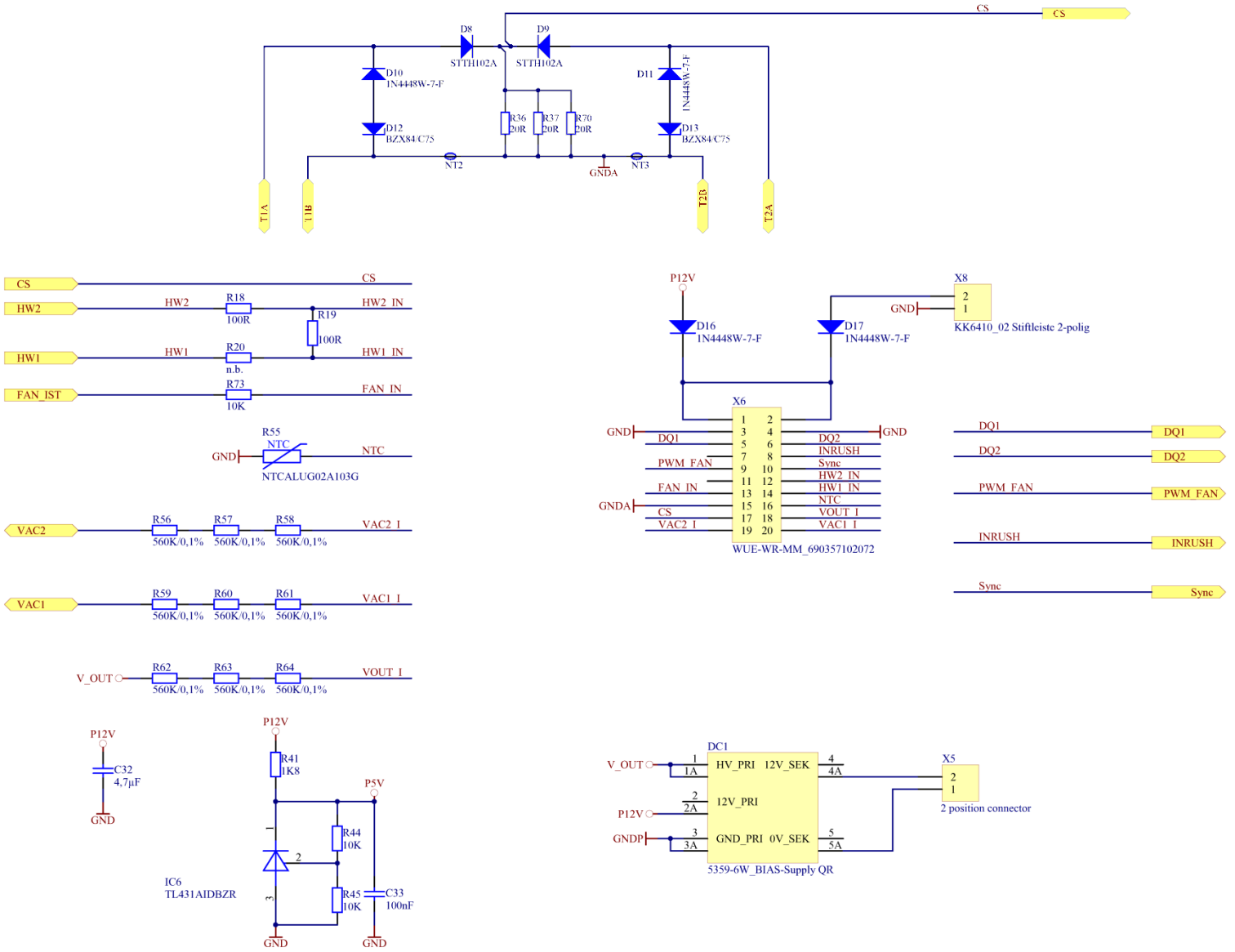
XMC™ microcontroller schematic



Auxiliary SMPS

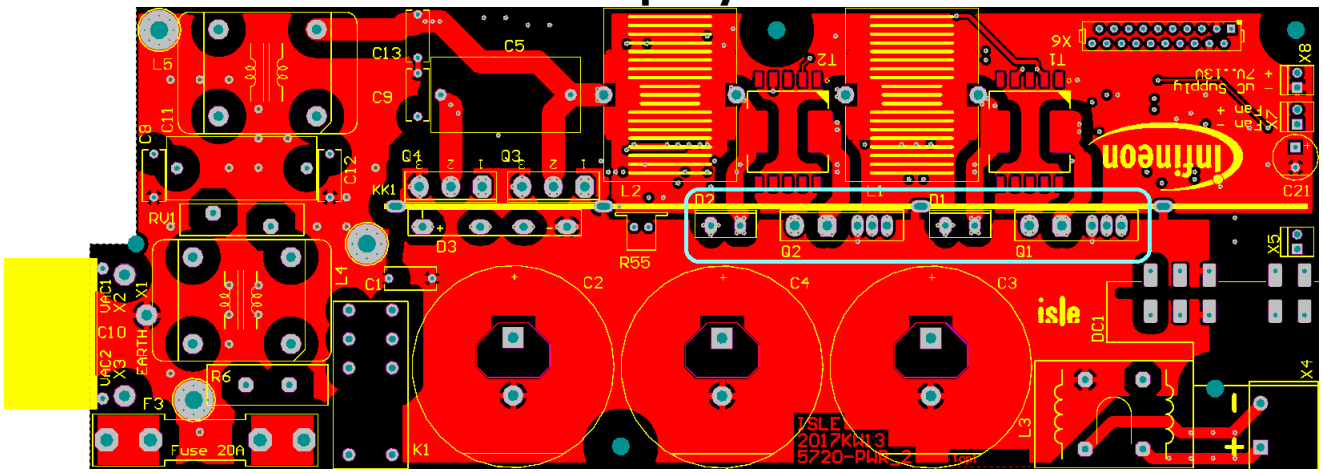


Current sense circuitry and daughter card connector schematics

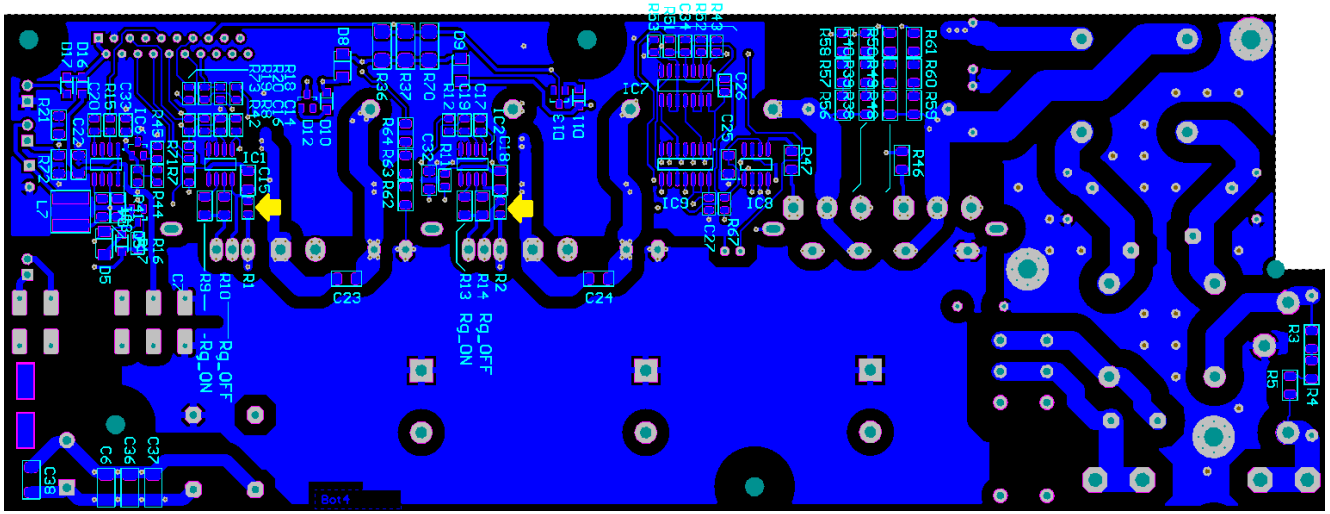


3 kW 90 kHz bridgeless dual boost PFC board main board PCB layout

Top layer



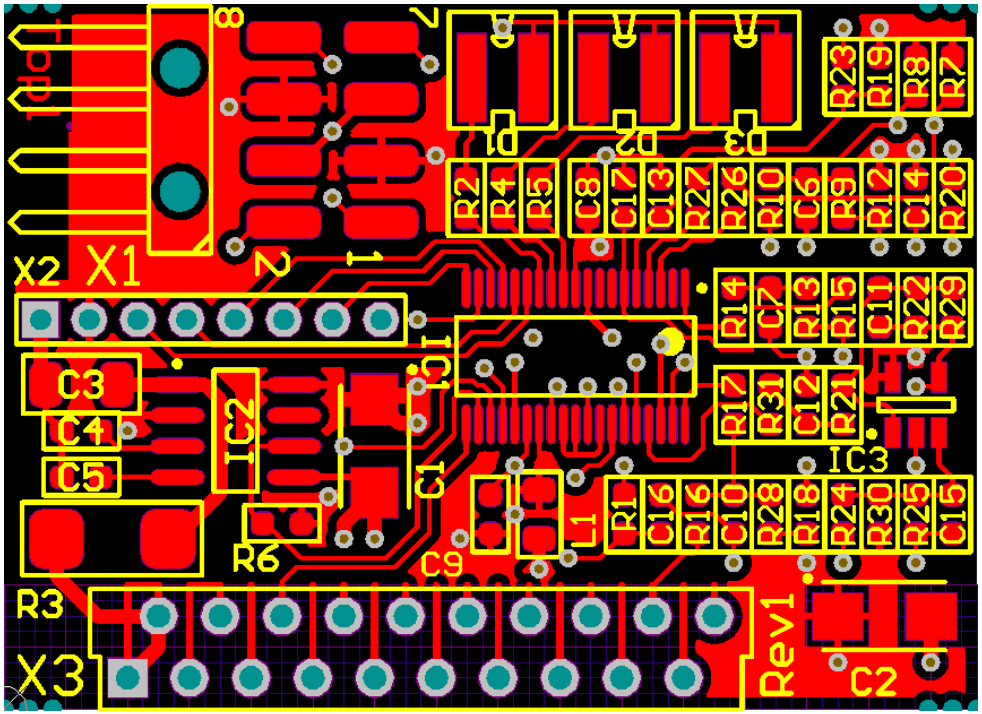
Bottom layer



As can be observed in the cyan rectangle highlighted in the top layer figure, the layout of the board allows the user to evaluate the performance of the Dual Boost PFC converter using either TO-247 3pin or TO-247 4pin Q1 and Q2 PFC MOSFETs. The pin configuration is the following:

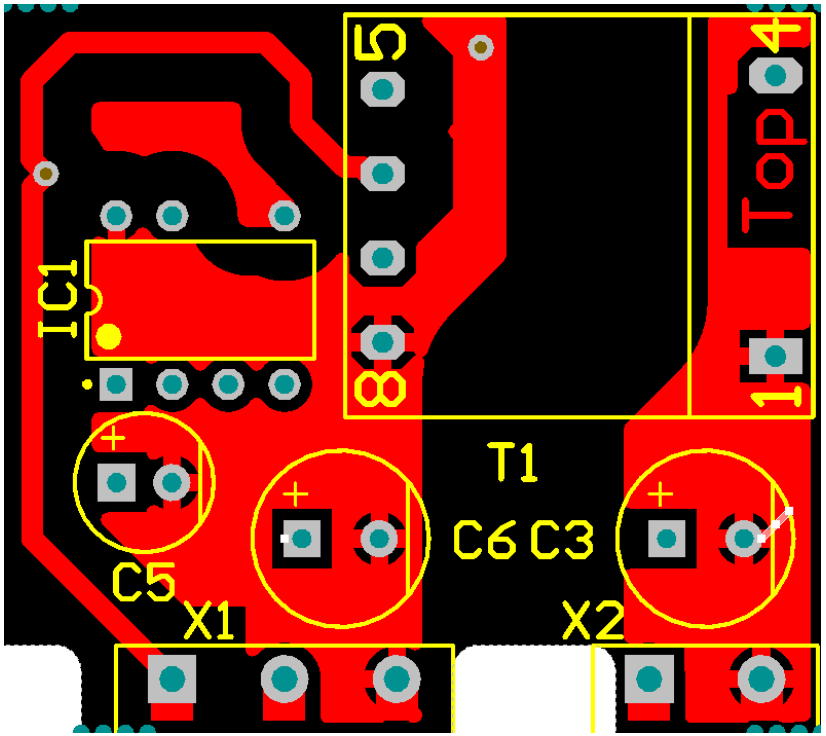
Please be aware that when using TO-247 3pin devices, 0 Ω resistors must be populated in R1 and R2, as indicated by the yellow arrows shown in the bottom layer figure.

3 kW 90 kHz bridgeless dual boost PFC board digital control daughter card PCB layout

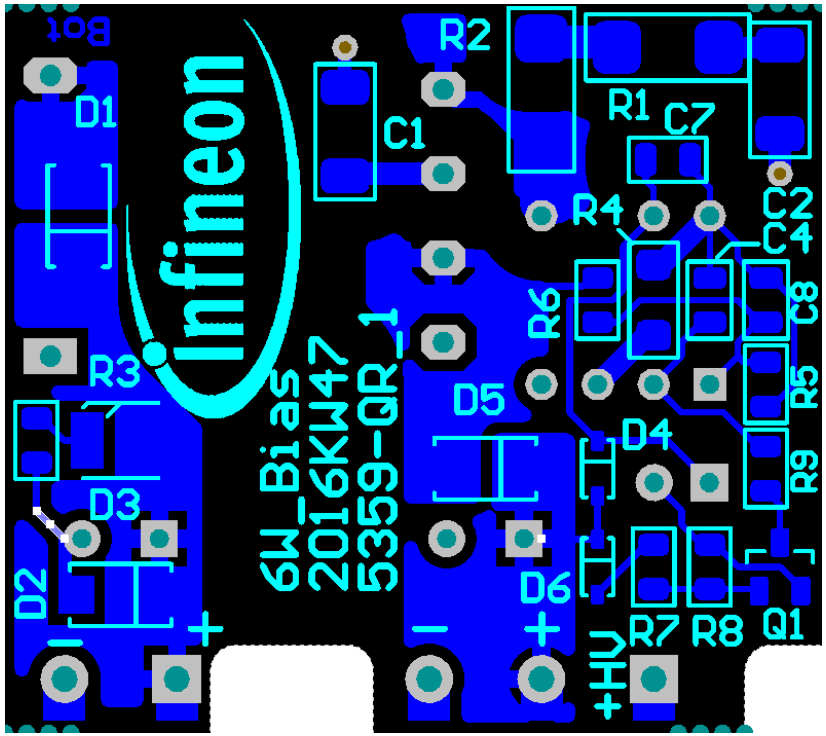


Top layer

3 kW 90 kHz bridgeless dual boost PFC board aux SMPS daughter card PCB layout



Top layer



Bottom layer

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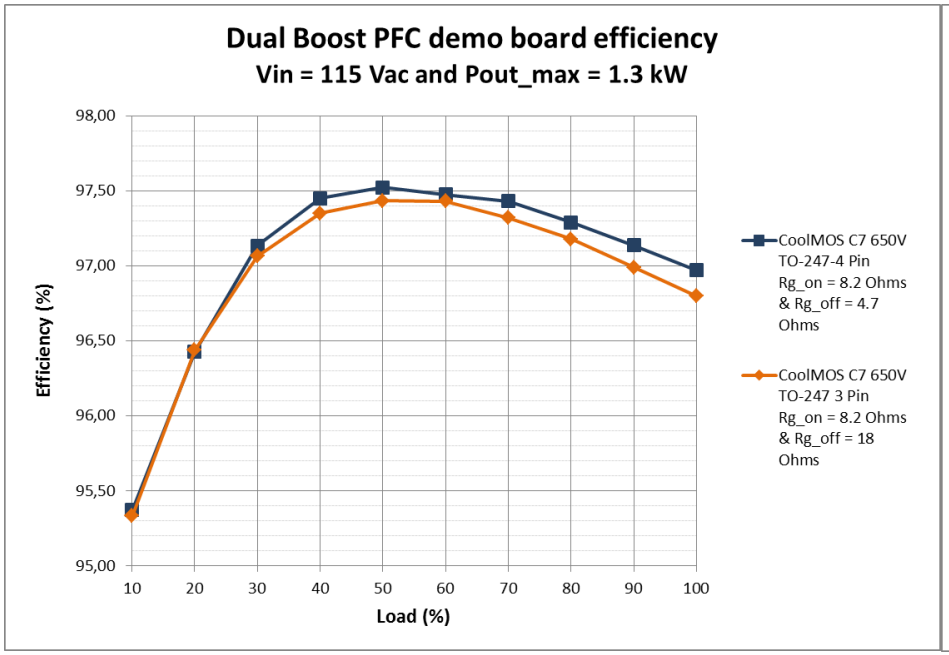
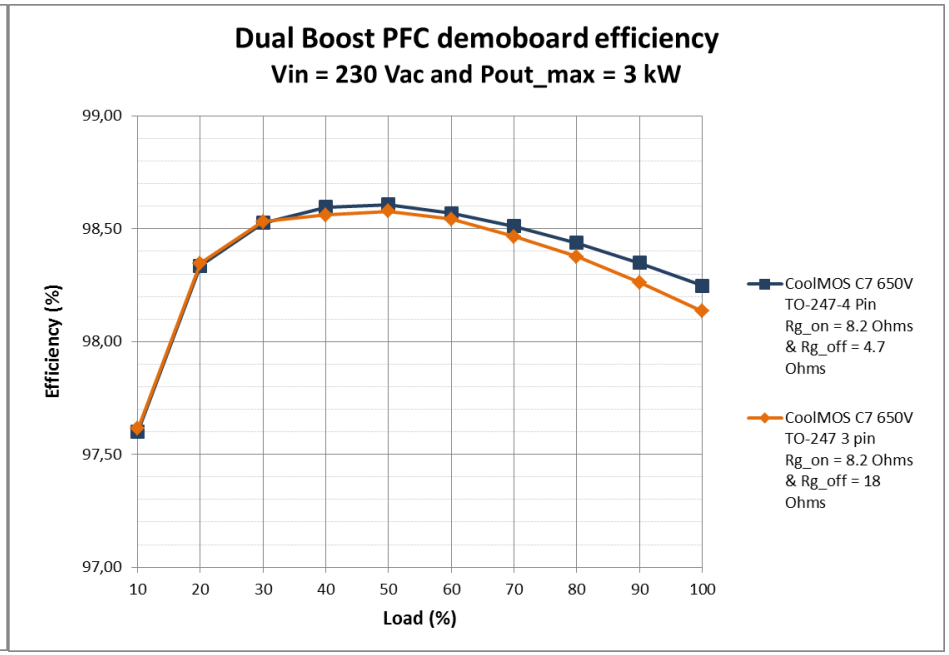
Specifications and requirements

Parameter	Value
Input voltage range, V_{in_range}	90 V_{AC} – 265 V_{AC}
Nominal input voltage, V_{in}	230 V_{AC}
AC line frequency range, f_{AC}	47 Hz – 63 Hz
Max peak input current, I_{in_max}	14.9 A_{RMS} @ V_{in} = 90 V_{AC} & P_{OUT} = 1.3 kW 15.46 A_{RMS} @ V_{in} = 200 V_{AC} & P_{OUT} = 3 kW
Turn on input voltage, V_{in_on}	80 V_{AC} – 87 V_{AC}, ramping up
Turn off input voltage, V_{in_off}	75 V_{AC} – 85 V_{AC}, ramping down
Power factor (PF)	Greater than 0.95 from 10% rated load and above
Hold up time	10 ms after last AC zero point @ P_{OUT}, V_{OUT_MIN} = 320 V_{AC} 20 ms after last AC zero point @ 0.5 x P_{OUT}, V_{OUT_MIN} = 320 V_{DC}
Total harmonic distortion (THD)	<10% from 10% load @ nominal input voltage for class A equipment

Parameter	Value
Nominal output voltage, V_{out}	400 V_{DC}
Maximum output power, P_{out}	3 kW
Maximum output current, I_{out_max}	7.5 A
Output voltage ripple	Max 20 V_{pk-pk} @ V_{out} and I_{out}
Maximum output overvoltage threshold	435 V_{DC}
Minimum output overvoltage threshold	430 V_{DC}

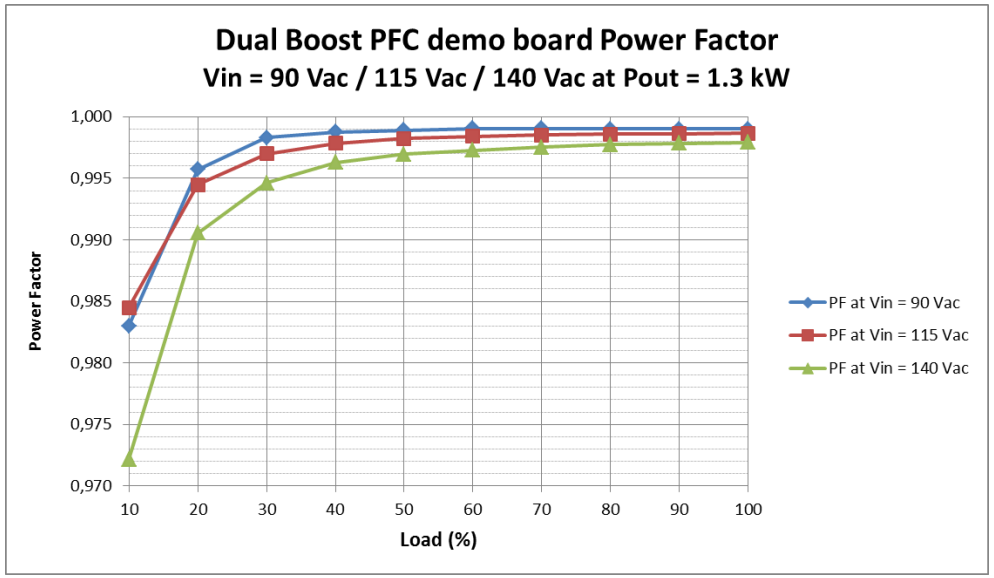
Efficiency results at low and high-line using 650 V CoolMOS™ C7 and CoolSiC™ G5

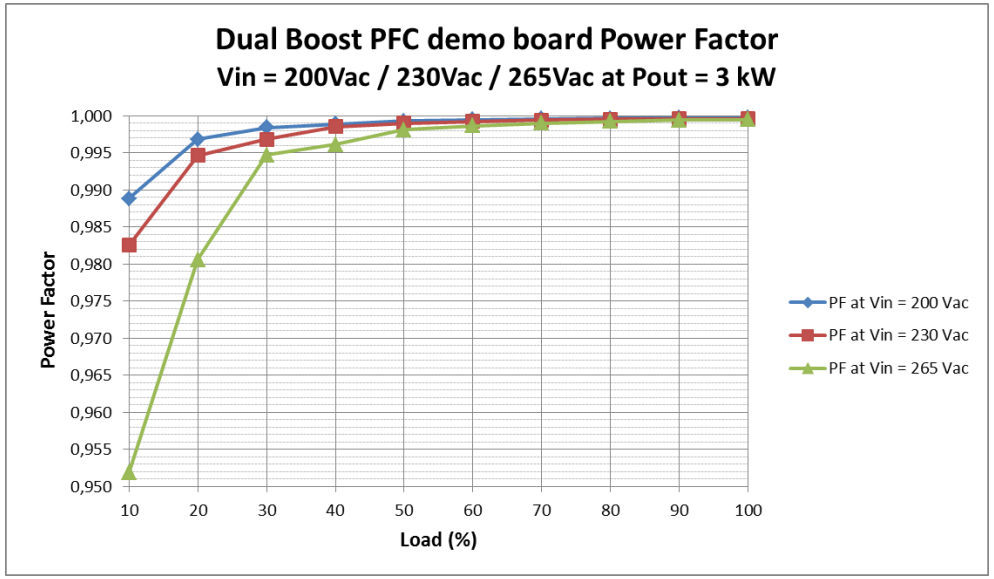




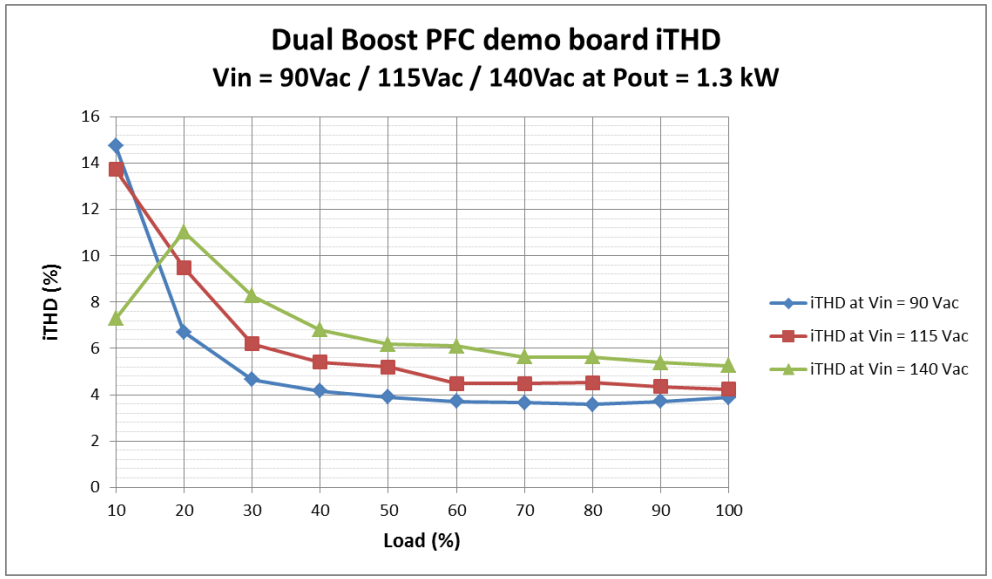
TO-247 4pin with R_{g_on} = 8.2 Ω and R_{g_off} = 4.7 Ω **vs** TO-247 with R_{g_on} = 8.2 Ω and R_{g_off} = 18 Ω

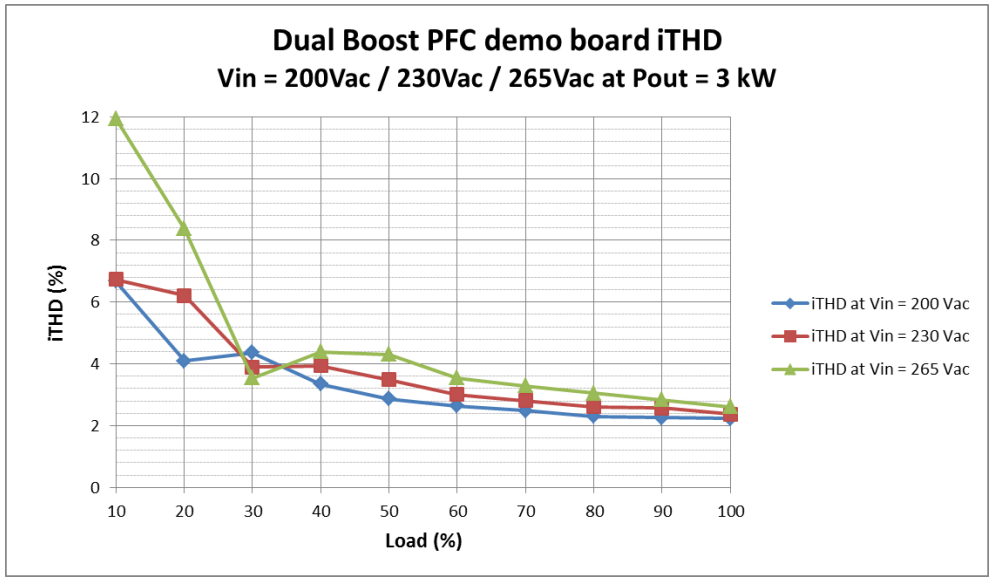
Power factor results using 650 V CoolMOS™ C7 and CoolSiC™ G5





Total harmonic distortion results using 650 V CoolMOS™ C7 and CoolSiC™ G5





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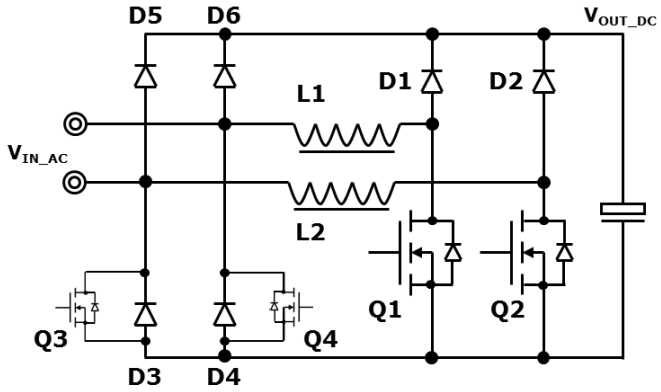
Power factor correction (PFC)

A power factor current converter shapes the input current of the power supply so that it is synchronized with the mains voltage, in order to maximize the real power drawn from the mains. In a actual power factor correction circuits, the input current should follow as close as possible the input voltage as if it was a pure resistive load, with quite limited harmonic distortion.

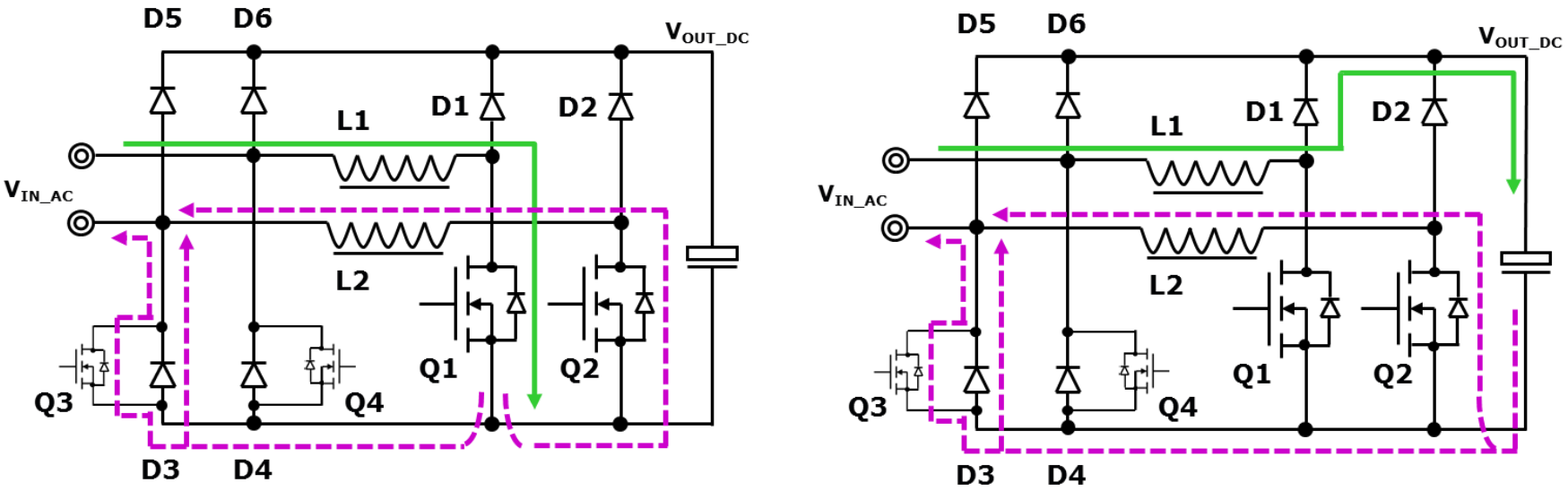
Although active PFC can be achieved by several topologies, the dual boost converter (see figure below) is a very attractive solution for high power supply solutions for the following reasons:

- Compared to the standard/classic PFC rectifier based on a diode bridge (with two active diodes at all time), a single PFC MOSFET and a PFC diode, the dual boost has lower conduction losses because there always two power semiconductors (e.g. Q1 + D3 or Q2 + D4) in the current path per AC semi-cycle. However, due to driving control ease as well as on the impedance of the returning path, even three can be active (e.g. Q1 + D3 ‖ Q2 or Q2 + D4 ‖ Q1)
- Higher efficiency at a higher power density compared to the same rated power standard/classic PFC rectifier due to less cooling effort and better heat spot distribution
- More efficient and easier to control compared to an interleaved PFC rectifier, as this is a bridgeless topology with no need to make phase shedding between the PFC legs
- To increase the efficiency further, low R_{DS_ON} MOSFETs (Q3 and Q4) can be placed in parallel with each of the returning path diodes (i.e. D3 and D4). As these MOSFETs will be conducting at the AC line frequency, then the switching losses and gate driving losses are considerably much lower than conduction ones. This benefit comes at the expense of increasing bill of material count and cost as well as accurate control and driving circuitry.



Operation modes per leg

As explained before, due to driving control ease both PFC MOSFETs, Q1 and Q2, can be driven by the same PWM signal. Additionally, in order to boost the efficiency of the topology active rectification MOSFETs, Q3 and Q4, are added. This gives as a result that the inductor current has different returning paths during the charging and discharging time slots of the corresponding inductor. As an example, the figure below clearly shows such different paths of the inductor current during the positive AC semi-cycle.

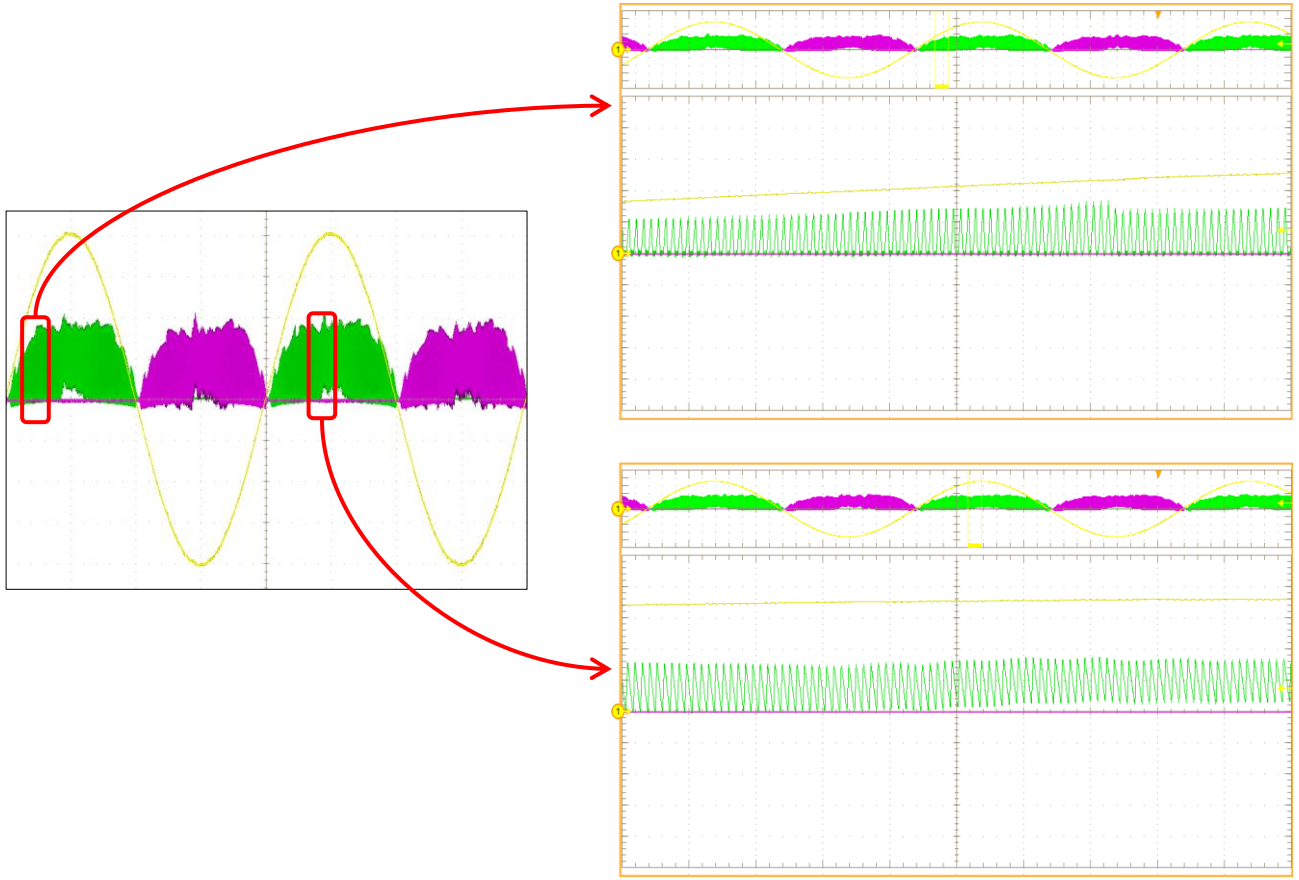


Example of the paths of the inductor current in different operation modes

- Left: when the PFC MOSFET Q1 is turned-on
- Right: when the PFC MOSFET Q1 is turned-off

PFC conduction modes

The boost converter can operate in three modes: continuous conduction mode (CCM), critical conduction mode (CrCM) and discontinuous conduction mode (DCM). The next figures show actual waveforms to illustrate the inductor currents in the three operating modes at different load conditions.

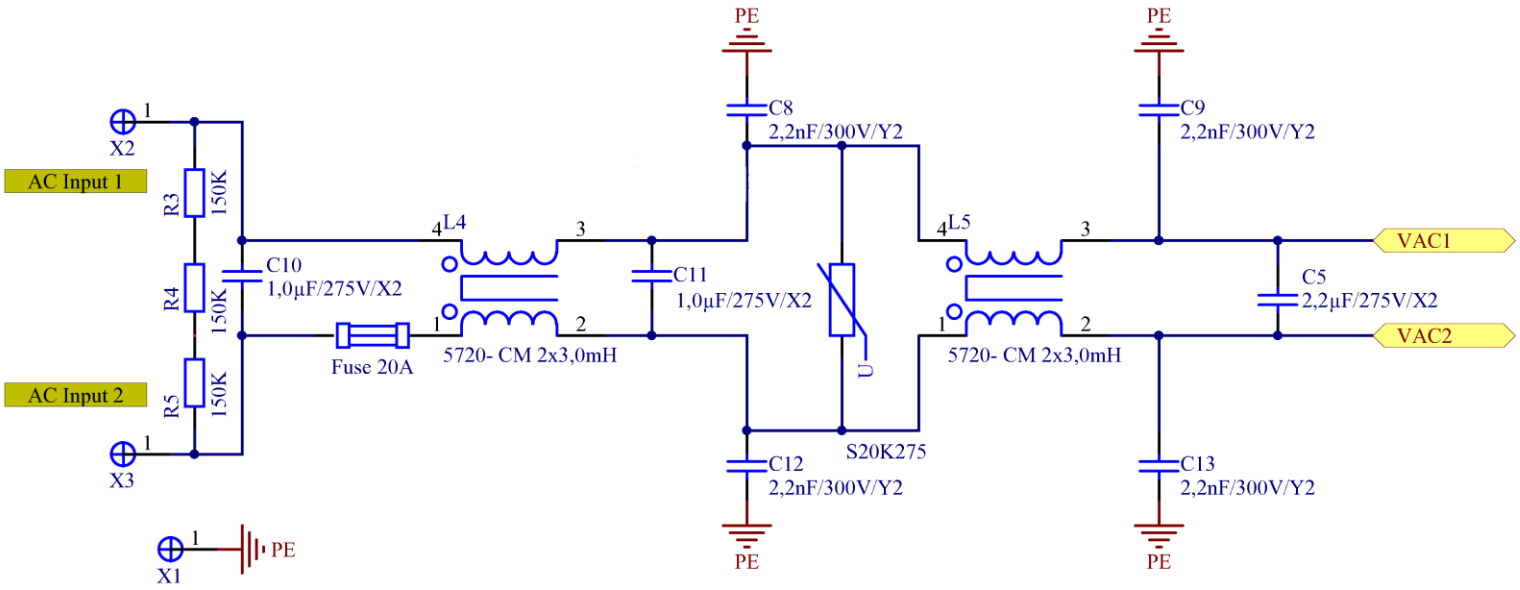


For fixed switching frequency operation, the input voltage and output power of the PFC will determine the operation mode. In this way we may have:

- Complete half AC cycle in DCM operation mode.
- DCM, CrCM and CCM operation modes during half AC cycle.
- Complete half AC cycle in CCM operation mode.

EMI filter

The EMI filter implemented is as a two-stage filter, which provides sufficient attenuation for both differential mode (DM) and common mode (CM) noise.



The two high current CM chokes L4 and L5 cm are based on high permeability toroid ferrite cores. Eacg of these have 2 x 18 turns or 2 x 3 mH inductance.
The relatively high number of turns causes a considerable amount of stray inductance, which ensures sufficient DM attenuation.

In case the fuse is blown due to any abnormal condition during the operation of the converter, the C10 X-capacitor in the figure above is fully discharged thru resistors R3, R4 and R5 in order to prevent any electric shock injuries to the operator of the demo board.

Rectifier bridge

Taking the previous figures of the topology as a reference, in contrast with the standard/classic and interleave topologies, the bridge rectifier employed in this demo board has two main purposes:

- Diodes D5 and D6 support the pre-charging of the bulk capacitors to the peak value of the AC line voltage. Once the bulk capacitors are charged, these diodes are no longer active during the steady state operation of the topology
- Diodes D3 and D4 support the returning path between the AC input and the output ground, so the voltage potential of the output is stabilized and the common mode noise of the converter is drastically reduced.

To determine the proper selection and losses of the bridge rectifier, it is necessary to calculate the input RMS and average input current at the worst operating condition, i.e. efficiency of 97% at V_{in} = 178 V_{AC}:

Maximum RMS value of the input current:

$$I_{IN\_RMS} = \frac{P_{OUT\_MAX}}{\eta \cdot V_{IN\_RMS}} = \frac{3000W}{0{,}97 \cdot 178V} = 17.37A$$

Maximum RMS current value per diode, D3 or D4:

$$I_{BR-D\_RMS} = \frac{\sqrt{2} \cdot I_{IN\_RMS}}{2} = 12{,}28\ A$$

Maximum average current value per diode:

$$I_{BR-D\_avg} = \frac{\sqrt{2} \cdot I_{IN\_RMS}}{\pi} = 7{,}82A$$

Due to the calculated average and effective current values, the rectifier type LVB2560 with very low forward voltage drop was selected. This 600 V device has sufficient voltage reserve with V_{in} = 265 V_{AC}. For the following formula, the instantaneous forward resistance (r_D) and forward voltage drop (V_{BR-D}) are extracted from the characteristic curves of the corresponding data sheet (T_A = 100 °C).

Conduction losses of a rectifier diode, D3 or D4, per AC cycle:

$$P_{BR-D} = I_{BR-D\_avg} \cdot V_{BR-D} + \left(I_{BR-D_{RMS}}\right)^2 \cdot r_D = 7{,}82 \cdot 0{,}75 + (12{,}28)^2 \cdot 65\ m\Omega \cong 15.6W$$

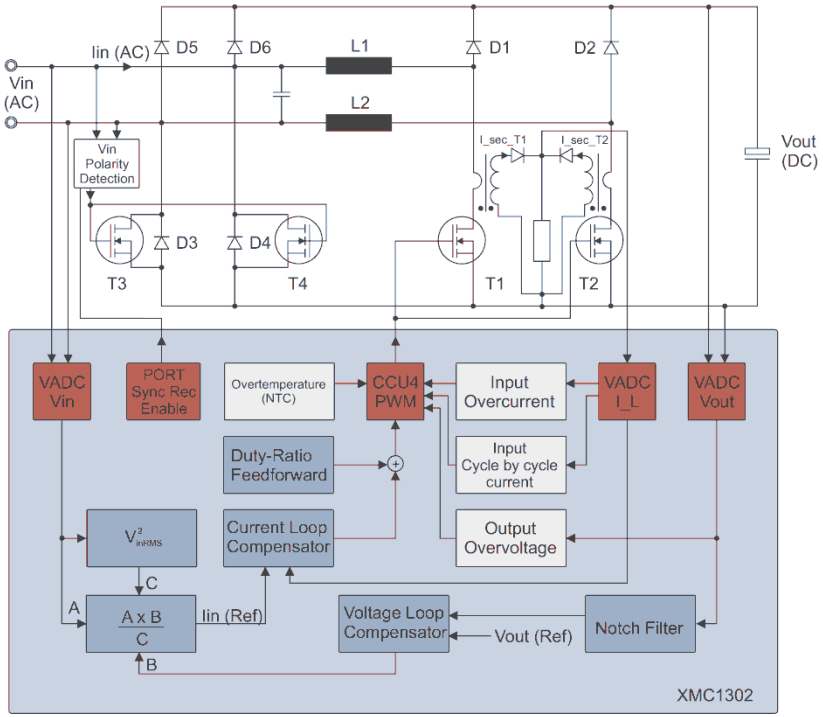
PFC choke

The PFC choke design is based on a toroidal high performance magnetic powder core.
Toroidal chokes have a large surface area and allow a good balance, minimizing core and winding losses, and achieving a homogeneous heat distribution without hot spots. Hence they are suitable for systems that are targeting the highest power density with forced air cooling. Very small choke sizes are feasible.

The chosen core material is HIGH FLUX from Chang Sung Corporations (CSC), which has an excellent DC bias and good core loss behavior. The part number is CH270060E18. The outer diameter of the core is 27 mm with a height is 19 mm.
The winding was implemented using enameled copper wire AWG 16 (1.37 mm diameter). The winding covers approximately 2 layers. This arrangement allows a good copper fill factor, while still having good AC characteristics, and is a preferred fill form factor for high power toroidal inductors.

There are 46 turns, taking advantage of the high permitted DC bias. The resulting small signal bias inductance is 254 µH

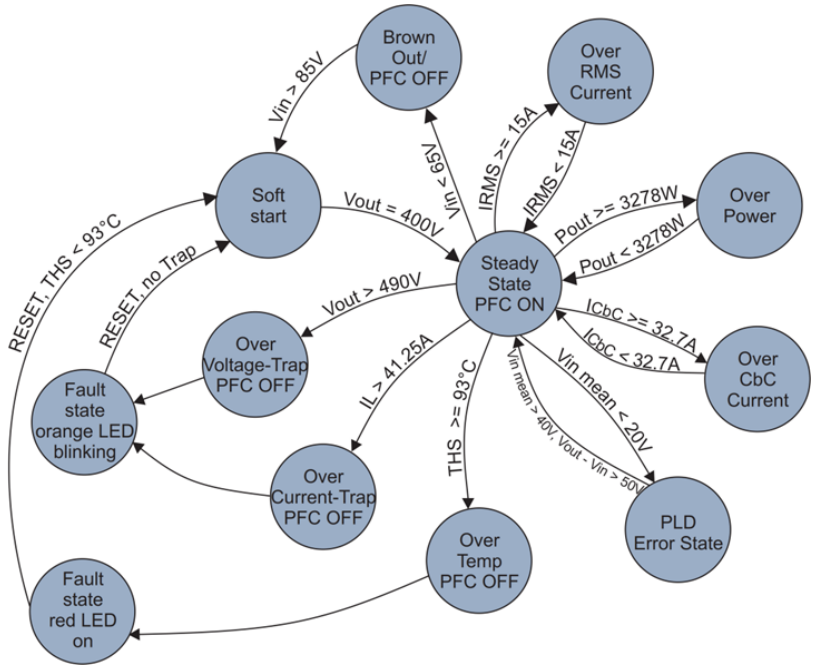
Software and control implementation



The figure on the left shows how each of the internal blocks of the XMC1302 microcontroller is connected to the topology.

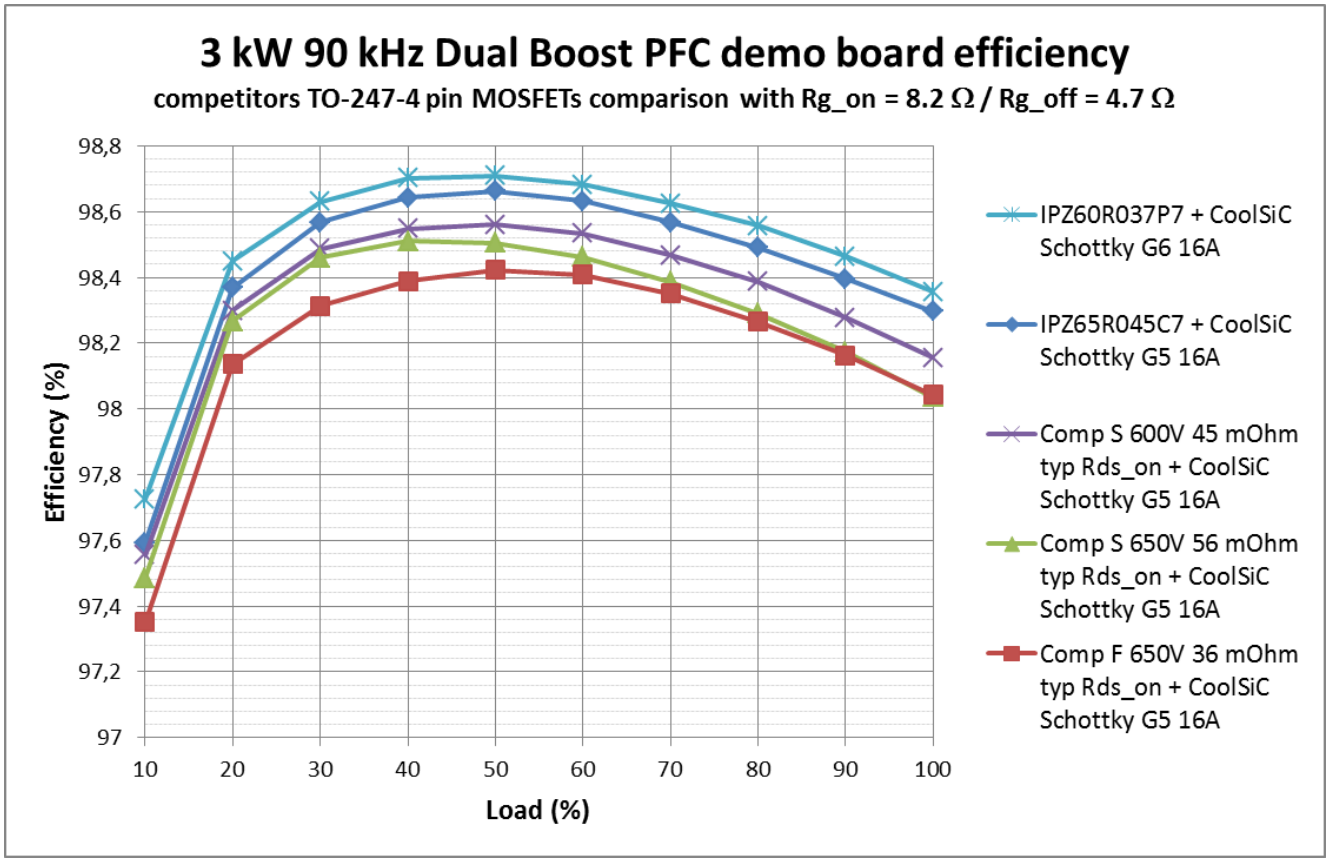
The red blocks mark the hardware units that are necessary to handle the input and output signals, respectively. Blue boxes show programmed software parts for the application and finally the grey boxes identify the abnormal conditions and their interactions.

The different states of the PFC-control which are handled in the XMC1302 software are shown in the figure on the right.

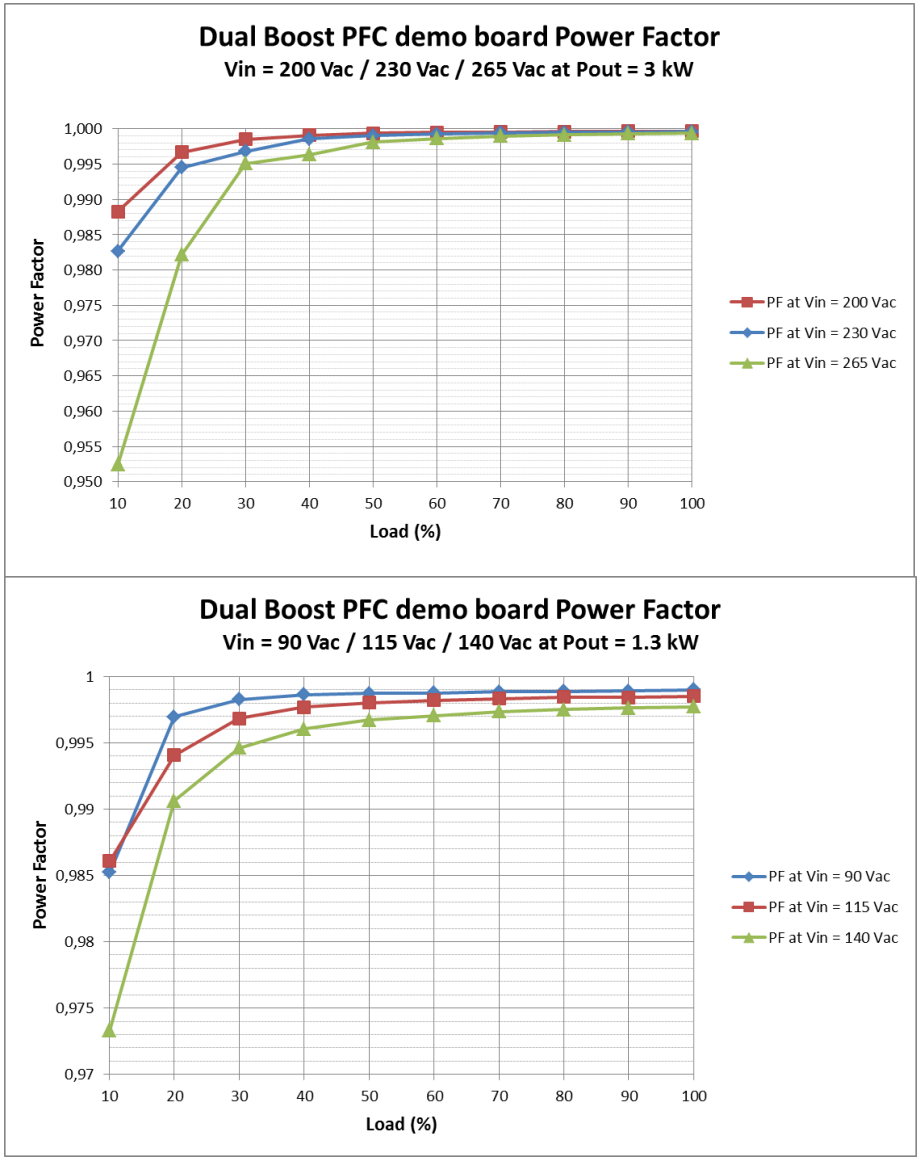


Further efficiency performance evaluation by using the latest 600 V CoolMOS™ P7 + CoolSIC™ G6

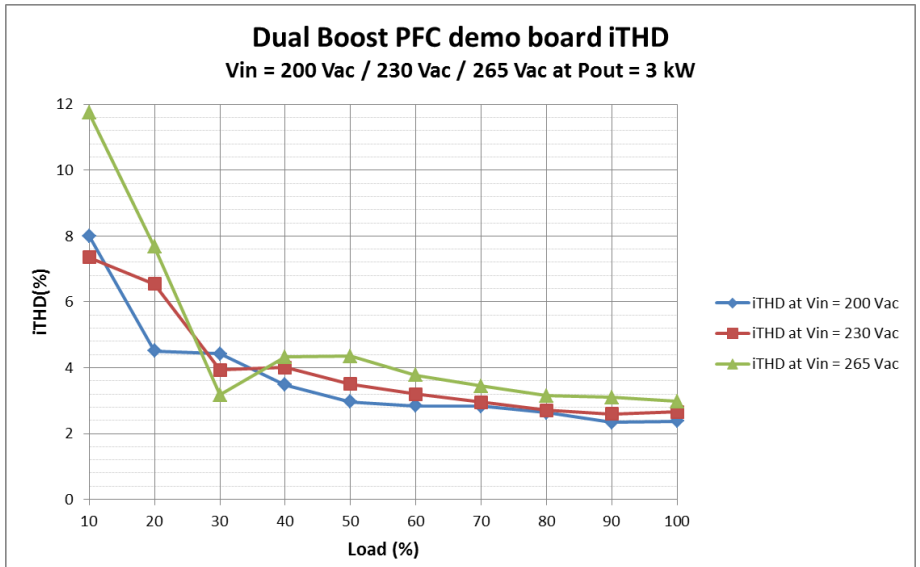
Even though it is not in the current scope of this demo board, in the outlook of product launches like 600 V CoolMOS™ P7 + CoolSIC™ Schottky diodes 650 V G6, this demo board has been used for evaluating Infineon´s latest price/performance solution. These results can be appreciated in the following figures:

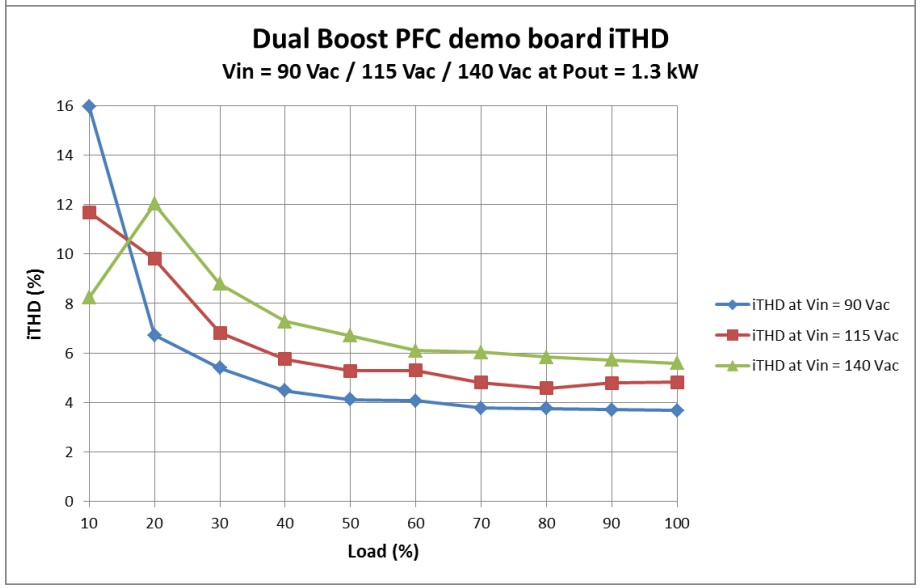


Further power factor performance evaluation by using the latest 600 V CoolMOS™ P7 + CoolSIC™ G6



Further iTHD performance evaluation by using the latest 600 V CoolMOS™ P7 + CoolSIC™ G6





Support
3 kW bridgeless dual boost PFC design

Evaluation board page

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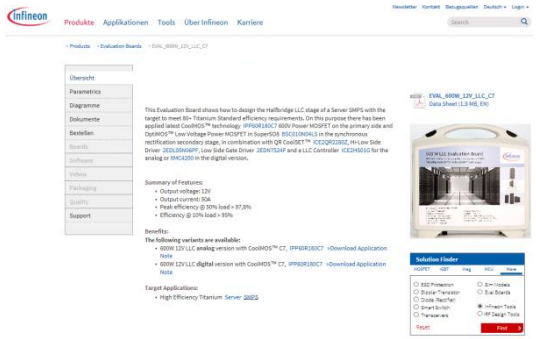

- EVAL_3KW_DB_PFC_C7

Product family pages

- Product brief
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- IDH06G65C5
- 1EDI60N12AF & 2EDN7524F
- XMC1302-T038X0200
- TLF4949
- ICE2QR4780Z

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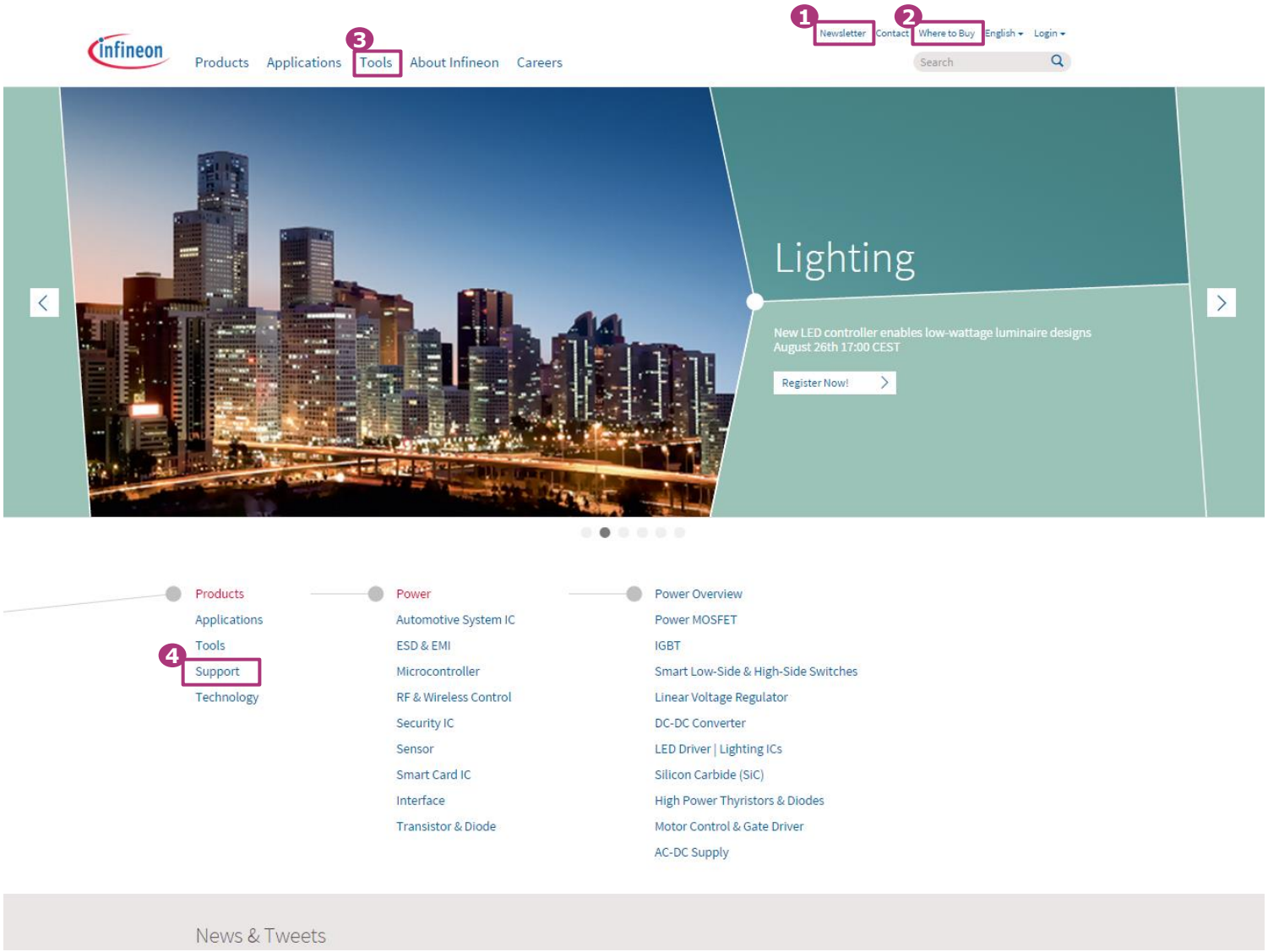
Online tools and services



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