TS5A3159
1-Ω SPDT ANALOG SWITCH

SCDS174B – AUGUST 2004 – REVISED MAY 2005

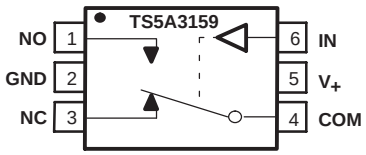
Description

The TS5A3159 is a single-pole double-throw (SPDT) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers a low ON-state resistance and an excellent ON-resistance, matching with the break-before-make feature to prevent signal distortion during the transferring of a signal from one channel to another. The device has an excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.

Applications

- **Cell Phones**
- **PDAs**
- **Portable Instrumentation**

SOT-23 OR SC-70 PACKAGE
(TOP VIEW)



FUNCTION TABLE

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

Features

- **Specified Break-Before-Make Switching**
- **Low ON-State Resistance (1 Ω)**
- **Control Inputs Are 5-V Tolerant**
- **Low Charge Injection**
- **Excellent ON-Resistance Matching**
- **Low Total Harmonic Distortion**
- **1.65-V to 5.5-V Single-Supply Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**

Summary of Characteristics

V_+ = 5 V and T_A = 25 °C

Configuration	2:1 Multiplexer/ Demultiplexer (1 × SPDT)
Number of channels	1
ON-state resistance (r_{on})	1.1 Ω
ON-state resistance match (Δr_{on})	0.1 Ω
ON-state resistance flatness ($r_{on(flat)}$)	0.15 Ω
Turn on/turn off time (t_{ON}/t_{OFF})	20 ns/15 ns
Break-before-make time (t_{BBM})	12 ns
Charge injection (Q_C)	36 pC
Bandwidth (BW)	100 MHz
OFF isolation (O_{ISO})	−65 dB at 1 MHz
Crosstalk (X_{TALK})	−65 dB at 1 MHz
Total harmonic distortion (THD)	0.01%
Leakage current ($I_{NO(OFF)}$/$I_{NC(OFF)}$)	±20 nA
Package option	6-pin DBV or DCK

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(2)
−40°C to 85°C	SOT (SOT-23) − DBV	Tape and reel	TS5A3159DBVR	JA8_
	SOT (SC-70) − DCK(2)	Tape and reel	TS5A3159DCKR	JA_

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_+	Supply voltage range(2)		−0.5	6.5	V
V_{NO}, V_{COM}	Analog voltage range(2)(3)(4)		−0.5	V_+ + 0.5	V
$I_{I/OK}$	Analog port diode current	V_{NO}, V_{COM} < 0 or V_{NO}, V_{COM} > V_+		±50	mA
I_{NO}, I_{COM}	ON−state switch current	V_{NO}, V_{COM} = 0 to V_+		±200	mA
	ON−state peak switch current(5)			±400	mA
V_{IN}	Digital input voltage range(2)(3)		−0.5	6.5	V
I_{IK}	Digital input clamp current	V_{IN} < 0		−50	mA
	Continuous current through V_+ or GND			±100	mA
θ_{JA}	Package thermal impedance(6)			165	°C
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) This value is limited to 5.5 V maximum.
(5) Pulse at 1 ms duration < 10% duty cycle.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

Electrical Characteristics for 5-V Supply

V_+ = 4.5 V to 5.5 V and T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
Peak ON resistance	r_{peak}	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = −30 mA,	Switch ON, See Figure 11	25°C	4.5 V		1	1.5	Ω
				Full				1.5	
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 2.5 V, I_{COM} = −30 mA,	Switch ON, See Figure 11	25°C	4.5 V		0.75	1.1	Ω
				Full				1.1	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 2.5 V, I_{COM} = −30 mA,	Switch ON, See Figure 11	25°C	4.5 V		0.1		Ω
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = −30 mA,	Switch ON, See Figure 11	25°C	4.5 V		0.233		Ω
		V_{NO} or V_{NC} = 1 V, 1.5 V, 2.5 V, I_{COM} = −30 mA,		25°C			0.15		
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 4.5 V, V_{COM} = 0,	Switch OFF, See Figure 12	25°C	5.5 V	−2	0.2	2	nA
				Full		−20		20	
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 4.5 V, V_{COM} = Open,	Switch ON, See Figure 13	25°C	5.5 V	−4	2.8	4	nA
				Full		−40		40	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = 4.5 V or Open, V_{COM} = 4.5 V,	Switch ON, See Figure 13	25°C	5.5 V	−4	0.47	4	nA
				Full		−40		40	
Digital Inputs (IN)									
Input logic high	V_{IH}			Full		2.4		5.5	V
Input logic low	V_{IL}			Full		0		0.8	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = 5.5 V or 0		Full	5.5 V	−1		1	µA

(1) T_A = 25°C

Electrical Characteristics for 5-V Supply (continued)

V_+ = 4.5 V to 5.5 V and T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 15	25°C	4.5 V to 5.5 V		20	35	ns
				Full				40	
Turn-off time	t_{OFF}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 15	25°C	4.5 V to 5.5 V		15	20	ns
				Full				35	
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, See Figure 16	25°C	4.5 V to 5.5 V	1	12	14.5	ns
				Full		1			
Charge injection	Q_C	C_L = 1 nF, V_{GEN} = 0 V,	See Figure 20	25°C	5 V		36		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 14	25°C	5 V		23		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_+ or GND, Switch ON,	See Figure 14	25°C	5 V		84		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 14	25°C	5 V		84		pF
Digital input capacitance	C_{IN}	V_{IN} = V_+ or GND,	See Figure 14	25°C	5 V		2.1		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 17	25°C	5 V		100		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 18	25°C	5 V		−65		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 19	25°C	5 V		−65		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 600 Hz to 20 kHz, See Figure 21	25°C	5 V		0.01		%
Supply									
Positive supply current	I_+	V_{IN} = V_+ or GND,	Switch ON or OFF	Full	5.5 V			0.1	µA

(1) T_A = 25°C

Electrical Characteristics for 3.3-V Supply

V_+ = 3 V to 3.6 V and T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
Peak ON-state resistance	r_{peak}	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = −24 mA,	Switch ON, See Figure 11	25°C	3 V		1.35	2.1	Ω
				Full				2.1	
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 2 V, I_{COM} = −24 mA,	Switch ON, See Figure 11	25°C	3 V		1.15	1.5	Ω
				Full				1.5	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 2 V, 0.8 V, I_{COM} = −24 mA,	Switch ON, See Figure 11	25°C	3 V		0.11		Ω
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = −24 mA,	Switch ON, See Figure 11	25°C	3 V		0.225		Ω
		V_{NO} or V_{NC} = 2 V, 0.8 V, I_{COM} = −24 mA,		25°C			0.25		
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 3 V, V_{COM} = 0,	Switch OFF, See Figure 12	25°C	3.6 V		0.2		nA
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 3 V, V_{COM} = Open,	Switch ON, See Figure 13	25°C	3.6 V		2.8		nA
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = 3 V or Open, V_{COM} = 3 V,	Switch ON, See Figure 13	25°C	3.6 V		0.47		nA
Digital Inputs (IN)									
Input logic high	V_{IH}			Full		2		5.5	V
Input logic low	V_{IL}			Full		0	0.6		V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = 5.5 V or 0		Full	3.6 V	−1		1	µA

(1) T_A = 25°C

Electrical Characteristics for 3.3-V Supply (continued)

(V_+ = 3 V to 3.6 V and T_A = −40 °C to 85 °C) (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 15	25°C	3 V to 3.6 V		30	40	ns
				Full				55	
Turn-off time	t_{OFF}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 15	25°C	3 V to 3.6 V		20	25	ns
				Full				40	
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, See Figure 16	25°C	3 V to 3.6 V	1	21	29	ns
				Full		1			
Charge injection	Q_C	C_L = 1 nF, V_{GEN} = 0 V,	See Figure 20	25°C	3.3 V		20		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 14	25°C	3.3 V		23		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_+ or GND, Switch ON,	See Figure 14	25°C	3.3V		84		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 14	25°C	3.3 V		84		pF
Digital input capacitance	C_{IN}	V_{IN} = V_+ or GND,	See Figure 14	25°C	3.3 V		2.1		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 17	25°C	3.3 V		100		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 18	25°C	3.3 V		−65		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 19	25°C	3.3 V		−65		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 600 Hz to 20 kHz, See Figure 21	25°C	3.3 V		0.015		%
Supply									
Positive supply current	I_+	V_{IN} = V_+ or GND,	Switch ON or OFF	Full	3.6 V			0.1	µA

(1) T_A = 25°C

Electrical Characteristics for 2.5-V Supply

V_+ = 2.3 V to 2.7 V and T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
Peak ON-state resistance	r_{peak}	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = −8 mA,	Switch ON, See Figure 11	25°C	2.5 V		1.7	2.7	Ω
				Full				2.7	
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 1.8 V, I_{COM} = −8 mA,	Switch ON, See Figure 11	25°C	2.5 V		1.45	2	Ω
				Full				2	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 0.8 V, 1.8 V, I_{COM} = −8 mA,	Switch ON, See Figure 11	25°C	2.5 V		0.7		Ω
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = −8 mA,	Switch ON, See Figure 11	25°C	2.5 V		0.5		Ω
		V_{NO} or V_{NC} = 0.8 V, 1.8 V, I_{COM} = −8 mA,		25°C			0.45		
NC, NO Off leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 2.3 V, V_{COM} = 0,	Switch OFF, See Figure 12	25°C	2.7 V		0.2		nA
NC, NO On leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 2.3 V, V_{COM} = Open,	Switch ON, See Figure 13	25°C	2.7 V		2.8		nA
COM On leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = 2.3 V or Open, V_{COM} = 2.3 V,	Switch ON, See Figure 13	25°C	2.7 V		0.47		nA
Digital Inputs (IN)									
Input logic high	V_{IH}			Full		1.8		5.5	V
Input logic low	V_{IL}			Full		0		0.6	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = 5.5 V or 0		Full	2.7 V	−1		1	µA

(1) T_A = 25°C

Electrical Characteristics for 2.5-V Supply (continued)

V_+ = 2.3 V to 2.7 V and T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 15	25°C	2.3 V to 2.7 V		40	55	ns
				Full				70	
Turn-off time	t_{OFF}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 15	25°C	2.3 V to 2.7 V		30	40	ns
				Full				55	
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, See Figure 16	25°C	2.3 V to 2.7 V	1	33	39	ns
				Full		1			
Charge injection	Q_C	C_L = 1 nF, V_{GEN} = 0 V,	See Figure 20	25°C	2.5 V		13		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 14	25°C	2.5 V		23		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_+ or GND, Switch ON,	See Figure 14	25°C	2.5V		84		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 14	25°C	2.5 V		84		pF
Digital input capacitance	C_{IN}	V_{IN} = V_+ or GND,	See Figure 14	25°C	2.5 V		2.1		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 17	25°C	2.5 V		100		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 18	25°C	2.5 V		−64		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 19	25°C	2.5 V		−64		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 600 Hz to 20 kHz, See Figure 21	25°C	2.5 V		0.025		%
Supply									
Positive supply current	I_+	V_{IN} = V_+ or GND,	Switch ON or OFF	Full	2.7 V			0.1	µA

(1) T_A = 25°C

Electrical Characteristics for 1.8-V Supply

V_+ = 1.65 V to 1.95 V and T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
Peak ON-state resistance	r_{peak}	$0 \le V_{NO}$ or $V_{NC} \le V_+$, I_{COM} = −2 mA,	Switch ON, See Figure 11	25°C	1.8 V		4	4.9	Ω
				Full				4.9	
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 1.5 V, I_{COM} = −2 mA,	Switch ON, See Figure 11	25°C	1.8 V		1.7	3.2	Ω
				Full				3.2	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 0.6 V, 1.5 V, I_{COM} = −2 mA,	Switch ON, See Figure 11	25°C	1.8 V		0.7		Ω
				Full			0.7		
ON-state resistance flatness	$r_{on(flat)}$	$0 \le V_{NO}$ or $V_{NC} \le V_+$, I_{COM} = −2 mA,	Switch ON, See Figure 11	25°C	1.8 V		1.85		Ω
				Full			1.85		
		V_{NO} or V_{NC} = 0.6 V, 1.5 V, I_{COM} = −2 mA,		25°C			0.9		
				Full			0.9		
NC, NO Off leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 1.65 V, V_{COM} = 0,	Switch OFF, See Figure 12	25°C	1.95 V		0.2		nA
NC, NO On leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 1.65 V, V_{COM} = Open,	Switch ON, See Figure 13	25°C	1.95 V		2.8		nA
COM On leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = 1.65 V or Open, V_{COM} = 1.65 V,	Switch ON, See Figure 13	25°C	1.95 V		0.47		nA
Digital Inputs (IN)									
Input logic high	V_{IH}			Full		1.5		5.5	V
Input logic low	V_{IL}			Full		0		0.6	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = 5.5 V or 0		Full	1.95 V	−1		1	µA

(1) T_A = 25°C

Electrical Characteristics for 1.8-V Supply (continued)

V_+ = 1.65 V to 1.95 V and T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 15	25°C	1.65 V to 1.95 V		65	70	ns
				Full				95	
Turn-off time	t_{OFF}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 15	25°C	1.65 V to 1.95 V		40	55	ns
				Full				70	
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, See Figure 16	25°C	1.65 V to 1.95 V	1	60	72	ns
				Full		0.5			
Charge injection	Q_C	C_L = 1 nF, V_{GEN} = 0 V,	See Figure 20	25°C	1.8 V		13		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 14	25°C	1.8 V		23		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_+ or GND, Switch ON,	See Figure 14	25°C	1.8V		84		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 14	25°C	1.8 V		84		pF
Digital input capacitance	C_{IN}	V_{IN} = V_+ or GND,	See Figure 14	25°C	1.8 V		2.1		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 17	25°C	1.8 V		100		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 18	25°C	1.8 V		−63		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 19	25°C	1.8 V		−63		dB
Supply									
Positive supply current	I_+	V_{IN} = V_+ or GND,	Switch ON or OFF	Full	1.95 V			0.1	µA

(1) T_A = 25°C

TYPICAL PERFORMANCE

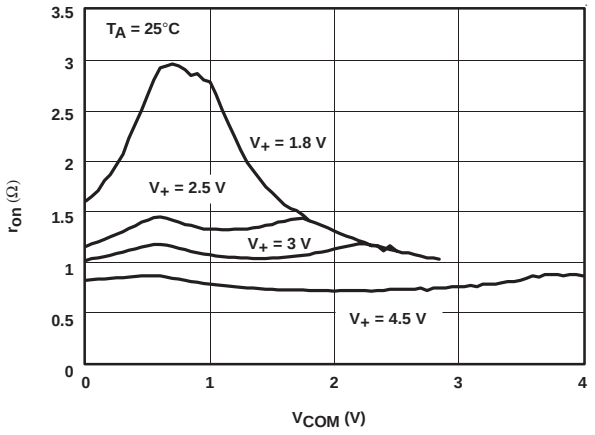


Figure 1. r_{on} vs V_{COM}

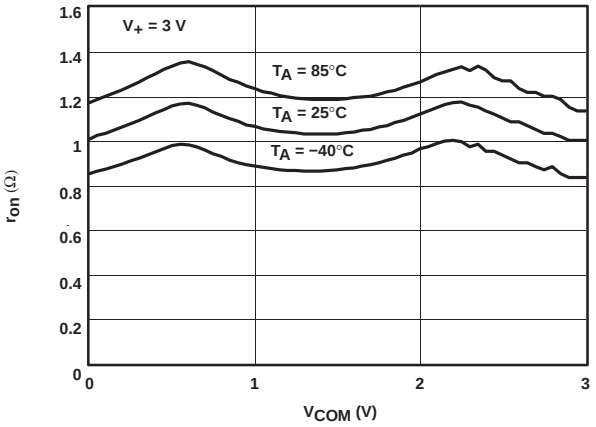


Figure 2. r_{on} vs V_{COM}

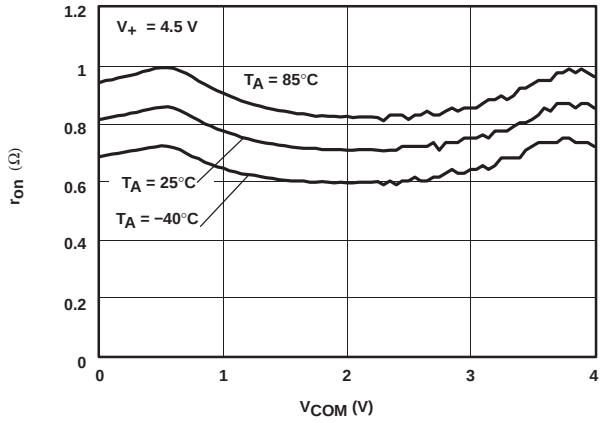


Figure 3. r_{on} vs V_{COM}

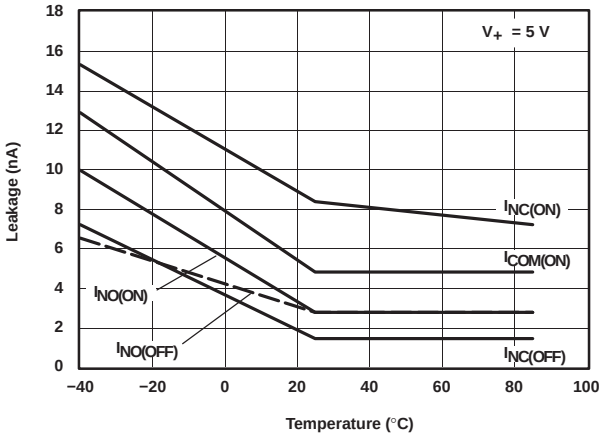


Figure 4. Leakage Current vs Temperature

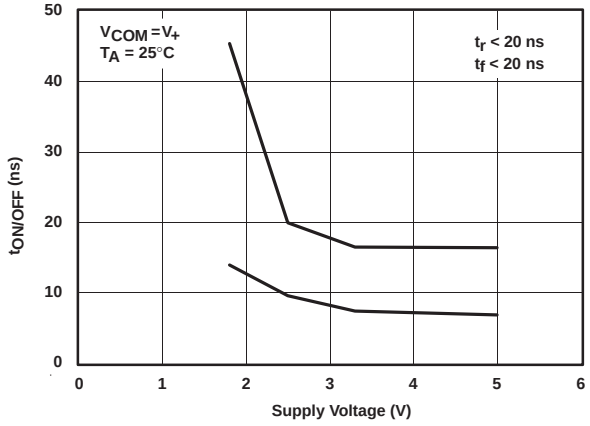


Figure 5. $t_{ON/OFF}$ vs V_+

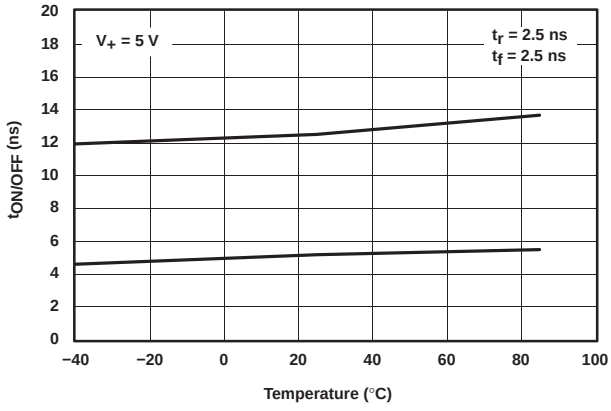


Figure 6. $t_{ON/OFF}$ vs Temperature

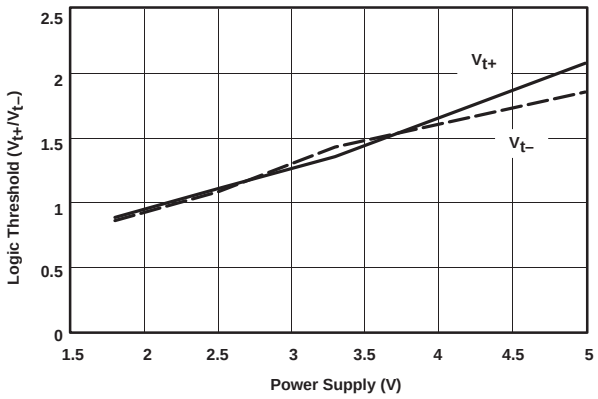


Figure 7. Logic Threshold vs Power Supply

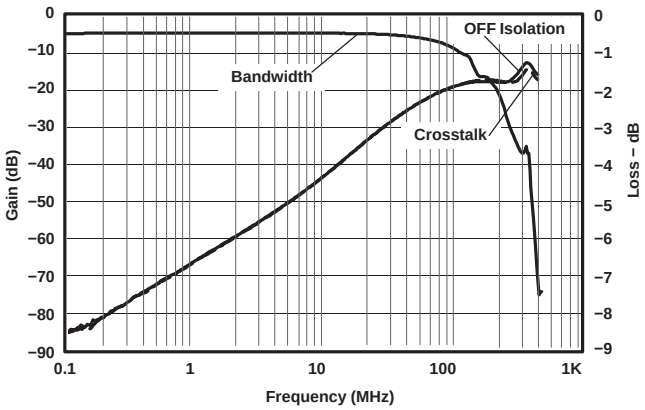


Figure 8. Frequency Response

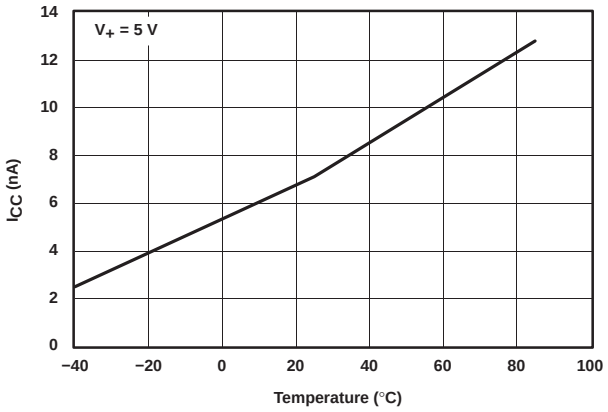


Figure 9. Power-Supply Current vs Temperature

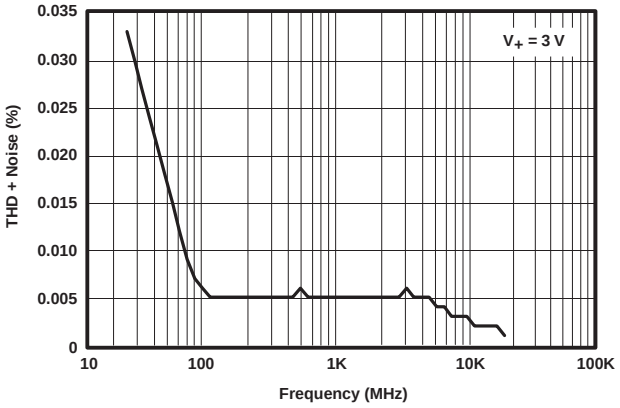


Figure 10. Total Harmonic Distortion (THD) vs Frequency

PIN DESCRIPTION

PIN NUMBER	NAME	DESCRIPTION
1	NO	Normally-open terminal
2	GND	Digital ground
3	NC	Normally-closed terminal
4	COM	Common terminal
5	V_+	Power supply
6	IN	Digital control pin to connect COM terminal to NO or NC terminals

PARAMETER DESCRIPTION

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NC}	Voltage at NC
V_{NO}	Voltage at NO
r_{on}	Resistance between COM and NC or COM and NO ports, when the channel is ON
r_{peak}	Peak ON-state resistance over a specified voltage range
Δr_{on}	Difference of r_{on} between channels
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state under worst-case input and output conditions
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) being open
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) being open
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) being open
V_{IH}	Minimum input voltage for logic high for the control input (IN)
V_{IL}	Minimum input voltage for logic low for the control input (IN)
V_{IN}	Voltage at IN
I_{IH}, I_{IL}	Leakage current measured at IN
t_{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog outputs (COM, NC, or NO) signal, when the switch is turning ON.
t_{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog outputs (COM, NC, or NO) signal, when the switch is turning OFF.
t_{BBM}	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO), when the control signal changes state.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_O$, C_L is the load capacitance, and ΔV_O is the change in analog output voltage.

PARAMETER DESCRIPTION (continued)

SYMBOL	DESCRIPTION
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON
C_{IN}	Capacitance of IN
O_{ISO}	OFF isolation of the switch is a measurement OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is −3 dB below the DC gain.
I_+	Static power-supply current with the control (IN) pin at V_+ or GND
ΔI_+	This is the increase in I_+ for each control (IN) input that is at the specified voltage, rather than at V_+ or GND.

PARAMETER MEASUREMENT INFORMATION

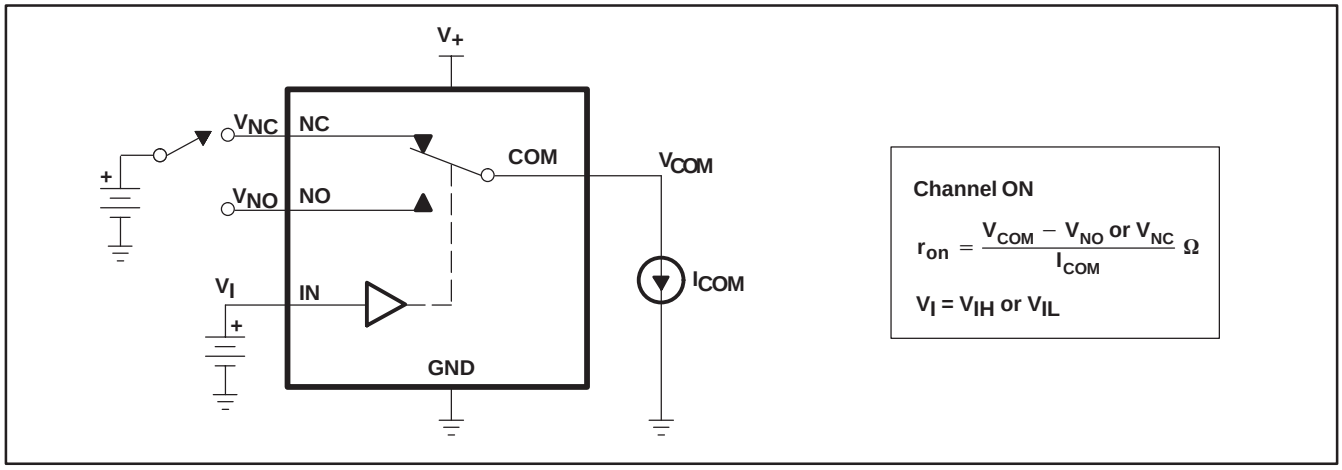


Figure 11. ON-State Resistance (r_{on})

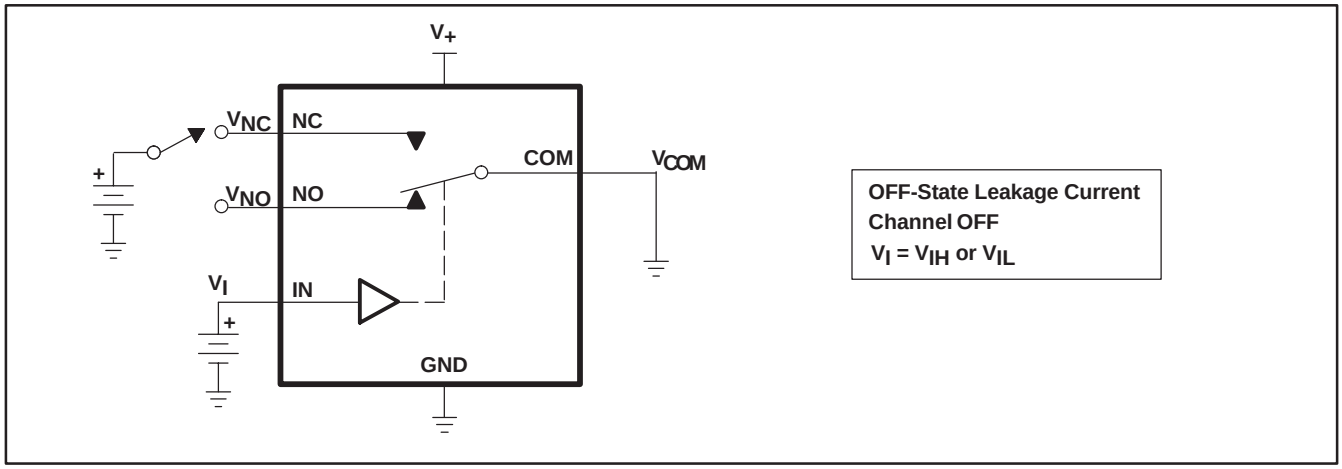


Figure 12. OFF-State Leakage Current ($I_{NC(OFF)}$, $I_{NO(OFF)}$)

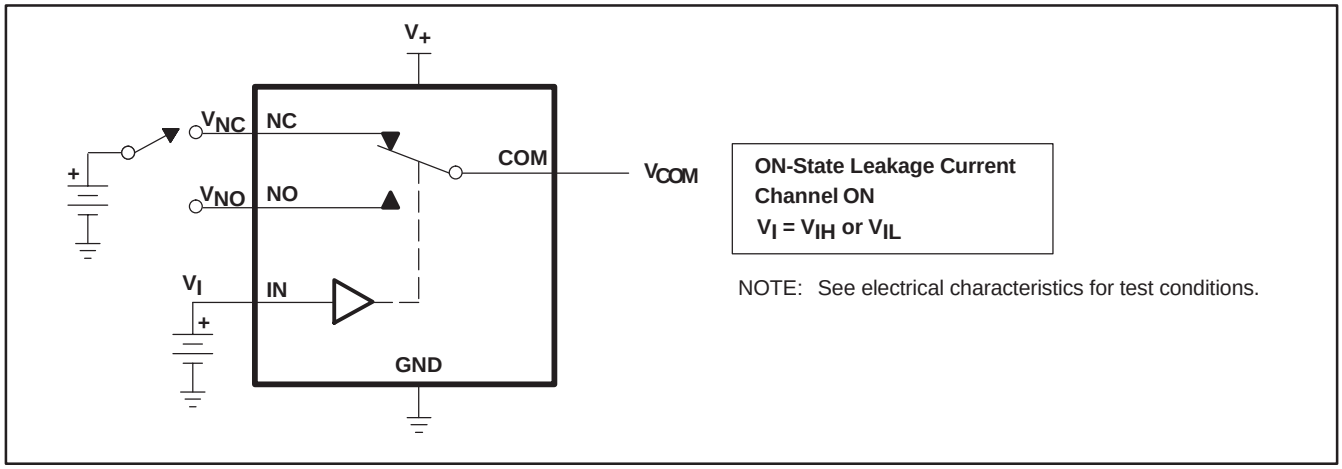


Figure 13. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)

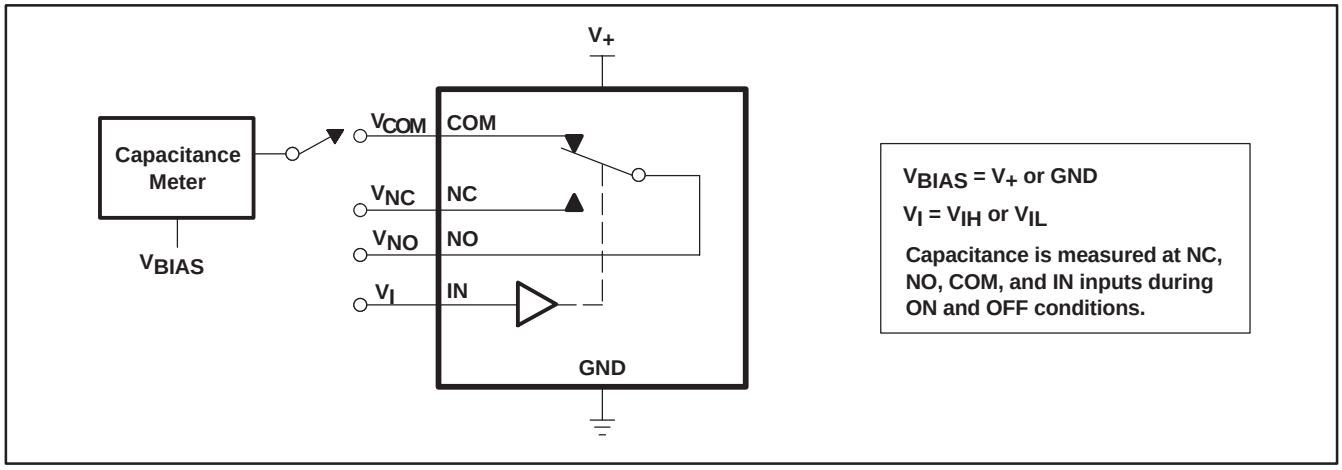
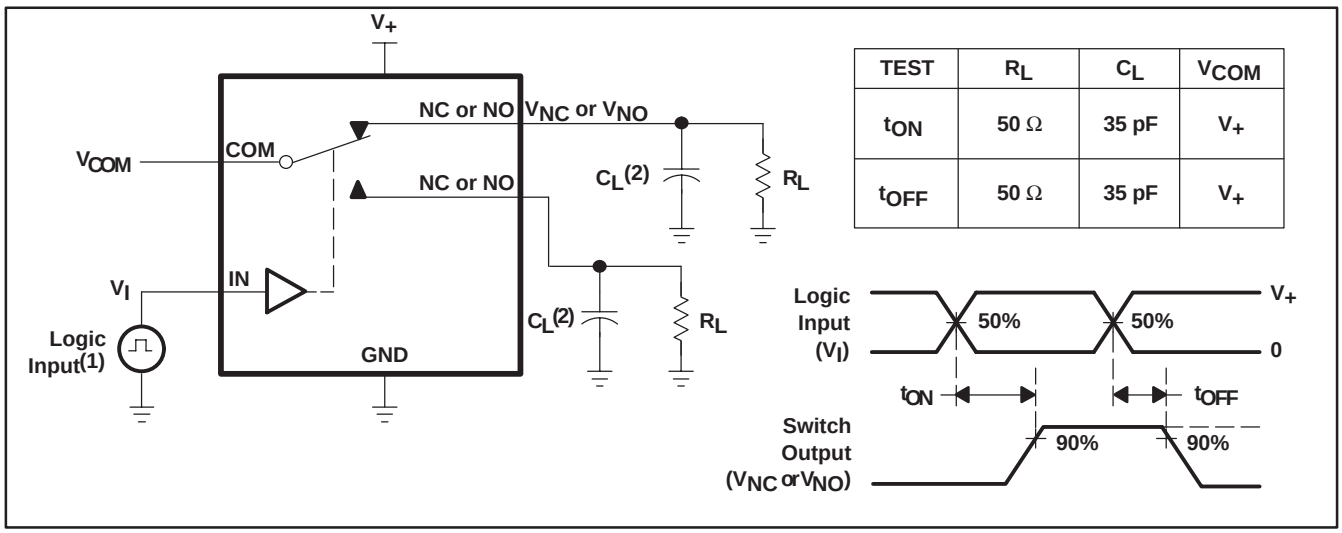


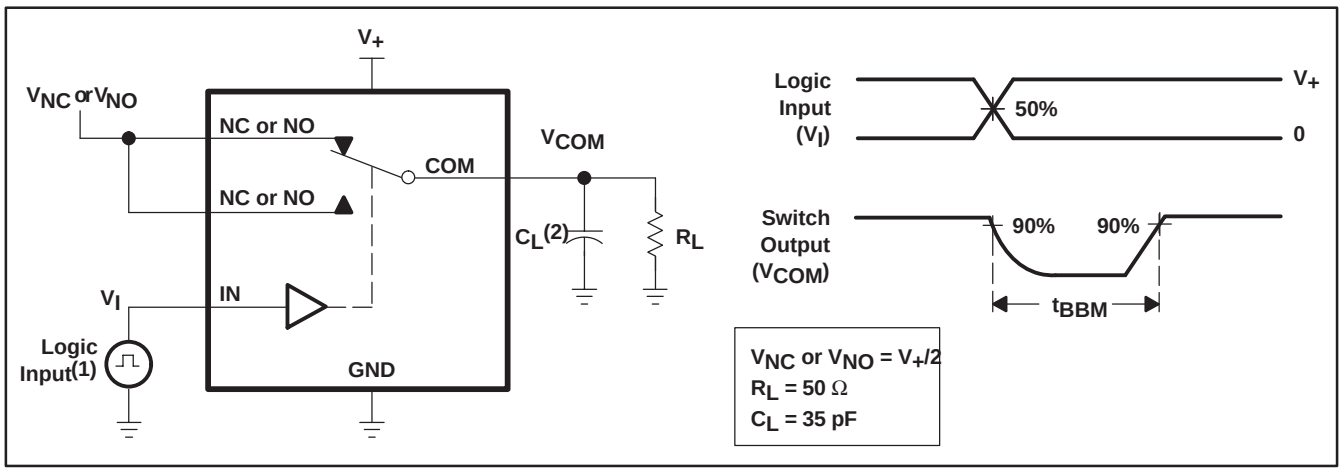
Figure 14. Capacitance (C_I, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)



TEST	R_L	C_L	V_{COM}
t_{ON}	50 Ω	35 pF	V_+
t_{OFF}	50 Ω	35 pF	V_+

(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
(2) C_L includes probe and jig capacitance.

Figure 15. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
(2) C_L includes probe and jig capacitance.

Figure 16. Break-Before-Make Time (t_{BBM})

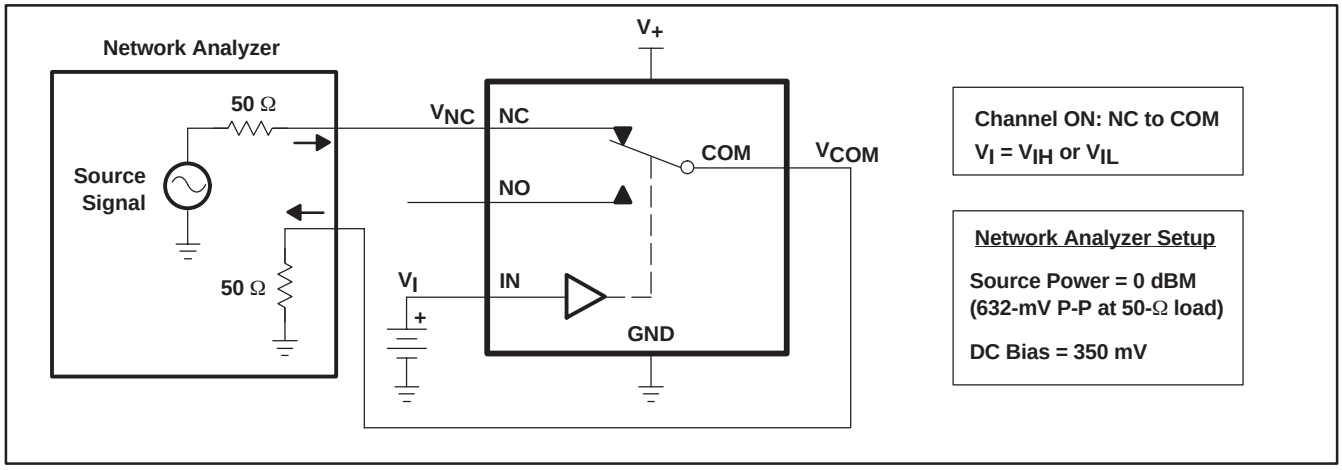


Figure 17. Bandwidth (BW)

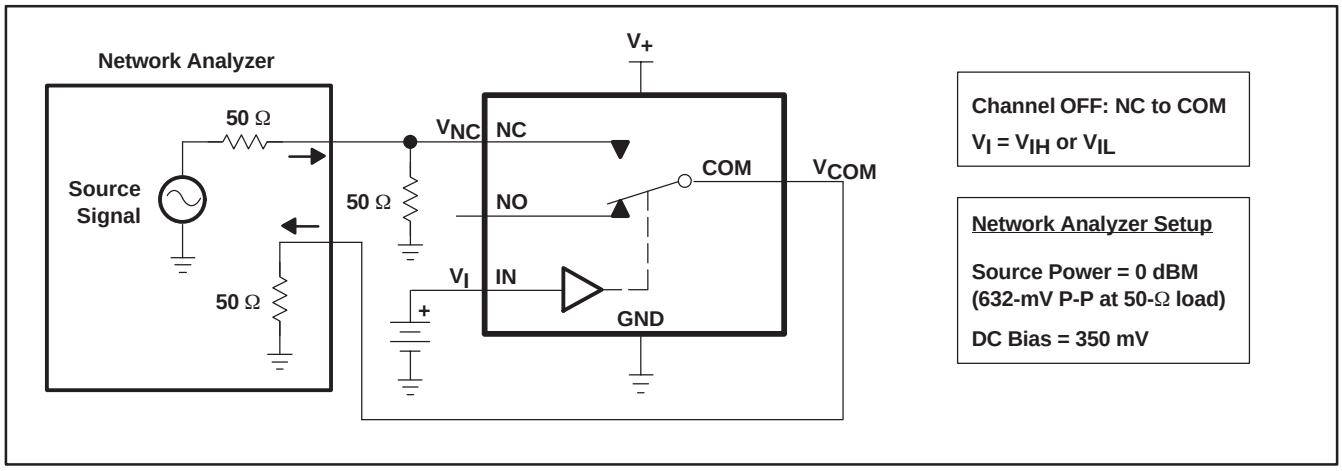


Figure 18. OFF Isolation (O_{ISO})

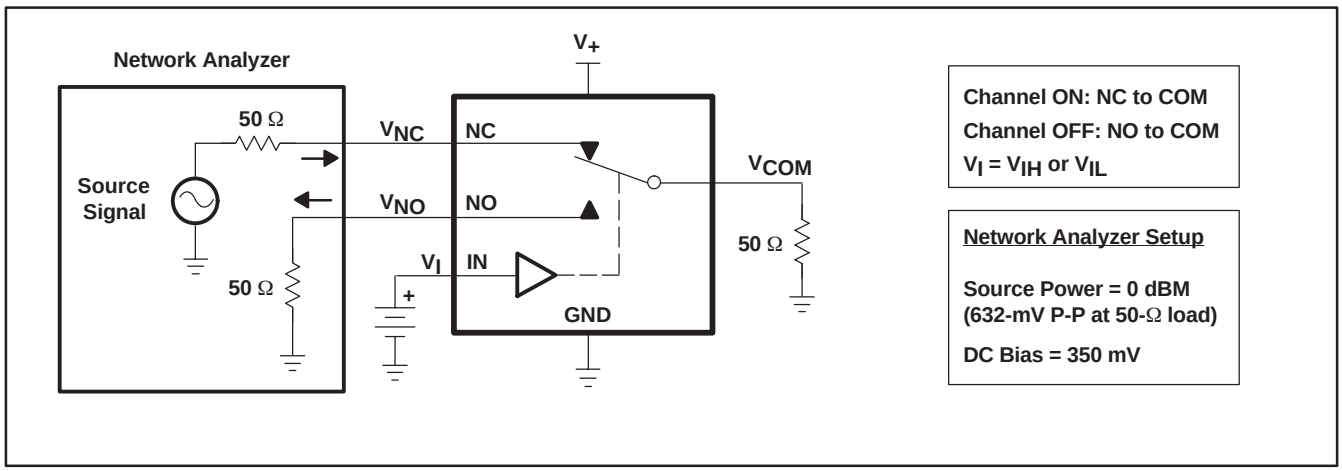
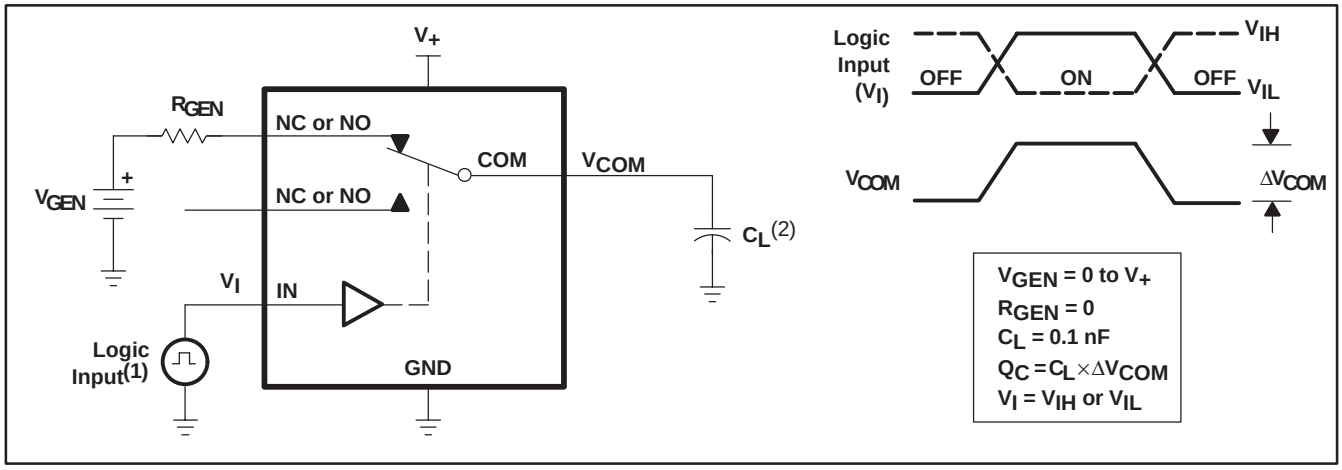
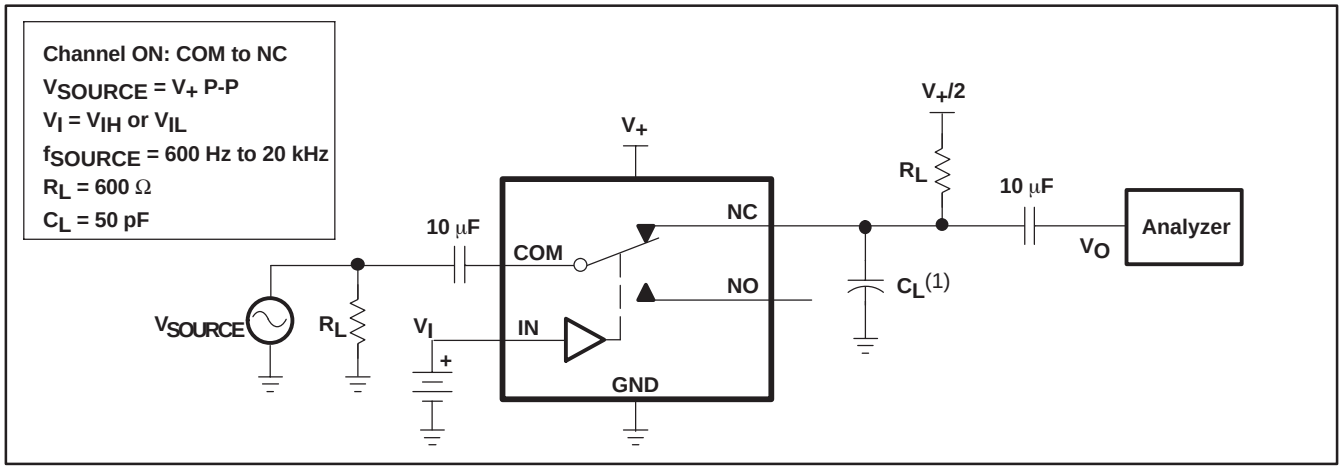


Figure 19. Crosstalk (X_{TALK})



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
(2) C_L includes probe and jig capacitance.

Figure 20. Charge Injection (Q_C)



(1) C_L includes probe and jig capacitance.

Figure 21. Total Harmonic Distortion (THD)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TS5A3159DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JA8K ~ JA8R)	Samples
TS5A3159DBVRE4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JA8K ~ JA8R)	Samples
TS5A3159DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JA8K ~ JA8R)	Samples
TS5A3159DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JA8K ~ JA8R)	Samples
TS5A3159DBVTE4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JA8K ~ JA8R)	Samples
TS5A3159DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JA8K ~ JA8R)	Samples
TS5A3159DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JAK ~ JAR ~ JAZ)	Samples
TS5A3159DCKRE4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JAK ~ JAR ~ JAZ)	Samples
TS5A3159DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JAK ~ JAR ~ JAZ)	Samples
TS5A3159DCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JAK ~ JAR ~ JAZ)	Samples
TS5A3159DCKTE4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JAK ~ JAR ~ JAZ)	Samples
TS5A3159DCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JAK ~ JAR ~ JAZ)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

OTHER QUALIFIED VERSIONS OF TS5A3159 :

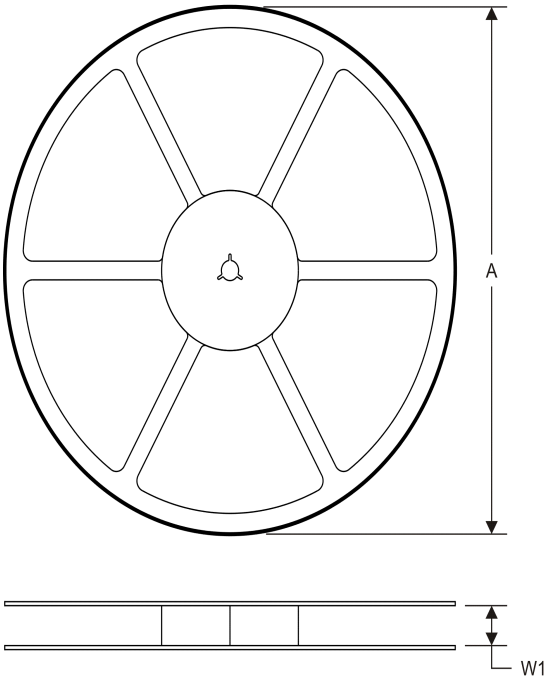
- Automotive: TS5A3159-Q1
- Enhanced Product: TS5A3159-EP

NOTE: Qualified Version Definitions:

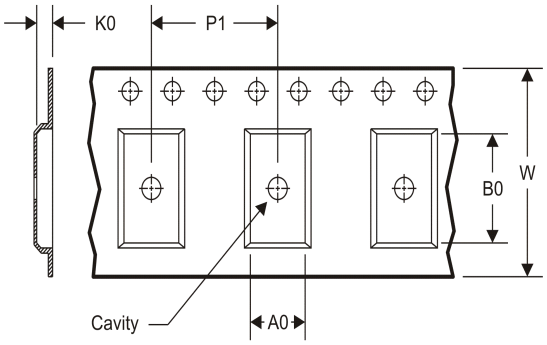
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



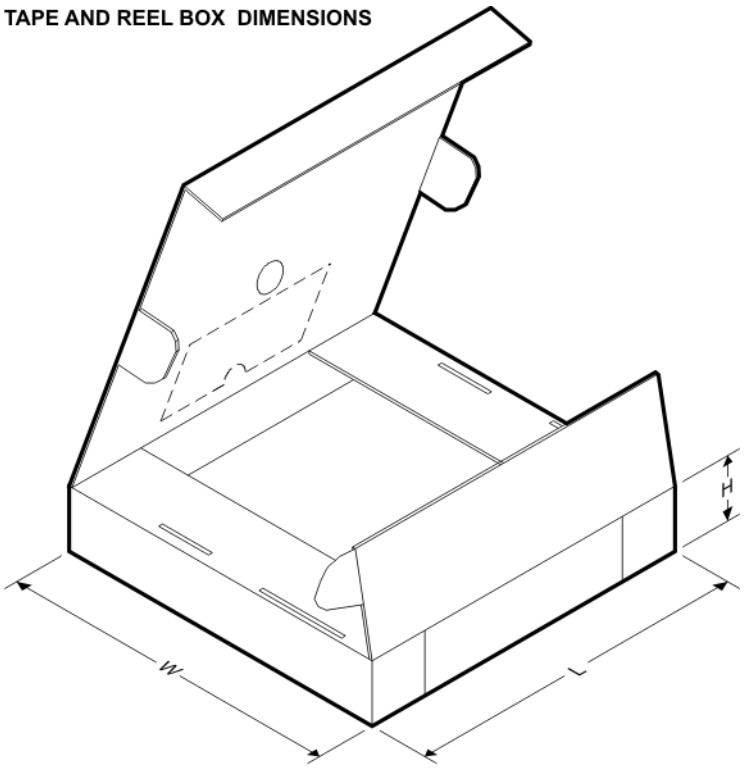
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3159DBVR	SOT-23	DBV	6	3000	180.0	9.2	3.17	3.23	1.37	4.0	8.0	Q3
TS5A3159DBVT	SOT-23	DBV	6	250	180.0	9.2	3.17	3.23	1.37	4.0	8.0	Q3
TS5A3159DCKR	SC70	DCK	6	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
TS5A3159DCKT	SC70	DCK	6	250	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3

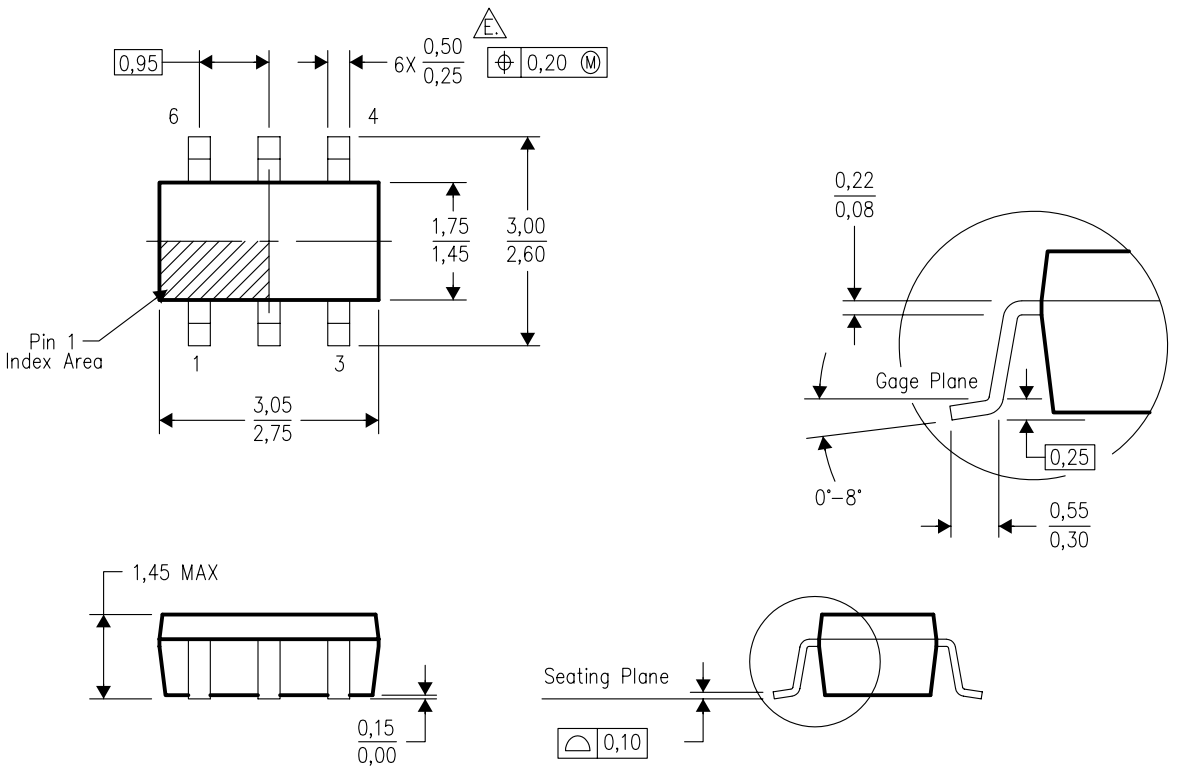
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A3159DBVR	SOT-23	DBV	6	3000	205.0	200.0	33.0
TS5A3159DBVT	SOT-23	DBV	6	250	205.0	200.0	33.0
TS5A3159DCKR	SC70	DCK	6	3000	205.0	200.0	33.0
TS5A3159DCKT	SC70	DCK	6	250	205.0	200.0	33.0

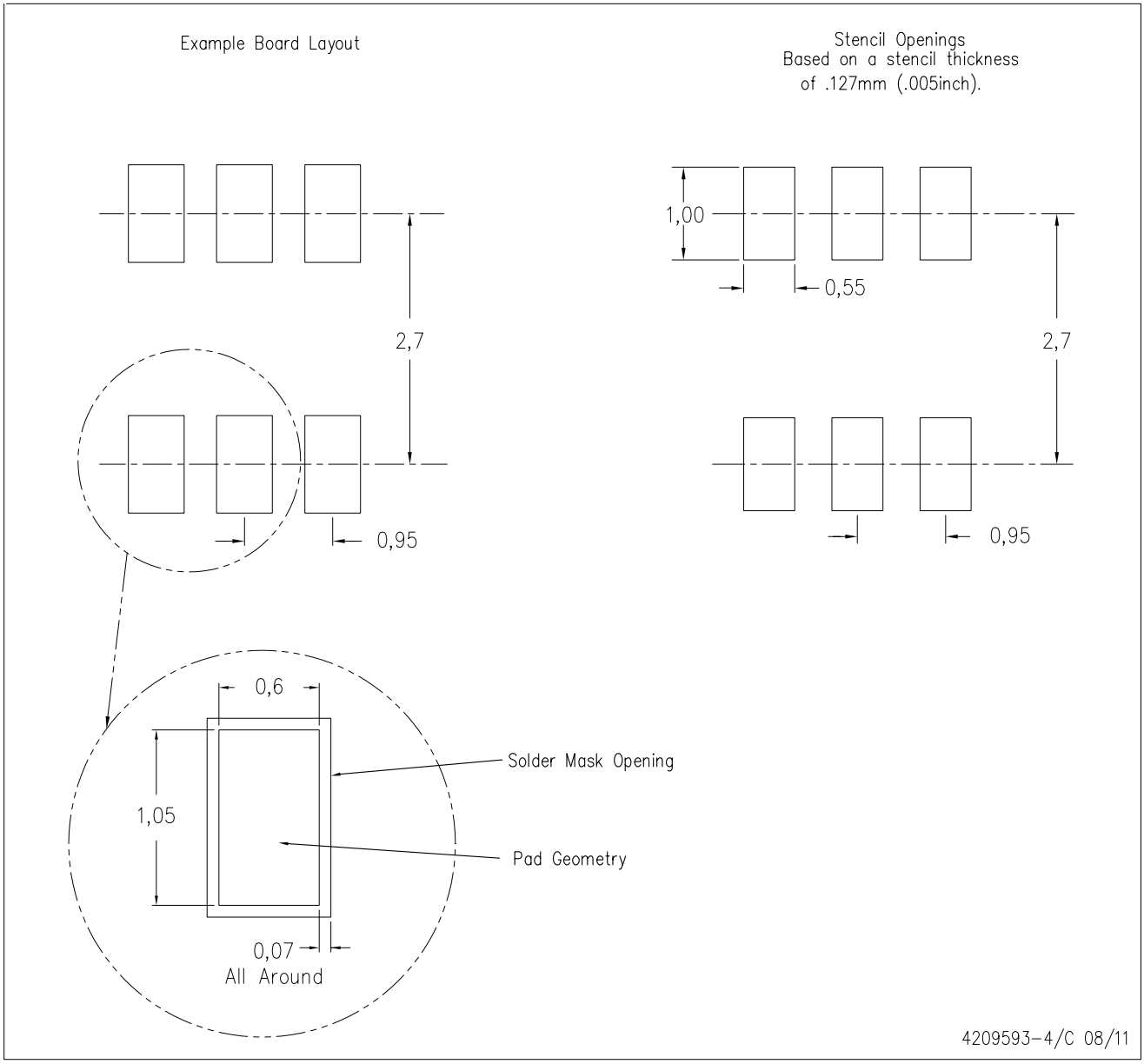
DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4073253–5/K 03/2006

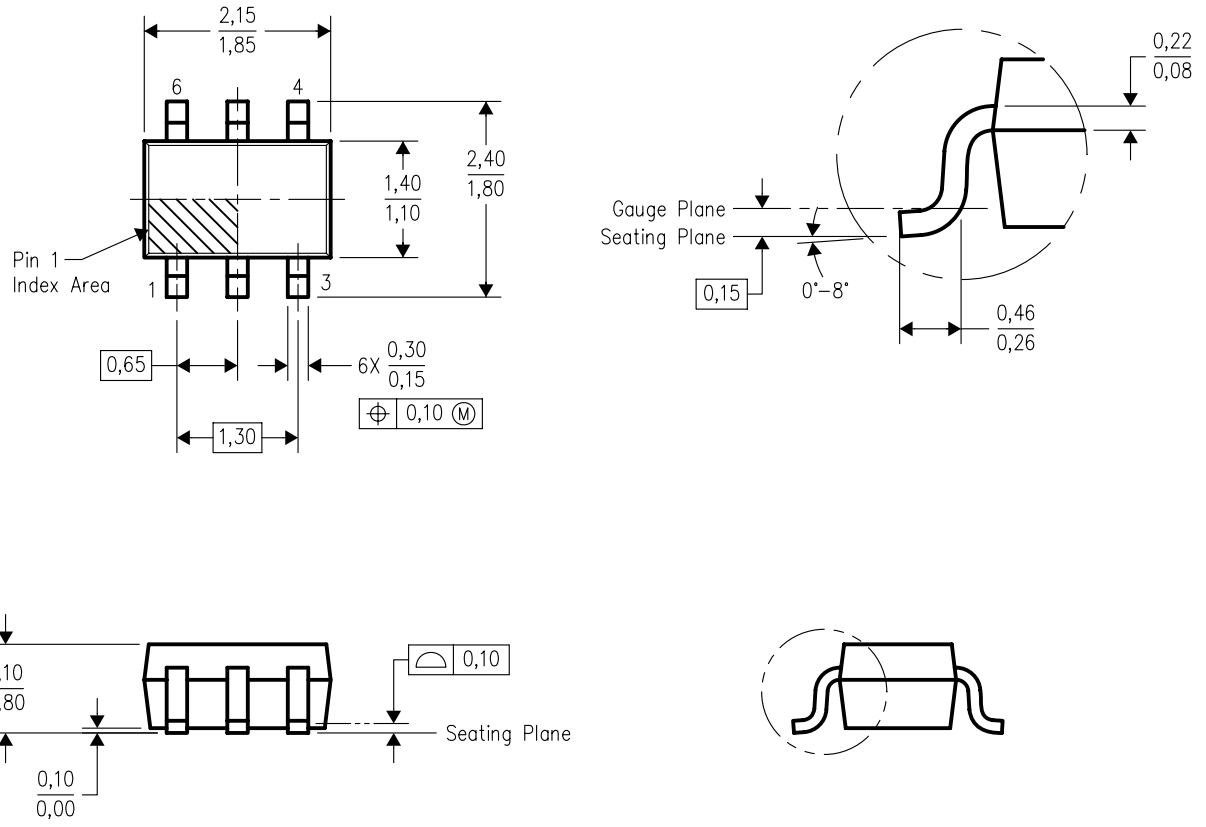
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

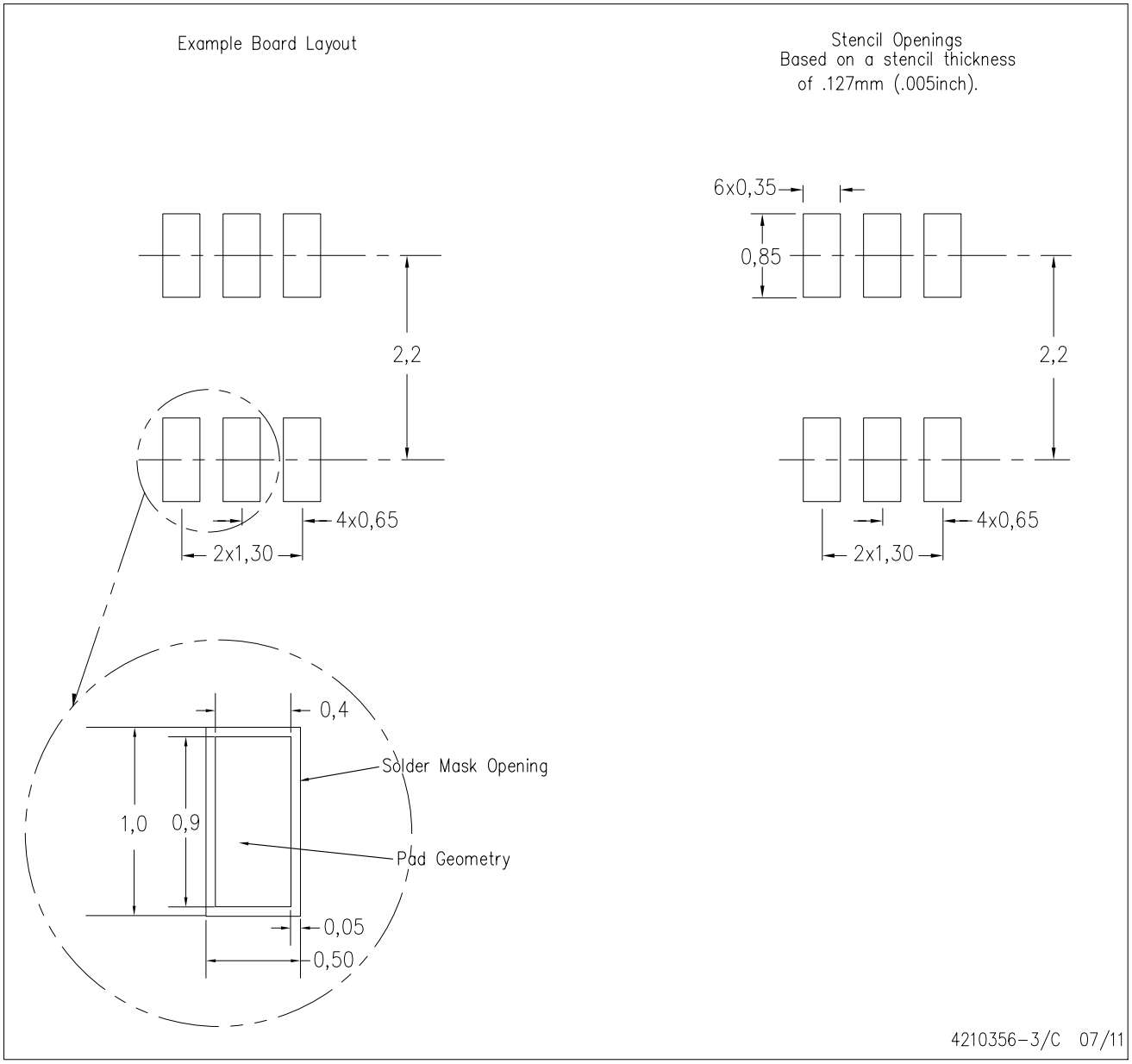
DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4093553–4/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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