



# PSMN2R0-30BL

N-channel 30 V 2.1 mΩ logic level MOSFET in D2PAK

Rev. 1 — 20 March 2012

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel MOSFET in D2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

### 1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources

### 1.3 Applications

- DC-to-DC converters
- Motor control
- Load switching
- Server power supplies

### 1.4 Quick reference data

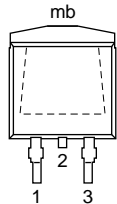
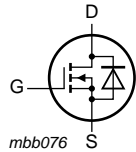
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	30	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see <a href="#">Figure 1</a> <sup>[1]</sup>	-	-	100	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ see <a href="#">Figure 2</a>	-	-	211	W
$T_j$	junction temperature		-55	-	175	°C
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 100\text{ °C};$ see <a href="#">Figure 12</a> ; see <a href="#">Figure 11</a>	-	2.51	2.9	mΩ
		$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C};$ see <a href="#">Figure 11</a>	-	1.79	2.1	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 4.5\text{ V}; I_D = 25\text{ A}; V_{DS} = 15\text{ V};$ see <a href="#">Figure 13</a> ; see <a href="#">Figure 14</a>	-	16	-	nC
$Q_{G(tot)}$	total gate charge		-	55	-	nC
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C}; I_D = 100\text{ A}; V_{sup} \leq 30\text{ V}; R_{GS} = 50\text{ Ω};$ unclamped	-	-	555	mJ

[1] Continuous current is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain <sup>[1]</sup>		
3	S	source		
mb	D	mounting base; connected to drain		

SOT404 (D2PAK)

[1] It is not possible to make connection to pin 2

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN2R0-30BL	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Marking

Table 4. Marking codes

Type number	Marking code
PSMN2R0-30BL	PSMN2R0-30BL

## 5. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	30	V
$V_{DGR}$	drain-gate voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	30	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; see <a href="#">Figure 1</a> <sup>[1]</sup>	-	100	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a> <sup>[1]</sup>	-	100	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 3</a>	-	943	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	211	W
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C
$T_{slid(M)}$	peak soldering temperature		-	260	°C

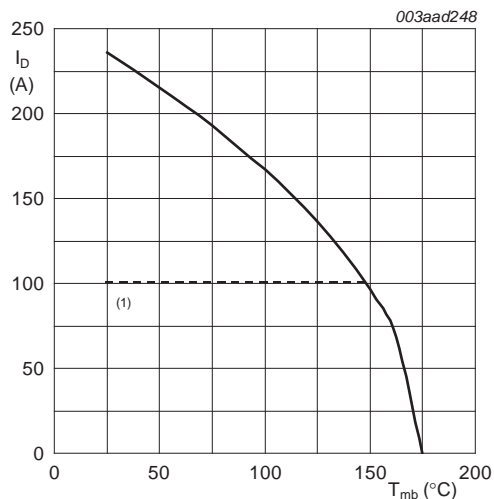
**Source-drain diode**

$I_S$	source current	$T_{mb} = 25\text{ °C}$ <sup>[1]</sup>	-	100	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$	-	943	A

**Avalanche ruggedness**

$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; $I_D = 100\text{ A}$ ; $V_{sup} \leq 30\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; unclamped	-	555	mJ
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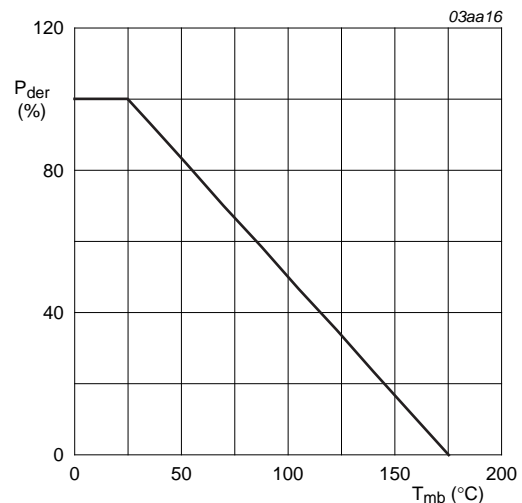
[1] Continuous current is limited by package.



$$V_{GS} \geq 10\text{ V}$$

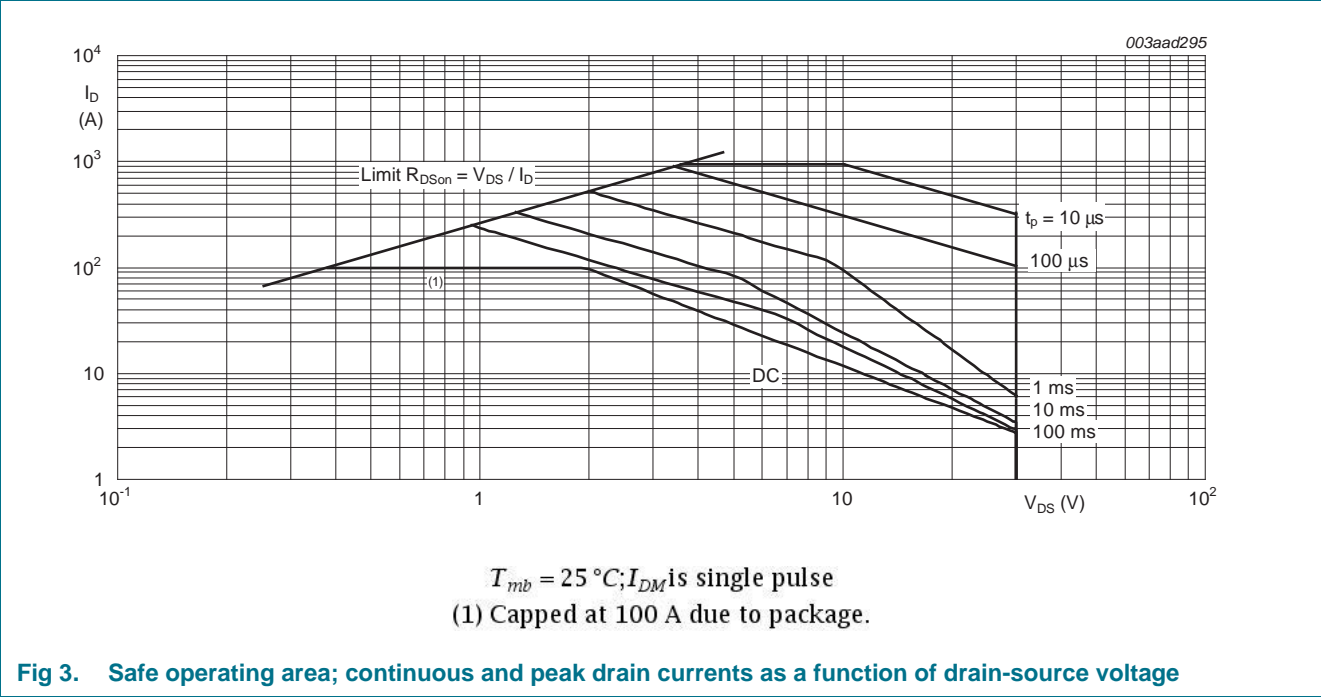
(1) Capped at 100 A due to package.

**Fig 1. Normalized continuous drain current as a function of mounting base temperature**



$$P_{der} = \frac{P_{tot}}{P_{tot(25\text{ °C})}} \times 100\%$$

**Fig 2. Normalized total power dissipation as a function of mounting base temperature**



6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	0.41	0.71	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	maximum foot print; mounted on a printed circuit board	-	50	-	K/W

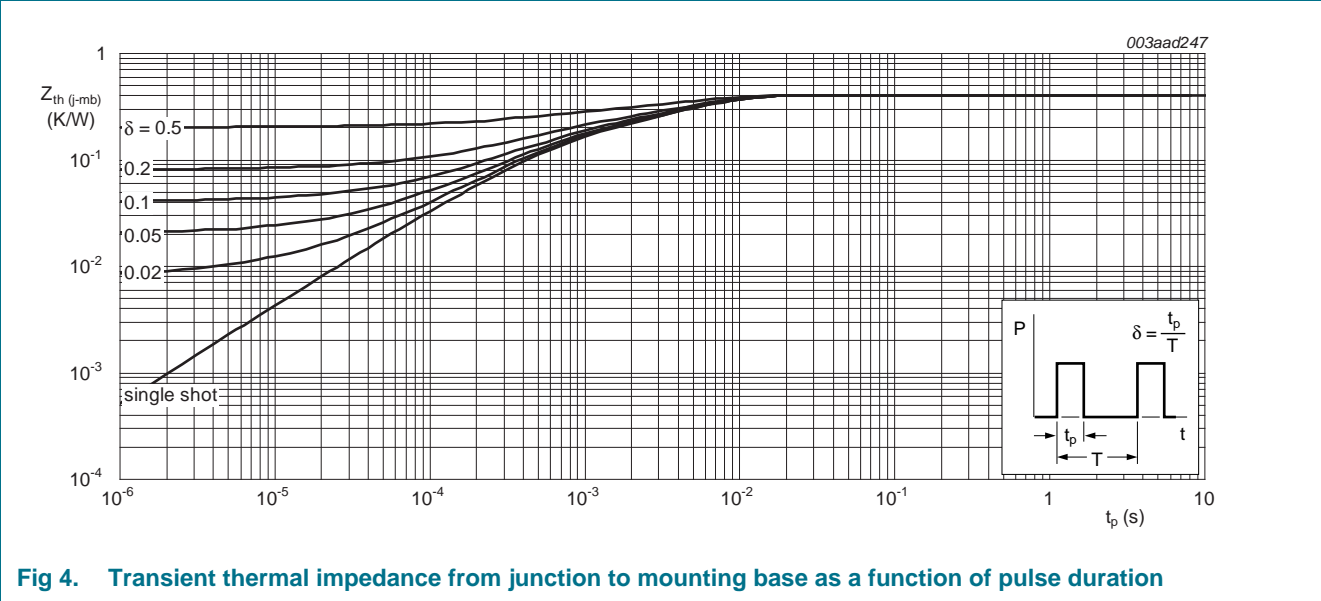


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 7. Characteristics

**Table 7. Characteristics**

Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$ ; $V_{GS} = 0 V$ ; $T_j = 25 ^\circ C$	30	-	-	V
		$I_D = 250 \mu A$ ; $V_{GS} = 0 V$ ; $T_j = -55 ^\circ C$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 ^\circ C$ ; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	1.3	1.7	2.15	V
		$I_D = 1 mA$ ; $V_{DS} = V_{GS}$ ; $T_j = 175 ^\circ C$ ; see <a href="#">Figure 10</a>	0.5	-	-	V
		$I_D = 1 mA$ ; $V_{DS} = V_{GS}$ ; $T_j = -55 ^\circ C$ ; see <a href="#">Figure 10</a>	-	-	2.45	V
$I_{DSS}$	drain leakage current	$V_{DS} = 30 V$ ; $V_{GS} = 0 V$ ; $T_j = 25 ^\circ C$	-	0.02	3	$\mu A$
		$V_{DS} = 30 V$ ; $V_{GS} = 0 V$ ; $T_j = 125 ^\circ C$	-	-	70	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 16 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 ^\circ C$	-	10	100	nA
		$V_{GS} = -16 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 ^\circ C$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5 V$ ; $I_D = 25 A$ ; $T_j = 25 ^\circ C$ ; see <a href="#">Figure 11</a>	-	2.47	2.9	mΩ
		$V_{GS} = 10 V$ ; $I_D = 25 A$ ; $T_j = 175 ^\circ C$ ; see <a href="#">Figure 12</a> ; see <a href="#">Figure 11</a>	-	3.4	4	mΩ
		$V_{GS} = 10 V$ ; $I_D = 25 A$ ; $T_j = 100 ^\circ C$ ; see <a href="#">Figure 12</a> ; see <a href="#">Figure 11</a>	-	2.51	2.9	mΩ
		$V_{GS} = 10 V$ ; $I_D = 25 A$ ; $T_j = 25 ^\circ C$ ; see <a href="#">Figure 11</a>	-	1.79	2.1	mΩ
$R_G$	gate resistance	$f = 1 MHz$	-	0.78	-	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 0 A$ ; $V_{DS} = 0 V$ ; $V_{GS} = 10 V$	-	107	-	nC
		$I_D = 25 A$ ; $V_{DS} = 15 V$ ; $V_{GS} = 10 V$ ; see <a href="#">Figure 13</a> ; see <a href="#">Figure 14</a>	-	117	-	nC
		$I_D = 25 A$ ; $V_{DS} = 15 V$ ; $V_{GS} = 4.5 V$ ; see <a href="#">Figure 13</a> ; see <a href="#">Figure 14</a>	-	55	-	nC
$Q_{GS}$	gate-source charge		-	17	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	11	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	6	-	nC
$Q_{GD}$	gate-drain charge		-	16	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 A$ ; $V_{DS} = 25 V$ ; see <a href="#">Figure 13</a> ; see <a href="#">Figure 14</a>	-	2.6	-	V
$C_{iss}$	input capacitance	$V_{DS} = 15 V$ ; $V_{GS} = 0 V$ ; $f = 1 MHz$ ;	-	6810	-	pF
$C_{oss}$	output capacitance	$T_j = 25 ^\circ C$ ; see <a href="#">Figure 15</a>	-	1410	-	pF
$C_{rss}$	reverse transfer capacitance		-	650	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15 V$ ; $R_L = 0.5 \Omega$ ; $V_{GS} = 4.5 V$ ;	-	63	-	ns
$t_r$	rise time	$R_{G(ext)} = 4.7 \Omega$	-	125	-	ns
$t_{d(off)}$	turn-off delay time		-	111	-	ns
$t_f$	fall time		-	59	-	ns

Table 7. Characteristics ...continued  
Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 16</a>	-	0.76	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 25\text{ A}$ ; $di_S/dt = -100\text{ A/}\mu\text{s}$ ;	-	49	-	ns
$Q_r$	recovered charge	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 15\text{ V}$	-	66	-	nC

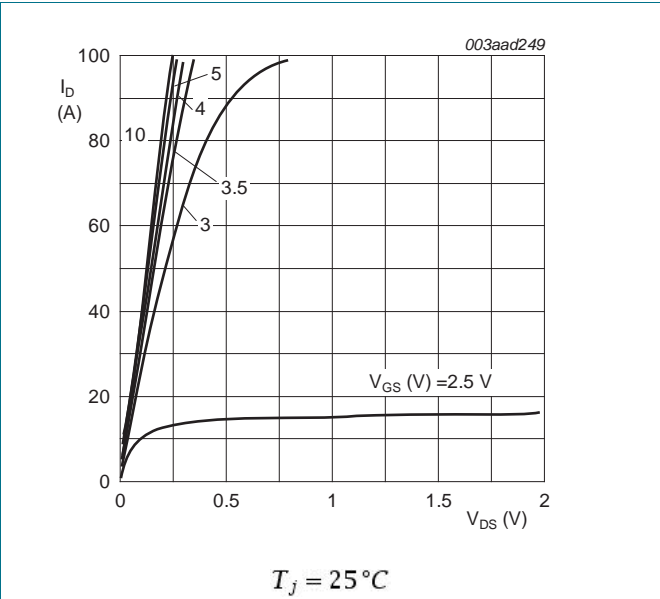


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

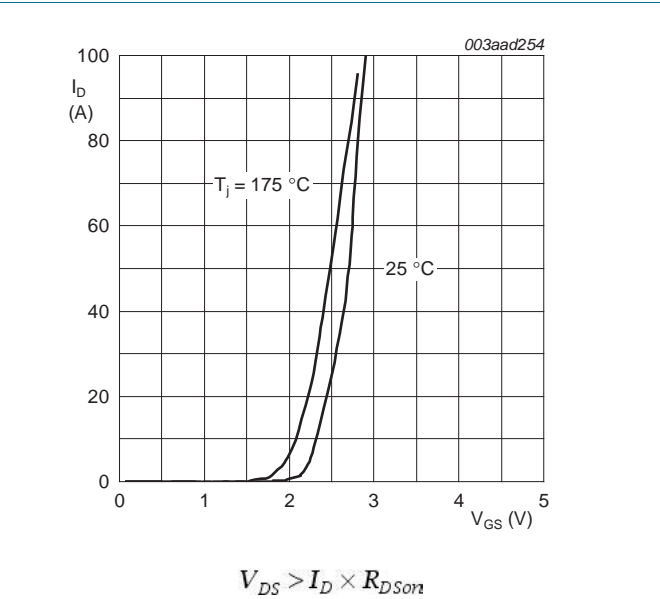


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

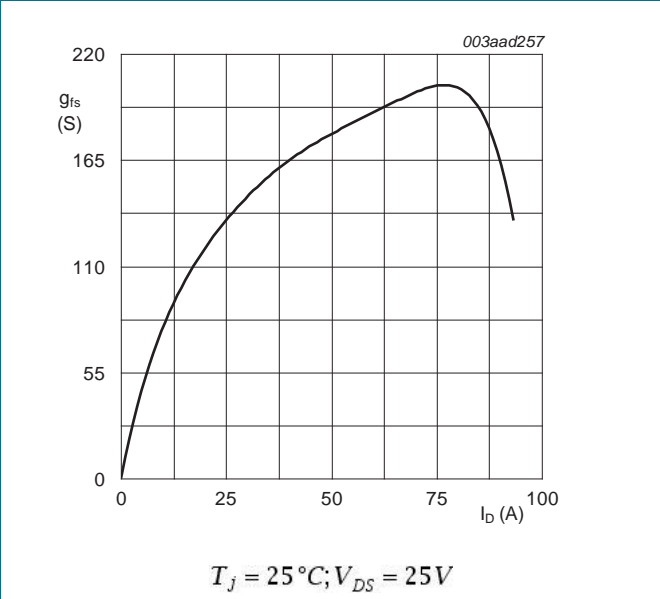


Fig 7. Forward transconductance as a function of drain current; typical values

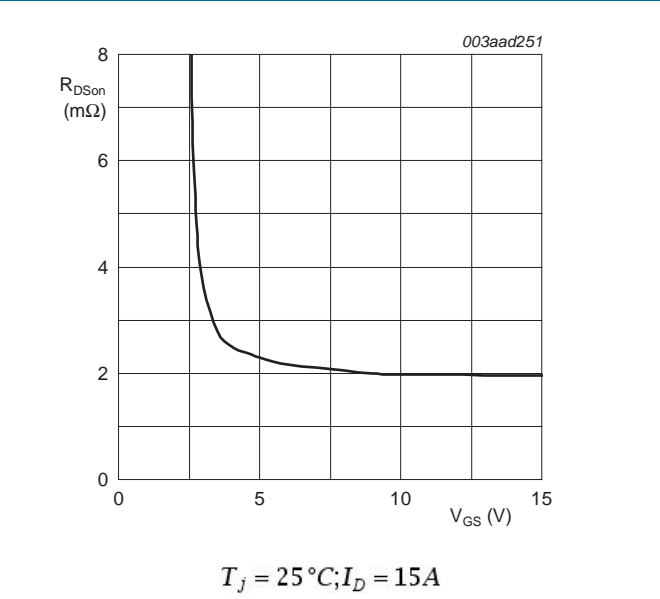
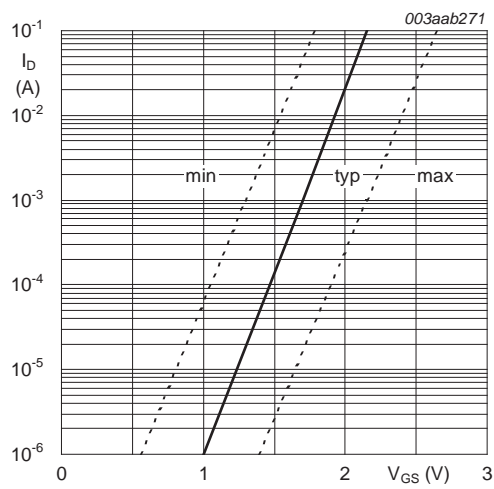
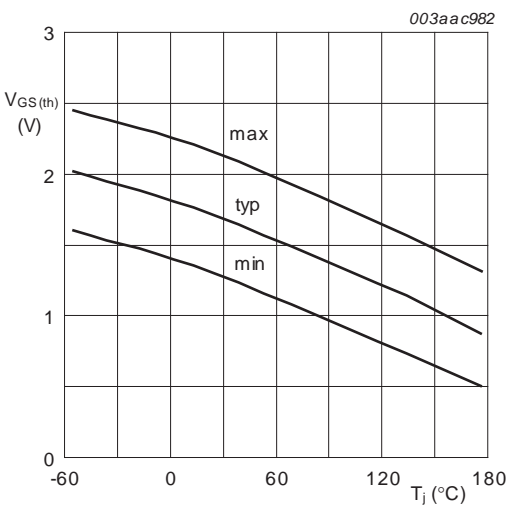


Fig 8. Drain source on-state resistance as a function of gate-source voltage; typical values



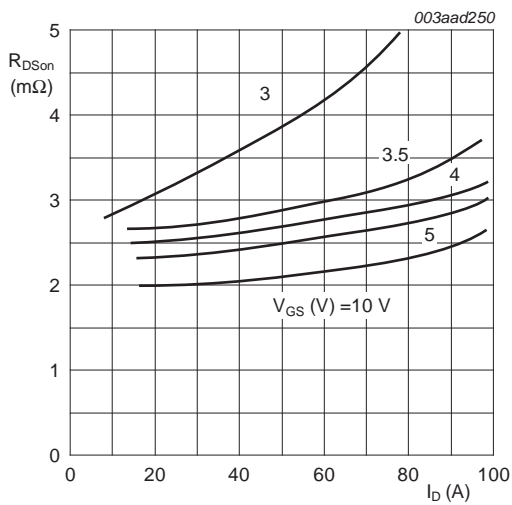
$T_j = 25\text{ }^{\circ}\text{C}; V_{DS} = 5\text{ V}$

Fig 9. Sub-threshold drain current as a function of gate-source voltage



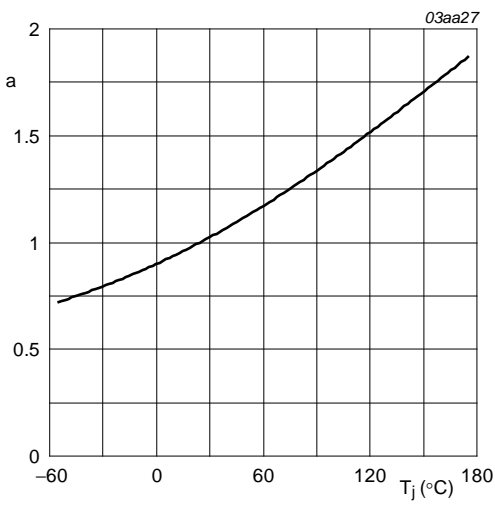
$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature



$T_j = 25\text{ }^{\circ}\text{C}$

Fig 11. Drain-source on-state resistance as a function of drain current; typical values



$a = \frac{R_{DS(on)}}{R_{DS(on)25^{\circ}\text{C}}}$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature



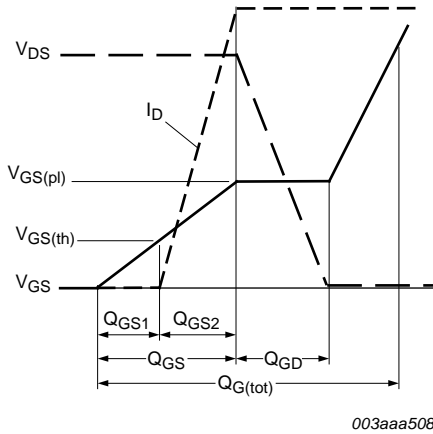
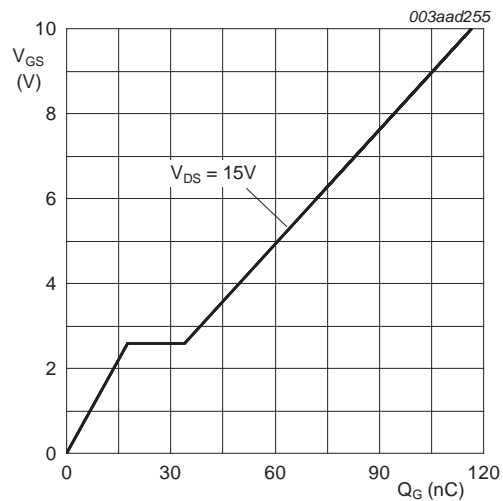
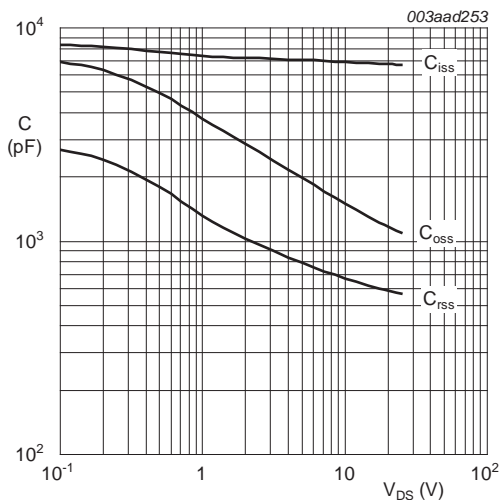


Fig 13. Gate charge waveform definitions



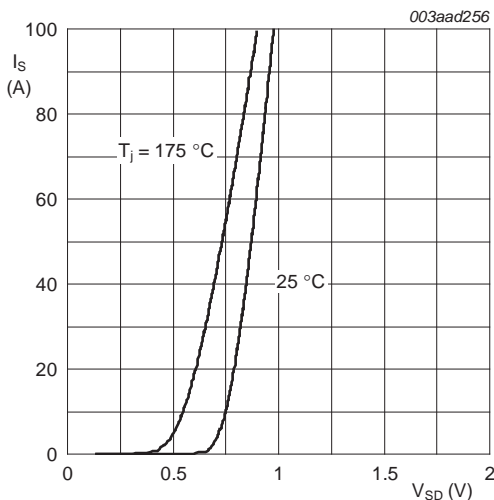
$T_j = 25\text{ }^{\circ}\text{C}; I_D = 25\text{ A}$

Fig 14. Gate-source voltage as a function of gate charge; typical values



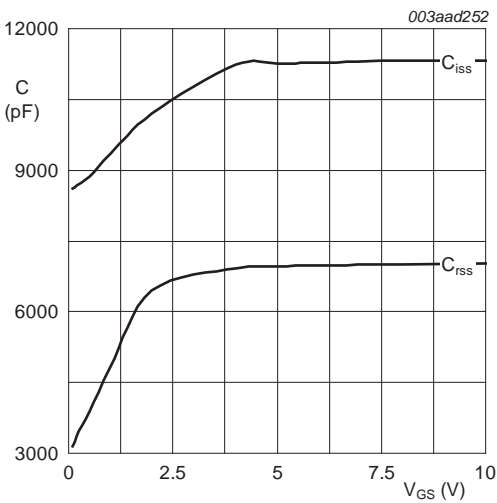
$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0\text{ V}$

Fig 16. Source current as a function of source-drain voltage; typical values



$V_{DS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 17. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

8. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	c	D <sub>max.</sub>	D <sub>1</sub>	E	e	L <sub>p</sub>	H <sub>D</sub>	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						05-02-11 06-03-16

Fig 18. Package outline SOT404 (D2PAK)

## 9. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN2R0-30BL v.1	20120320	Product data sheet	-	-

## 10. Legal information

### 10.1 Data sheet status

Document status <sup>[1] [2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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