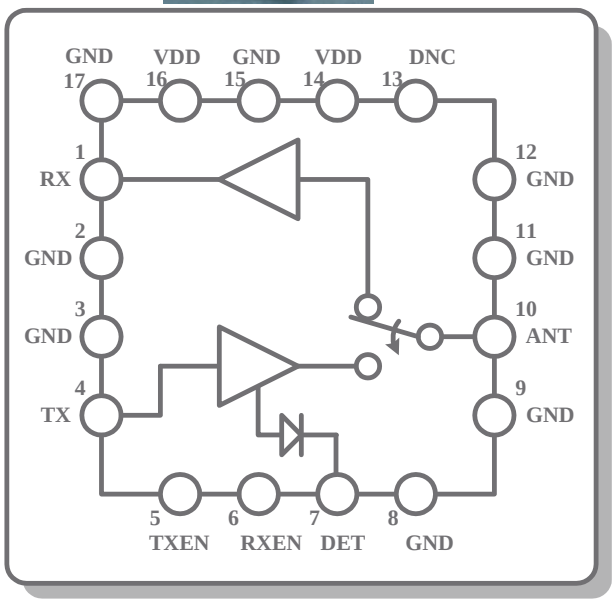
RFX2402E Single-Chip/Single-Die CMOS RFeIC with PA, LNA, Power Detector and Antenna Switch for 802.11ac/n/g/b

Eval Board Test Summary & Technical Notes

Key Features and Benefits

(3x3x0.55mm
16L QFN)



RFX2402E Differentiating Features

- All Key Functions for WiFi 802.11ac/n/g/b Including PA, LNA, Tx-Rx Switching Circuitry, Matching, Harmonic Filter, and Power Detector in a Single-Chip Single-Die CMOS Device
- Reduced and Simplified Tx/Rx Control Lines
- Digital Logic with 1.2V Turn-On Voltage
- No Vref Regulator for Biasing
- Minimal External Component Requirements
- Small, Ultra-Thin 3x3x0.55mm 16L QFN Package

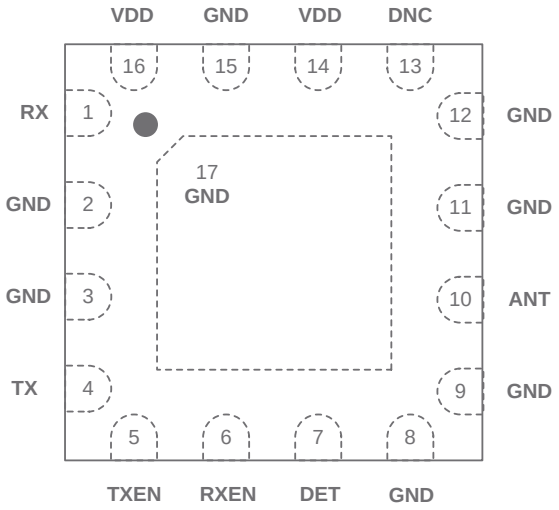
APPLICATIONS

- WLAN 11ac/n/g/b NIC Card and Access Point
- Laptops, Netbooks, Tablets, MIDs and Smartbooks with Embedded WLAN
- Other Portable with Integrated 802.11ac/n/g/b
- Multi-Radio 2.4GHz Transceivers

RFX2402E Customer Benefits

- Simple 50-Ohm “Plug & Play” Implementation onto Customer’s PCB
- Reduced Product Design Cycle and TTM
- Enabling Very Small Product Form-Factor
- Available in Bare-Die for Compact SiP Design
- Best-Class RF Performance for both Tx and Rx
- Very Competitive Price & Overall BOM Cost
- Ideal Building Block for 2x2/3x3/4x4 11n MIMO
- Pin Compatible with Legacy RFX2402C

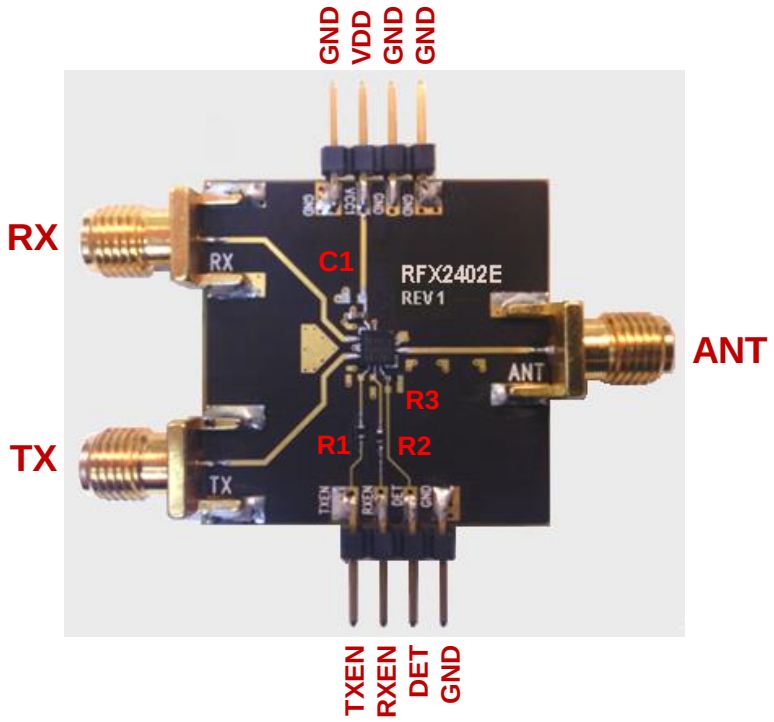
Package Pin Out and Pin Description



(Top "See Through" View)

Pin Number	Pin Name	Description
1	RX	Received RF Signal from the LNA to the Transceiver; DC Shorted to GND
2, 3, 8, 9, 11,12, 15, 17	GND	Ground – Must Be Connected to Ground in the Application Circuit
4	TX	Transmitted RF Signal from the Transceiver to the PA: DC Shorted to GND
5	TXEN	CMOS Input to Enable the PA
6	RXEN	CMOS Input to Enable the LNA
7	DET	Analog Voltage Proportional to the PA Output Power
10	ANT	Antenna Port RF Signal from the PA or RF Signal Applied to the LNA; DC Shorted to GND
13	DNC	Reserved Pin, Do Not Connect in the Application Circuit
14, 16	VDD	Voltage Supply Connection (Pin 14 and 16 are internally connected)

Evaluation Board and Preliminary BOM



Recommended BOM

Designator	Value	Footprint	Notes
C1	1uF	0402	X5R/X7R
R1, R2	1KΩ	0402	*
R3	10KΩ	0402	Det. Load

* Only needed if the control pin is directly connected to VDD

Control Logic Truth Table

TXEN	RXEN	Mode of Operating
0	0	Shutdown Mode
1	0	Transmit Mode
0	1	Receive Mode

Note: "1" denotes high voltage state (> 1.2V) at Control Pins
"0" denotes low voltage state (< 0.3V) at Control Pins

Evaluation Board Information:

- 4-Layer Stack, 10mil/40mil/10mil
- FR4 with εr=4.5, tan δ = 0.02 (Typ)
- RFIN, RFOUT trace losses are ~0.25dB @ 2.4GHz – 2.5GHz
- Results in following slides are referenced to device pins with the trace loss de-embedded
- VDD should be on before applying ctrl signals
-VDD Nominal 3.3 Vdc. Operational from 2.7 to 3.6 Vdc

DEVM Measurement

Vector Signal Generator
- Calibrated for input power level of DUT

Signal Analyzer
- Level calibrated for DUT Pout at Ant pin

Demodulation:
- no amplitude correction
- tracking on preamble only

Gating

Burst 200 us / 50% duty cycle
unless otherwise specified

RF

TXEN pulse
400 ns prior to gating

EVB with DUT

VDD

TX
port

ANT
port

10 dB
pad

No cable between
EVB and pad

TXEN

VDET

VDD

Supply

Burst
Gating

A/D

A/D

VDET

I DD

Bandwidth / Band Limit Dependence

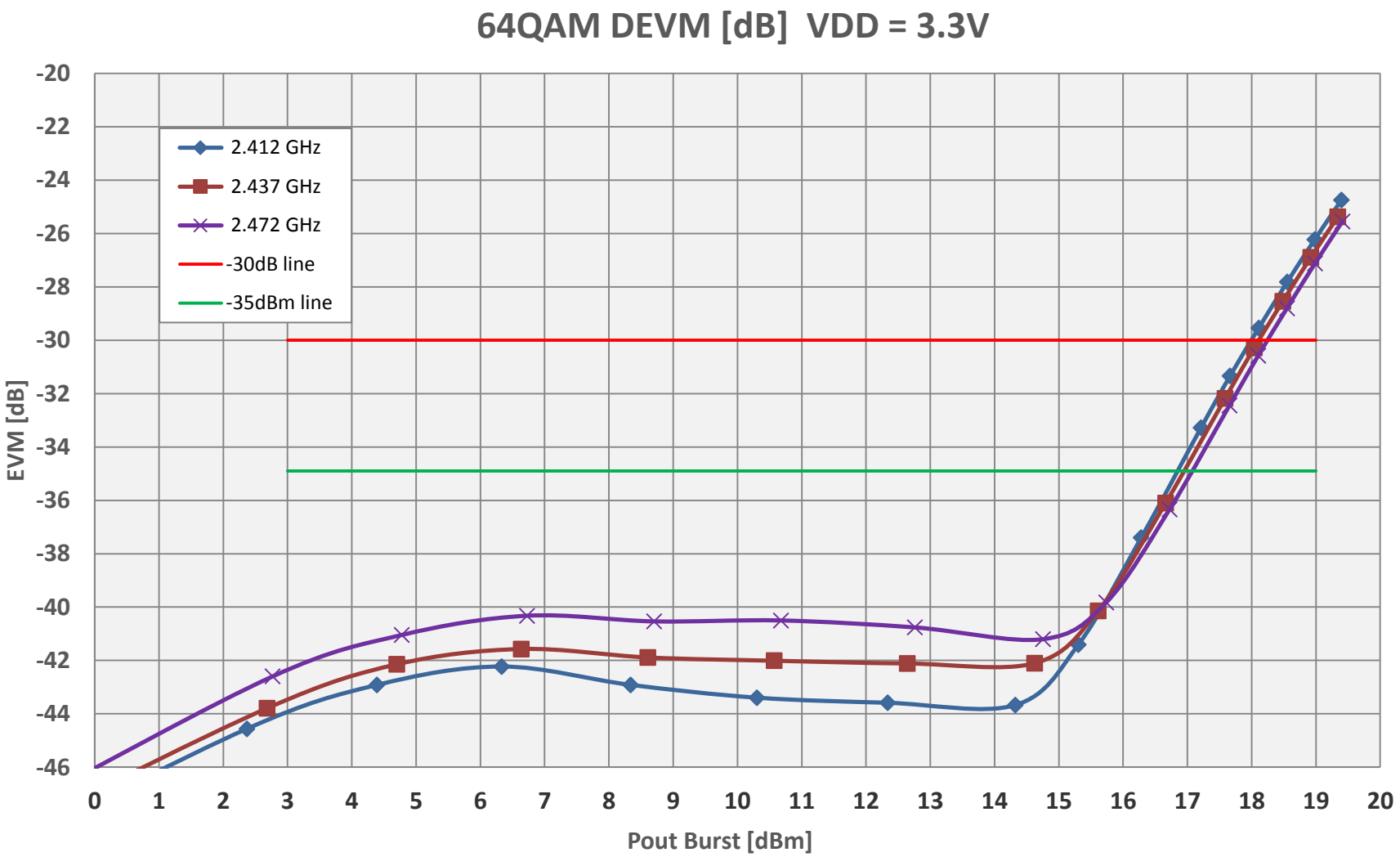
40 MHz Channels in 2.5 GHz Band:
Lowest Channel: 2422 MHz
Highest Channel: 2462 MHz

80 MHz Channels in 5.5 GHz Band:
Lowest Channel: 5210 MHz
Highest Channel: 5775 MHz

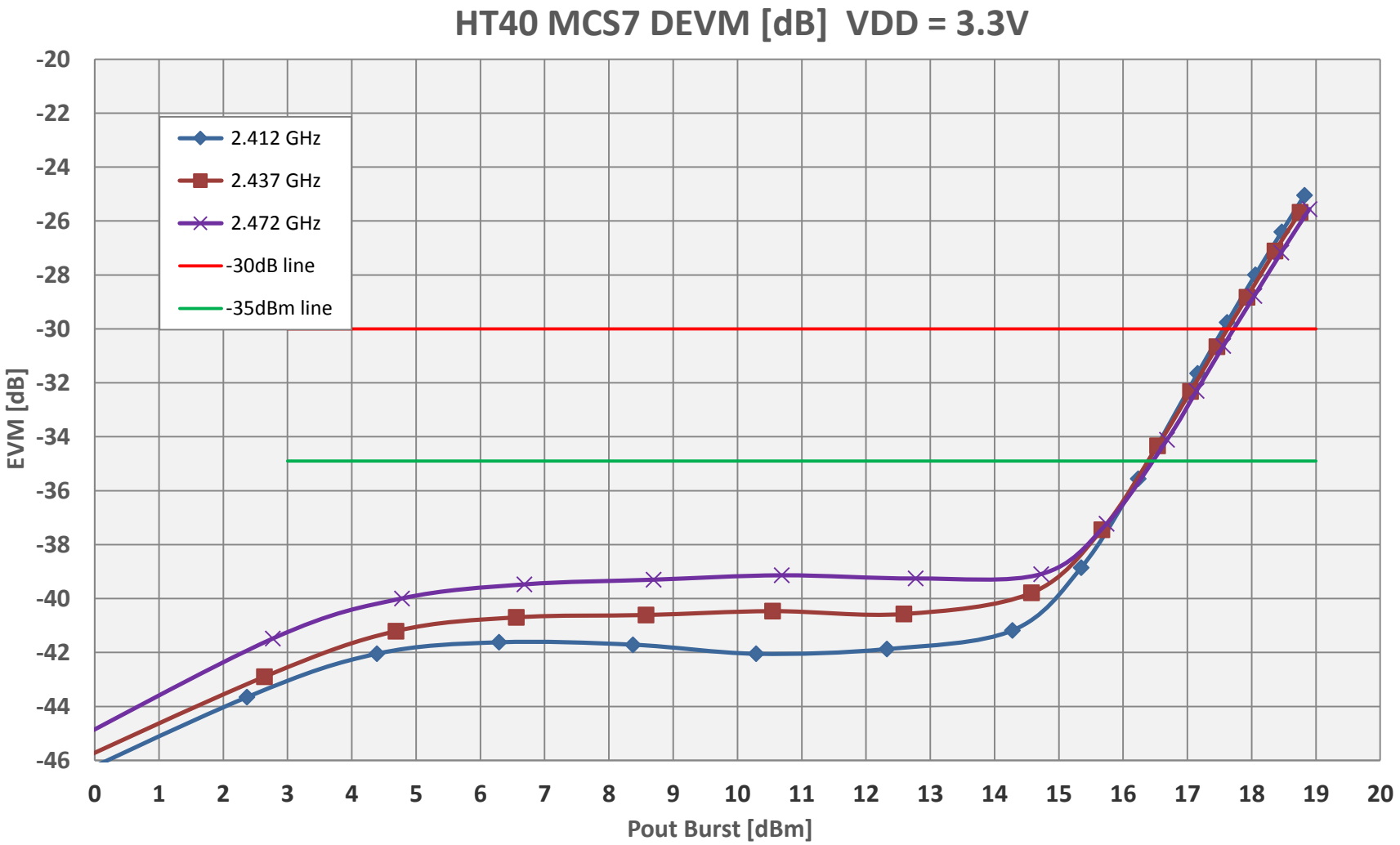
Analyzer Offset Correction:
EVB loss + 10dB + cable loss

EVB Loss	2.5 GHz	5.5 GHz
ANT	0.20 dB	0.35 dB
TX in	0.20 dB	0.35 dB

RFX2402E TX 802.11g DEVM over Frequency VDD = 3.3V

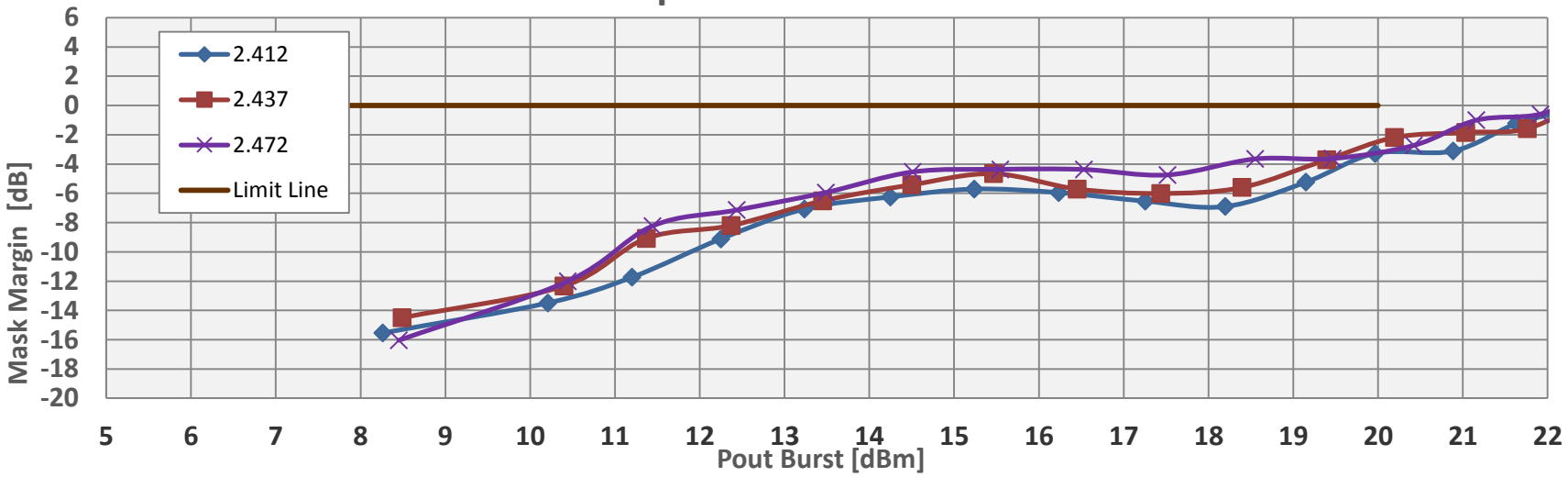


RFX2402E 802.11n TX DEVM over Frequency VDD = 3.3V

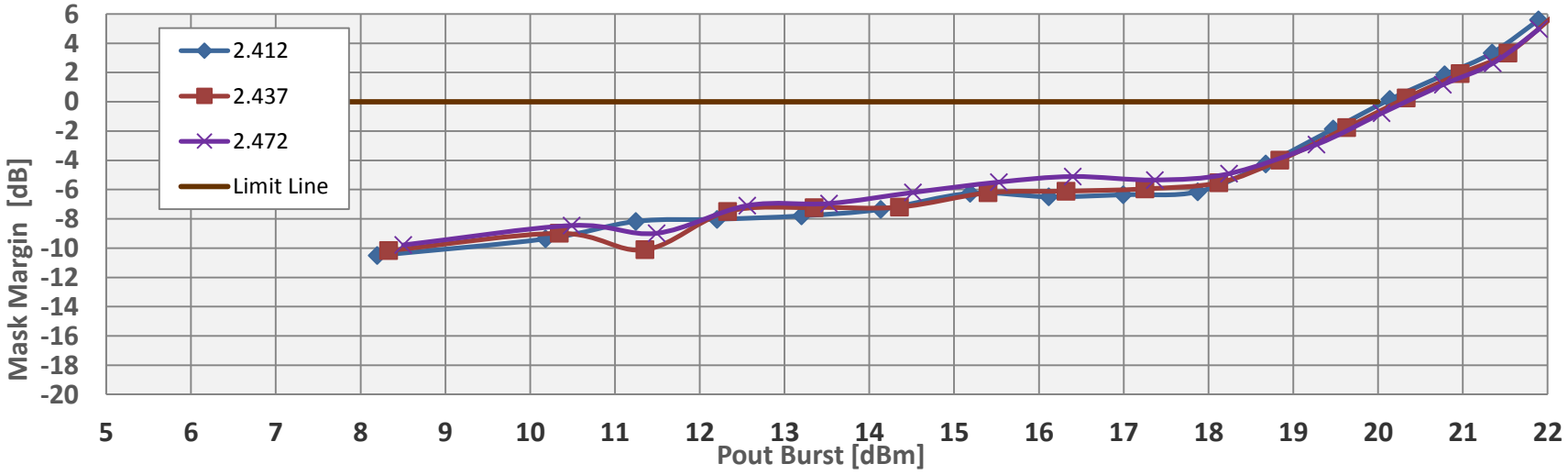


RFX2402E TX Mask over Frequency
VDD = 3.3V

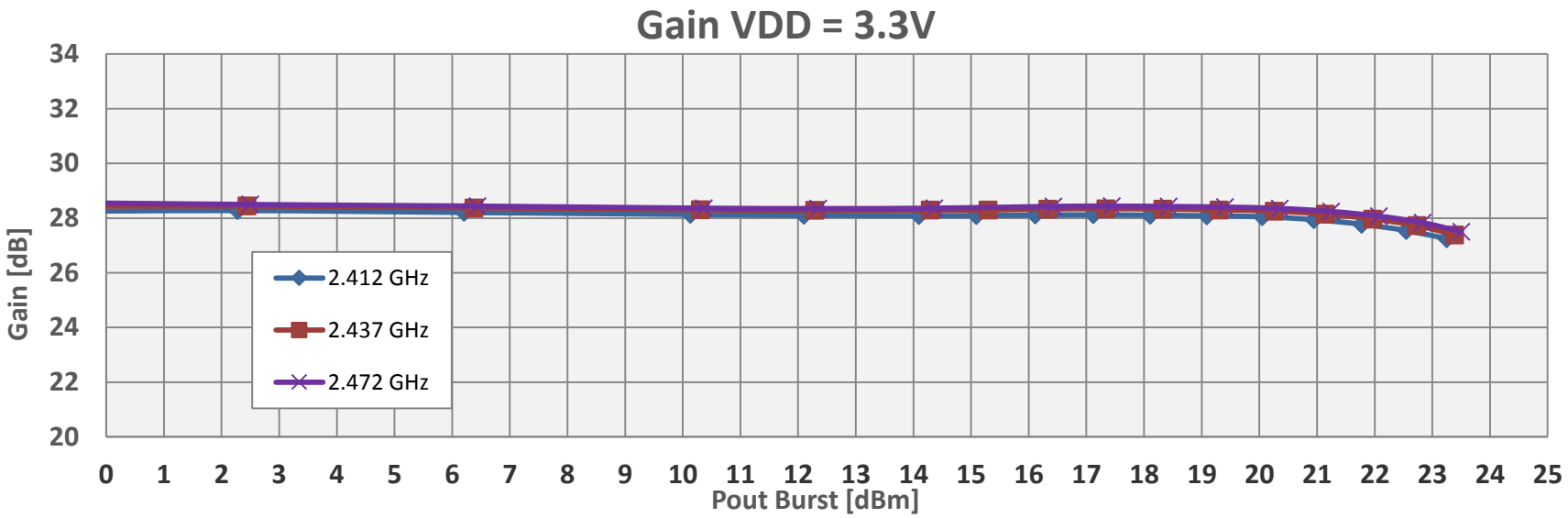
11b 1Mbps Gaussian Mask VDD = 3.3V

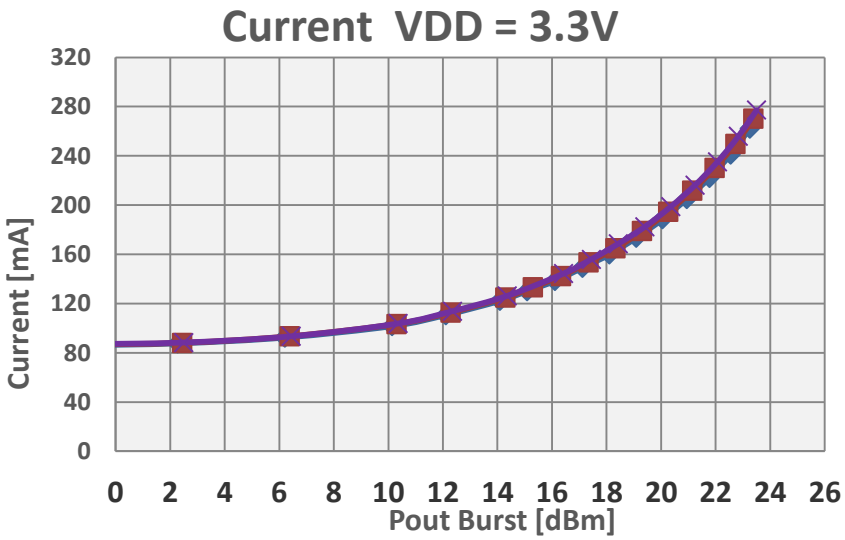


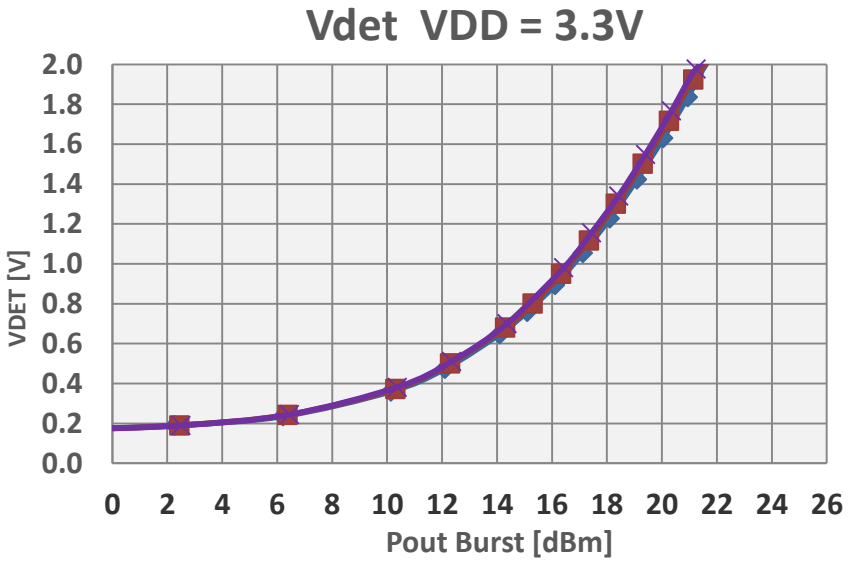
HT40 MCS7 Mask VDD = 3.3V



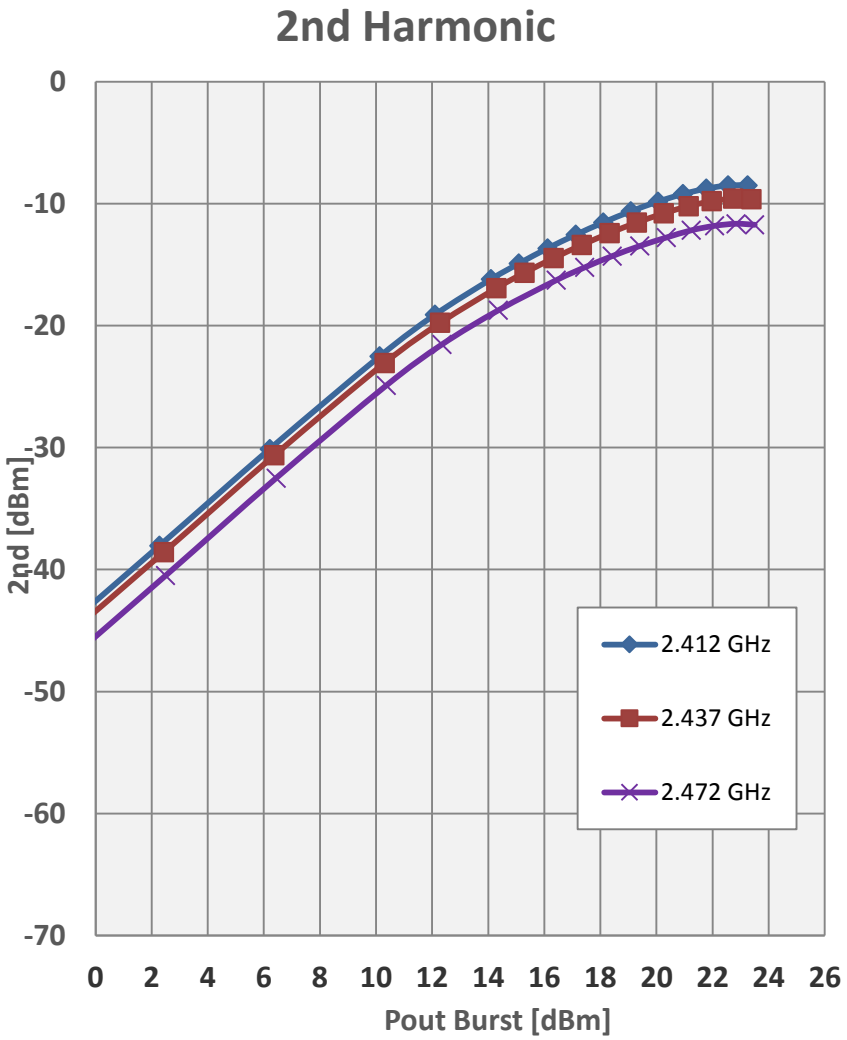
RFX2402E TX CW Gain, Current, and Vdet
VDD = 3.3V

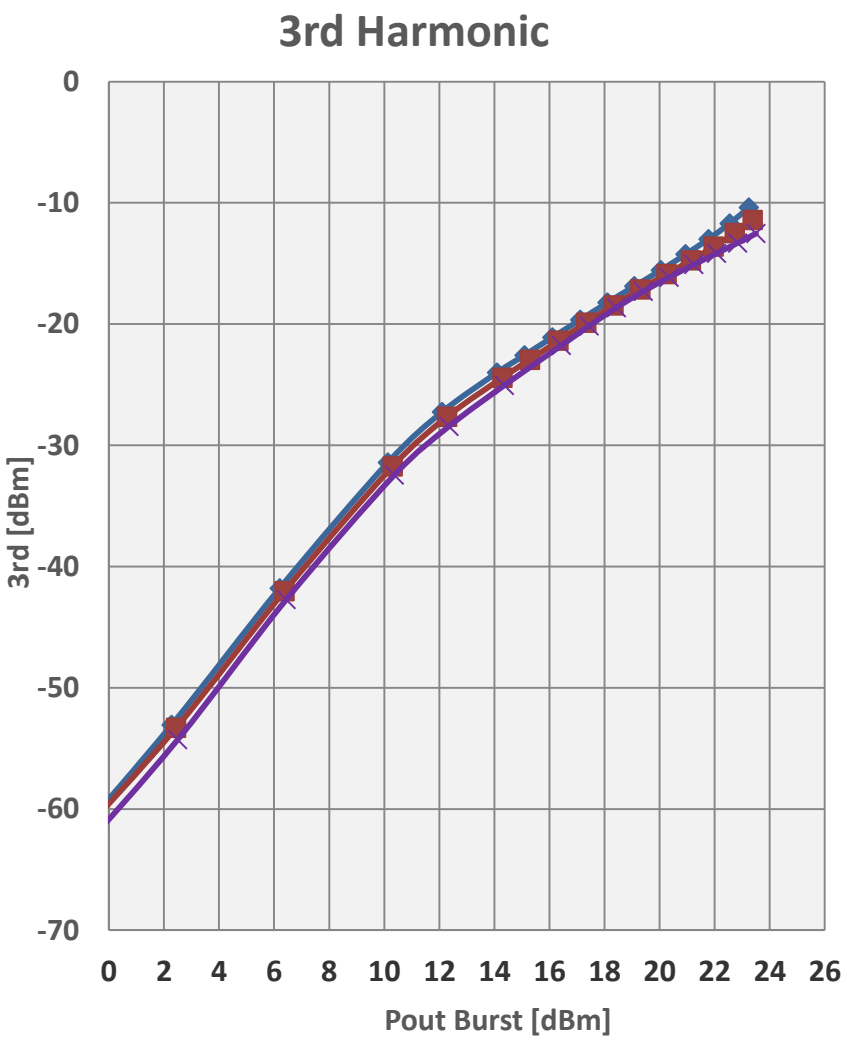




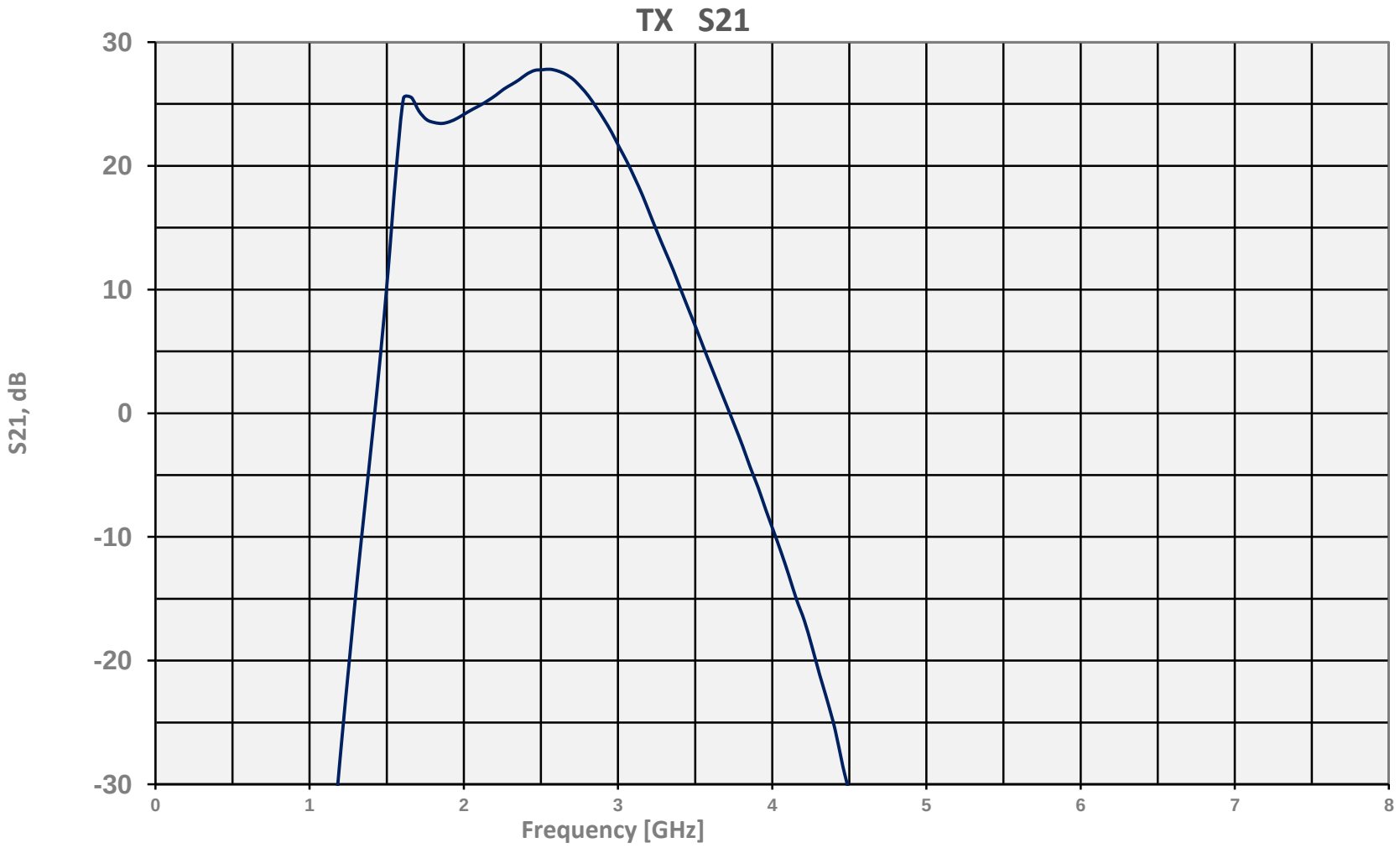


RFX2402E CW TX Harmonics
VDD = 3.3V



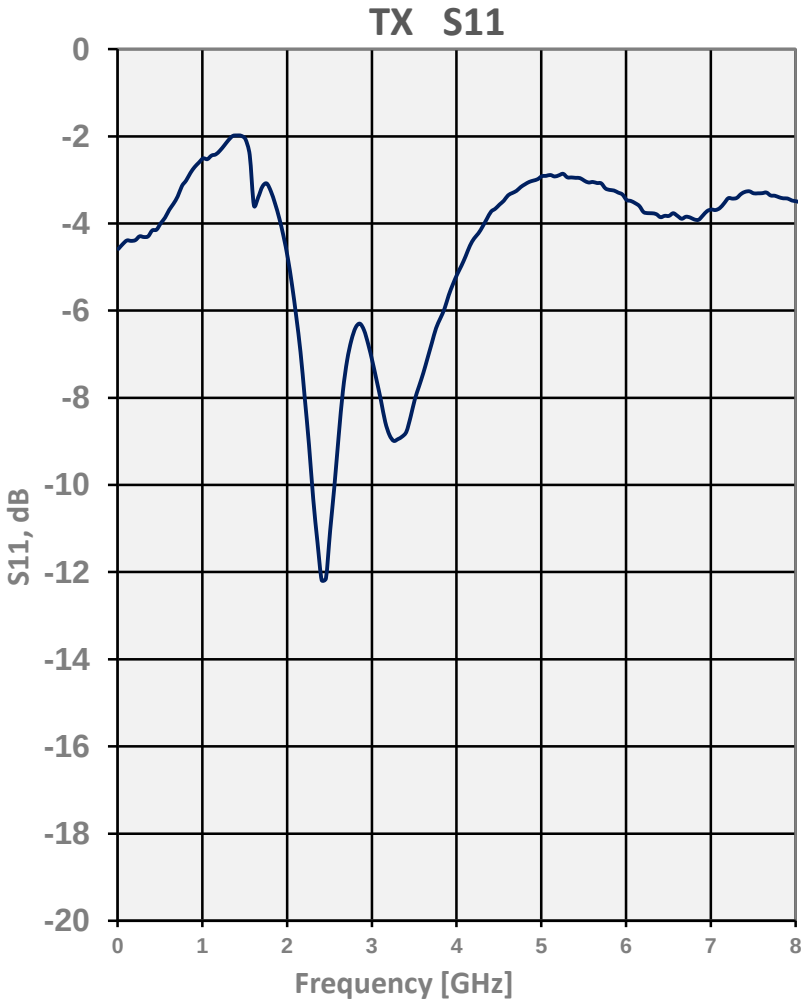


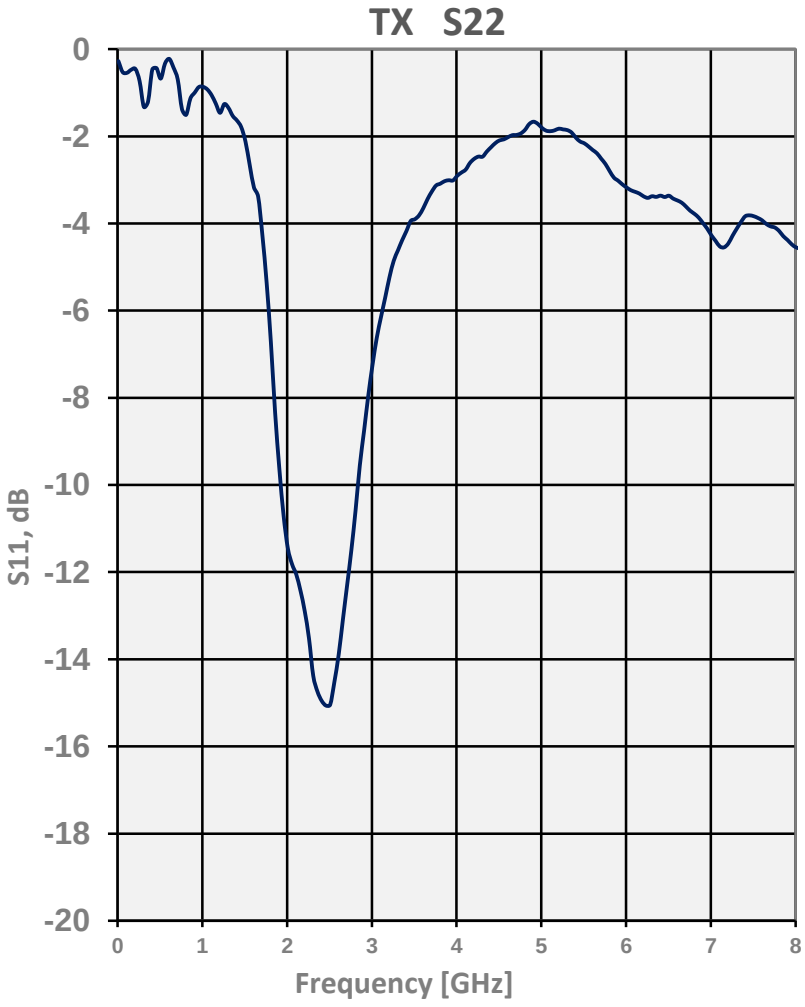
RFX2402E TX S-Parameters
VDD = 3.3V



TX Iq = 83mA

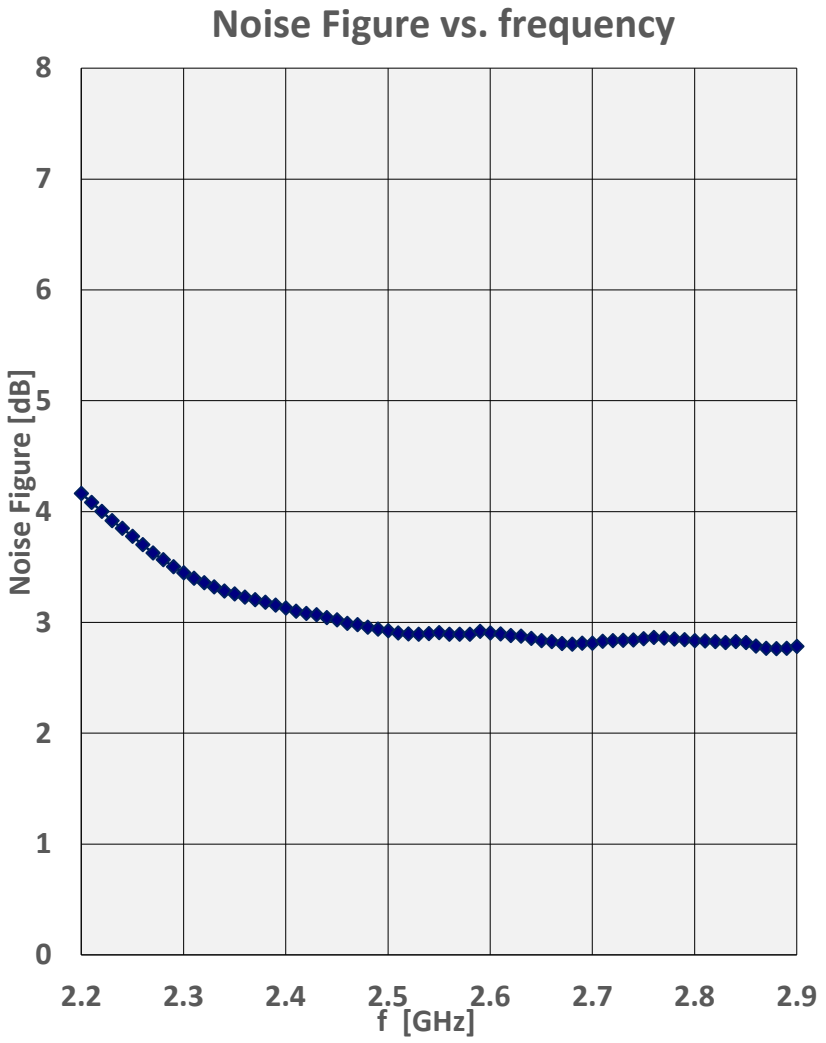
RFX2402E TX S-Parameters
VDD = 3.3V

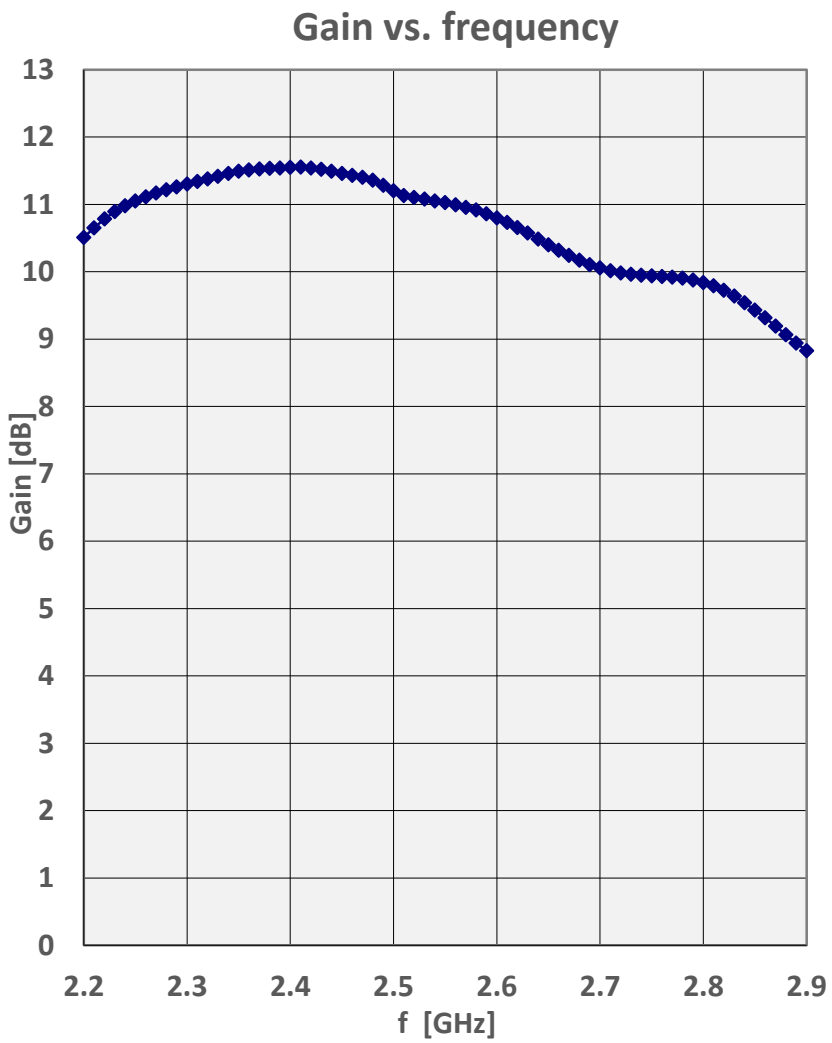




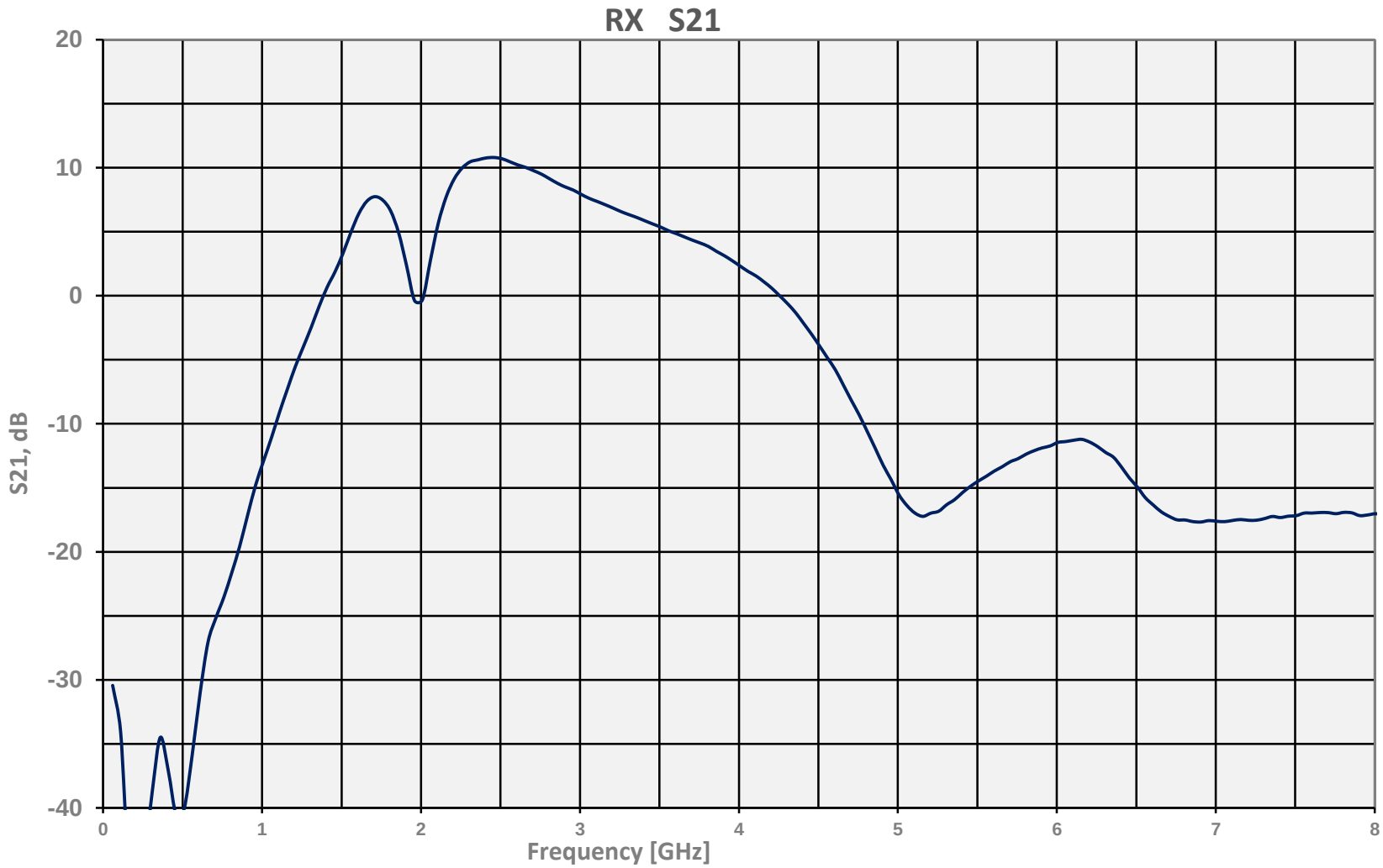
TX Iq = 83mA

RFX2402E RX Gain and Noise Figure
VDD = 3.3V





RFX2402E RX S-Parameters
VDD = 3.3V

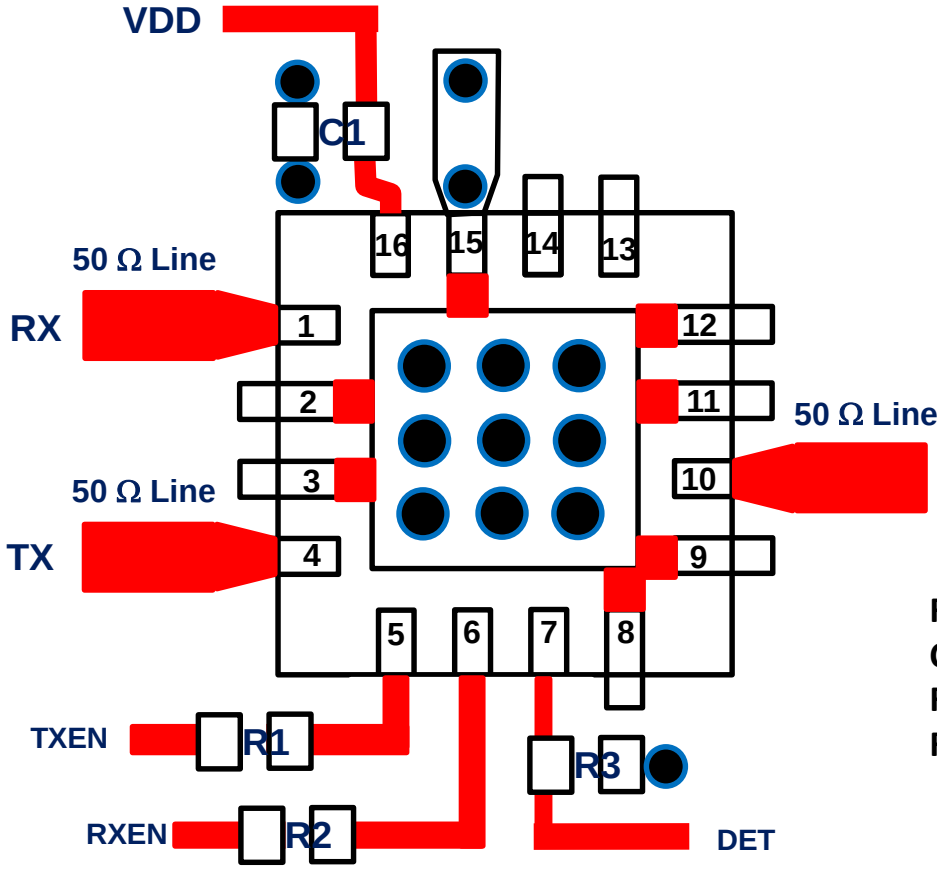


RX Iq = 11mA

RFX2402E RX S-Parameters
VDD = 3.3V

RX Iq = 11mA

RFX2402E PCB Layout Recommendation



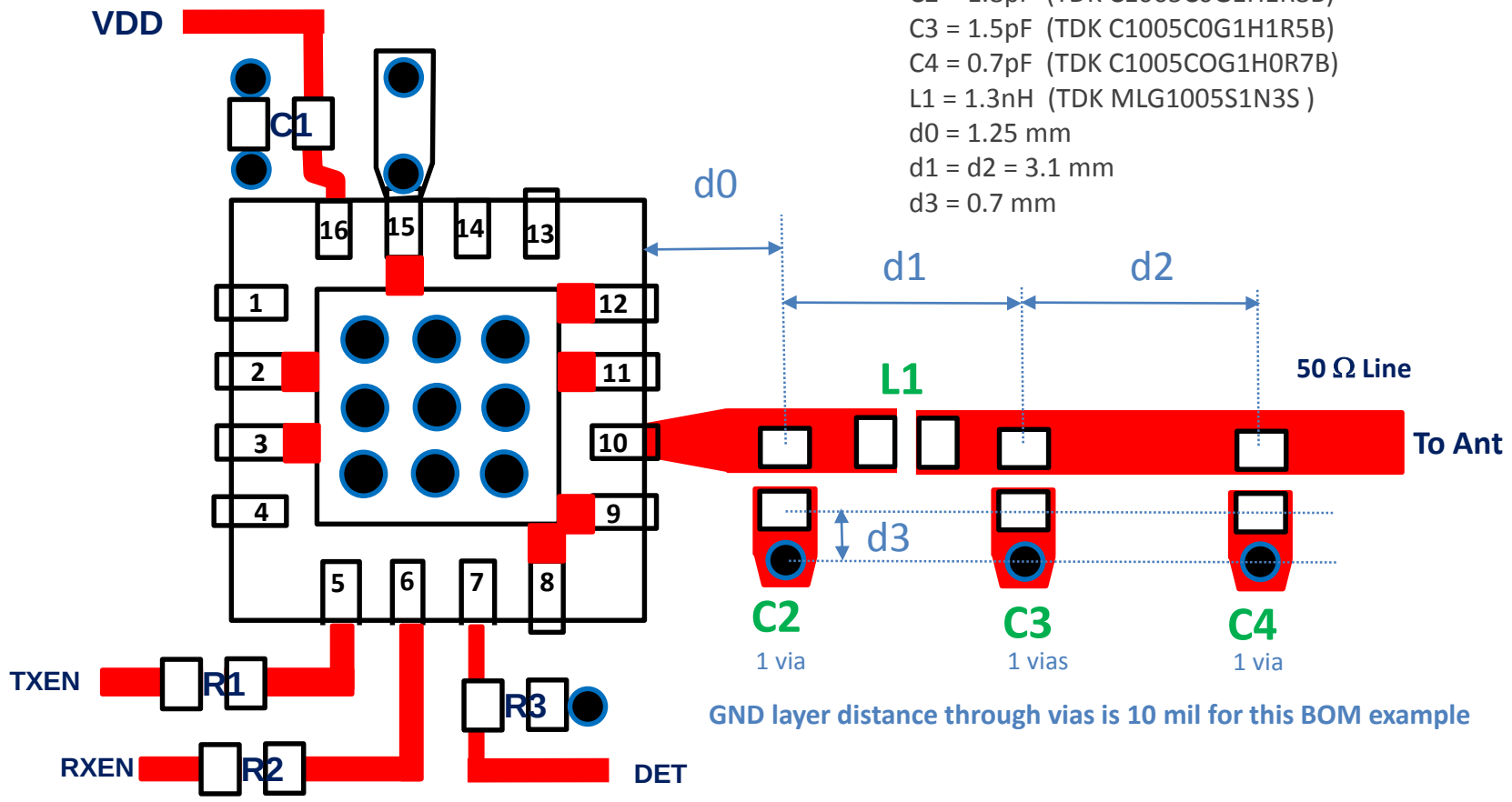
Recommended BOM:
C1=1uF
R1=R2=1KΩ
R3=10KΩ

Notes:
-Tie GND pins (2,3,8,9,11,12,15) to center ground paddle
-DNC (pin 13) must be left disconnected in the application circuit
-VDD pins (14, 16) are internally connected; only one needs to be tied to the VDD supply
-For best RF performance place 9 vias under the center ground paddle
-Place two vias immediately next to the VDD shunt cap (C1) if possible

PCB Layout/BOM Harmonic Suppression

Recommended BOM with 4-Element Lumped Filter:

C1 = 1uF
R1 = R2 = 1KΩ
R3 = 10KΩ
C2 = 1.8pF (TDK C1005C0G1H1R8B)
C3 = 1.5pF (TDK C1005C0G1H1R5B)
C4 = 0.7pF (TDK C1005COG1H0R7B)
L1 = 1.3nH (TDK MLG1005S1N3S)
d0 = 1.25 mm
d1 = d2 = 3.1 mm
d3 = 0.7 mm



GND layer distance through vias is 10 mil for this BOM example

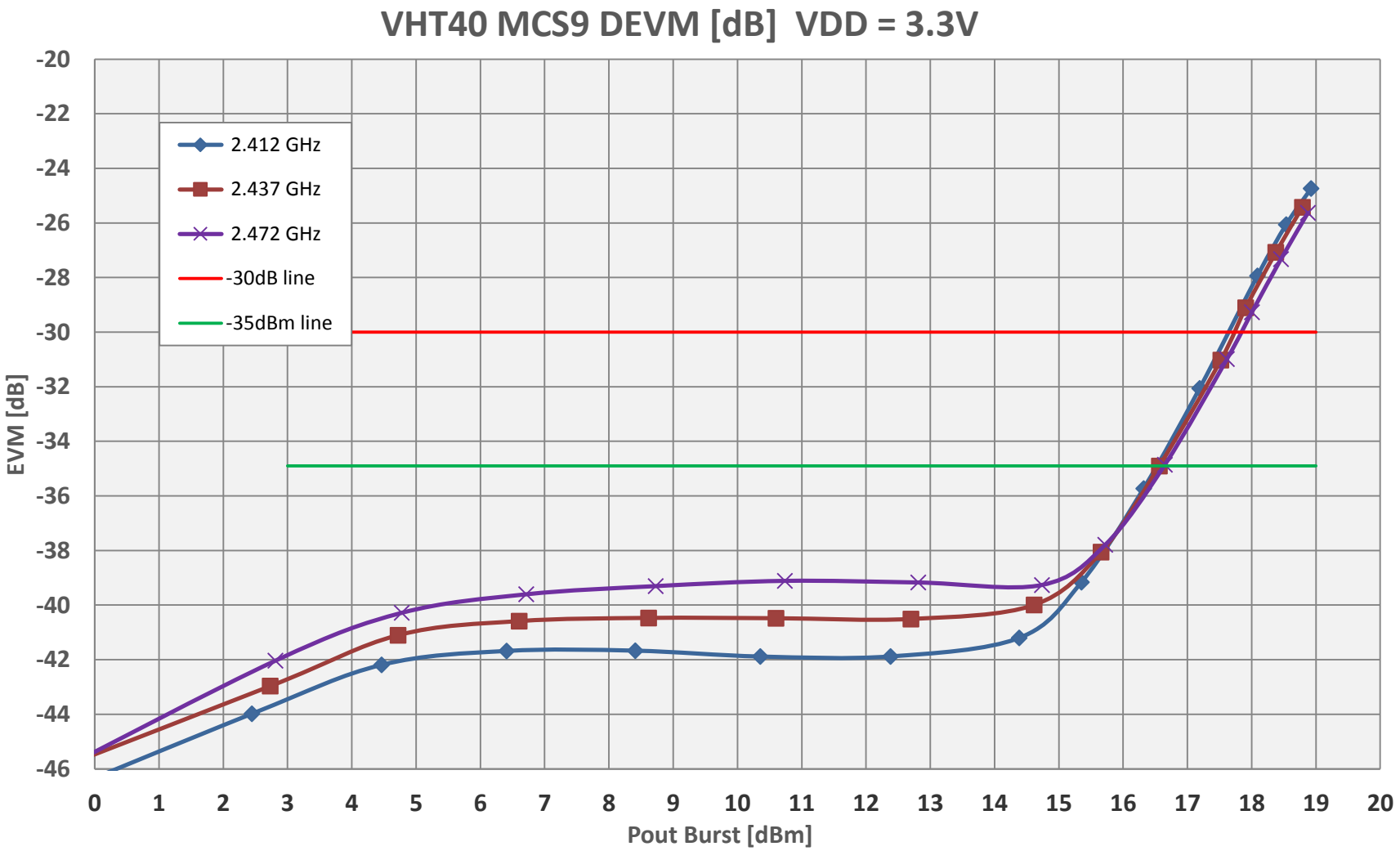
Notes:

- For best RF performance please place 9 vias under the center ground paddle, and tie all unused pins to it
- Filter performance is impacted significantly by distances , vias, layer thickness and make of SMD elements
- Please contact RFaxis for layout recommendations if PCB stack is different from eval board (4-layer FR4, 10mil/40mil/10mil)

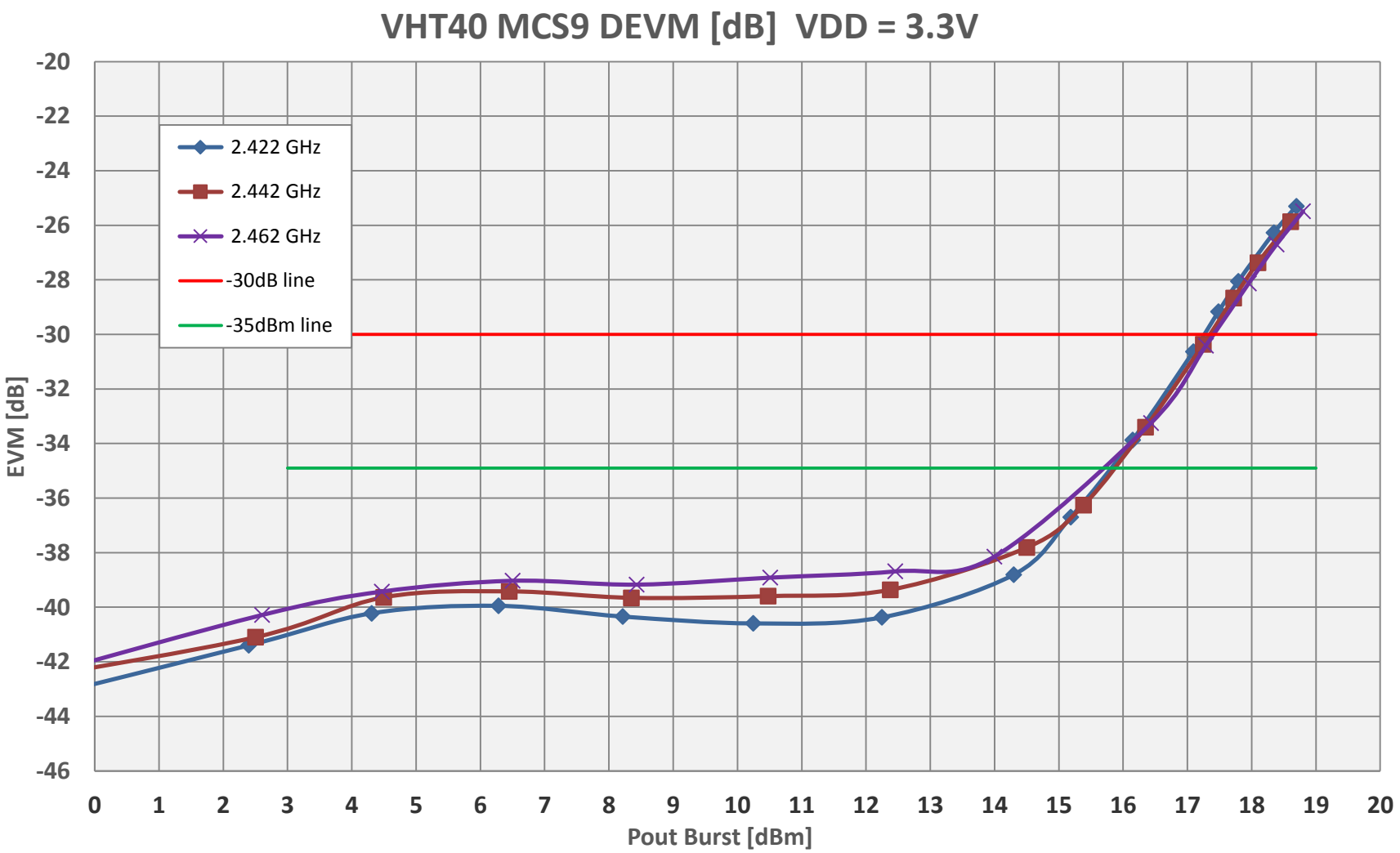
Appendix A

802.11ac

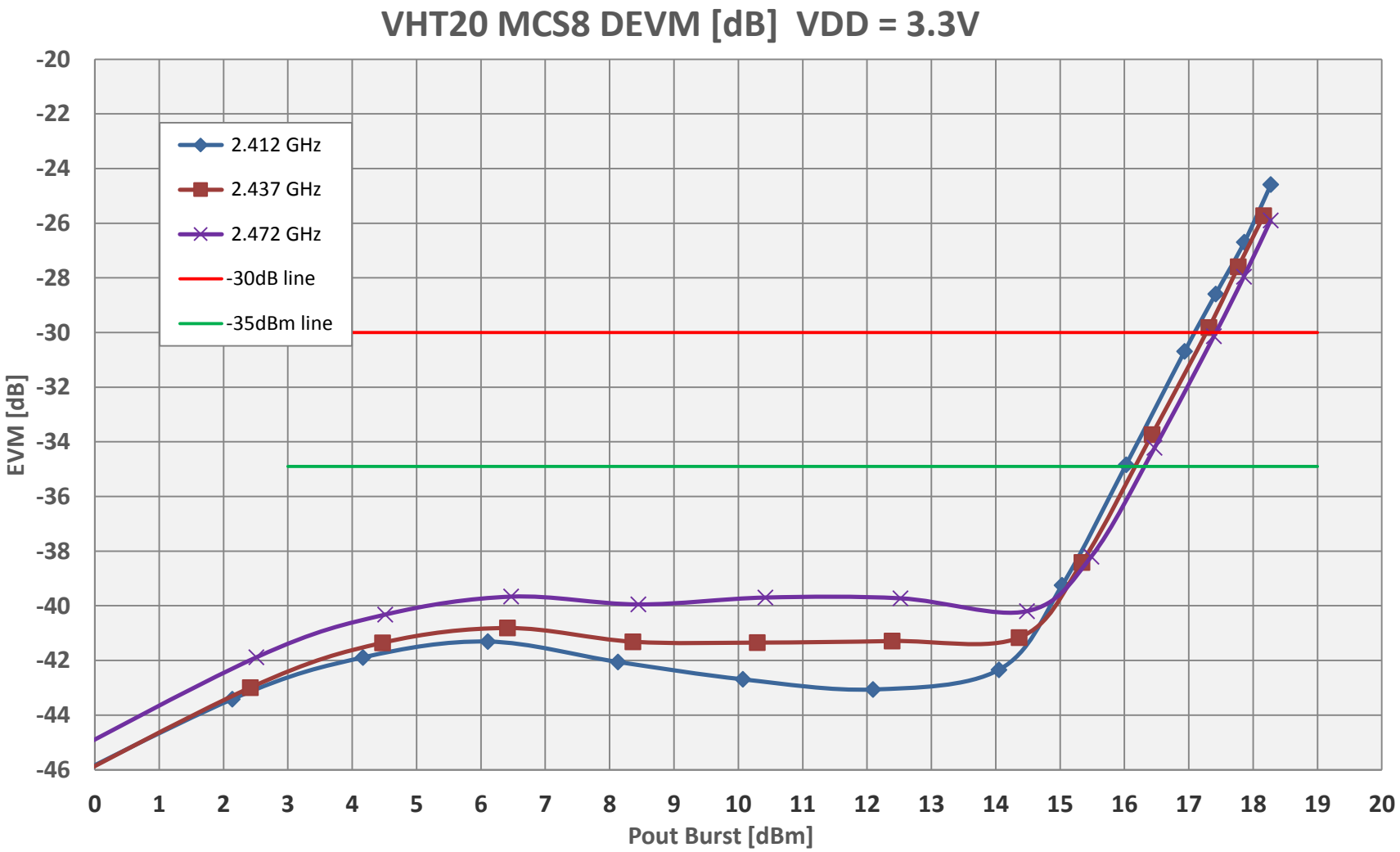
RFX2402E 802.11ac TX DEVM over Frequency VDD = 3.3V, 100 us



RFX2402E 802.11ac TX DEVM over Frequency VDD = 3.3V, 4 ms



RFX2402E 802.11ac TX DEVM over Frequency VDD = 3.3V, 100 us



RFX2402E 802.11ac TX Mask over Frequency
VHT20 MCS0, VDD = 3.3V