Click here for production status of specific part numbers.

MAX77640/MAX77641

Ultra-Low Power PMIC with 3-Output SIMO, 150mA LDO, and Power Sequencer

General Description

The MAX77640/MAX77641 are a low-I_Q power solution for applications where size and efficiency are critical. The device integrates a 3-output single-inductor multiple-output (SIMO) buck-boost regulator, a 150mA LDO, and a 3-channel current-sink driver.

The SIMO operates on an input between 2.7V and 5.5V. The outputs are independently programmable between 0.8V and 5.25V depending on ordering option. Each output is a buck-boost with glitchless transition between buck and boost operation. The SIMO can support >300mA loads ($1.8V_{OUT}$, $3.7V_{IN}$).

The 150mA LDO provides ripple rejection for noise-sensitive applications. The current sinks can be programmed to blink LEDs in custom patterns. The device integrates a power sequencer to control power-up/down order of each output. Default output voltages and sequence order are factory-programmable. An I^2C serial interface further configures the device.

The MAX77640/MAX77641 are available in a 30-bump wafer-level package (WLP). Total solution size is $16mm^2$. For a similar product with a battery charger, refer to the MAX77650.

Applications

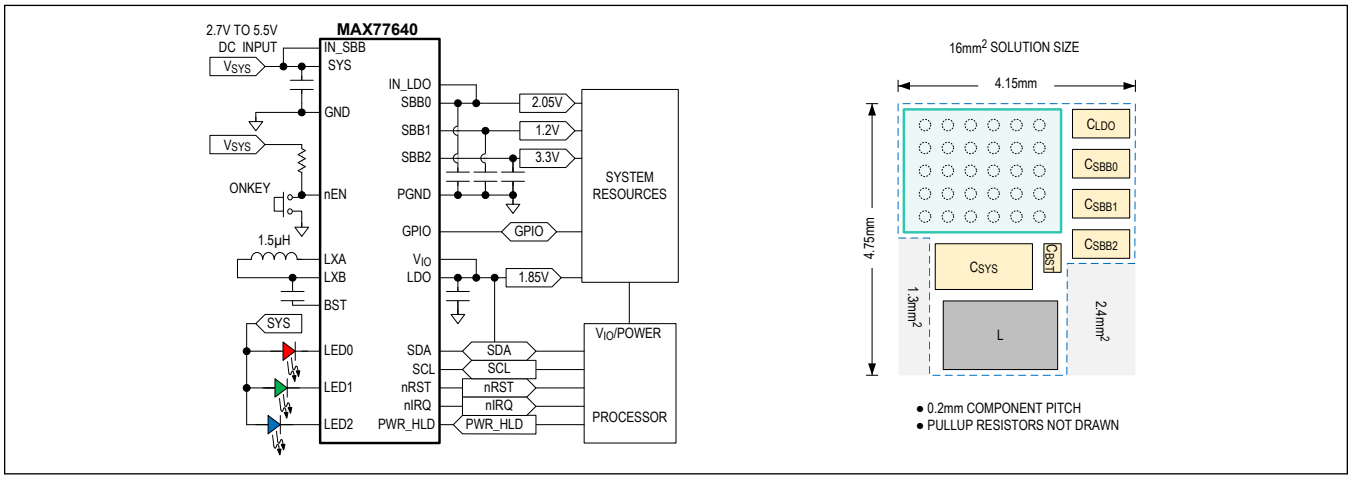
- Hearables: Bluetooth Headphones and Earbuds
- Wearables: Fitness, Health, and Activity Monitors
- Action Cameras, Wearable/Body Cameras
- Internet of Things (IoT) Gadgets

Benefits and Features

- Compact, High-Efficiency Power Solution
  - 3-Output Single-Inductor Multiple-Output (SIMO) Buck-Boost Regulator
  - 150mA LDO
  - 3-Channel Current-Sink Driver
  - Flexible Power Sequencing
  - GPIO and Reset Output
- 3-Output SIMO Extends Battery Life
  - 2.7V to 5.5V Input Voltage Range from Single Cell Li-Ion
  - 0.8V to 5.25V Output Voltage Range (Table 1)
  - Supports >300mA loads ($1.8V_{OUT}$, $3.7V_{IN}$)
  - Improves Overall System Efficiency while Reducing Size
  - Maintains Regulation without Dropout unlike Traditional Bucks
  - Glitchless Buck-Boost Operation
- Low Quiescent Current
  - 300nA Shutdown Current
  - 5.6µA Operating Current (3 SIMO Channels and LDO On)
- Small Size
  - 2.75mm x 2.15mm (0.7mm max heigh) WLP
  - 30-Bump, 0.4mm Pitch, 6 x 5 Array
  - $16mm^2$ Total Solution Size

***Ordering Information* appears at end of data sheet.**

Simplified Application Circuit



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Absolute Maximum Ratings

nEN, PWR_HLD, nIRQ, nRST to GND .....-0.3V to V_{SYS} + 0.3V
SCL, SDA, GPIO to GND .....-0.3V to V_{IO} + 0.3V
SYS to GND ..... -0.3V to +6.0V
SYS to IN_SBB ..... -0.3V to +0.3V
nIRQ, nRST, SDA, GPIO Continous Current ..... ±20mA
LDO to GND (Note 1) ..... -0.3V to V_{IN_LDO} + 0.3V
IN_LDO, V_{IO} to GND.....-0.3V to V_{SYS} + 0.3V
LED0, LED1, LED2 to LGND ..... -0.3V to +6.0V
IN_SBB to PGND ..... -0.3V to +6.0V
LXA Continuous Current (Note 1) ..... $1.2A_{RMS}$
LXB Continuous Current (Note 2) ..... $1.2A_{RMS}$
SBB0, SBB1, SBB2 to PGND (Note 3) ..... -0.3V to +6.0V
BST to IN_SBB..... -0.3V to +6.0V
BST to LXB ..... -0.3V to +6.0V
SBB0, SBB1, SBB2 Short-Circuit Duration.....Continuous
PGND to GND..... -0.3V to +0.3V
LGND to GND ..... -0.3V to +0.3V
Operating Temperature Range .....-40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range .....-65°C to +150°C
Soldering Temperature (reflow) ..... +260°C
Continuous Power Dissipation (Multilayer Board)
(T_A = +70°C, derate 20.4mW/°C above +70°C).....1632mW

Note 1: LXA has internal clamping diodes to PGND and IN_SBB. It is normal for these diodes to briefly conduct during switching events. Avoid steady-state conduction of these diodes.

Note 2: Do not externally bias LXB. LXB has an internal low-side clamping diode to PGND, and an internal high-side clamping diode that dynamically shifts to the selected SIMO output. It is normal for these internal clamping diodes to briefly conduct during switching events. When the SIMO regulator is disabled, the LXB to PGND absolute maximum voltage is -0.3V to V_{SBB0} +0.3V.

Note 3: When the active discharge resistor is engaged, limit its power dissipation to an average of 10mW.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

30 WLP 0.4mm Pitch

Package Code	W302H2+1
Outline Number	21-100047
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	49°C/W (2s2p board)

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics—Top Level

(V_{SYS} = V_{IN_SBB} = V_{IN_LDO} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, Min/Max limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{SYS}			2.7		5.5	V
Shutdown Supply Current	I_{SHDN}	Current measured into SYS, IN_SBB, and IN_LDO, all resources are off (LDO, SBB0, SBB1, SBB2, LED0, LED1, LED2), T_A = +25°C	Main bias is off (SBIA_EN = 0). This is the standby state		0.3	1	µA
			Main bias is on in low-power mode (SBIA_EN = 1, SBIA_LPM = 1)		1.0		
			Main bias is on in normal mode (SBIA_EN = 1, SBIA_LPM = 0)		28.0		
Quiescent Supply Current	I_Q	Current measured into SYS, IN_SBB, and IN_LDO. LDO, SBB0, SBB1, and SBB2 are enabled with no load. LED0, LED1, and LED2 are disabled	Main bias is in low-power mode (SBIA_LPM = 1)		5.6	13	µA
			Main bias is normal-power mode (SBIA_LPM = 0)		40	60	
POWER-ON RESET (POR)							
POR Threshold	V_{POR}	V_{SYS} falling		1.6	1.9	2.1	V
POR Threshold Hysteresis					100		mV
UNDERVOLTAGE LOCKOUT (UVLO)							
UVLO Threshold	$V_{SYSUVLO}$	V_{SYS} falling, UVLO_F[3:0] = 0xA		2.5	2.6	2.7	V
		V_{SYS} falling, UVLO_F[3:0] = 0xF		2.75	2.85	2.95	
UVLO Threshold Hysteresis	$V_{SYSUVLO\_HYS}$	UVLO_H[3:0] = 0x5			300		mV
OVERVOLTAGE LOCKOUT (OVLO)							
OVLO Threshold	$V_{SYSOVLO}$	V_{SYS} rising		5.70	5.85	6.00	V
THERMAL MONITORS							
Overtemperature-Lockout Threshold	T_{OTLO}	T_J rising			165		°C
Thermal Alarm Temperature 1	T_{JAL1}	T_J rising			80		°C
Thermal Alarm Temperature 2	T_{JAL2}	T_J rising			100		°C
Thermal Alarm Temperature Hysteresis					15		°C

Electrical Characteristics—Top Level (continued)

(V_{SYS} = V_{IN_SBB} = V_{IN_LDO} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, Min/Max limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ENABLE INPUT (nEN)							
nEN Input Leakage Current	I_{nEN_LKG}	V_{SYS} = 5.5V, V_{nEN} = 0V, and 5.5V	T_A = +25°C	-1	±0.001	+1	µA
		V_{SYS} = 5.5V, V_{nEN} = 0V and 5.5V	T_A = +85°C		±0.01		
nEN Input Falling Threshold	$V_{TH\_nEN\_F}$	nEN falling		V_{SYS} - 1.4	V_{SYS} - 1.0		V
nEN Input Rising Threshold	$V_{TH\_nEN\_F}$	nEN falling			V_{SYS} - 0.9	V_{SYS} - 0.6	V
nEN Debounce Time	t_{DBNC_nEN}	DBEN_nEN = 0			100		µs
		DBEN_nEN = 1			30		ms
nEN Manual Reset Time	t_{MRST}	MRT_OTP = 0		14	16	20	s
		MRT_OTP = 1		7	8	10.5	
POWER HOLD INPUT (PWR_HLD)							
PWR_HLD Input Leakage Current	$I_{PWR\_HLD\_LKG}$	V_{SYS} = V_{IO} = 5.5V, V_{PWR_HLD} = 0V, and 5.5V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		
PWR_HLD Input Voltage Low	V_{IL}	V_{IO} = 1.8V				0.3 x V_{IO}	V
PWR_HLD Input Voltage High	V_{IH}	V_{IO} = 1.8V		0.7 x V_{IO}			V
PWR_HLD Input Hysteresis	V_{HYS}	V_{IO} = 1.8V			50		mV
PWR_HLD Glitch Filter	$t_{PWR\_HLD\_GF}$	Both rising and falling edges are filtered			100		µs
PWR_HLD Wait Time	$t_{PWR\_HLD\_WAIT}$	Maximum time for PWR_HLD input to assert after nRST deasserts during the power-up sequence		3.5	4.0	5.0	s
OPEN-DRAIN INTERRUPT OUTPUT (nIRQ)							
nIRQ Output Voltage Low	V_{OL}	I_{SINK} = 2mA				0.4	V
nIRQ Output Falling Edge Time	t_{f_nIRQ}	$C_{\overline{IRQ}}$ = 25pF			2		ns
nIRQ Output High Leakage Current	I_{nIRQ_LKG}	V_{SYS} = V_{IO} = 5.5V, nIRQ set to be high impedance (i.e., no interrupts), V_{nIRQ} = 0V and 5.5V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		
OPEN-DRAIN RESET OUTPUT (nRST)							
nRST Output Voltage Low	V_{OL}	I_{SINK} = 2mA				0.4	V

Electrical Characteristics—Top Level (continued)

(V_{SYS} = V_{IN_SBB} = V_{IN_LDO} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, Min/Max limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
nRST Output Falling Edge Time	t_{f_nRST}	C_{RST} = 25pF			2		ns
nRST Deassert Delay Time	t_{RSTODD}	See Figure 5 for more information			5.12		ms
nRST Assert Delay Time	t_{RSTOAD}	See Figure 5 for more information			10.24		ms
nRST Output High Leakage Current	I_{nRST_LKG}	V_{SYS} = V_{IO} = 5.5V, nRST set to be high impedance (i.e., not reset), V_{nRST} = 0V and 5.5V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		
GENERAL-PURPOSE INPUT/OUTPUT (GPIO)							
Input Voltage Low	V_{IL}	V_{IO} = 1.8V				0.3 x V_{IO}	V
Input Voltage High	V_{IH}	V_{IO} = 1.8V		0.7 x V_{IO}			V
Input Leakage Current	I_{GPI_LKG}	DIR = 1, V_{IO} = 5.5V, V_{GPIO} = 0V and 5.5V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		
Output Voltage Low	V_{OL}	I_{SINK} = 2mA				0.4	V
Output Voltage High	V_{OH}	I_{SOURCE} = 1mA		0.8 x V_{IO}			V
Input Debounce Time	t_{DBNC_GPI}	DBEN_GPI = 1			30		ms
Output Falling Edge Time	t_{f_GPIO}	C_{GPIO} = 25pF			3		ns
Output Rising Edge Time	t_{r_GPIO}	C_{GPIO} = 25pF			3		ns
FLEXIBLE POWER SEQUENCER							
Power-Up Event Periods	t_{EN}	See Figure 6 for more information			1.28		ms
Power-Down Event Periods	t_{DIS}	See Figure 6 for more information			2.56		ms

Electrical Characteristics—SIMO Buck-Boost

(V_{SYS} = 3.7V, V_{IN_SBB} = 3.7V, C_{SBBx} = 10µF, L = 1.5µH, limits are 100% production tested at T_A = +25°C, Min/Max limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT VOLTAGE RANGE (SBB0)						
Minimum Output Voltage				0.8		V
Maximum Output Voltage				2.375		V
Output DAC Bits				6		bits

Electrical Characteristics—SIMO Buck-Boost (continued)

(V_{SYS} = 3.7V, V_{IN_SBB} = 3.7V, C_{SBBx} = 10µF, L = 1.5µH, limits are 100% production tested at T_A = +25°C, Min/Max limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output DAC LSB Size					25		mV
OUTPUT VOLTAGE RANGE (SBB1)							
Minimum Output Voltage		MAX77640			0.8		V
		MAX77641			2.4		
Maximum Output Voltage		MAX77640			1.5875		V
		MAX77641			5.25		
Output DAC Bits					6		bits
Output DAC LSB Size		MAX77640			12.5		mV
		MAX77641			50		
OUTPUT VOLTAGE RANGE (SBB2)							
Minimum Output Voltage		MAX77640			0.8		V
		MAX77641			2.4		
Maximum Output Voltage		MAX77640			3.95		V
		MAX77641			5.25		
Output DAC Bits					6		bits
Output DAC LSB Size					50		mV
STATIC OUTPUT VOLTAGE ACCURACY							
Output Voltage Accuracy		V_{SBBx} falling, threshold where LXA switches high. Specified as a percentage of target output voltage.	T_A = +25°C	-2.5		+2.5	%
			T_A = -40°C to +85°C	-4.0		+4.0	
TIMING CHARACTERISTICS							
Enable Delay		Delay time from the SIMO receiving its first enable signal to when it begins to switch in order to service that output.			60		µs
Soft-Start Slew Rate	dV/dt_{SS}			3.3	5.0	6.6	mV/µs
POWER STAGE CHARACTERISTICS							
LXA Leakage Current		SBB0, SBB1, SBB2 are disabled, V_{IN_SBB} = 5.5V, V_{LXA} = 0V, or 5.5V	T_A = +25°C	-1.0	±0.1	+1.0	µA
			T_A = +85°C		±1.0		
LXB Leakage Current		SBB0, SBB1, SBB2 are disabled, V_{IN_SBB} = 5.5V, V_{LXA} = 0V or 5.5V, all V_{SBBx} = 5.5V	T_A = +25°C	-1.0	±0.1	+1.0	µA
			T_A = +85°C		±1.0		
BST Leakage Current		V_{IN_SBB} = 5.5V, V_{LXB} = 5.5V, V_{BST} = 11V	T_A = +25°C		+0.01	+1.0	µA
			T_A = +85°C		+0.1		

Electrical Characteristics—SIMO Buck-Boost (continued)

(V_{SYS} = 3.7V, V_{IN_SBB} = 3.7V, C_{SBBx} = 10µF, L = 1.5µH, limits are 100% production tested at T_A = +25°C, Min/Max limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Disabled Output Leakage Current		SBB0, SBB1, SBB2 are disabled, active-discharge disabled (ADE_SBBx = 0), V_{SBBx} = 5.5V, V_{LXB} = 0V, V_{SYS} = V_{IN_SBB} = V_{BST} = 5.5V	T_A = +25°C		+0.1	+1.0	µA
			T_A = +85°C		+0.2		
Active Discharge Impedance	R_{AD_SBBx}	SBB0, SBB1, SBB2 are disabled, active discharge enabled (ADE_SBBx = 1)		80	140	260	Ω
CONTROL SCHEME							
Peak Current Limit (Note 5)	I_{P_SBB}	IP_SBBx = 0b11		0.414	0.500	0.586	A
		IP_SBBx = 0b10		0.589	0.707	0.806	
		IP_SBBx = 0b01		0.713	0.866	0.947	
		IP_SBBx = 0b00		0.892	1.000	1.108	

Note 4: Guaranteed by design and characterization but not directly production tested. Production test coverage is provided by the Shutdown Supply Current and Quiescent Supply Current specification in the *Electrical Characteristics—Top Level* table.

Note 5: Typical values align with bench observations using the stated conditions. Minimum and maximum values are tested in production with DC currents. See the *Typical Operating Characteristics* SIMO switching waveforms to gain more insight on this specification.

Electrical Characteristics—LDO

(V_{SYS} = 3.7V, V_{IN_LDO} = 2.05V, V_{LDO} = 1.85V, C_{LDO} = 10µF, limits are 100% production tested at T_A = +25°C, Min/Max limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS							
Input Voltage	V_{IN_LDO}	IN_LDO cannot exceed SYS voltage (Note 6)		1.8		5.5	V
LDO Shutdown Current	I_{IN_LDO}	Current measured into IN_LDO, LDO output disabled (Note 4)			0.1	1	µA
LDO Quiescent Supply Current (Note 4)	I_{IN_LDO}	Current measured into IN_LDO, I_{LDO}= 0mA	LDO output enabled and in regulation, V_{IN_LDO} = 2.05V, V_{LDO} = 1.85V		1.7	5.15	µA
			LDO output enabled and in dropout, V_{IN_LDO} = 1.8V, V_{LDO} target is 1.85V		2.3		
Maximum Output Current	I_{OUT}			150			mA

Electrical Characteristics—LDO (continued)

(V_{SYS} = 3.7V, V_{IN_LDO} = 2.05V, V_{LDO} = 1.85V, C_{LDO} = 10µF, limits are 100% production tested at T_A = +25°C, Min/Max limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Current Limit	I_{LIM_LDO}	V_{LDO} externally forced to 1.3V		165	255	375	mA
GENERAL CHARACTERISTICS / OUTPUT VOLTAGE RANGE							
Output Voltage Range		Programmable with TV_LDO[6:0] in 12.5mV steps		1.3500		2.9375	V
Output DAC Bits					7		bits
Output DAC LSB Size					12.5		mV
STATIC CHARACTERISTICS							
Initial Output Voltage Accuracy		I_{LDO} = 75mA, T_A = +25°C		-2.5		+2.5	%
Output Voltage Accuracy		V_{LDO} programmed from 1.35V to 2.9375V, V_{IN_LDO} = 1.8V to 5.5V, LDO not in dropout, I_{LDO} = 0mA to 150mA, T_A = -5°C to +85°C		-3		+3	%
Output Noise		f = 10Hz to 100kHz, I_{OUT} = 15mA, V_{SYS} = 3.7V, V_{IN_LDO} = 2.05V, V_{LDO} = 1.85V	Main bias circuits are in normal-power mode (SBIA_LPM = 0)		550		μV_{RMS}
			Main bias circuits are in low-power mode (SBIA_LPM = 1)		800		
TIMING CHARACTERISTICS							
Enable Delay		T_A = +25°C			0.6	1.25	ms
Soft-Start Slew Rate	dV/dt_{SS}	V_{LDO} from 10% to 90% of final value, T_A = +25°C		0.5	1.25	2.50	mV/µs
POWER STAGE CHARACTERISTICS							
Dropout Voltage	V_{LDO_DO}	V_{SYS} = 3.7V, 1.85V programmed output voltage (TV_LDO[6:0] = 0x20), V_{IN_LDO} = 1.7V, I_{LDO} = 150mA (Note 1)			90	180	mV
Dropout On-Resistance	R_{DSON}	V_{SYS} = 3.7V, 1.85V programmed output voltage (TV_LDO[6:0] = 0x20), V_{IN_LDO} = 1.7V, I_{LDO} = I_{MAX} (Note 1)	T_A = +25°C		0.6	0.9	Ω
		V_{SYS} =3.7V, 1.85V programmed output voltage (TV_LDO[6:0] = 0x20), V_{IN_LDO} = 1.7V, I_{LDO} = I_{MAX} (Note 1)	T_A = +85°C			1.2	

Electrical Characteristics—LDO (continued)

(V_{SYS} = 3.7V, V_{IN_LDO} = 2.05V, V_{LDO} = 1.85V, C_{LDO} = 10µF, limits are 100% production tested at T_A = +25°C, Min/Max limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Active-Discharge Impedance	R_{AD_LDO}	Regulator disabled, active discharge enabled (ADE_LDO = 1)		50	100	200	Ω
Disabled Output Leakage Current		Regulator disabled, active discharge disabled (ADE_LDO = 0), V_{SYS} = V_{IN_LDO} = 5.5V, V_{LDO} = 5.5V and 0V	T_A = +25°C (Note 7)		+0.1	+1.0	µA
			T_A = +85°C		+1.0		

Note 6: Dropout is the condition where the input voltage is in its valid input range but the output cannot be properly regulated because the input voltage is not sufficiently higher than the output voltage. See the *LDO Dropout* section for more information.

Note 7: Guaranteed by design and characterization but not directly production tested. The ability to disconnect the active discharge resistance is functionally checked in a production test.

Electrical Characteristics—Current Sinks

(V_{SYS} = V_{IN_SBB} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, Min/Max limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS							
Current-Sink Quiescent Current	I_Q	Change in supply current at SYS when one channel is enabled and delivering 12.8mA, V_{LEDx} = 0.2V			6	12	µA
Current-Sink Leakage		All current-sink drivers combined, outputs disabled, V_{LEDx} = 5.5V	T_A = +25ºC		+0.1	+1.0	µA
			T_A = +85ºC		+1.0		
3.2mA CURRENT-SINK RANGE (LED_FSx[1:0] = 0b01, VLEDx = 0.2V)							
Minimum Sink Current		BRT_LEDx[4:0] = 0b00000			0.1		mA
Maximum Sink Current		BRT_LEDx[4:0] = 0b11111			3.2		mA
Current-Sink DAC Bits					5		bits
Current-Sink DAC LSB					0.1		mA
Current-Sink Accuracy		BRT_LEDx[4:0] = 0b11111	T_A = +25ºC	3.10	3.20	3.25	mA
			T_A = -40ºC to +85ºC	3.03	3.20	3.36	
Dropout Voltage	V_{DO}	BRT_LEDx[4:0] = 0b11111, I_{LEDx} = 2.9mA			35	70	mV
6.4mA CURRENT-SINK RANGE (LED_FSx[1:0] = 0b10, VLEDx = 0.2V)							
Minimum Sink Current		BRT_LEDx[4:0] = 0b00000			0.2		mA
Maximum Sink Current		BRT_LEDx[4:0] = 0b11111			6.4		mA
Current-Sink DAC Bits					5		bits
Current-Sink DAC LSB					0.2		mA

Electrical Characteristics—Current Sinks (continued)

(V_{SYS} = V_{IN_SBB} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, Min/Max limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Current-Sink Accuracy		BRT_LEDx[4:0] = 0b11111	T_A = +25ºC	6.30	6.40	6.50	mA
			T_A = -40ºC to +85ºC	6.06	6.40	6.72	
Dropout Voltage	V_{DO}	LED_FSx[1:0] = 0b11, BRT_LEDx[4:0] = 0b11111, I_{LEDx} = 5.75mA			35	70	mV
12.8mA CURRENT-SINK RANGE (LED_FSx[1:0] = 0b11, VLEDx = 0.2V)							
Minimum Sink Current		BRT_LEDx[4:0] = 0b00000			0.4		mA
Maximum Sink Current		BRT_LEDx[4:0] = 0b11111			12.8		mA
Current-Sink DAC Bits					5		bits
Current-Sink DAC LSB					0.4		mA
Current-Sink Accuracy		BRT_LEDx[4:0] = 0b11111	T_A = +25ºC	12.6	12.8	13.0	mA
			T_A = -40ºC to +85ºC	12.16	12.80	13.44	
Dropout Voltage	V_{DO}	BRT_LEDx[4:0] = 0b11111, I_{LEDx} = 11.5mA			35	70	mV
TIMING CHARACTERISTICS							
Root Clock Frequency				25.6	32.0	38.4	Hz
TIMING CHARACTERISTICS / BLINK PERIOD SETTINGS							
Minimum Blink Period		P_LEDx[3:0] = 0b0000			0.5		s
					16		clocks
Maximum Blink Period		P_LEDx[3:0] = 0b1111			8		s
					256		clocks
Blink Period LSB					0.5		s
					16		clocks
TIMING CHARACTERISTICS / BLINK DUTY CYCLE							
Minimum Blink Duty Cycle		D_LEDx[3:0] = 0b0000			6.25		%
Maximum Blink Duty Cycle		D_LEDx[3:0] = 0b1111			100		%
Blink Duty Cycle LSB					6.25		%

Electrical Characteristics—I²C Serial Interface

(V_{SYS} = V_{IN_SBB} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, Min/Max limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
V_{IO} Voltage Range	V_{IO}		1.7	1.8	3.6	V

Electrical Characteristics—I²C Serial Interface (continued)

(V_{SYS} = V_{IN_SBB} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, Min/Max limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IO} Bias Current		V_{IO} = 3.6V, V_{SDA} = V_{SCL} = 0V or 3.6V	-1	0	+1	µA
		V_{IO} = 1.7V, V_{SDA} = V_{SCL}= 0V or 1.7V	-1	0	+1	
SDA AND SCL I/O STAGE						
SCL, SDA Input High Voltage	V_{IH}	V_{IO} = 1.7V to 3.6V	0.7 x V_{IO}			V
SCL, SDA Input Low Voltage	V_{IL}	V_{IO} = 1.7V to 3.6V			0.3 x V_{IO}	V
SCL, SDA Input Hysteresis	V_{HYS}			0.05 x V_{IO}		V
SCL, SDA Input Leakage Current	I_I	V_{IO} = 3.6V, V_{SCL} = V_{SDA} = 0V and 3.6V	-10		+10	µA
SDA Output Low Voltage	V_{OL}	Sinking 20mA			0.4	V
SCL, SDA Pin Capacitance	C_I			10		pF
Output Fall Time from V_{IH} to V_{IL} (Note 1)	t_{OF}				120	ns
I²C-COMPATIBLE INTERFACE TIMING (STANDARD, FAST, AND FAST-MODE PLUS) (Note 8)						
Clock Frequency	f_{SCL}		0		1000	kHz
Hold Time (REPEATED) START Condition	t_{HD_STA}		0.26			µs
SCL Low Period	t_{LOW}		0.5			µs
SCL High Period	t_{HIGH}		0.26			µs
Setup Time REPEATED START Condition	t_{SU_STA}		0.26			µs
Data Hold Time	t_{HD_DAT}		0			µs
Data Setup Time	t_{SU_DAT}		50			ns
Setup Time for STOP Condition	t_{SU_STO}		0.26			µs
Bus Free Time between STOP and START Condition	t_{BUF}		0.5			µs
Pulse Width of Suppressed Spikes	t_{SP}	Maximum pulse width of spikes that must be suppressed by the input filter		50		ns
I²C-COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, CB = 100pF) (Note 8)						
Clock Frequency	f_{SCL}				3.4	MHz
Setup Time REPEATED START Condition	t_{SU_STA}		160			ns
Hold Time (REPEATED) START Condition	t_{HD_STA}		160			ns
SCL Low Period	t_{LOW}		160			ns

Electrical Characteristics—I²C Serial Interface (continued)

(V_{SYS} = V_{IN_SBB} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, Min/Max limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

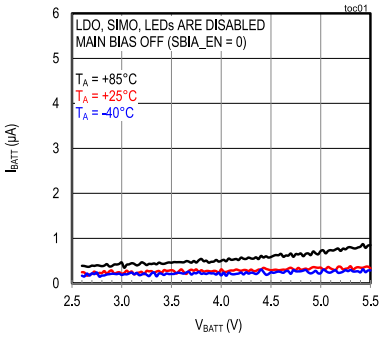
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL High Period	t_{HIGH}		60			ns
Data Setup Time	t_{SU_DAT}		10			ns
Data Hold Time	t_{HD_DAT}		0		70	ns
SCL Rise Time	t_{rCL}	T_A = +25°C	10		40	ns
Rise Time of SCL Signal after REPEATED START Condition and after Acknowledge Bit	t_{rCL1}	T_A = +25°C	10		80	ns
SCL Fall Time	t_{fCL}	T_A = +25°C	10		40	ns
SDA Rise Time	t_{rDA}	T_A = +25°C	10		80	ns
SDA Fall Time	t_{fDA}	T_A = +25°C	10		80	ns
Setup Time for STOP Condition	t_{SU_STO}		160			ns
Bus Capacitance	C_B				100	pF
Pulse Width of Suppressed Spikes	t_{SP}	Maximum pulse width of spikes that must be suppressed by the input filter		10		ns
I²C-COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, CB = 400pF) (Note 8)						
Clock Frequency	f_{SCL}				1.7	MHz
Setup Time REPEATED START Condition	t_{SU_STA}		160			ns
Hold Time (REPEATED) START Condition	t_{HD_STA}		160			ns
SCL Low Period	t_{LOW}		320			ns
SCL High Period	t_{HIGH}		120			ns
Data Setup Time	t_{SU_DAT}		10			ns
Data Hold Time	t_{HD_DAT}		0		150	ns
SCL Rise Time	t_{RCL}	T_A = +25°C	20		80	ns
Rise Time of SCL Signal after REPEATED START Condition and after Acknowledge Bit	t_{RCL1}	T_A = +25°C	20		80	ns
SCL Fall Time	t_{FCL}	T_A = +25°C	20		80	ns
SDA Rise Time	t_{RDA}	T_A = +25°C	20		160	ns
SDA Fall Time	t_{FDA}	T_A = +25°C	20		160	ns
Setup Time for STOP Condition	t_{SU_STO}		160			ns
Bus Capacitance	C_B				400	pF
Pulse Width of Suppressed Spikes	t_{SP}	Maximum pulse width of spikes that must be suppressed by the input filter		10		ns

Note 8: Design guidance only. Not production tested.

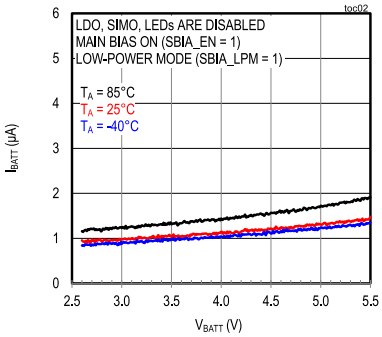
Typical Operating Characteristics

(Typical Applications Circuit, V_{SYS} = V_{IN_SBB} = 3.7V, V_{IO} = 1.8V, T_A = +25°C, unless otherwise noted.)

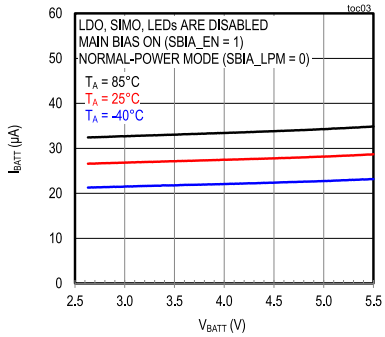
SHUTDOWN SUPPLY CURRENT vs. BATTERY VOLTAGE



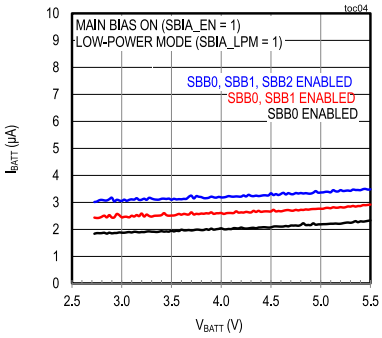
SHUTDOWN SUPPLY CURRENT vs. BATTERY VOLTAGE



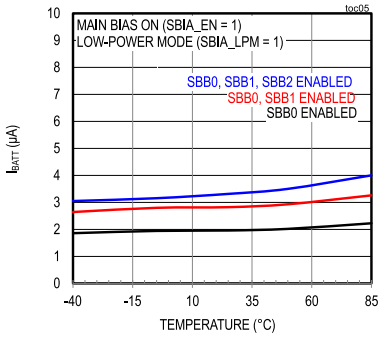
SHUTDOWN SUPPLY CURRENT vs. BATTERY VOLTAGE



QUIESCENT SUPPLY CURRENT vs. BATTERY VOLTAGE



QUIESCENT SUPPLY CURRENT vs. TEMPERATURE

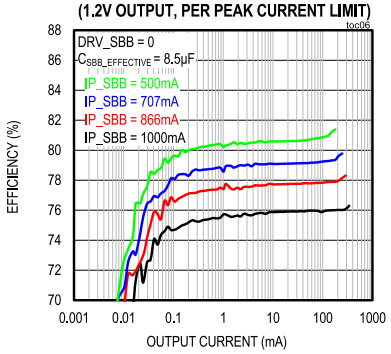


Typical Operating Characteristics (continued)

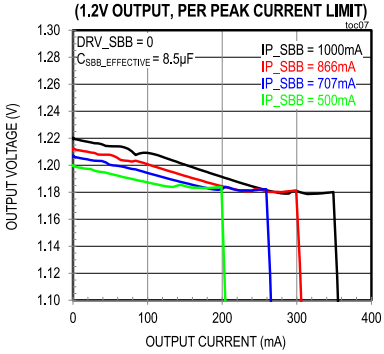
(Typical Applications Circuit, V_{SYS} = V_{IN_SBB} = 3.7V, V_{IO} = 1.8V, T_A = +25°C, unless otherwise noted.)

(Inductor = Toko DFE201210S-2R2M, 2.2µH, 127mΩ, ISAT = 1.5A, 2.0x1.2x1.0mm)

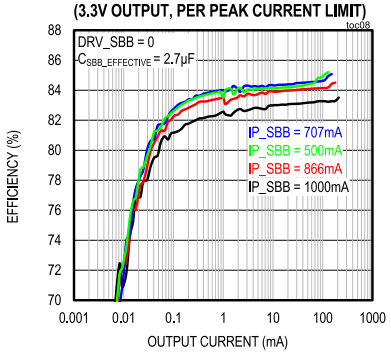
SIMO EFFICIENCY vs. OUTPUT CURRENT
(1.2V OUTPUT, PER PEAK CURRENT LIMIT)



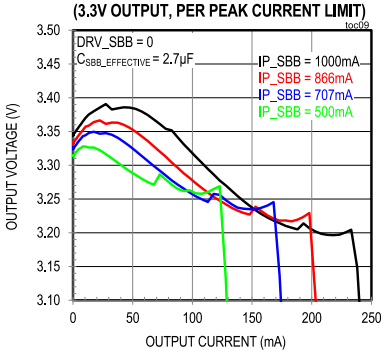
SIMO LOAD REGULATION
(1.2V OUTPUT, PER PEAK CURRENT LIMIT)



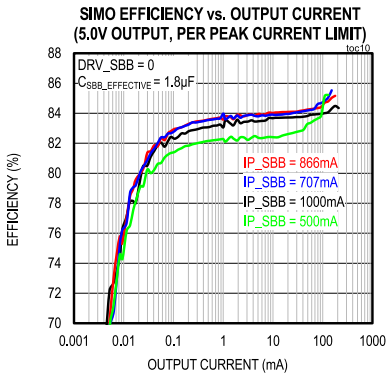
SIMO EFFICIENCY vs. OUTPUT CURRENT
(3.3V OUTPUT, PER PEAK CURRENT LIMIT)



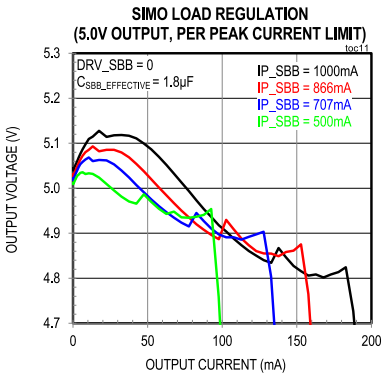
SIMO LOAD REGULATION
(3.3V OUTPUT, PER PEAK CURRENT LIMIT)



SIMO EFFICIENCY vs. OUTPUT CURRENT
(5.0V OUTPUT, PER PEAK CURRENT LIMIT)



SIMO LOAD REGULATION
(5.0V OUTPUT, PER PEAK CURRENT LIMIT)

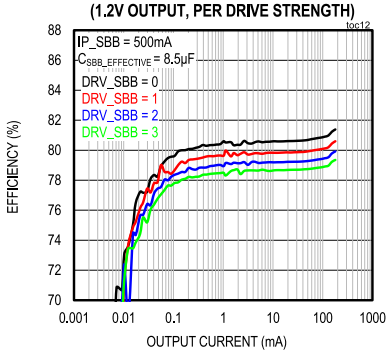


Typical Operating Characteristics (continued)

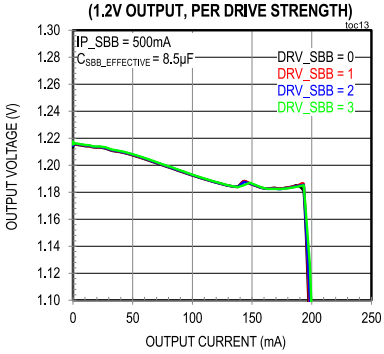
(Typical Applications Circuit, V_{SYS} = V_{IN_SBB} = 3.7V, V_{IO} = 1.8V, T_A = +25°C, unless otherwise noted.)

(Inductor = Toko DFE201210S-2R2M, 2.2µH, 127mΩ, ISAT = 1.5A, 2.0x1.2x1.0mm)

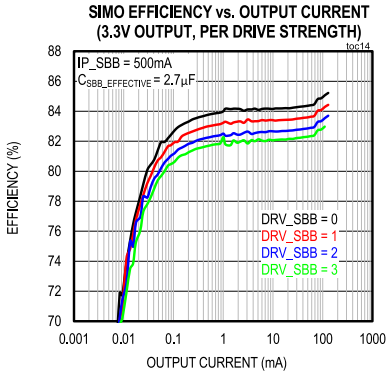
SIMO EFFICIENCY vs. OUTPUT CURRENT
(1.2V OUTPUT, PER DRIVE STRENGTH)



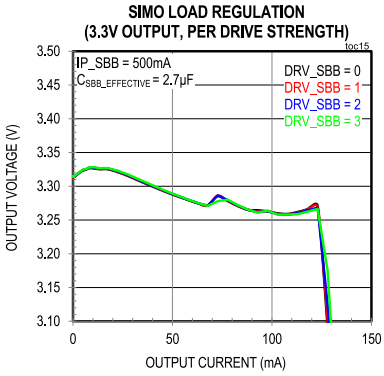
SIMO LOAD REGULATION
(1.2V OUTPUT, PER DRIVE STRENGTH)



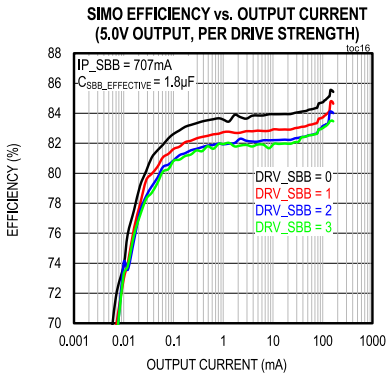
SIMO EFFICIENCY vs. OUTPUT CURRENT
(3.3V OUTPUT, PER DRIVE STRENGTH)



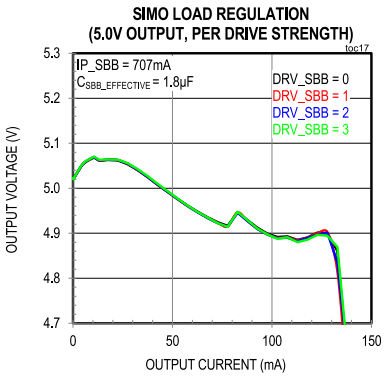
SIMO LOAD REGULATION
(3.3V OUTPUT, PER DRIVE STRENGTH)



SIMO EFFICIENCY vs. OUTPUT CURRENT
(5.0V OUTPUT, PER DRIVE STRENGTH)



SIMO LOAD REGULATION
(5.0V OUTPUT, PER DRIVE STRENGTH)

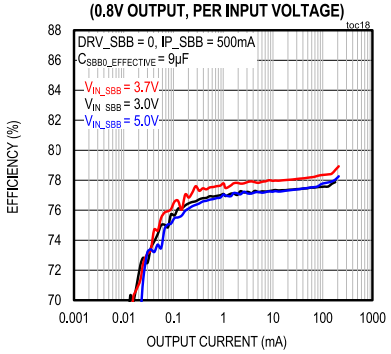


Typical Operating Characteristics (continued)

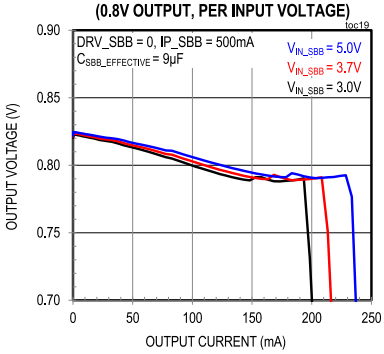
(Typical Applications Circuit, V_{SYS} = V_{IN_SBB} = 3.7V, V_{IO} = 1.8V, T_A = +25°C, unless otherwise noted.)

(Inductor = Toko DFE201210S-2R2M, 2.2µH, 127mΩ, ISAT = 1.5A, 2.0x1.2x1.0mm)

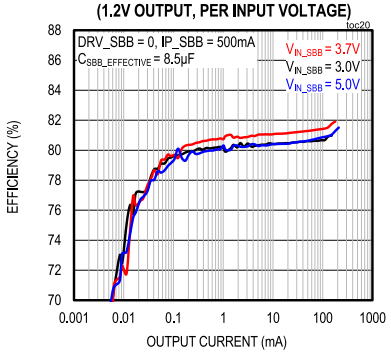
SIMO EFFICIENCY vs. OUTPUT CURRENT
(0.8V OUTPUT, PER INPUT VOLTAGE)



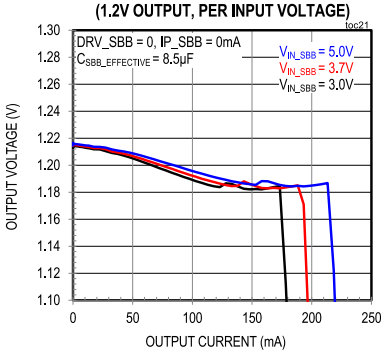
SIMO LOAD REGULATION
(0.8V OUTPUT, PER INPUT VOLTAGE)



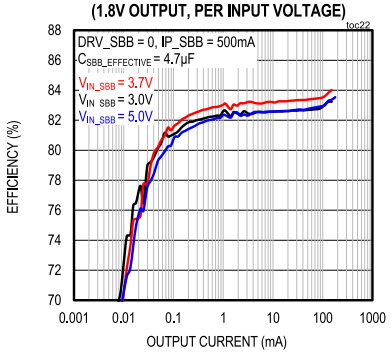
SIMO EFFICIENCY vs. OUTPUT CURRENT
(1.2V OUTPUT, PER INPUT VOLTAGE)



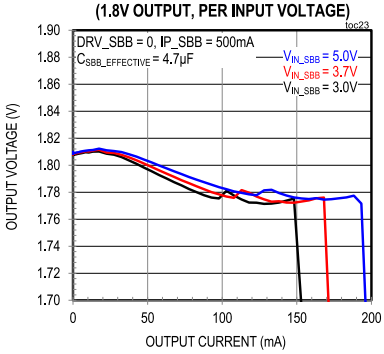
SIMO LOAD REGULATION
(1.2V OUTPUT, PER INPUT VOLTAGE)



SIMO EFFICIENCY vs. OUTPUT CURRENT
(1.8V OUTPUT, PER INPUT VOLTAGE)



SIMO LOAD REGULATION
(1.8V OUTPUT, PER INPUT VOLTAGE)

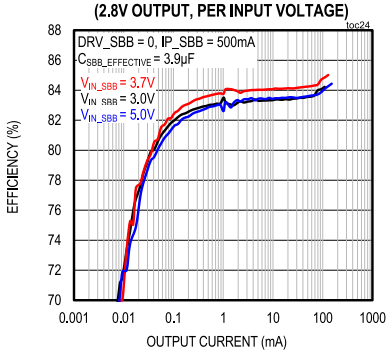


Typical Operating Characteristics (continued)

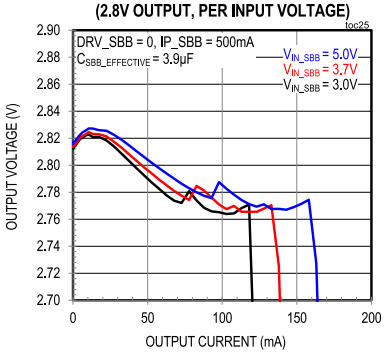
(Typical Applications Circuit, V_{SYS} = V_{IN_SBB} = 3.7V, V_{IO} = 1.8V, T_A = +25°C, unless otherwise noted.)

(Inductor = Toko DFE201210S-2R2M, 2.2µH, 127mΩ, ISAT = 1.5A, 2.0x1.2x1.0mm)

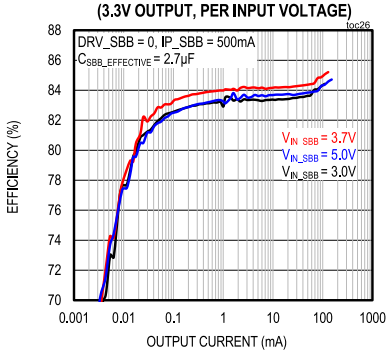
SIMO EFFICIENCY vs. OUTPUT CURRENT
(2.8V OUTPUT, PER INPUT VOLTAGE)



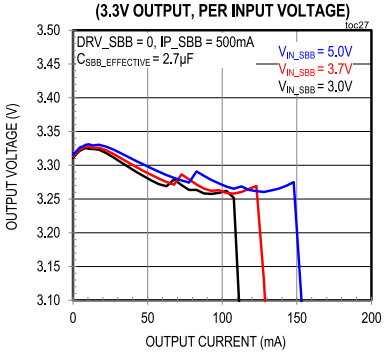
SIMO LOAD REGULATION
(2.8V OUTPUT, PER INPUT VOLTAGE)



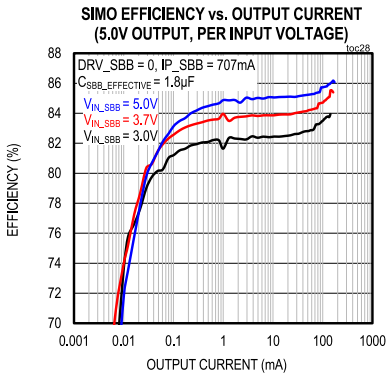
SIMO EFFICIENCY vs. OUTPUT CURRENT
(3.3V OUTPUT, PER INPUT VOLTAGE)



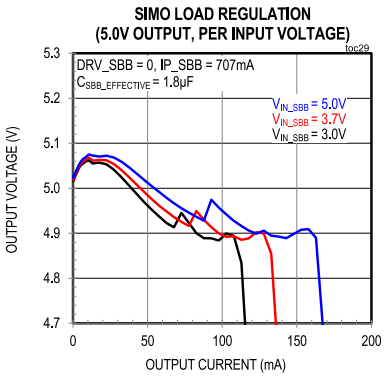
SIMO LOAD REGULATION
(3.3V OUTPUT, PER INPUT VOLTAGE)



SIMO EFFICIENCY vs. OUTPUT CURRENT
(5.0V OUTPUT, PER INPUT VOLTAGE)



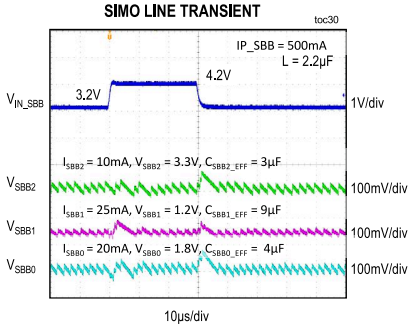
SIMO LOAD REGULATION
(5.0V OUTPUT, PER INPUT VOLTAGE)



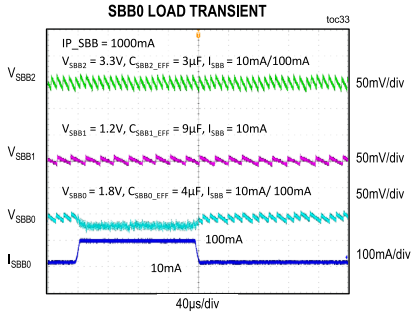
Typical Operating Characteristics (continued)

(Typical Applications Circuit, V_{SYS} = V_{IN_SBB} = 3.7V, V_{IO} = 1.8V, T_A = +25°C, unless otherwise noted.)

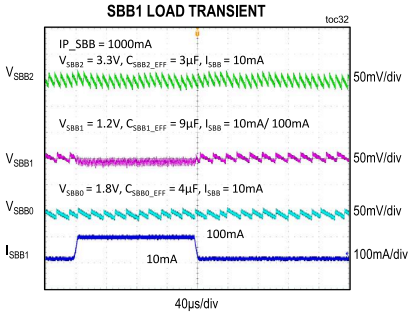
SIMO LINE TRANSIENT



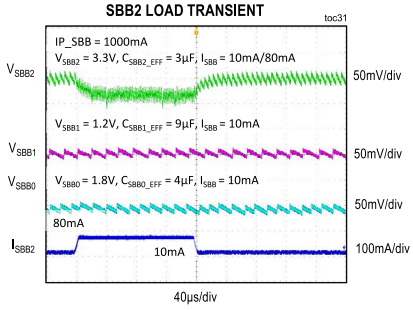
SBB0 LOAD TRANSIENT



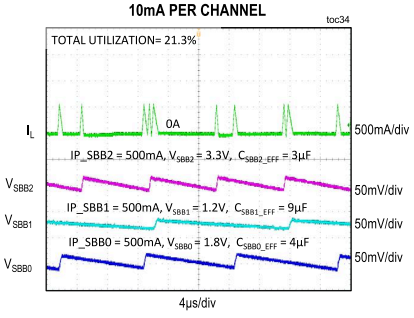
SBB1 LOAD TRANSIENT



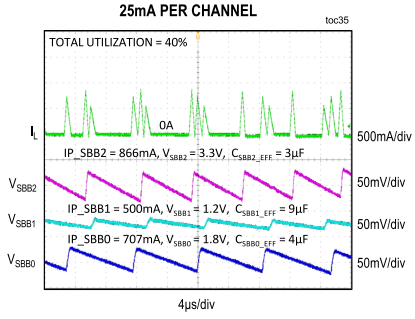
SBB2 LOAD TRANSIENT



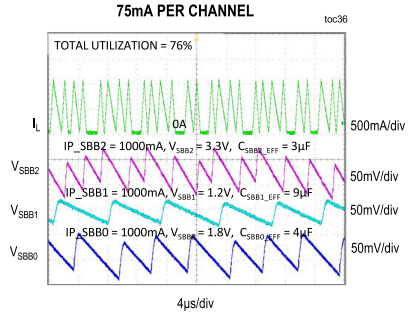
SIMO SWITCHING WAVEFORMS
LIGHT UTILIZATION
10mA PER CHANNEL



SIMO SWITCHING WAVEFORMS
MEDIUM UTILIZATION
25mA PER CHANNEL



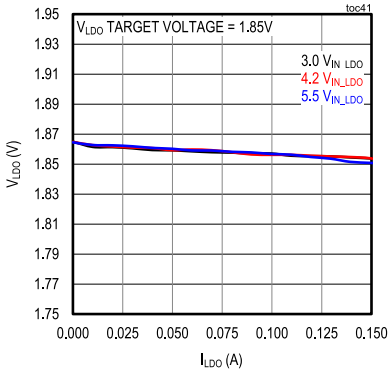
SIMO SWITCHING WAVEFORMS
HEAVY UTILIZATION
75mA PER CHANNEL



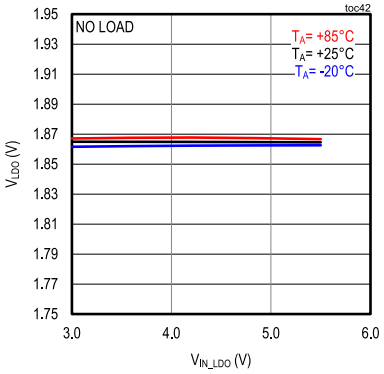
Typical Operating Characteristics (continued)

(Typical Applications Circuit, V_{SYS} = V_{IN_SBB} = 3.7V, V_{IO} = 1.8V, T_A = +25°C, unless otherwise noted.)

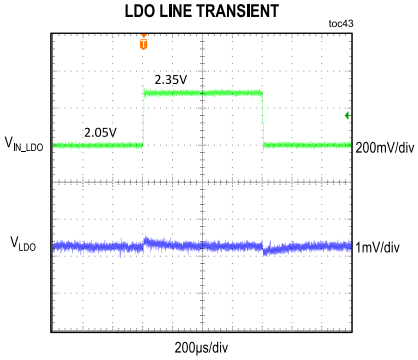
LDO LOAD REGULATION



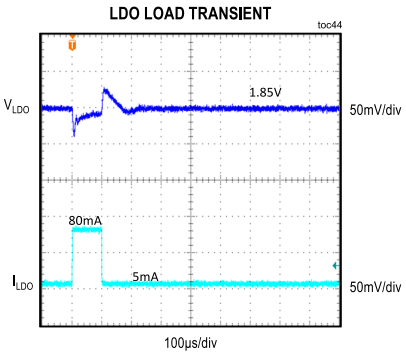
LDO LINE REGULATION



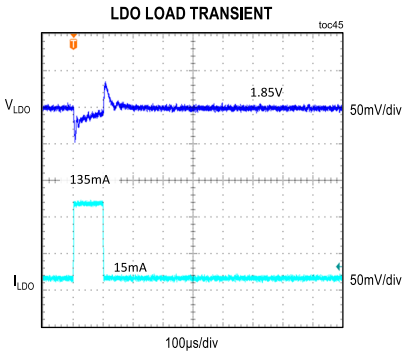
LDO LINE TRANSIENT



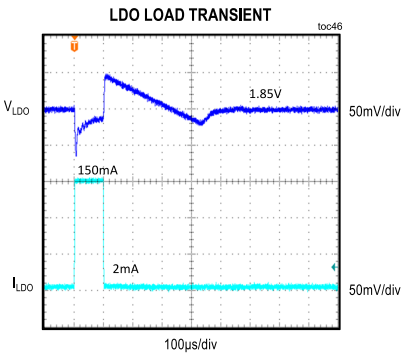
LDO LOAD TRANSIENT



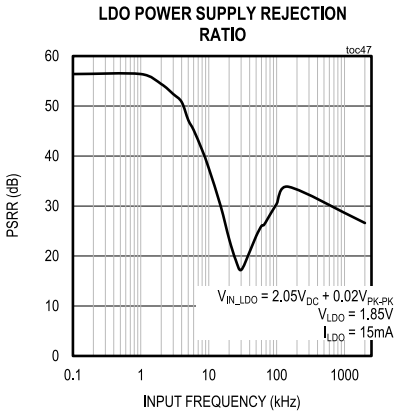
LDO LOAD TRANSIENT



LDO LOAD TRANSIENT



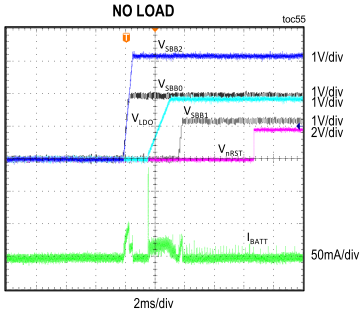
LDO POWER SUPPLY REJECTION RATIO



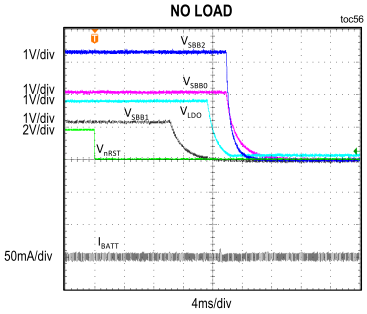
Typical Operating Characteristics (continued)

(Typical Applications Circuit, V_{SYS} = V_{IN_SBB} = 3.7V, V_{IO} = 1.8V, T_A = +25°C, unless otherwise noted.)

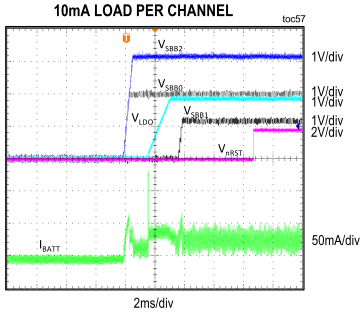
POWER UP
NO LOAD



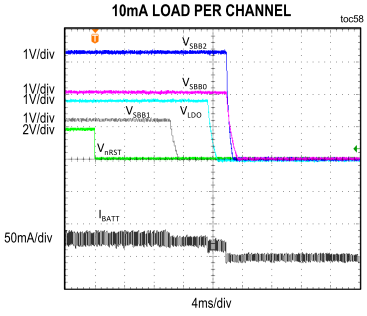
POWER DOWN
NO LOAD



POWER UP
10mA LOAD PER CHANNEL

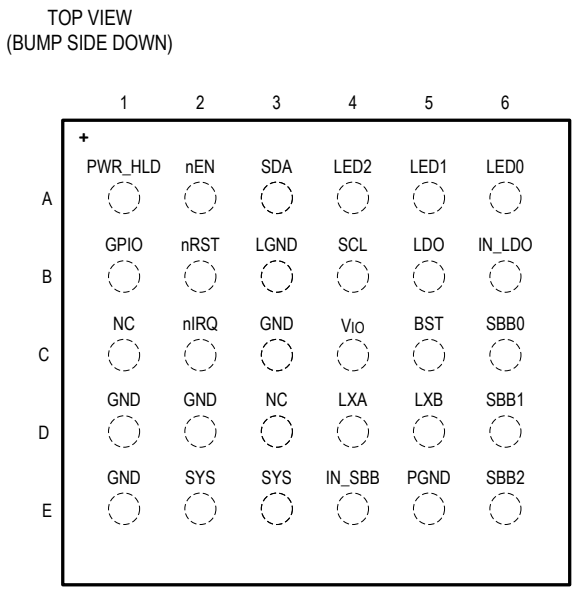


POWER DOWN
10mA LOAD PER CHANNEL



Bump Configuration

MAX77640/MAX77641



WLP
(2.75mm x 2.15mm x 0.7mm)

Bump Descriptions

PIN	NAME	FUNCTION	TYPE
TOP LEVEL			
A1	PWR_HLD	Active-High Power Hold Input. Assert PWR_HLD to keep the on/off controller in its on state. If PWR_HLD is not needed, connect it to SYS and use the SFT_RST bits to power the device down.	digital input
A2	nEN	Active-Low Enable Input. nEN supports push-button or slide-switch configurations. An external pullup resistor (10kΩ to 100kΩ) to SYS is required.	digital input
A3	SDA	I^2C Data	digital i/o
B4	SCL	I^2C Clock	digital input
B1	GPIO	General Purpose Input/Output. The GPIO I/O stage is internally biased with V_{IO}.	digital i/o
B2	nRST	Active-Low, Open-Drain Reset Output. Connect a 100kΩ pullup resistor between nRST and a voltage equal to or less than V_{SYS}.	digital output
C2	nIRQ	Active-Low, Open-Drain Interrupt Output. Connect a 100kΩ pullup resistor between nIRQ and a voltage equal to or less than V_{SYS}.	digital output
E2, E3	SYS	System Power Output. SYS provides power to the system resources as well as the control logic of the device. Connect to IN_SBB and bypass to GND with a 22µF ceramic capacitor.	power input
C3, D1, D2, E1	GND	Quiet Ground. Connect GND to PGND, LGND, and the low-impedance ground plane of the PCB.	ground

Bump Descriptions (continued)

PIN	NAME	FUNCTION	TYPE
C4	V_{IO}	I²C Interface and GPIO Driver Power	power input
C1, D3	N.C.	No Connection. Leave this pin unconnected.	
LDO			
B5	LDO	Linear Regulator Output. Connect to GND if unused.	power output
B6	IN_LDO	Linear Regulator Input. Connect to GND if unused.	power input
RGB LED DRIVER			
A6	LED0	Current Sink Port 0. LED0 is typically connected to the cathode of an LED and is capable of sinking up to 12.5mA. Connect to ground if unused.	power
A5	LED1	Current Sink Port 1. LED1 is typically connected to the cathode of an LED and is capable of sinking up to 12.5mA. Connect to ground if unused.	power
A4	LED2	Current Sink Port 2. LED2 is typically connected to the cathode of an LED and is capable of sinking up to 12.5mA. Connect to ground if unused.	power
B3	LGND	Current Sink Ground. Connect LGND to GND, PGND, and the low-impedance ground plane of the PCB.	ground
SIMO BUCK-BOOST			
E4	IN_SBB	SIMO Power Input. Connect IN_SBB to SYS and bypass to PGND with a 22µF ceramic capacitor as close as possible to the IN_SBB pin.	power input
C6	SBB0	SIMO Buck-Boost Output 0. SBB0 is the power output for channel 0 of the SIMO buck-boost. Bypass SBB0 to PGND with a 10µF ceramic capacitor.	power output
D6	SBB1	SIMO Buck-Boost Output 1. SBB1 is the power output for channel 1 of the SIMO buck-boost. Bypass SBB1 to PGND with a 10µF ceramic capacitor.	power output
E6	SBB2	SIMO Buck-Boost Output 2. SBB2 is the power output for channel 2 of the SIMO buck-boost. Bypass SBB2 to PGND with a 10µF ceramic capacitor.	power output
C5	BST	SIMO Power Input for the High-Side Output NMOS Drivers. Connect a 3300pF ceramic capacitor between BST and LXB.	power input
D4	LXA	Switching Node A. LXA is driven between PGND and IN_SBB when any SIMO channel is enabled. LXA is driven to PGND when all SIMO channels are disabled. Connect a 1.5µH inductor between LXA and LXB.	power i/o
D5	LXB	Switching Node B. LXB is driven between PGND and SBBx when SBBx is enabled. LXB is driven to PGND when all SIMO channels are disabled. Connect a 1.5µH inductor between LXA and LXB.	power i/o
E5	PGND	Power ground for the SIMO low-side FETs. Connect PGND to GND, LGND, and the low-impedance ground plane of the PCB.	ground

Detailed Description—Top Level

The MAX77640/MAX77641 provide highly-integrated power solutions for low-power applications where small size, low-quiescent current, and efficiency are critical. These devices integrate a single-inductor, multiple-output (SIMO) buck-boost regulator with three output channels. See Table 1. The three outputs of the SIMO regulator share capacity and are typically capable of providing 300mA total to the system.

A 150mA LDO is available to post-regulate SIMO outputs for audio, sensors, or other noise-sensitive applications. The LDO can also operate directly from SYS.

These devices also integrate 3-channel LED current sink drivers with individual pattern control, and a general-purpose input/output (GPIO). A bidirectional I²C serial interface allows for configuring and checking the status of the device. An internal on/off controller interfaces to either a momentary push-button on-key or an on-key slider switch. The on/off controller provides regulator power-up/down sequencing as well as other functions such as manual reset.

Table 1. Regulator Summary

REGULATOR NAME	REGULATOR TOPOLOGY	MAXIMUM I_{OUT} (mA)	V_{IN} RANGE (V)	MAX77640 V_{OUT} RANGE/ RESOLUTION	MAX77641 V_{OUT} RANGE/ RESOLUTION
SBB0	SIMO	up to 300*	2.5 to 5.5	0.8 to 2.375V in 25mV steps	0.8 to 2.375V in 25mV steps
SBB1	SIMO	up to 300*	2.5 to 5.5	0.8 to 1.5875V in 12.5mV steps	2.4 to 5.25V in 50mV steps
SBB2	SIMO	up to 300*	2.5 to 5.5	0.8 to 3.95V in 50mV steps	2.4 to 5.25V in 50mV steps
LDO	PMOS LDO	150	1.8 to 5.5	1.35 to 2.9375V in 12.5mV steps	1.35 to 2.9375V in 12.5mV steps

**Shared capacity with other SBBx channels. See the SIMO Available Output Current section for more information.*

Support Materials

The following support materials are available for these devices:

- *AN6516: MAX77640/MAX77641 Programmer's Guide* provides a description of all device registers and software advice.
- *AN6515: MAX77640/MAX77641 I²C Implementer's Guide* provides a detailed look at the I²C serial interface and standard read/write patterns.
- *MAX77640/MAX77641 SIMO Calculator* details the SIMO design procedure. See the *SIMO Available Output Current* section of the data sheet for more information.

Visit the product page at *www.maximintegrated.com/MAX77640* and/or *contact Maxim* for more information.

Top-Level Interconnect Simplified Diagram

Figure 1 shows simplified internal signal routing.

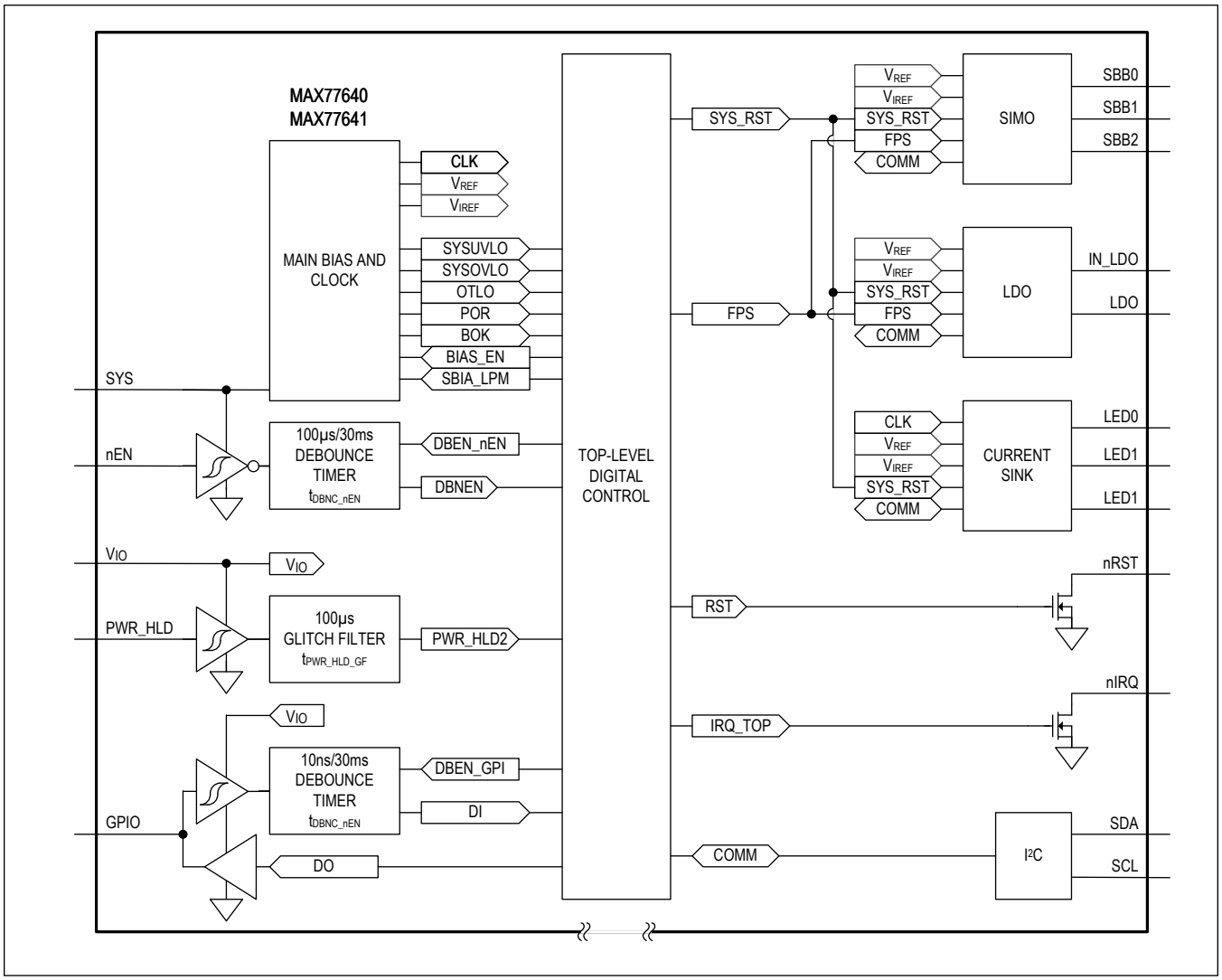


Figure 1. Top-Level Interconnect Simplified Diagram

Voltage Monitors

SYS POR Comparator

The SYS POR comparator monitors V_{SYS} and generates a power-on reset signal (POR). When V_{SYS} is below V_{POR}, the device is held in reset (SYSRST = 1). When V_{SYS} rises above V_{POR}, internal signals and on-chip memory stabilize and the device is released from reset (SYSRST = 0).

SYS Undervoltage-Lockout Comparator

The SYS undervoltage lockout (UVLO) comparator monitors V_{SYS} and generates a SYSUVLO signal when the V_{SYS} falls below UVLO threshold. The SYSUVLO signal is provided to the top-level digital controller. See Figure 4 and Table 2 for additional information regarding the UVLO comparator:

- When the device is in the STANDBY state, the UVLO comparator is disabled.
- When transitioning out of the STANDBY state, the UVLO comparator is enabled allowing the device to check for sufficient input voltage. If the device has sufficient input voltage, it can transition to the on-state; if there is insufficient input voltage, the device transitions back to the STANDBY state.

SYS Overvoltage-Lockout Comparator

These devices are rated for 5.5V maximum operating voltage (V_{SYS}) with an absolute maximum input voltage of 6.0V. An overvoltage-lockout monitor increases the robustness of the device by inhibiting operation when the supply voltage is greater than $V_{SYSOVLO}$. See Figure 4 and Table 2 for additional information regarding the OVLO comparator:

- When the device is in the STANDBY state, the OVLO comparator is disabled.

nEN Enable Input

nEN is an active-low internally debounced digital input that typically comes from the system's on-key. The debounce time is programmable with DBEN_nEN. The primary purpose of this input is to generate a wake-up signal for the PMIC that turns on the SIMO and/or LDO. Maskable rising/falling interrupts are available for nEN (nEN_R and nEN_F) for alternate functionality. nEN requires and external pullup resistor (10kΩ to 100kΩ) to SYS.

The nEN input can be configured to work either with a momentary push-button (nEN_MODE = 0) or a persistent slide-switch (nEN_MODE = 1). See Figure 2 for more information. In both push-button mode and slide-switch mode, the on/off controller looks for a falling edge on the nEN input to initiate a power-up sequence.

nEN Manual Reset

nEN works as a manual reset input when the on/off controller is in the on via on/off controller state. The manual reset function is useful for forcing a power-down in case the communication with the processor fails. When nEN is configured for a push-button mode and the input is asserted (nEN = low) for an extended period (t_{MRST}), the on/off controller initiates a power-down sequence and goes to standby mode. When nEN is configured for a slide-switch mode and the input is deasserted (nEN = high) for an extended period (t_{MRST}), the on/off controller initiates a power-down sequence and goes to standby mode.

A dedicated internal oscillator is used to create the 30ms (t_{DBNC_nEN}) and 8s/16s (t_{MRST}) timers for nEN. Whenever the device is actively counting either of these times, the supply current increases by the oscillator's supply current (65µA when the battery voltage is at 3.7V). As soon as the event driving the timer goes away or is fulfilled, the oscillator automatically turns off and its supply current goes away.

nEN Dual-Functionality: Push-Button vs. Slide-Switch

The nEN digital input can be configured to work with a push-button switch or a slide-switch. Figure 2 shows nEN's dual functionality for power-on sequencing and manual reset. The default configuration of the device is push-button mode (nEN_MODE = 0) and no additional programming is necessary. Applications that use a slide-switch on-key configuration must set nEN_MODE = 1 within t_{MRST}.

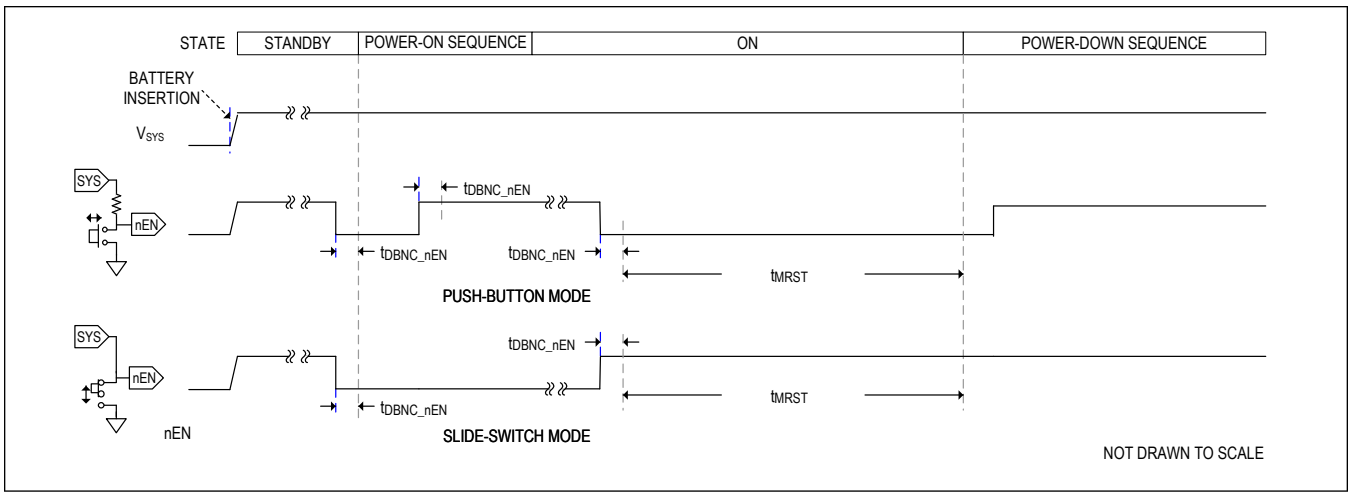


Figure 2. nEN Usage Timing Diagram

Interrupts (nIRQ)

nIRQ is an active-low, open-drain output that is typically routed to the host processor's interrupt input to signal an important change in the device's status. Refer to the Programmer's Guide for a comprehensive list of all interrupt bits and status registers.

A pullup resistor to a voltage less than or equal to V_{SYS} is required for this node. nIRQ is the logical *NOR* of all unmasked interrupt bits in the register map.

All interrupts are masked by default. Masked interrupt bits do not cause the nIRQ pin to change. Unmask the interrupt bits to allow nIRQ to assert.

Reset Output (nRST)

nRST is an open-drain, active-low output that is typically used to hold the processor in a reset state when the device is powered down. During a power-up sequence, the nRST deasserts after the last regulator in the power-up chain is enabled (t_{RSTODD}). During a power-down sequence, the nRST output asserts before any regulator is powered down (t_{RSTOAD}). See Figure 5 for nRST timing.

A pullup resistor to a voltage less than or equal to V_{SYS} is required for this node.

Power Hold Input (PWR_HLD)

PWR_HLD is an active-high digital input. PWR_HLD has a 100µs glitch filter ($t_{PWR\_HLD\_GF}$). As shown in Figure 1, the output of this glitch filter is PWR_HLD2 that drives the top-level digital control. Figure 4 and its associated transition Table 2 shows how PWR_HLD is processed by the top-level digital control.

- After the power-up sequence, the system processor must assert PWR_HLD within the PWR_HLD wait time ($t_{PWR\_HLD\_WAIT}$) to hold the power supply in the on-state. If the PWR_HLD input is not asserted within the $t_{PWR\_HLD\_WAIT}$ period, a power-down sequence is initiated.
- While in the on-state, the system processor must assert PWR_HLD as long as power is required. If the system processor wants to turn off, it can either pull PWR_HLD low or it can write the SFT_RST bits to execute the software cold reset (SFT_CRST) or software off (SFT_OFF) functions to execute the power-down sequence.

If the power hold function is not used, connect PWR_HLD to SYS and use the SFT_RST bits to power the device down.

General-Purpose Input Output (GPIO)

A general-purpose input/output (GPIO) is provided to increase system flexibility. See Figure 3 for the GPIO block diagram.

Clear DIR to configure GPIO as a general-purpose output (GPO). The GPO can either be in push-pull mode (DRV = 1) or open-drain mode (DRV = 0).

- The push-pull output mode is ideal for applications that need fast (~2ns) edges and low-power consumption.
- The open-drain mode requires an external pullup resistor (typically 10kΩ to 100kΩ). Connect the external pullup resistor to a bias voltage that is less than or equal to V_{IO}.
  - The open-drain mode can be used to communicate to different logic domains. For example, to send a signal from the GPO on a 1.8V logic domain (V_{IO} = 1.8V) to a device on a 1.2V logic domain, connect the external pullup resistor to 1.2V.
  - The open-drain mode can be used to connect several open-drain (or open-collector) devices together on the same bus to create wired logic (wired AND logic is positive-true; wired OR logic is negative-true).
- The general-purpose input (GPI) functions are still available while the pin is configured as a GPO. In other words, the DI (input status) bit still functions properly and does not collide with the state of the DIR bit.

Set DIR to disable the output drivers associated with the GPO and have the device function as a GPI. The GPI features a 30ms debounce timer (t_{DBNC_GPI}) that can be enabled or disabled with DBEN_GPI.

- Enable the debounce timer (DBEN_GPI = 1) if the GPI is connected to a device that can bounce or chatter (like a mechanical switch).
- If the GPI is connected to a circuit with clean logic transitions and no risk of bounce, disable the debounce timer (DBEN_GPI = 0) to eliminate unnecessary logic delays. With no debounce timer, the GPI input logic propagates to nIRQ in 10ns.

A dedicated internal oscillator is used to create the 30ms (t_{DBNC_GPI}) debounce timer. Whenever the device is actively counting this time, the supply current increases by the oscillator's supply current (65µA when the battery voltage is at 3.7V). As soon as the event driving the timer goes away or is fulfilled, the oscillator automatically turns off and its supply current goes away.

Maskable rising and falling interrupts (GPI_R and GPI_F) are available to signal a change in the GPI's status.

- To interrupt on a rising edge only: unmask the rising edge interrupt and mask the falling edge interrupt (GPI_RM = 0, GPI_FM = 1).
- To interrupt on a falling edge only: unmask the falling edge interrupt and mask the rising edge interrupt (GPI_RM = 1, GPI_FM = 0).
- To interrupt on either rising or falling edge: unmask both rising and falling edge interrupts (GPI_RM = 0, GPI_FM = 0).

Refer to the *Programmer's Guide* for more details.

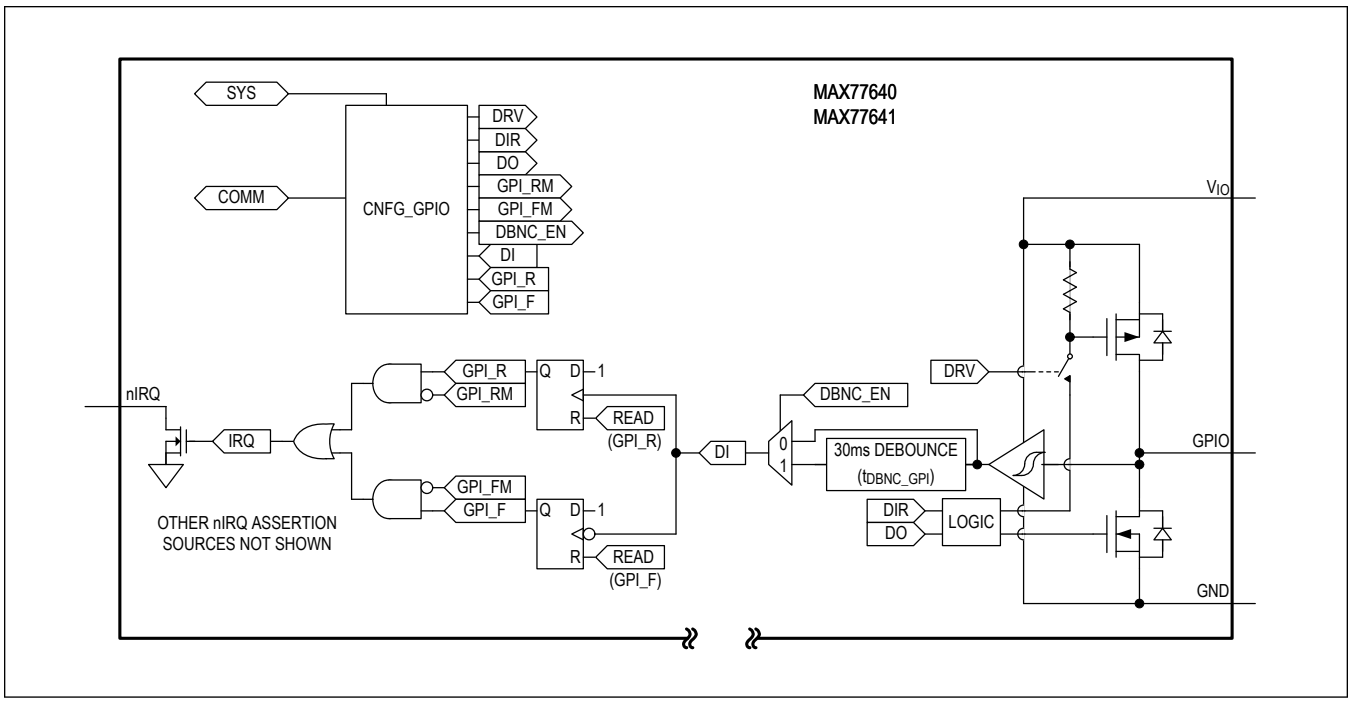


Figure 3. GPIO Block Diagram

On/Off Controller

The on/off controller monitors multiple power-up (wakeup) and power-down (shutdown) conditions to enable or disable the SIMO channels and LDO.

The basic function of the on/off controller is to control the power sequencer (see Figure 4 and Table 2). A typical use case is described as follows:

1. Start in the no-power state.
2. Apply a battery to the system and transition through path 1 and 2 to the standby state.
3. Press the system's on-key (nEN = low) and transition through path 3A and 4 to the "PWR_HLD?" state.
4. The processor boots up and drives PWR_HLD high, which drives the transition through path 4C to the on through the on/off controller state.
5. These devices perform its desired functions in the on through on/off controller state. When it is ready to turn off, the processor drives PWR_HLD low that drives the transition through path 5B and 8 to the standby state.

The SIMO can be enabled through the I^2C interface for systems that do not require a hardware (on-key) input. Connect nEN to SYS and follow this procedure:

1. Start in the no-power state.
2. Apply a battery to the system and transition through path 1 and 2 to the standby state.
3. Go to the on via software state by writing SBIA_EN = 1 through I^2C.
4. In the on via software state, the host controller can now enable/disable SIMO outputs through I^2C writes.
5. To return to standby state (shutdown), first disable all SIMO outputs then write SBIA_EN = 0.

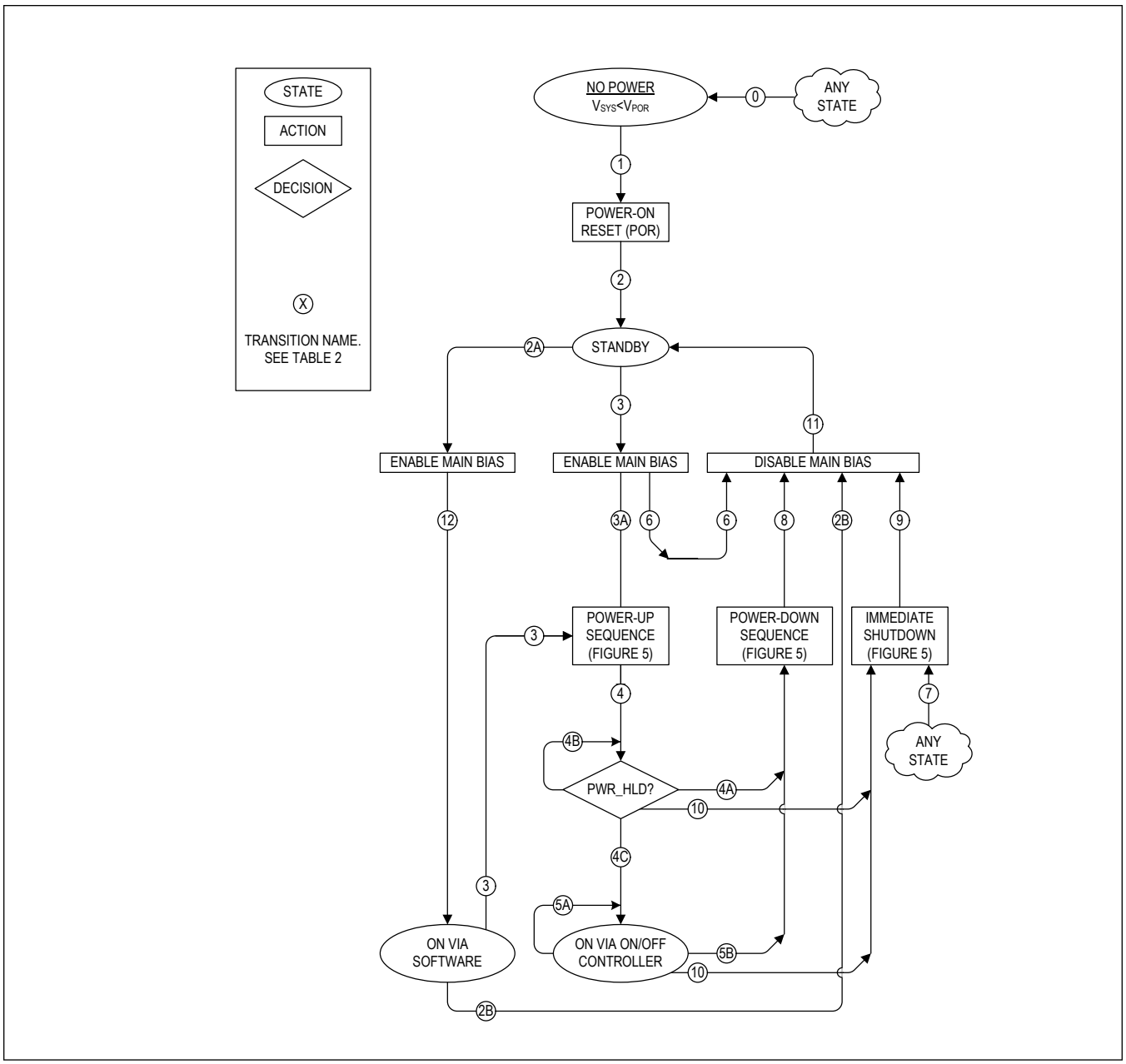


Figure 4. Top-Level On/Off Controller

Table 2. On/Off Controller Transitions

TRANSITION/ STATE	CONDITION
0	System voltage is below the POR threshold ($V_{SYS} < V_{POR}$).
1	System voltage is above the POR threshold ($V_{SYS} > V_{POR}$).

Table 2. On/Off Controller Transitions (continued)

TRANSITION/ STATE	CONDITION
2	Internal signals and on-chip memory stabilize and the device is released from reset.
STANDBY	The device is waiting for a wake-up signal or an I²C command to enable the main bias circuits. ● This is the lowest current state of the device (I_Q = 0.3µA typ). ● Main bias circuits are off, POR comparator is on. ● I²C is on when V_{IO} is valid. ● Peripheral functions do not operate in this state because the main bias circuits are off. To utilize a function, enter the on through software or on through on/off controller states.
2A	Main bias circuits enabled through I²C (SBIA_EN = 1).
2B	Main bias circuits disabled through I²C (SBIA_EN = 0).
ON VIA SOFTWARE	The main bias circuits are enabled through software and all peripheral functions can be manually enabled or disabled through I²C.
3	A wake-up signal has been received. ● A debounced on-key (nEN) falling edge has been detected (DBNEN = 1) or ● Internal wake-up flag has been set due to SFT_RST = 0b01 (WKUP = 1)
3A	Main bias circuits are OK (BOK = 1)
4	Power-up sequence complete.
4A	PWR_HLD wait time has expired and PWR_HLD2 is low ($t > t_{PWR\_HLD\_WAIT}$ && PWR_HLD2 = 0).
4B	PWR_HLD wait time has not expired and PWR_HLD2 is low ($t < t_{PWR\_HLD\_WAIT}$ && PWR_HLD2 = 0).
4C	PWR_HLD2 = 1
ON VIA ON/OFF CONTROLLER	On state. ● All flexible power sequencers (FPS) are on. ● The main bias circuits are enabled. ● I_Q = 5.6µA (typ) with all regulators enabled (no load) and the main bias circuits in low-power mode.
5A	PWR_HLD2 = 1
5B	PWR_HLD2 = 0 OR System overtemperature lockout ($T_J > T_{OTLO}$) or Software cold reset (SFT_RST[1:0] = 0b01) or Software power off (SFT_RST[1:0] = 0b10) or Manual reset occurred. See the *nEN Manual Reset* section for more information.
6	System overtemperature lockout ($T_J > T_{OTLO}$) or System undervoltage lockout ($V_{SYS} < V_{SYSUVLO} + V_{SYSUVLO\_HYS}$) or System overvoltage lockout ($V_{SYS} > V_{SYSOVLO}$)
7	System undervoltage lockout ($V_{SYS} < V_{SYSUVLO}$) or System overvoltage lockout ($V_{SYS} > V_{SYSOVLO}$) Note: The overvoltage-lockout transition does not apply to the ON VIA SOFTWARE state.
8	Finished with the power-down sequence.
9	Finished with immediate shutdown.
10	System overtemperature lockout ($T_J > T_{OTLO}$).
11	Done disabling main bias.
12	Done enabling main bias.

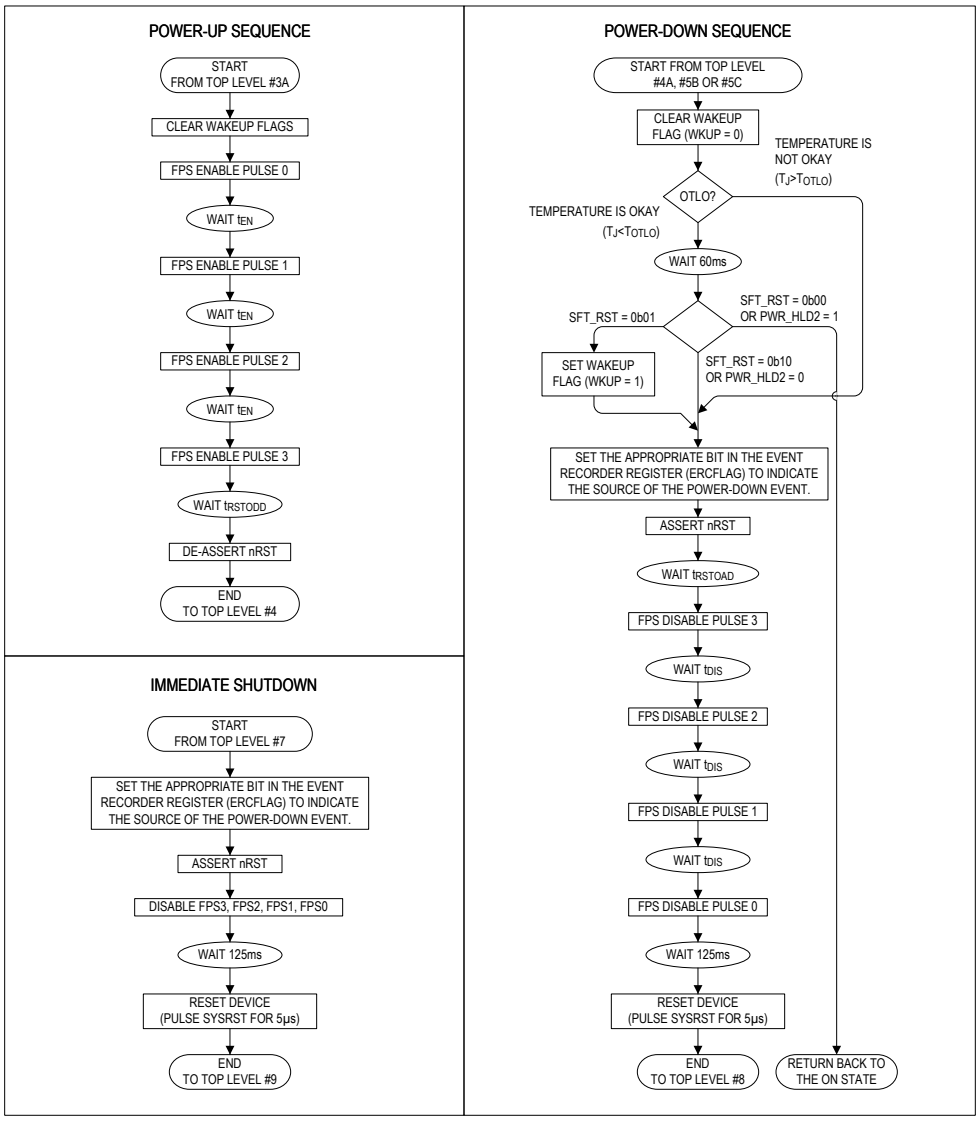


Figure 5. Power-Up/Power-Down Sequence

Flexible Power Sequencer (FPS)

The FPS allows SIMO channels to power up under hardware or software control. Additionally, each channel can power up independently or together with adjustable power-up and power-down delays (sequencing). Figure 6 shows four resources powering up under FPS control.

The FPS consists of 1 master sequencing timer and 4 slave resources (SBB0, SBB1, SBB2, and LDO). When the FPS is enabled, a master timer generates four sequencing events for device power-up and power-down.

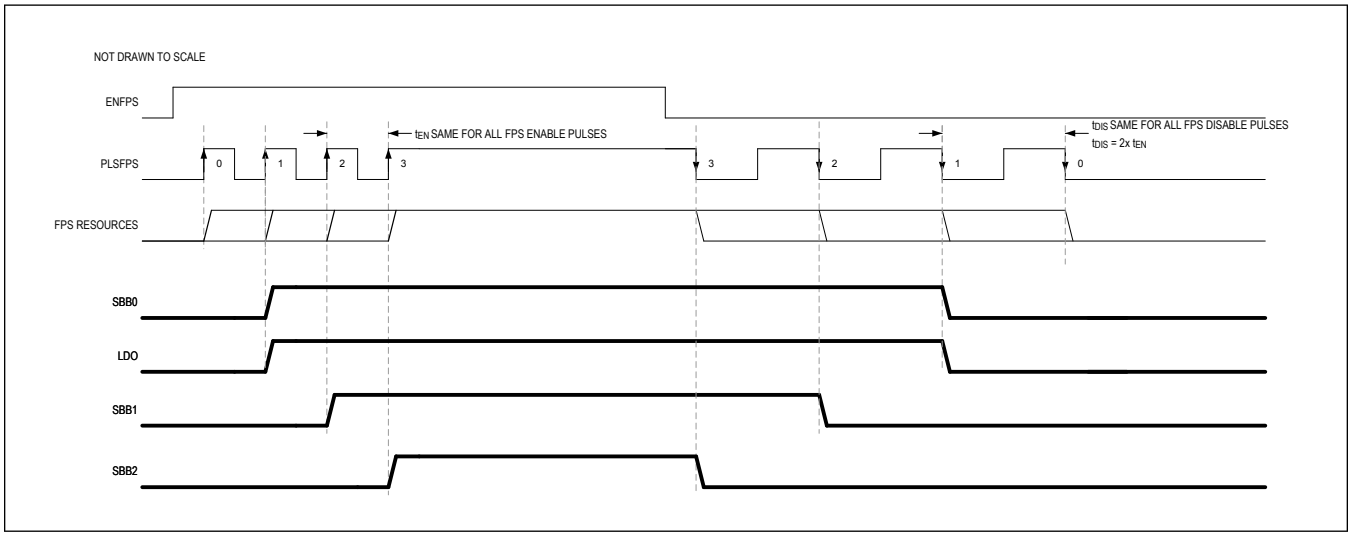


Figure 6. Flexible Power Sequencer Basic Timing Diagram

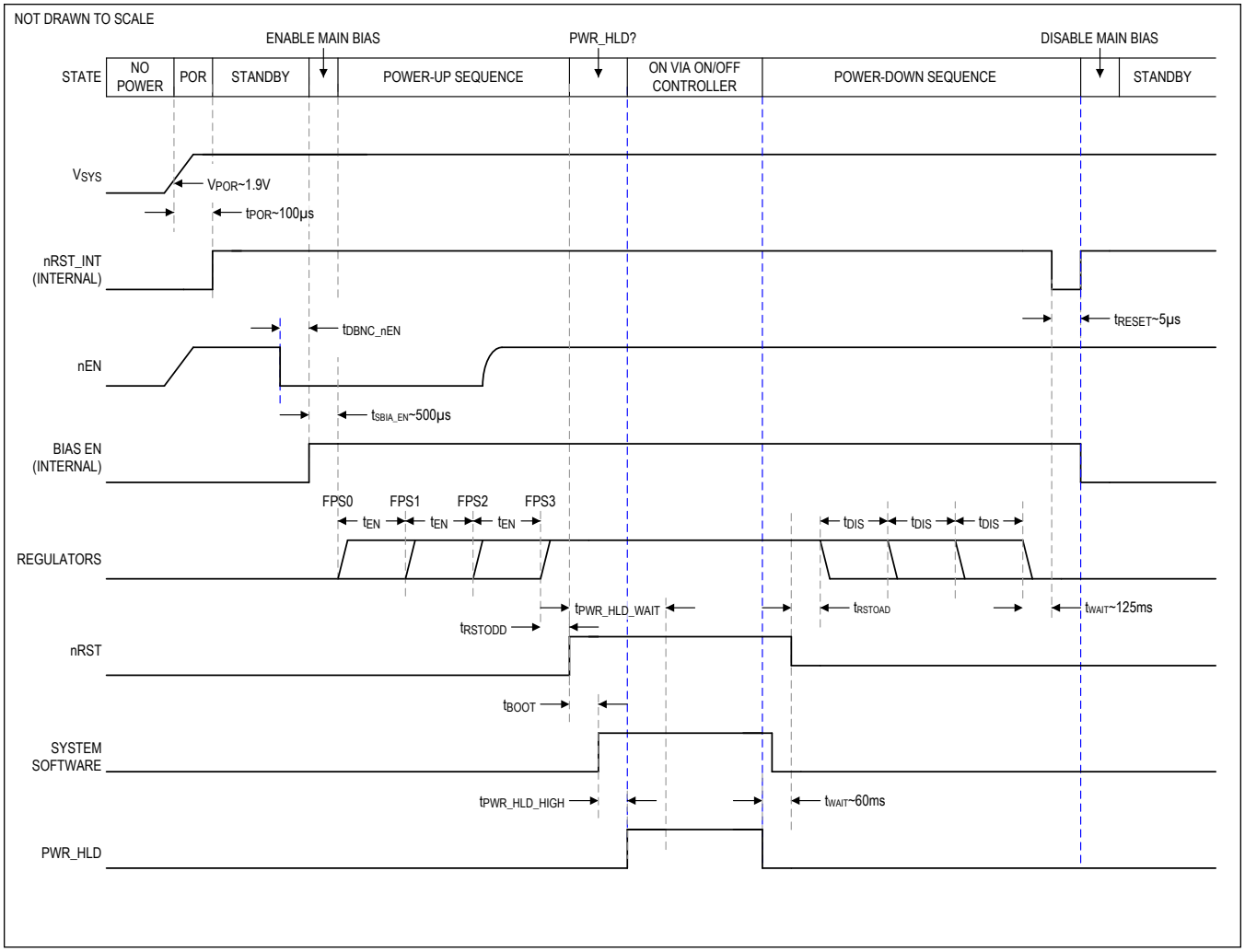


Figure 7. Startup Timing Diagram Due to nEN

Debounced Inputs (nEN and GPI)

nEN is debounced on both rising and falling edges to reject undesired transitions. The input must be at a stable logic level for the entire debounce period for the output to change its logic state. Figure 8 shows an example timing diagram for the nEN debounce.

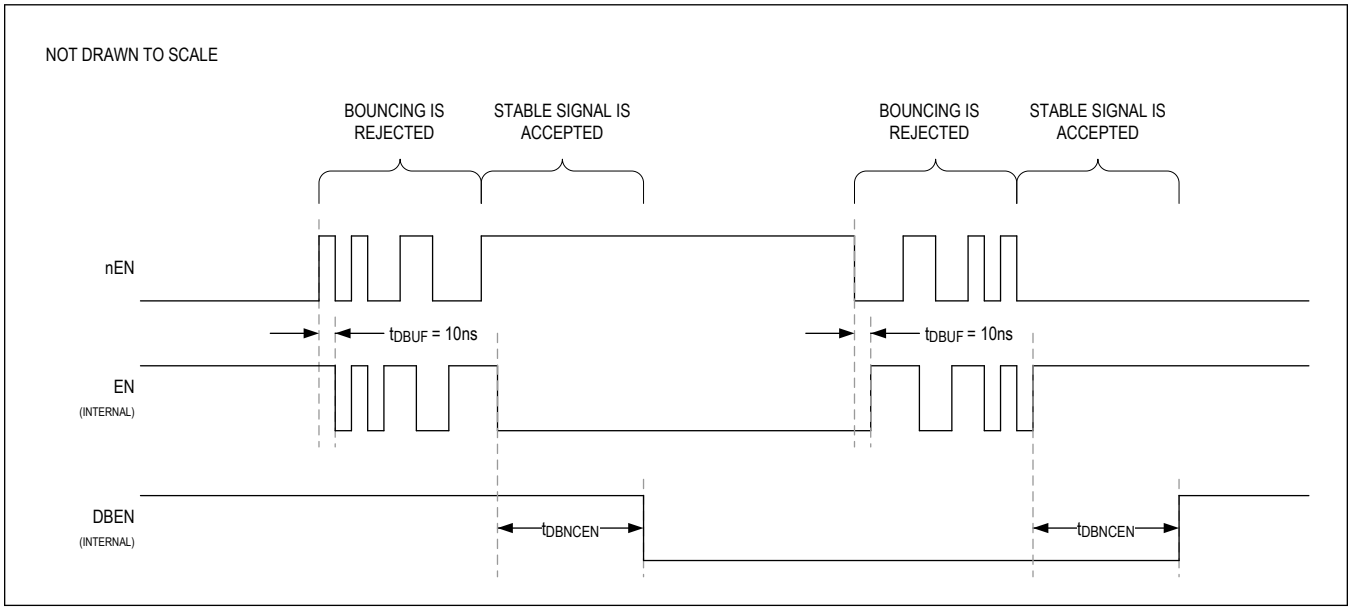


Figure 8. Debounced Inputs Timing Diagram

Thermal Alarms and Protection

These devices have thermal alarms to monitor if the junction temperature rises above 80°C (T_{JAL1}) and 100ºC (T_{JAL2}). Over-temperature lockout (OTLO) is entered if the junction temperature exceeds T_{OTLO} (approximately 165ºC typ). OTLO causes transition 10 in Figure 4 which causes the SIMO to immediately shutdown from the on via on/off controller state. Resources do not enable until the temperature falls below T_{OTLO} by approximately 15ºC.

The TJAL1_S and TJAL2_S status bits continuously indicate the junction temperature alarm status. Maskable interrupts are available to singal a change in either of these bits. Refer to the *Programmer's Guide* for details.

Register Map

The register map and register reset conditions are detailed in the *Programmer's Guide*.

Detailed Description—SIMO Buck-Boost

These devices have a micropower single-inductor, multiple-output (SIMO) buck-boost DC-to-DC converter designed for applications that emphasize low supply current and small solution size (Figure 9). A single inductor is used to regulate three separate outputs, saving board space while delivering better total system efficiency than equivalent power solutions using one buck and linear regulators.

The SIMO configuration utilizes the entire battery voltage range due to its ability to create output voltages that are above, below, or equal to the input voltage. Peak inductor current for each output is programmable to optimize the balance between efficiency, output ripple, EMI, PCB design, and load capability.

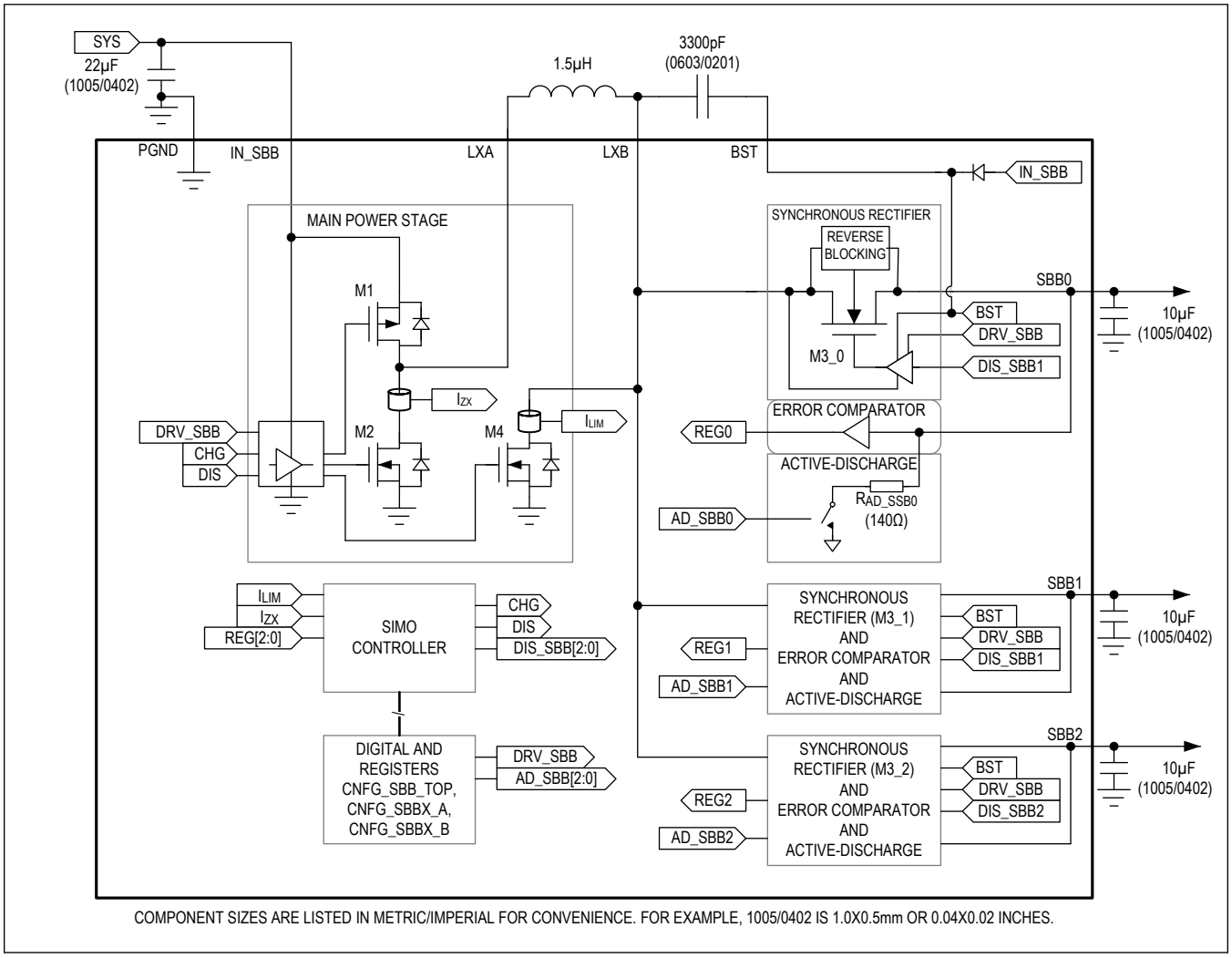


Figure 9. SIMO Detailed Block Diagram

SIMO Features and Benefits

- 3 Output Channels
- Ideal for Low-Power Designs
  - Delivers > 300mA at 1.8V from a 3.7V Input
  - ±3% Accurate Output Voltage
- Small Solution Size
  - Multiple Outputs from a Single 1.5µH Inductor
  - Small 10µF (0402) Output Capacitors
- Flexible and Easy to Use
  - Single Mode of Operation
  - Glitchless Transitions Between Buck, Buck-Boost, and Boost Scenarios
  - Programmable Peak Inductor Current
  - Programmable On-Chip Active Discharge
- Long Battery Life
  - High-Efficiency, > 87% at 3.3V Output
  - Better Total System Efficient than Buck + LDOs
  - Low Quiescent Current, 1µA per Output
  - Low Input Operating Voltage, 2.7V (min)

SIMO Control Scheme

The SIMO buck-boost is designed to service multiple outputs simultaneously. A proprietary controller ensures that all outputs get serviced in a timely manner, even while multiple outputs are contending for the energy stored in the inductor. When no regulator needs service, the state machine rests in a low-power rest state.

When the controller determines that a regulator requires service, it charges the inductor (M1 + M4) until the peak current limit is reached (I_{LIM} = IP_SBB). See Figure 9. The inductor energy then discharges (M2 + M3_x) into the output until the current reaches zero (I_{ZX}). In the event that multiple output channels need servicing at the same time, the controller ensures that no output utilizes all of the switching cycles. Instead, cycles interleave between all the outputs that are demanding service, while outputs that do not need service are skipped.

SIMO Soft-Start

The soft-start feature of the SIMO limits inrush current during startup. The soft-start feature is achieved by limiting the slew rate of the output voltage during startup (dV/dt_{SS}).

More output capacitance results in higher input current surges during startup. The following set of equations and example describes the input current surge phenomenon during startup.

The current into the output capacitor (I_{CSBB}) during soft-start is:

$$I_{CSBB} = C_{SBB}\frac{dV}{dt_{SS}} \quad \text{(Equation 1)}$$

where C_{SBB} is the capacitance on the output of the regulator, and dV/dtSS is the voltage change rate of the output.

The input current (I_{IN}) during soft-start is:

$$I_{IN} = \frac{\left(I_{CSBB} + I_{LOAD}\right)\frac{V_{SBBx}}{V_{IN}}}{\xi} \quad \text{(Equation 2)}$$

where I_{CSBB} is from the calculation above, I_{LOAD} is current consumed from the external load, V_{SBBx} is the output voltage, V_{IN} is the input voltage, and ξ is the efficiency of the regulator.

For example, given the following conditions, the peak input current (I_{IN}) during soft-start is ~71mA:

Given:

- V_{IN} is 3.5V
- V_{SBB2} is 3.3V
- C_{SBB2} = 10µF
- dV/dt_{SS} = 5mV/µs
- R_{LOAD2} = 330Ω (I_{LOAD2} = 3.3V/330Ω = 10mA)
- ξ is 85%

Calculation:

- I_{CSBB} = 10µF x 5mV/µs (from Equation 1)
- I_{CSBB} = 50mA
- $I_{IN} = \frac{(50mA + 10mA)\frac{3.3V}{3.5V}}{0.85}$ (from Equation 2)
- I_{IN} = 71mA

SIMO Output Voltage Configuration

Each SIMO buck-boost channel has a dedicated register to program its target output voltage (TV_SBBx) and its peak current limit (IP_SBBx). Additional controls are available for enabling/disabling the active discharge resistors (ADE_SBBx), as well as enabling/disabling the SIMO buck-boost channels (EN_SBBx). For a full description of bits, registers, default values, and reset conditions, refer to the *Programmer's Guide*.

SIMO Active Discharge Resistance

Each SIMO buck-boost channel has an active-discharge resistor (R_{AD_SBBx}) that is automatically enabled/disabled based on a ADE_SBBx and the status of the SIMO regulator. The active discharge feature may be enabled (ADE_SBBx = 1) or disabled (ADE_SBBx = 0) independently for each SIMO channel. Enabling the active discharge feature helps ensure a complete and timely power down of all system peripherals. If the active-discharge resistor is enabled by default, then the active-discharge resistor is on whenever V_{SYS} is below $V_{SYSUVLO}$ and above V_{POR}.

These resistors discharge the output when ADE_SBBx = 1, and their respective SIMO channel is off. Note if the regulator is forced on through EN_SBBx = 0b110 or 0b111, then the resistors do not discharge the output even if the regulator is disabled by the main-bias.

Note that when V_{SYS} is less than 1.0V, the NMOS transistors that control the active-discharge resistors lose their gate drive and become open.

When the active-discharge resistor is engaged, limit its power dissipation to an average of 10mW. For example, consider the case where the active-discharge resistance is discharging the output capacitor each time the regulator turns off; the 10mW limit allows discharge of 80µF of capacitance charged to 5V every 100ms (P = 1/2xCxV^2/t = 1/2x80µFx5V^2/100ms = 10mW).

Applications Information

SIMO Available Output Current

The available output current on a given SIMO channel is a function of the input voltage, output voltage, the peak current limit setting, and the output current of the other SIMO channels. Maxim offers a *SIMO calculator* that outlines the available capacity for specific conditions. Table 3 is an extraction from the calculator.

Table 3. SIMO Available Output Current for Common Applications

PARAMETERS	EXAMPLE 1	EXAMPLE 2	EXAMPLE 3
V.IN.MIN	2.7V	3.2V	3.4V
R.L.DCR	0.1Ω	0.1Ω	0.12Ω
SBB1	1V at 100mA	1.2V at 50mA	1.2V at 20mA
SBB0	1.2V at 75mA	2.05V at 100mA	2.05V at 80mA
SBB2	1.8V at 50mA	3.3V at 30mA	3.3V at 10mA
I.PEAK.0	1A	0.866A	0.5A
I.PEAK.1	1A	0.707A	0.5A
I.PEAK.2	1A	1A	0.5A
Utilized Capacity	73%	79%	73%

**R.C.IN = R.C.OUT = 5mΩ, L = 1.5µH*

Inductor Selection

Choose an inductance from 1.0µH to 2.2µH (1.5µH inductors is recommended for most designs). Larger inductances transfer more energy to the output for each cycle and typically result in larger output voltage ripple and better efficiency. See the *Output Capacitor Selection* section for more information on how to size the output capacitor in order to control ripple.

Choose the inductor saturation current to be greater than or equal to the maximum peak current limit setting that is used for all of the SIMO buck-boost channels (I_{P_SBB}). For example, if SBB0 is set for 0.5A, SBB1 is set for 0.866A, and SBB2 is set for 1.0A, then choose the saturation current to be greater than or equal to 1.0A.

Choose the RMS current rating of the inductor (typically the current at which the temperature rises appreciably) based on the expected load currents for the system.

Carefully consider the DC-resistance (DCR), AC-resistance (ACR) and physical size of the inductor. Smaller size inductors tend to have higher DCR and ACR which reduces SIMO efficiency. Inductors with low ACR in the 1MHz to 2MHz range are recommended for best efficiency.

See Table 4 for examples of inductors that work well with this device. This table was created in 2016. Inductor technology advances rapidly. Always consider the most current inductor technology for new designs to achieve the best possible performance.

Table 4. Example Inductors

MANUFACTURER	PART	L (µH)	I_{SAT} (A)	I_{RMS} (A)	DCR (Ω)	X (mm)	Y (mm)	Z (mm)
Samsung	CIGT201610EH2R2MN	2.2	2.9	2.7	0.073	2.0	1.6	1.0
Murata	DFE201610E-2R2M	2.2	2.6	1.9	0.117	2.0	1.6	1.0
Murata	DFE201610E-1R5M	1.5	2.4	3.2	0.076	2.0	1.6	1.0
Murata	DFE201210S-2R2M	2.2	2.3	1.80	0.127	2.0	1.2	1.0
Murata	DFE201210S-1R5M	1.5	2.2	2.6	0.086	2.0	1.2	1.0
Samsung	CIGT201208EH2R2MN	2.2	2.0	1.8	0.095	2.0	1.25	0.8
Murata	DFE201208S-1R5M	1.5	2.4	2.0	0.110	2.0	1.2	0.8
Murata	DFE201208S-2R2M	2.2	2.0	1.6	0.170	2.0	1.2	0.8

Input Capacitor Selection

Bypass IN_SBB to GND with a minimum 10µF ceramic capacitor (CIN_SBB). Larger values of CIN_SBB improve the decoupling for the SIMO regulator. CIN_SBB reduces the current peaks drawn from the battery and reduces switching noise in the system. The ESR/ESL of the input capacitor should be very low (i.e., ≤ 5mΩ and ≤ 500pH) for frequencies up to 2MHz. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. A 6.3V capacitor voltage rating is recommended for the input voltage range of up to 5.5V.

Boost Capacitor Selection

Choose the boost capacitance (C_{BST}) to be 3.3nF. Smaller values of C_{BST} (<1nF) result in insufficient gate drive for M3. Larger values of C_{BST} (>10nF) have the potential to degrade the startup performance. Ceramic capacitors with 0201 or 0402 case size are recommended.

Output Capacitor Selection

Choose each output bypass capacitor (C_{SBBx}) based on the desired output voltage ripple (typically 10µF). Larger values of C_{SBBx} improve output voltage ripple but increase input surge current during soft-start and output voltage change. The output voltage ripple is a function of the inductor, output voltage, and peak current limit setting. Maxim offers a *calculator* to aid output capacitance selection. Do not exceed the maximum output capacitance as calculated by the SIMO calculator.

The impedance of the output capacitor (ESR, ESL) should be very low (i.e., ≤ 5mΩ & ≤ 500pH) for frequencies up to 2MHz. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. Generally, small case size capacitors derate heavily compared to larger case sizes (0603 case size performs better than 0402). Consider the effective capacitance value carefully by consulting the manufacturer's data sheet.

SIMO Switching Frequency

The SIMO buck-boost regulator utilizes a pulse frequency modulation (PFM) control scheme. The switching frequency for each output is a function of the input voltage, output voltage, load current, and inductance. For example, switching frequency increases when load is increased and decreases when inductor value is increased. Maxim offers a *SIMO Calculator* to help calculate the switching frequency. See Figure 10 for examples of trends based on these parameters.

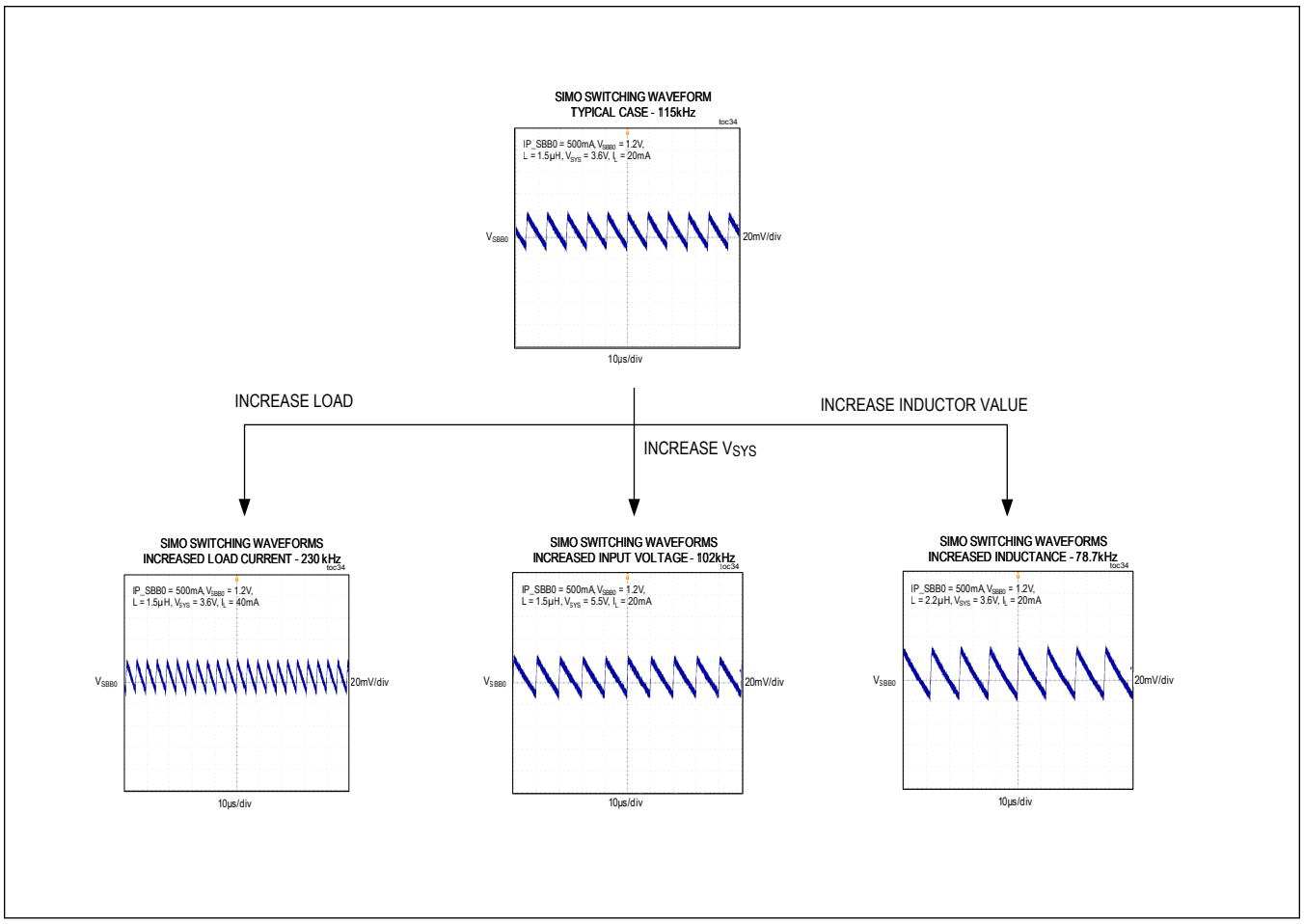


Figure 10. SIMO Switching Frequency Measurements

Unused SIMO Outputs

Do not leave unused outputs unconnected. If an output is unconnected and enabled, inductor current discharges into that unconnected pin (~50nF parasitic capacitance only), and the output voltage soars above the absolute maximum rating, potentially causing damage to the device. If the unused output is always disabled (EN_SBBx = 0x4 or 0x5), connect that output to ground. If an unused output can be enabled at any point during operation (such as startup or accidental software access), then implement one of the following:

1. Bypass the unused output with a 1µF ceramic capacitor to ground.
2. Connect the unused output to the power input (IN_SBB). This connection is beneficial because it does not require an external component for the unused output. The power input and its capacitance receives the energy packets when the regulator is enabled and V_{IN_SBB} is below the target output voltage of the unused output. Circulating the energy back to the power input ensures that the unused output voltage does not fly high.
    - Note that some OTP options of the device have the active-discharge resistors enabled by default (ADE_SBBx) such that connecting an unused output SBBx to IN_SBB creates a 140Ω (R_{AD_SBBx}) to ground until software can be ran to disable the active-discharge resistor. Connecting an unused SBBx to IN_SBB is not recommended if the regulator's active-discharge resistor is enabled by default.

3. Connect the unused output to another power output that is above the target voltage of the unused output. In the same way as the option listed above, this connection is beneficial because it does not require an external component for the unused output. Unlike the option above, this connection is preferred in cases where the unused output voltage bias level is always above the unused output voltage target because no energy packages are provided to the unused output.
   - Note that some OTP options of the device have the active-discharge resistors enabled by default (ADE_SBBx). If the other power output used to bias the unused output is normally off, then the active-discharge resistor of the unused output does not create a continuous current draw. Once the system is enabled, it should turn off the unused output's active-discharge resistor (ADE_SBBx = 0).

PCB Layout

Use the *MAX77640/MAX77641 evaluation kit* as a PCB layout reference. Good printed circuit board (PCB) layout is necessary to achieve optimal performance. The evaluation kit (EVKIT) provides an example layout that optimizes its performance. PCB layouts must:

1. Minimize parasitic inductance in the SIMO input capacitor loop which is from the IN_SBB pin to the capacitor's positive terminal and from the PGND pin to the capacitor's negative terminal.
2. Minimize the parasitic inductance in the SIMO output capacitor loop which is from SBBx to the capacitor's positive terminal and from the PGND pin to the capacitor's negative terminal.
3. Use wide traces for the inductor connections in order to minimize the resistance. Do not make the traces too large. Trace width that doesn't directly lower impedance of the LX connection only increases the fringe capacitance of the LX connection to adjacent nodes and therefore increases noise coupling.

Figure 11 shows an example PCB top-metal layout.

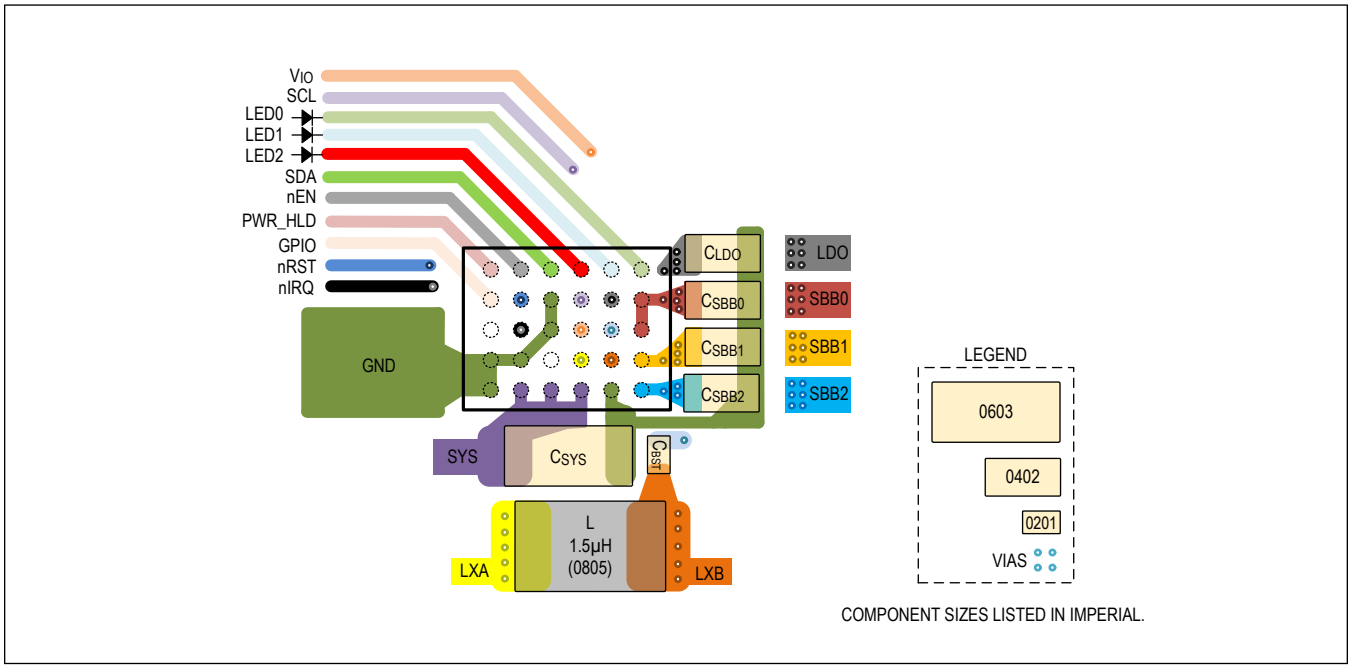


Figure 11. PCB Top-Metal and Component Layout Example

Detailed Description—LDO

These devices include a 150mA low-dropout linear regulator (LDO). Output voltage is programmable through I^2C between 1.35V and 2.9375V in 12.5mV steps using the TV_LDO[6:0] bitfield. The LDO input (INLDO) can be connected directly to SYS or supplied by an external stepdown regulator for increased power efficiency. A 100Ω (typ) active-discharge resistor is available to quickly discharge the LDO's output after the regulator has been disabled. See Figure 12 for a simplified block diagram.

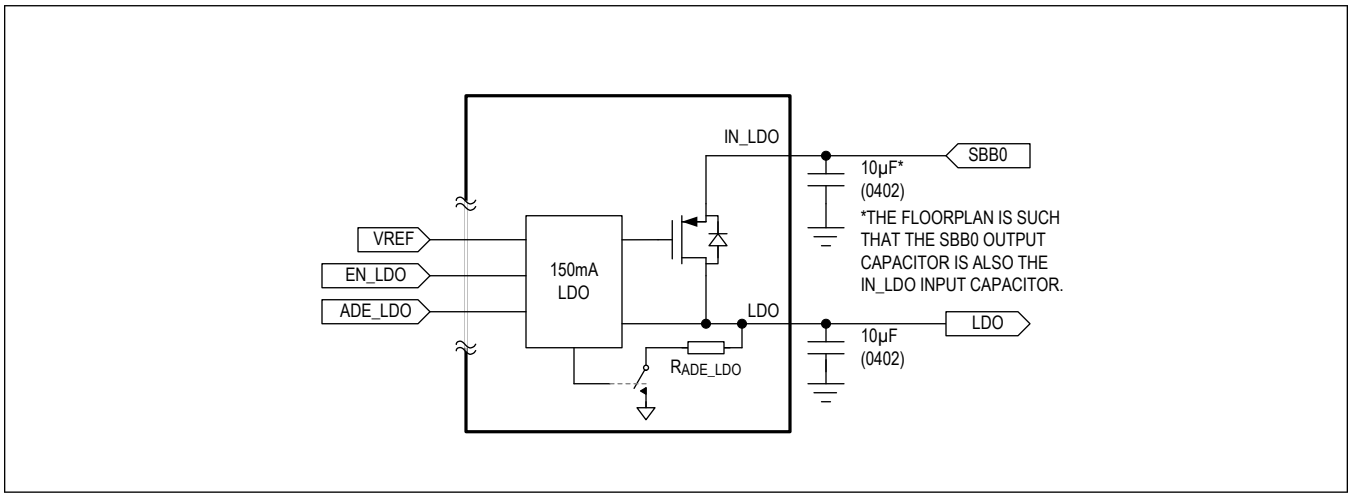


Figure 12. LDO Simplified Block Diagram

Features and Benefits

- 150mA LDO
- 1.8V to 5.5V Input Volage Range
- Adjustable Output Voltage
- 180mV Maximum Dropout Voltage
- Programmable On-Chip Active Discharge

LDO Active-Discharge Resistor

The LDO has a 100Ω active-discharge resistor (R_{AD_LDO}) that is enabled based on a configuration bit (ADE_LDO) and the status of the LDO regulator. Enabling the active discharge feature helps ensure a complete and timely power down of all system peripherals. The active-discharge resistance is disabled when $V_{SYS} < V_{POR}$ or $V_{IN\_LDO} < 1.0V$.

LDO Dropout

When the LDO input voltage is sufficiently higher than the LDO target regulation voltage, the LDO provides voltage regulation, power-supply rejection (PSRR), and noise filtering as specified in the *Electrical Characteristics*. The LDO is in dropout when the input voltage is not sufficiently higher than the output voltage. In dropout, the voltage regulation is lost and only minimal PSRR and noise filtering is provided. The *Electrical Characteristics* table specifies both a dropout voltage and a dropout on-resistance for the LDO. Applications should avoid dropout by having an input voltage greater than the output voltage plus the dropout voltage. A dropout detection interrupt is available (DOD_R; refer to the *Programmer's Guide* for more information).

LDO Soft-Start

The soft-start feature of the LDO limits inrush current during startup. The soft-start feature is achieved by limiting the slew rate of the output voltage during startup (dV/dt_{SS}).

More output capacitance results in higher input current surges during startup. The following equation and example describes the input current surge phenomenon during startup.

The input current (I_{IN}) during soft-start is:

$$I_{IN} = C_{LDO}\frac{dV}{dt_{SS}} + I_{LDO}$$

where:

- C_{LDO} is the capacitance on the output of the regulator
- dV/dt_{SS} is the voltage change rate of the output

For example, given the following conditions, the input current (I_{IN}) during soft-start is 22.5mA:

Given:

- C_{LDO} = 10µF
- dV/dt_{SS} = 1.25mV/µs
- R_{LDO} = 185Ω (I_{LDO} = 1.85V/185Ω = 10mA)

Calculation:

- I_{IN} = 10µF x 1.25mV/µs + 10mA
- I_{IN} = 22.5mA

Applications Information

Current Limit

The LDO is rated for 150mA of output current with a typical current limit of 255mA (I_{LIM_LDO}). The LDO is a voltage regulator when it is enabled and its output current is less than I_{LIM_LDO}. The LDO becomes a current source when overloaded beyond I_{LIM_LDO}. When overloaded, the LDO continues to source current as long as the LDO is enabled and the overload persists. If the overload is removed, the LDO reverts back to operating as a voltage regulator.

Current limit provides short-circuit protection for the LDO output. A shorted LDO output creates power dissipation (P_{DISS}) in the device according to the following equation: $P_{DISS} = (V_{IN\_LDO}-V_{LDO}) \times I_{LIM\_LDO}$

For example, if the LDO input voltage (V_{IN_LDO}) is 5V and a hard short is causing the output voltage (V_{LDO}) to be 0V, then P_{DISS} is typically 1.275W. If this power dissipation causes significant self-heating, then the thermal alarm 1 (TJAL1) can be used to notify the system's processor of an issue.

Using the LDO as a Load Switch

If required, the LDO can be used as a load switch. For example, if a 1.8V load switch is desired, power the LDO input (IN_LDO) with 1.8V and program the LDO output voltage to 1.9V (any value 100mV or higher than the input voltage works). In this configuration, the LDO is in dropout and its quiescent current typically is 2.3µA (I_{IN_LDO}).

Input and Output Capacitor Selection

Sufficient input bypass capacitance (C_{IN_LDO}) and output capacitance (C_{LDO}) is required for stable operation of the LDO. Figure 13 provides guidance on capacitor selection, and refers to required effective capacitance which is the actual value of capacitance seen by the LDO during operation. Effective capacitance is almost always lower than the nominal capacitance and is a commonly overlooked design parameter. Determine the effective capacitance by assessing the capacitor's initial tolerance, variation with temperature, and variation with DC bias. Consult the capacitor manufacturer for the specific details of derating.

Choose the input capacitor C_{IN_LDO} such that the effective capacitance is equal to or greater than the value found

in Figure 13, based on expected load conditions for the application. A single 10µF, 1005/0402 (mm/inch) capacitor is recommended for typical applications, but ensure that the load current and derated capacitance does not compromise the stability curve in Figure 13. Larger values of C_{IN_LDO} improve stability and decoupling for the LDO regulator. The floorplan of the device is such that SBB0 is adjacent to IN_LDO, and if SBB0 powers the input of the LDO, then the two nodes can share the SBB0 output capacitor (C_{SBB0}). C_{IN_LDO} reduces the current peaks drawn from the battery or input power source during LDO regulator operation.

Choose the output capacitor C_{LDO} such that the effective capacitance is equal to or greater than the value found in Figure 13, based on expected load conditions for the application. A single 10µF, 1005/0402 (mm/inch) capacitor is recommended for typical applications, but ensure that the load current and derated capacitance does not compromise the stability curve in Figure 13. Larger values of C_{LDO} improve stability and output PSRR, but increases the input surge currents during soft-start and output voltage changes. The effective output capacitance should not exceed 100µF to maintain LDO stability.

For example, consider the case of the MAX77640A where:

1. Size is very important.
2. The LDO input is powered by SBB0 which is 2.05V.
3. The LDO output is 1.85V.
4. The LDO output current is ≤ 80mA.

A small 1005/0402 (mm/inch) capacitor such as the GRM155R60J106ME15 (Murata, 10µF, 6.3V X5R) gives 5.7µF at 60°C and 5.4µF at -20°C and has a ± 20% tolerance, so the worst-case effective capacitance is 4.3µF (5.4µF derated by 20% tolerance). With just 4.3µF of capacitance at the output, Figure 13 shows the LDO is stable with load currents of ≤ 35mA. To get stability at 80mA, 6µF is required. There are a few options to consider here:

- Add more capacitors to the design.
- Replace the 1005/0402 (mm/inch) capacitor with a 1608/0603 (mm/inch) capacitor.
- Consider point-of-load capacitance in the assessment of effective capacitance. For example, if there is a point-of-load capacitor downstream from the LDO that is sufficiently close to the local LDO output capacitor, it can cover the gap. The capacitor can be considered 'sufficiently close' if the PCB does not add more than 25nH and 25mΩ of extra ESR and ESL (more or less within 1").

Note the impedance of either the input or output capacitor (ESR, ESL) should be very low (i.e., ≤ 50mΩ + ≤ 5nH) for frequencies up to 0.5MHz. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients.

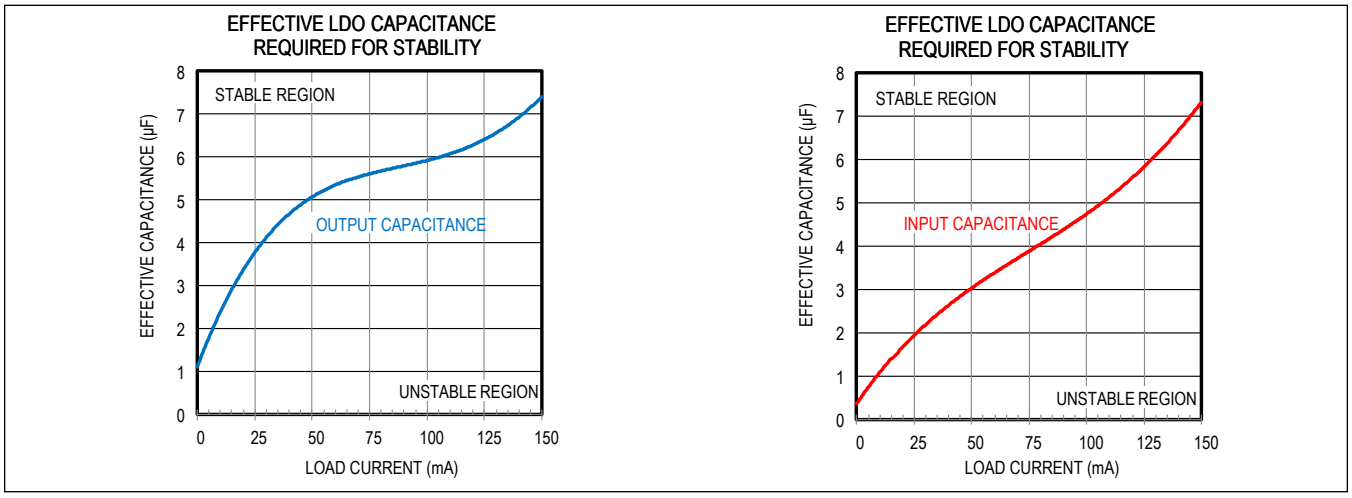


Figure 13. LDO Capacitance for Stability

Detailed Description—Current Sinks

These devices have a 3-channel current sink driver designed to drive LED's in portable devices. This block can also be used as a general-purpose current sink driver for other applications. The driver's on-time and frequency are independently programmable for each output to achieve a desired blink pattern. Alternatively, the LEDs can be continuously on (i.e., not blinking). The blink period is programmable from 0.5s to 8s, with an on-time duty cycle from 6.25% to 100%.

Figure 14 utilizes a common set of clock dividers to drive three identical current sink modules. Refer to the *Programmer's Guide* for more information.

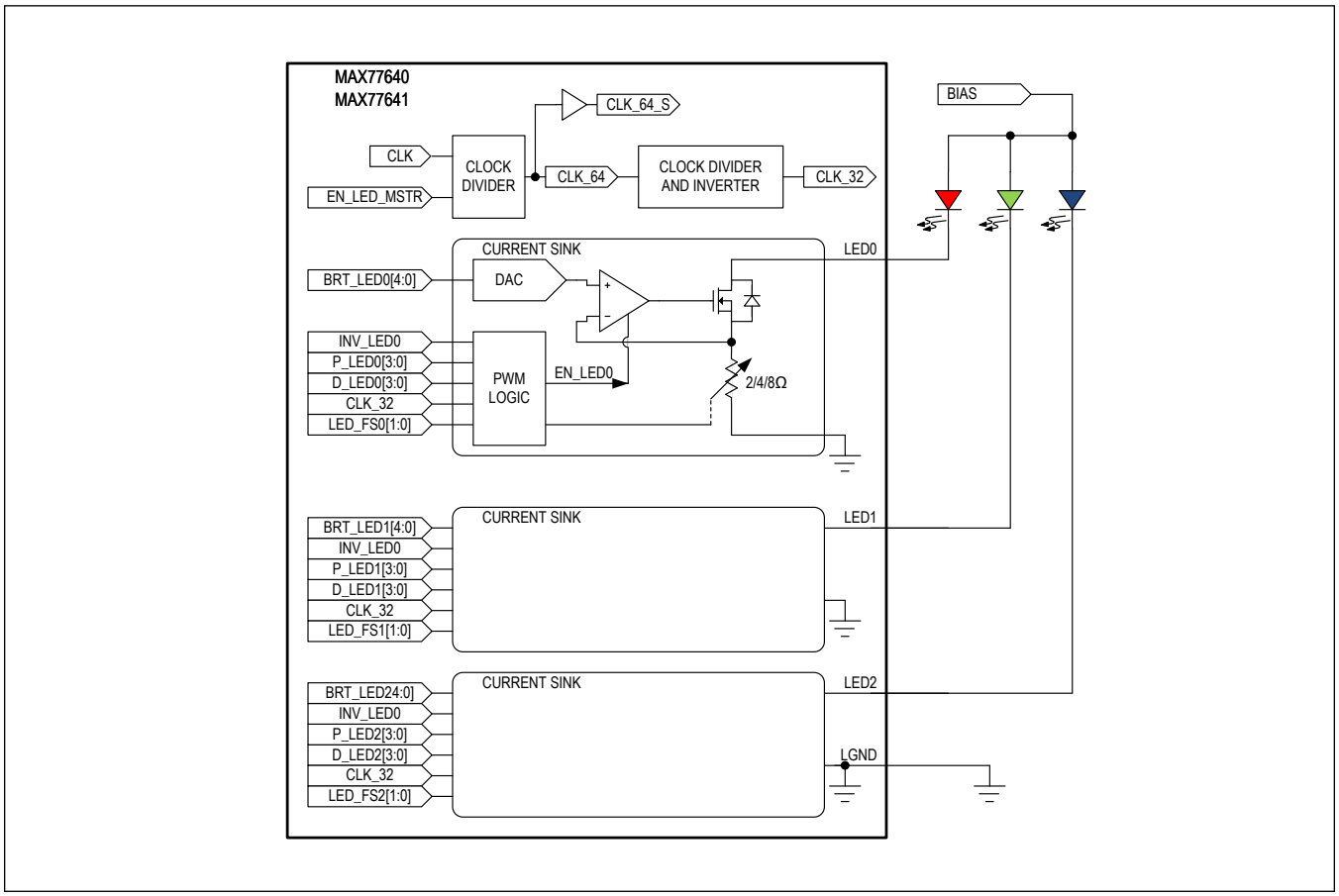


Figure 14. Current Sink Block Diagram

Applications Information

LED Assignment

The three current sinks (LED0, LED1, LED2) are identical. In the typical application where a red, green, blue LED cluster is used (RGB), the assignment of the RGB elements to the LED0/1/2 pins should be done in whatever way makes the PCB layout the easiest.

Unused Current Sink Ports

If a current sink port is not utilized in a given application, connect that port to ground. Additionally, software should ensure that the unused current sink is not enabled (EN_LEDx = 0).

Detailed Description—I²C Serial Interface

The MAX77640/MAX77641 feature a revision 3.0 I²C-compatible, 2-wire serial interface consisting of a bidirectional serial data line (SDA) and a serial clock line (SCL). As shown in Figure 15, the I²C SDA and SCL signals are internally decoded by the devices used to communicate with the top-level control logic as well as the SIMO, LDO, GPIO, and current sinks. The MAX77640/MAX77641 are slave-only devices which rely on an external bus master to generate SCL. SCL clock rates from 0Hz to 3.4MHz are supported. I²C is an open-drain bus and therefore, SDA and SCL require pullups.

The MAX77640/MAX77641 I²C communication controller implements 7-bit slave addressing. An I²C bus master initiates communication with the slave by issuing a START condition followed by the slave address (Figure 16). The OTP address is factory programmable for one of two options (Table 5). All slave addresses not mentioned in Table 5 are not acknowledged.

The devices use 8-bit registers with 8-bit register addressing. They support standard communication protocols: (1) writing to a single register (2) writing to multiple sequential registers with an automatically incrementing data pointer (3) reading from a single register (4) reading from multiple sequential registers with an automatically incrementing data pointer. For additional information on the I²C protocols, refer to the *MAX77640/MA77641 I²C Implementation Guide* and/or the I²C specification that is freely available on the internet.

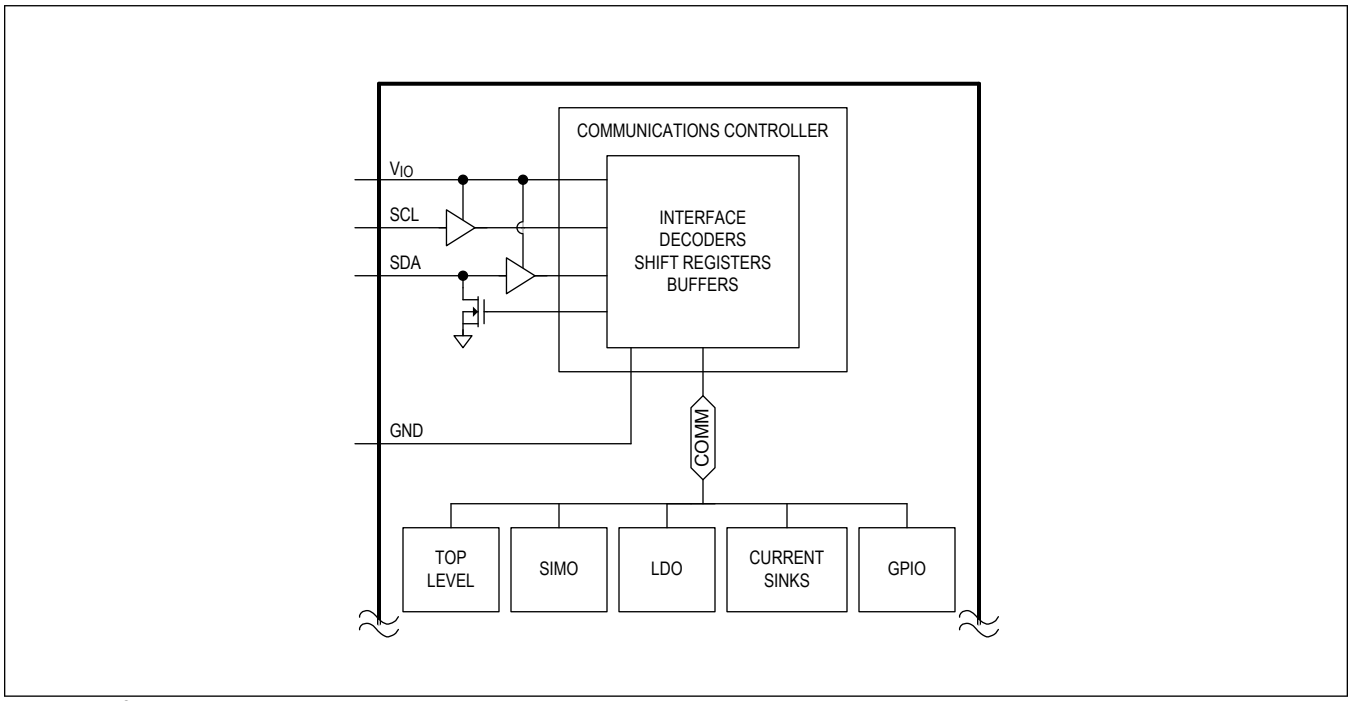


Figure 15. I²C Simplified Block Diagram

.

Table 5. I²C Slave Address Options

ADDRESS	7-BIT SLAVE ADDRESS	8-BIT WRITE ADDRESS	8-BIT READ ADDRESS
Main Address (ADDR = 1)*	0x48, 0b 100 1000	0x90, 0b 1001 0000	0x91, 0b 1001 0001
Main Address (ADDR = 0)*	0x40, 0b 100 0000	0x80, 0b 1000 0000	0x81, 0b 1000 0001
Test Mode**	0x49, 0b 100 1001	0x92, 0b 1001 0010	0x93, 0b 1001 0011

**Perform all reads and writes on the main address. ADDR is a factory one-time programmable (OTP) option, allowing for address changes in the event of a bus conflict. Contact Maxim for more information.*

**When test mode is unlocked, the additional address is acknowledged. Test mode details are confidential. If possible, leave the test mode address unallocated to allow for the rare event that debugging needs to be performed in cooperation with Maxim.

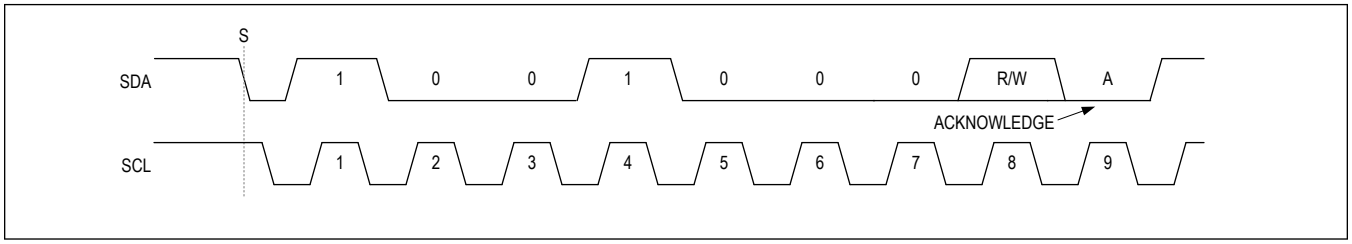
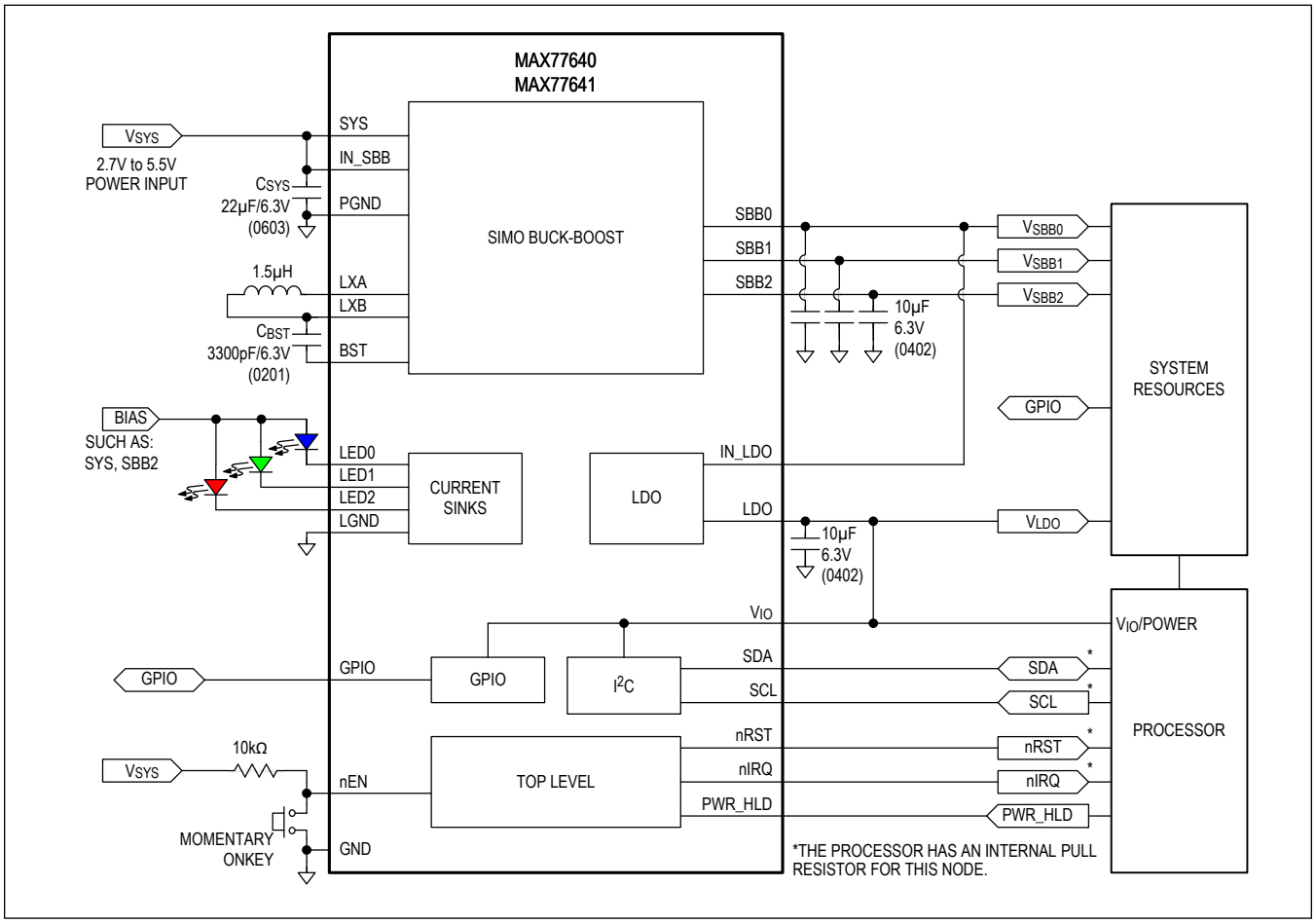


Figure 16. Slave Address Example

Typical Application Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	OPTIONS
MAX77640EWV+*	-40°C to +85°C	30 WLP	SBB0/SBB1/SBB2 upper values 2.375V/1.5875V/3.95V, samples with various OTP options
MAX77640AEWV+T	-40°C to +85°C	30 WLP	SBB0/SBB1/SBB2 upper values 2.375V/1.5875V/3.95V, production device, DIDM = 0b00, CID = 0b0000**
MAX77641EWV+*	-40°C to +85°C	30 WLP	SBB0/SBB1/SBB2 upper values 2.375V/5.25V/5.25V, samples with various OTP options
MAX77641AEWV+T	-40°C to +85°C	30 WLP	SBB0/SBB1/SBB2 upper values 2.375V/5.25V/5.25V, production device, DIDM = 0b01, CID = 0b0001**

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

**Custom samples only. Not for production or stock. Contact factory for more information.*

***See the Programmer's Guide for the options associated with a specified DIDM and CID.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/18	Initial release	—
1	6/18	Updated *Ordering Information* table	52
2	8/18	Updated bump pitch in *Benefits and Features* section	1

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