AVXX32E-B SERIES

DATA SHEET

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AVXX32E-B SERIES

21, 32, 43, 65 and 87 Seconds Complicate Pure Speech

Features

- Operating voltage: 2.4V~5.0V
- One single-key can implement play-all, play-next and random function. Maximum play count is 32.
- 4-column inputs and 3-row outputs can implement 4x4-matrix function.
- Each input can implement looping function.
- Single-key and 4-column inputs can be last-key priority for stand-alone input or first-key priority.
- Each input trigger can select trigger mode: (For OKY, TG0, TG1, TG2, TG3) Edge/Level, Hold/Unhold, Retrigger/Irretrigger.
- Each input trigger can select its own debounce time:
  Fast debounce: < 200us;
  Slow debounce: ~16ms (S.R.=6.0kHz)
- Support bouncing trigger solution for retrigger application. (Second trigger force to retrigger and slow debounce.)
- Maximum table entries are 460*8.
- Word count is only limited by ROM capacity.
- 4 output ports for Status or Led application:
  - OP_A Status:
    Busy_high ,DC_low, Stop_high,DC_high
    LED: +Fast,+Slow, Dyn(7/10), Off
  - OP_B Status:
    Busy_high, DC_low, Stop_high, DC_high
    LED: -Fast, -Slow, Dyn(9/10), On
  - OP_C Status: Busy_high, DC_low, Busy_low, DC_high
    LED: +Fast, +Slow, On, Off
  - OP_D Status0: Busy_high, DC_low
    Status1: Busy_low, DC_high
- Each output can specify its initial state (High or Low)
- Outputs can be set as constant current regardless of the supply voltage varied.
- Two PWM playing ports. Drive speaker or buzzer directly (For tone only).
- One DAC playing port, together with external bipolar to drive speaker. Ramp up/down is automatic.
- For DAC, AVXX32E-B series supports 8 levels of current control to offer flexible choises of corresponding BJT.
- Four-level volume control is provided for DAC or PWM output.
- Eight-pitch control is provided.
- Voice length: 21, 32, 43, 65 and 87 seconds. (ROM capacity : 131072*5, 196608*5, 262144*5, 393216*5 and 524288*5 bits)
- Voice algorithm: 5-bits LOG_PCM
- External resister or built-in resister for system frequency by bonding option on the same pad.
- Sixteen default sampling frequencies are supported. The default frequencies can be changed by an external applying resistor.
- Support single key play on/off. (For OKY, TG0, TG1)
- Programmable pull-high, pull-low or floating input. (For OKY, TG0, TG1)

General Description

The AVXX32E-B is a series of single-chip synthesizing CMOS VLSI which synthesizes voice by LOG_PCM algorithm. Table programming and shared multiple I/O pins make the applications flexible. Powerful functions and pure speech architecture make the AVXX32E-B series able to best fit most speech applications and a best cost/performance ratio as a result.

The programming of the AVXX32E-B series is first to define words. Each word contains voice data (or mute length), output method, pitch (if pitch control enabled), and volume (if volume control enabled). Assemble the words into sentences first, and then the programmer can assign the sentences to the keys corresponding to the user inputs.

The I/O pins of the AVXX32E-B series are multiplexed. This means the users have flexible I/O options for their applications in a minimum number of pin counts, that is, lower cost. The users can use maximum 4*4 matrix plus one single-key inputs, but less outputs; or 4 maximum outputs, but less inputs.

The AVXX32E-B series support DAC or PWM audio output, the users can select both if necessary.

The frequency stability in the AVXX32E-B series is outstanding. The frequency variation by voltage change is relatively small compared to the competitor. Furthermore, volume option offers users flexible selection for their applications. In addition, the AVXX32E-B series support current control for DAC output. Thus users can choose suitable current output for their BJT component.

The programming and the approval can be done in the EV chip of the AVXX32E-B series. It makes the programming and verification easy. Please contact APLUS sales for the EV chip if required.

Pin Description

Pin Name	I/O	Pad Assign	Description
VDD	Power		Positive power supply
TEST	In		Test enable pad, high-active, pull-low
OSC	In		With resister connected to VDD for system clock generating or connected to VSS using internal resister
OKY_RW3	In	OKY	Trigger input, active-high
	Out	ROW3	Row output for matrix function.
TG0,TG1	In		Column input or stand-alone input; active-high
TG2_OPD	In	TG2	Column input or stand-alone input; active-high
	Out	OP_D	Status output
TG3_OPC	In	TG3	Column input or stand-alone input; active-high
	Out	OP_C	Status output
RW1_OPB	Out	ROW1	Row output for matrix function
	Out	OP_B	Status output
RW2_OPA	Out	ROW2	Row output for matrix function
	Out	OP_A	Status output
PWM1	Out	PWM1	Voltage output to drive speaker or buzzer
	Out	OP_A OP_C	Status output
PWM2	Out	PWM2	Voltage output to drive speaker or buzzer
	Out	OP_B OP_D	Status output
DAC	Out	DAC	Current output for speaker application
	Out	OP_A OP_B OP_C OP_D	Status output
VSS	Power		Negative power supply

Absolute Maximum Rating

Symbol	Rating	Unit
V_{DD}~V_{SS}	-0.5 ~ +0.5	V
VIN (for input)	V_{SS}-0.3 < V_{IN} < V_{DD}+0.3	V
VOUT (for all outputs)	V_{SS} < V_{OUT} < V_{DD}	V
T (operating)	-10 ~ +60	℃
T (storage)	-55 ~ +125	℃

DC Characteristics

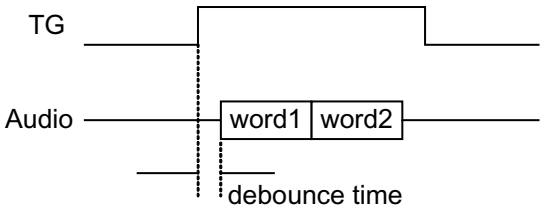
Symbol	Parameter		Min	Typ.	Max	Unit	Condition
VDD	Operating Voltage		2.4	3.0	5.0	V	
Isb	Supply Current	Standby	—	—	1	μA	V_{DD}=3.0V, I/O open
Iop		Operating	—	—	400	μA	V_{DD}=3.0V, No loading
Iih	Input Current		—	—	-20	μA	V_{DD}=3.0V, V_{IP}=0V
Iil			—	—	20	μA	V_{DD}=3.0V, V_{IP}=3.0V
Iol	Output Current		—	10	—	mA	V_{DD}=3.0V, V_{OP}=0.8V
Ioh			—	-5	—	mA	V_{DD}=3.0V, V_{OP}=2.5V
d F/F	Frequency Stability		—	—	±5	%	(f_{OSC} (4.5V)-f_{OSC}(4.0))/ f_{OSC} (4.5V)
d F/F	Frequency Variation by difference lot		—	—	±10	%	V_{DD}=4.5V f_{OSC} =384kHz

Function Diagram

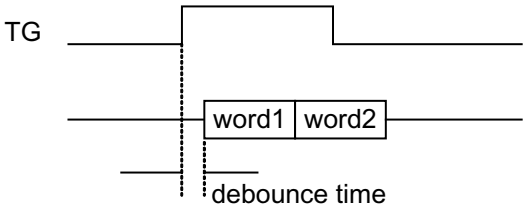
Edge/Level mode (If sentence = word1+word2)

- **Edge mode**

  Trigger length > Voice length

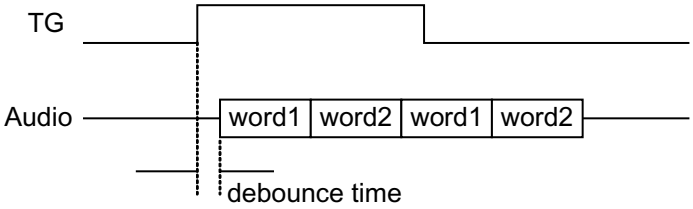


  Trigger length < Voice length

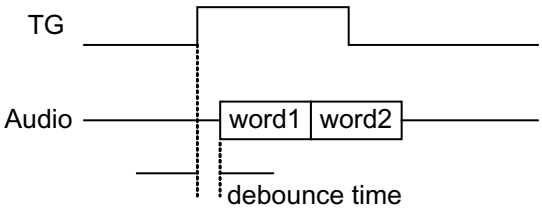


- **Level mode**

  Trigger length > Voice length (if sentence=word1+word2)

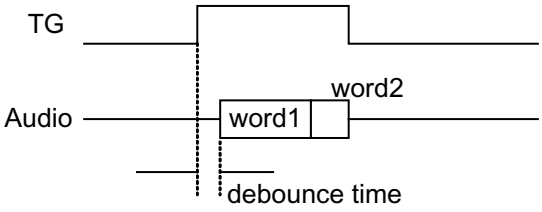


Trigger length < Voice length (if sentence = word1+word2)

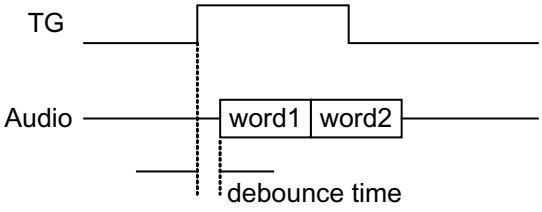


Hold/Unhold mode (If sentence = word1+word2)

- **Hold mode**

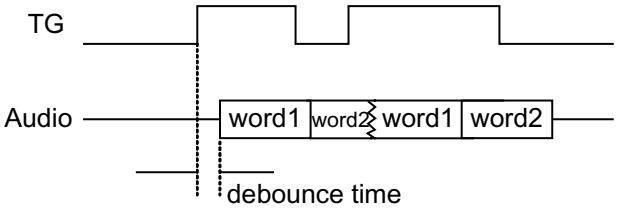


- **Unhold mode**

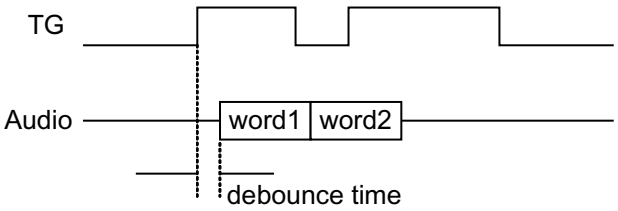


Retrigger/Irretrigger mode (If sentence = word1+word2)

- **Retrigger mode (Edge Unhold mode)**

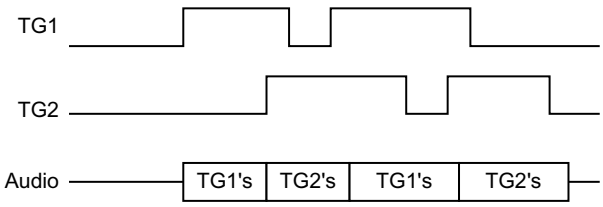


- **Irretrigger mode (Edge, Unhold mode)**



Last key priority

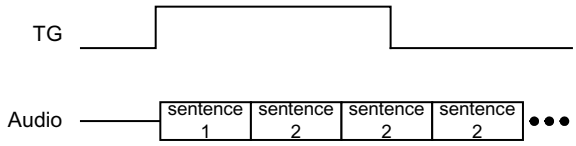
- **If TG1, TG2 are retrigger mode**



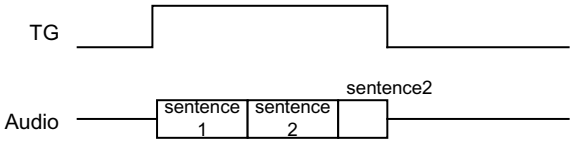
Looping function

If sentence is set to looping mode (sentence1_sentence2)

- **Unhold mode**

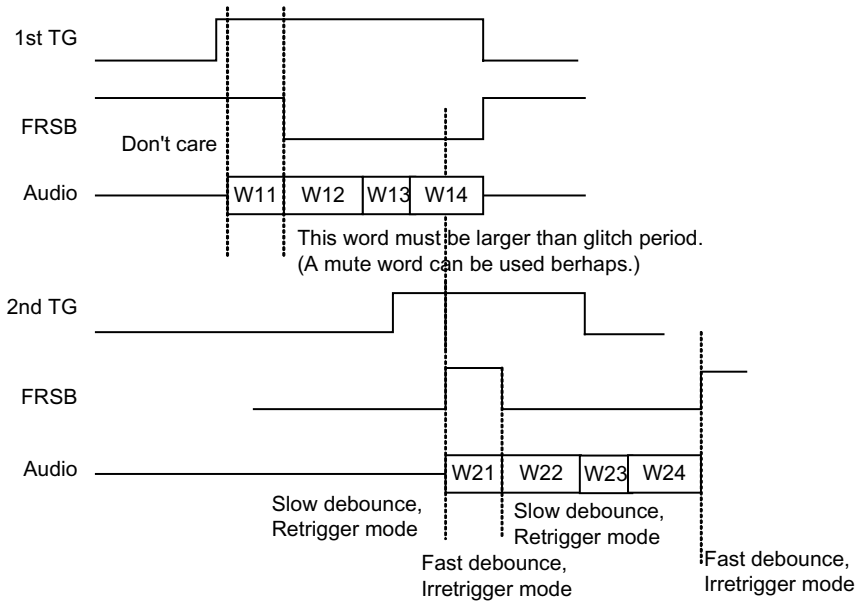


- **Hold mode**



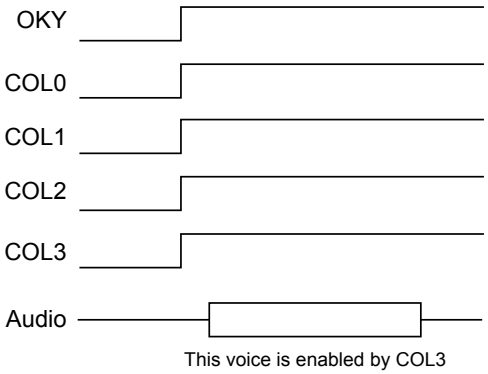
Force to retrigger and slow debounce option

(Trigger mode set to Fast debounce and Irretrigger mode)



Busy=0, FRSB set to high;
Busy=1, depending on FRSB setting.
If FRSB=0, force to slow debounce and retrigger mode;
If FRSB=1, no change (fast debounce and irretrigger mode).

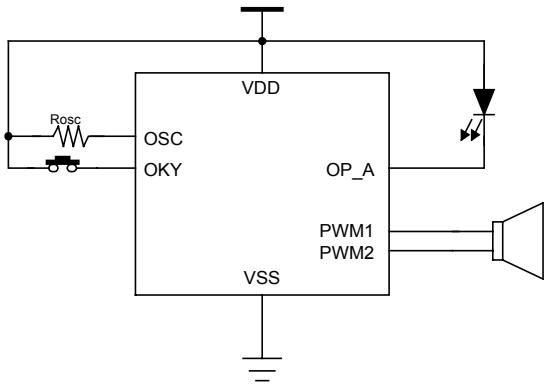
Stand-alone trigger inputs are enabled at the same time



Trigger input priority is COL3 > COL2 > COL1 > COL0 > OKY

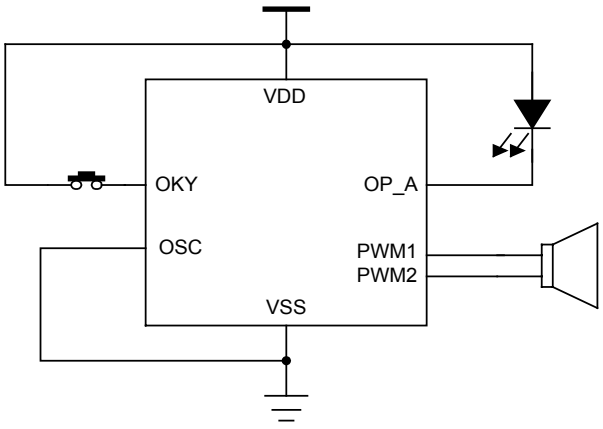
Application circuit

- **External resister, Driver speaker by PWM, driver LED**

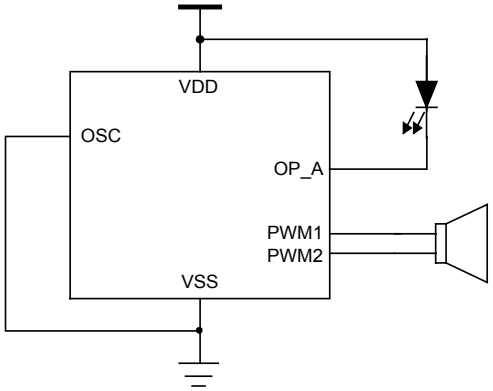


R_{OSC}=200kΩ for frequency option 8

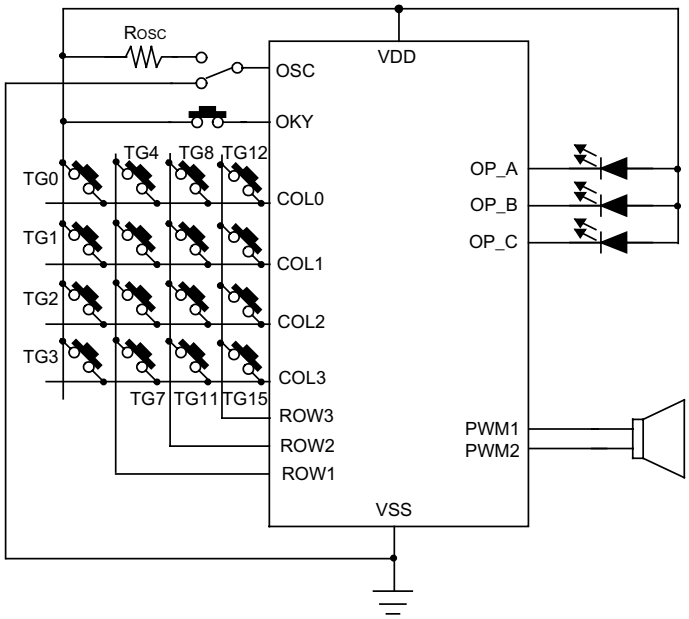
- **Internal resister, driver speaker by PWM, driver LED**
  If OSC bonds to VSS, this chip uses internal resister automatically.



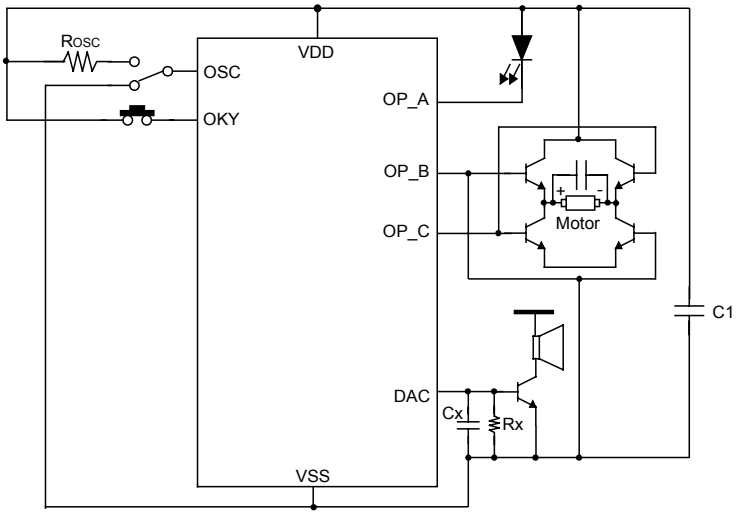
- **Power on play**
  Set the pull resisters of OKY, TG0 or TG1 to pull-high will cause the triggers to play immediately after power on.



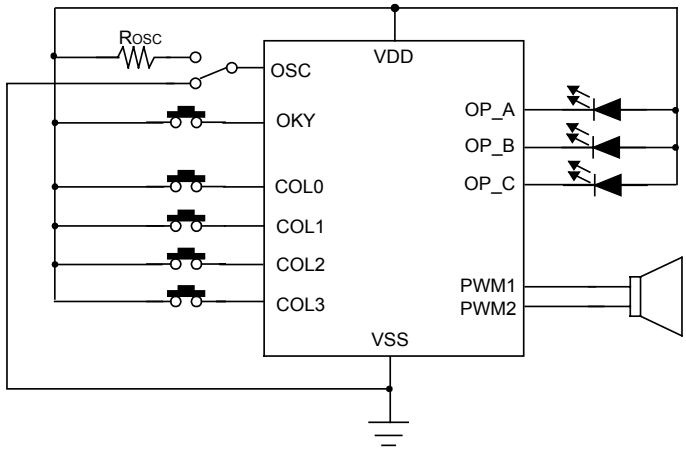
- **Matrix input**



- **Driver speaker by DAC and driver Motor application**



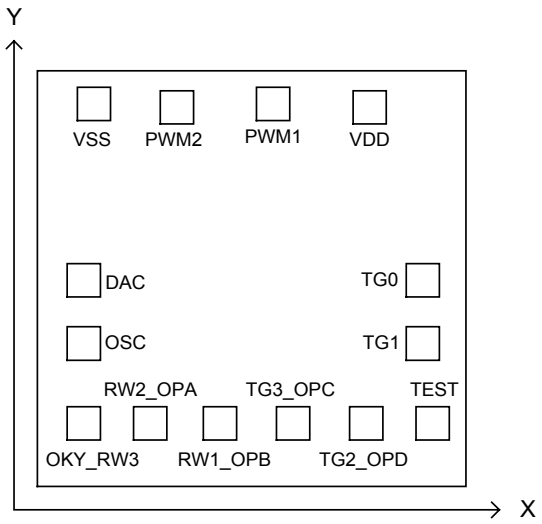
- **Stand-alone trigger input**



Output Definition

	Option	0	1	2	3
OPA	Status	BH	DL	SH	DH
	Standby state	L	L	L	H
	LED	+Fast	+Slow	Dy07	OFF
	Standby state	H	H	H	H
OPB	Status	BH	DL	SH	DH
	Standby state	L	L	L	H
	LED	-Fast	-Slow	Dy09	ON
	Standby state	H	H	H	H
OPC	Status	BH	DL	BL	DH
	Standby state	L	L	H	H
	LED	+Fast	+Slow	ON	OFF
	Standby state	H	H	H	H
OPD	Status1	BH	DL		
	Standby state	L	L		
	Satatus2	BH	DL		
	Standby state	H	H		

Bonding Diagram



Note: The IC substrate should be connect to VSS

(1) AV2132E

PIN Name	X(mm)	Y(mm)
OKY_RW3	250.75	94.00
RW2_OPA	451.50	94.25
RW1_OPB	660.25	94.25
TG3_OPC	861.00	94.25
TG2_OPD	1069.75	94.25
TEST	1270.25	94.25
OSC	94.00	271.25
TG1	1313.25	297.00
DAC	94.00	472.25
TG0	1313.25	501.00
VSS	410.75	1419.50
PWM2	631.00	1440.00
PWM1	1049.50	1440.00
VDD	1331.00	1440.00
DIE SIZE = 1510 * 1655 μm^2 (X*Y)		

(2) AV3232E

PIN Name	X(mm)	Y(mm)
OKY_RW3	250.75	94.00
RW2_OPA	451.50	94.25
RW1_OPB	660.25	94.25
TG3_OPC	861.00	94.25
TG2_OPD	1069.75	94.25
TEST	1270.25	94.25
OSC	94.00	271.25
TG1	1313.25	297.00
DAC	94.00	472.25
TG0	1313.25	501.00
VSS	410.75	1649.50
PWM2	631.00	1670.00
PWM1	1049.50	1670.00
VDD	1331.00	1670.00
DIE SIZE = 1510 * 1885 μm^2 (X*Y)		

(3) AV4332E

PIN Name	X(mm)	Y(mm)
OKY_RW3	250.75	94.00
RW2_OPA	451.50	94.25
RW1_OPB	660.25	94.25
TG3_OPC	861.00	94.25
TG2_OPD	1069.75	94.25
TEST	1270.25	94.25
OSC	94.00	271.25
TG1	1313.25	297.00
DAC	94.00	472.25
TG0	1313.25	501.00
VSS	410.75	1870.50
PWM2	631.00	1890.25
PWM1	1049.50	1890.25
VDD	1331.00	1890.25
DIE SIZE = 1510 * 2115 μm^2 (X*Y)		

(4) AV6532E

PIN Name	X(mm)	Y(mm)
OKY_RW3	259.25	94.00
RW2_OPA	460.00	94.25
RW1_OPB	668.75	94.25
TG3_OPC	869.50	94.25
TG2_OPD	1078.25	94.25
TEST	1278.75	94.25
OSC	102.50	271.25
TG1	1321.75	297.00
DAC	102.50	472.25
TG0	1321.75	501.00
VSS	419.25	2322.50
PWM2	639.50	2342.25
PWM1	1058.00	2342.25
VDD	1271.25	2364.25
DIE SIZE = 1427.25 * 2457.50 μm^2 (X*Y)		

(5) AV8732E

PIN Name	X(mm)	Y(mm)
OKY_RW3	266.00	94.00
RW2_OPA	466.75	94.25
RW1_OPB	675.50	94.25
TG3_OPC	876.25	94.25
TG2_OPD	1085.00	94.25
TEST	1285.50	94.25
OSC	109.25	271.25
TG1	1328.50	297.00
DAC	109.25	472.25
TG0	1328.50	501.00
VSS	426.00	2801.25
PWM2	646.25	2821.00
PWM1	1064.75	2821.00
VDD	1271.25	2815.00
DIE SIZE = 1427.25 * 2908.25 μm^2 (X*Y)		