DS90UB948-Q1 1080p FPD-Link III to OpenLDI Deserializer

1 Features

- Supports Pixel Clock Frequency up to 170 MHz for WUXGA (1920x1200) and 1080p60 Resolutions with 24-bit Color Depth
- 1-lane or 2-lane FPD-Link III Interface with De-skew Capability
- Single or Dual OpenLDI (LVDS) Transmitter
  - Single Channel: Up to 96 MHz Pixel Clock
  - Dual Channel: Up to 170 MHz Pixel Clock
  - Configurable 18-bit RGB or 24-bit RGB
- High Speed GPIO up to 2.0 Mbps
- Supports up to 15 meters of cable with automatic temperature and aging compensation
- SPI Control Interfaces up to 3.3 Mbps
- I^2C (Master/Slave) with 1 Mbps Fast-mode Plus
- Adaptive Receive Equalization
- Image Enhancement (White Balance and Dithering)
- Supports 7.1 Multiple I2S (4 data) Channels
- Backward Compatible to DS90UB925/925AQ-Q1 and DS90UB927Q-Q1 FPD-Link III Serializers
- Automotive Grade Product: AEC-Q100 Grade 2 Qualified

2 Applications

- Automotive Infotainment:
  - Central Information Displays
  - Rear Seat Entertainment Systems
  - Digital Instrument Clusters

3 Description

The DS90UB948-Q1 is a FPD-Link III Deserializer which, in conjunction with the DS90UB949/947/929-Q1 Serializers, converts 1-lane or 2-lane FPD-Link III streams into a FPD-Link (OpenLDI) interface. The Deserializer is capable of operating over cost-effective 50Ω single-ended coaxial or 100Ω differential shielded twisted-pair (STP) cables. It recovers the data from one or two FPD-Link III serial streams and translates it into dual pixel FPD-Link (8 LVDS data lanes + clock) supporting video resolutions up to WUXGA and 1080p60 with 24-bit color depth. This provides a bridge between HDMI enabled sources such as GPUs to connect to existing LVDS displays or Application Processors.

The FPD-Link III interface supports video and audio data transmission and full duplex control, including I^2C and SPI communication, over the same differential link. Consolidation of video data and control over two differential pairs reduces the interconnect size and weight and simplifies system design. EMI is minimized by the use of low voltage differential signaling, data scrambling, and randomization. In backward compatible mode, the device supports up to WXGA and 720p resolutions with 24-bit color depth over a single differential link.

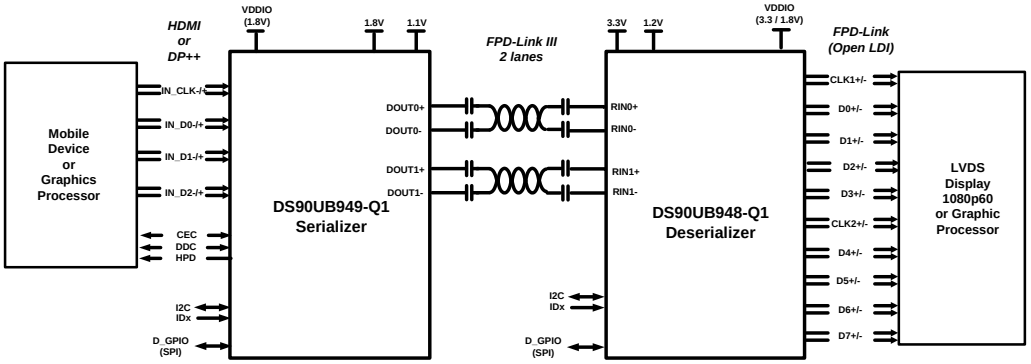
The device automatically detects the FPD-Link III channels and provides a clock alignment and de-skew functionality without the need for any special training patterns. This ensures skew phase tolerance from mismatches in interconnect wires such as PCB trace routing, cable pair-to-pair length differences, and connector imbalances.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS90UB948-Q1	WQFN NKD (64)	9.00 mm x 9.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Applications Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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5 Revision History

DATE	REVISION	NOTES
October 2014	*	Initial release.

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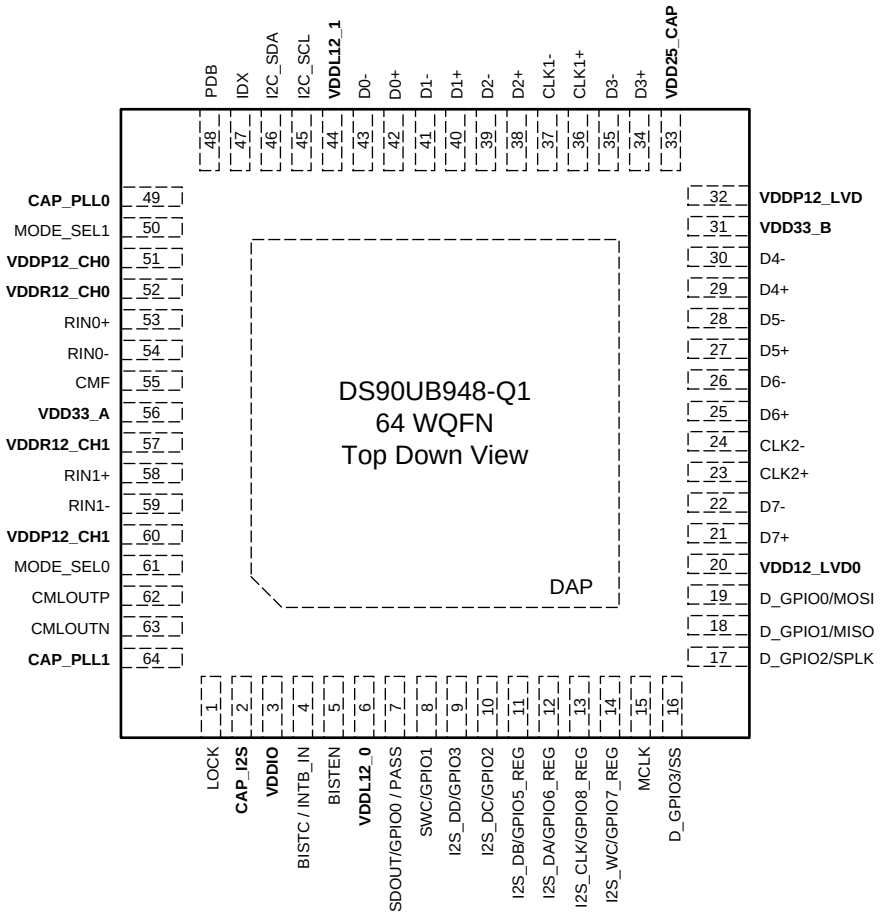
6 Pin Configurations and Functions



Pin Functions

PIN		I/O, TYPE	DESCRIPTION
NAME	NUMBER		
FPD-LINK OPENLDI OUTPUT PINS			
CLK1- CLK1+	37 36	O, LVDS	Clock Differential Output This pair requires an external 100Ω termination for LVDS
CLK2- CLK2+	24 23	O, LVDS	Clock Differential Output This pair requires an external 100Ω termination for LVDS
D0- D0+	43 42	O, LVDS	Channel 0 Differential Output This pair requires an external 100Ω termination for LVDS
D1- D1+	41 40	O, LVDS	Channel 1 Differential Output This pair requires an external 100Ω termination for LVDS
D2- D2+	39 38	O, LVDS	Channel 2 Differential Output This pair requires an external 100Ω termination for LVDS
D3- D3+	35 34	O, LVDS	Channel 3 Differential Output This pair requires an external 100Ω termination for LVDS
D4- D4+	30 29	O, LVDS	Channel 4 Differential Output This pair requires an external 100Ω termination for LVDS
D5- D5+	28 27	O, LVDS	Channel 5 Differential Output This pair requires an external 100Ω termination for LVDS
D6- D6+	26 25	O, LVDS	Channel 6 Differential Output This pair requires an external 100Ω termination for LVDS
D7- D7+	22 21	O, LVDS	Channel 7 Differential Output This pair requires an external 100Ω termination for LVDS

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Pin Functions (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NUMBER		
FPD-LINK III INTERFACE			
RIN0-	54	I/O, CML	FPD-Link III Inverting Input/Output The output must be AC-coupled with a 33nF capacitor.
RIN0+	53	I/O, CML	FPD-Link III True Input/Output The output must be AC-coupled with a 33nF capacitor.
RIN1-	59	I/O, CML	FPD-Link III Inverting Input/Output The output must be AC-coupled with a 33nF capacitor.
RIN1+	58	I/O, CML	FPD-Link III True Input/Output The output must be AC-coupled with a 33nF capacitor.
CMF	55	Analog	Common Mode Filter. Connect 0.1µF capacitor to GND
I2C PINS			
I2C_SDA	46	I/O, Open-Drain	I2C Data Input / Output Interface Open drain. Must have an external pull-up resistor to VDDIO **DO NOT FLOAT.** Recommended pull-up: 4.7kΩ.
I2C_SCL	45	I/O, Open-Drain	I2C Clock Input / Output Interface Open drain. Must have an external pull-up resistor to VDDIO **DO NOT FLOAT.** Recommended pull-up: 4.7kΩ.
IDX	47	I, Analog	Analog input. I2C Serial Control Bus Device ID Address.
SPI PINS			
MOSI	19	I/O, LVCMOS w/ pull-down	Master out, slave in. Pin is shared with D_GPIO0
MISO	18	I/O, LVCMOS w/ pull-down	Master in, slave out. Pin is shared with D_GPIO1
SPLK	17	I/O, LVCMOS w/ pull-down	Serial clock. Pin is shared with D_GPIO2
SS	16	I/O, LVCMOS w/ pull-down	Slave select. Pin is shared with D_GPIO3
CONTROL			
MODE_SEL0	61	I, Analog	Analog input. Mode Select 0. Connect to external pull-up to VDD33 and pull-down to GND to create a voltage divider. See Table 7
MODE_SEL1	50	I, Analog	Analog input. Mode Select 1. Connect to external pull-up to VDD33 and pull-down to GND to create a voltage divider. See Table 8
PDB	48	I, LVCMOS w/ pull-down	Power-Down Mode Input Pin PDB = 1, device is enabled (normal operation) PDB = 0, device is powered down. When the device is in the POWER DOWN state, the LVCMOS outputs are in TRI-STATE, the PLL is shutdown and IDD is minimized. **Note: PDB pin requires minimum ramp time of 200us**
BISTEN	5	I, LVCMOS w/ pull-down	Bist Enable Pin 0: BIST Mode is disabled. 1: BIST Mode is enabled.
BISTC	4	I, LVCMOS w/ pull-down	Bist Clock Select. Shared with INTB_IN. 0: PCLK; 1: 33MHz
INTB_IN	4	I, LVCMOS w/ pull-down	Interrupt input. Shared with BISTC.
BIDIRECTIONAL CONTROL CHANNEL (BCC) GPIO PINS			
GPIO0	7	I/O, LVCMOS	BCC GPIO0. Shared with SDOUT
GPIO1	8	I/O, LVCMOS	BCC GPIO1. Shared with SWC

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Pin Functions (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NUMBER		
GPIO2	10	I/O, LVCMOS	BCC GPIO2. Shared with I2S_DC
GPIO3	9	I/O, LVCMOS	BCC GPIO3. Shared with I2S_DD
HIGH-SPEED GPIO PINS			
D_GPIO0	19	I/O, LVCMOS	General Purpose I/O in 2-lane FPD-Link III mode
D_GPIO1	18	I/O, LVCMOS	General Purpose I/O in 2-lane FPD-Link III mode
D_GPIO2	17	I/O, LVCMOS	General Purpose I/O in 2-lane FPD-Link III mode
D_GPIO3	16	I/O, LVCMOS	General Purpose I/O in 2-lane FPD-Link III mode
REGISTER-ONLY GPIO PINS			
GPIO5_REG	11	I/O, LVCMOS	General Purpose Input/Output 5 Local register control only. Pin is shared with I2S_DB
GPIO6_REG	12	I/O, LVCMOS	General Purpose Input/Output 6 Local register control only. Pin is shared with I2S_DA
GPIO7_REG	14	I/O, LVCMOS	General Purpose Input/Output 7 Local register control only. Pin is shared with I2S_WC
GPIO8_REG	13	I/O, LVCMOS	General Purpose Input/Output 8 Local register control only. Pin is shared with I2S_CLK
SLAVE MODE LOCAL I2S CHANNEL PINS			
I2S_WC	14	O, LVCMOS	Slave Mode I2S Word Clock Output. Shared with GPIO7_REG
I2S_CLK	13	O, LVCMOS	Slave Mode I2S Clock Output. Shared with GPIO8_REG
I2S_DA	12	O, LVCMOS	Slave Mode I2S Data Output. Shared with GPIO6_REG
I2S_DB	11	O, LVCMOS	Slave Mode I2S Data Output. Shared with GPIO5_REG
I2S_DC	10	O, LVCMOS	Slave Mode I2S Data Output. Shared with GPIO2
I2S_DD	9	O, LVCMOS	Slave Mode I2S Data Output. Shared with GPIO3
MASTER MODE LOCAL I2S CHANNEL PINS			
SWC	8	O, LVCMOS	Master Mode I2S Word Clock Output. Shared with GPIO1
SDOUT	7	O, LVCMOS	Master Mode I2S Data Output. Shared with GPIO0
MCLK	15	O, LVCMOS	Master Mode I2S System Clock Output
STATUS PINS			
LOCK	1	O, LVCMOS	Lock Status Output LOCK = 1: PLL acquired lock to the reference clock input LOCK = 0: PLL is unlocked
PASS	7	O, LVCMOS	BIST mode status output pin (BISTEN = 1) PASS = 1: No error detected PASS = 0: Error detected

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Pin Functions (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NUMBER		
POWER & GROUND (1)			
VDD33_A, VDD33_B	56 31	Power	3.3V (±10%) supply. Power to on-chip regulator. Requires 10µF, 1µF, 0.1µF, and 0.01µF capacitors to GND
VDDIO	3	Power	LVCMOS I/O power supply, 1.8V (±5%) OR 3.3V (±10%). Requires 10µF, 1µF, 0.1µF, and 0.01µF capacitors to GND
VDD12_LVDS VDDP12_LVDS VDDL12_0 VDDL12_1 VDDP12_CH0 VDDR12_CH0 VDDP12_CH1 VDDR12_CH1	20 32 6 44 51 52 60 57	Power	1.2V (±5%) supplies. Requires 10µF, 1µF, 0.1µF, and 0.01µF capacitors to GND at each VDD pin.
CAP_PLL0 CAP_PLL1 CAP_I2S VDD25_CAP	49 64 2 33	CAP	Decoupling capacitor connection for on-chip regulator. Each requires a 0.1µF decoupling capacitor to GND.
VSS	DAP	G	DAP is the large metal contact at the bottom side, located at the center of the WQFN package. Connect to the ground plane (GND) with at least 32 vias.
OTHER PINS			
CMLOUTP CMLOUTN	62 63	O, CML	Monitor point for equalized differential signal.

(1) The V_{DD} (V_{DD12}, V_{DD33}, and V_{DDIO}) supply ramp should be faster than 1.5 ms with a monotonic rise.

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7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[(1) (2)]

PARAMETER		MIN	MAX	UNIT
V_{DD33}	Supply Voltage	–0.3	+4.0	V
V_{DD12}	Supply Voltage	-0.3	+1.8	V
V_{DDIO}	Supply Voltage	–0.3	+4.0	V
	LVCMOS I/O Voltage	–0.3	V_{DDIO} + 0.3	V
	FPD-Link III Input Voltage	–0.3	+2.75	V
T_J	Junction Temperature		+150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For soldering specifications, see product folder at www.ti.com and SNOA549

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range	64 Lead WQFN Package	-65	+150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[(1)]	-8	+8	kV
		Charged device model (CDM), per AEC Q100-011	-1.25	+1.25	
ESD Rating (IEC 61000-4-2) R_D = 330Ω, C_S = 150pF		Air Discharge (R_{IN0+}, R_{IN0-}, R_{IN1+}, R_{IN1-})	-15	+15	kV
		Contact Discharge (R_{IN0+}, R_{IN0-}, R_{IN1+}, R_{IN1-})	-8	+8	
ESD Rating (ISO10605) R_D = 330Ω, C_S = 150pF R_D = 2KΩ, C_S = 150pF or 330pF		Air Discharge (R_{IN0+}, R_{IN0-}, R_{IN1+}, R_{IN1-})	-15	+15	kV
		Contact Discharge (R_{IN0+}, R_{IN0-}, R_{IN1+}, R_{IN1-})	-8	+8	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

	MIN	TYP	MAX	UNIT
Supply Voltage (V_{DD33})	3.0	3.3	3.6	V
Supply Voltage (V_{DD18})	1.71	1.8	1.89	V
Supply Voltage (V_{DD12})	1.14	1.2	1.26	V
Operating Free Air Temperature (T_A)	−40	+25	+105	°C
OpenLDI Clock Frequency (Single Link)	25		96	MHz
OpenLDI Clock Frequency (Dual Link)	50		170	MHz
Supply Noise -- V_{DD33} (DC-50MHz)			100	mV_{P-P}
Supply Noise -- V_{DD18} (DC-50MHz)			50	mV_{P-P}
Supply Noise -- V_{DD12} (DC-50MHz)			25	mV_{P-P}

7.4 Thermal Information

THERMAL METRIC[(1)]		WQFN 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	24.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	6.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	3.6	
ψ_{JT}	Junction-to-top characterization parameter	0.1	
ψ_{JB}	Junction-to-board characterization parameter	3.6	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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7.5 DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
3.3V LVCMOS I/O (V_{DDIO} = 3.3V ± 10%)							
V_{IH}	High Level Input Voltage		PDB, BISTEN, BISTC, GPIO[3:0], D_GPIO[3:0], I2S_DA, I2S_DB, I2S_DC, I2S_DD, I2S_CLK, I2S_WC, LOCK, PASS	2.0		V_{DDIO}	V
V_{IL}	Low Level Input Voltage			0		0.8	V
I_{IN}	Input Current	V_{IN} = 0V or V_{DDIO}		-10		10	µA
V_{OH}	High Level Output Voltage	I_{OH} = -4mA		2.4		V_{DDIO}	V
V_{OL}	Low Level Output Voltage	I_{OL} = +4mA		0		0.4	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V			-55		mA
I_{OZ}	Tri-state Output Current	PDB = 0V V_{OUT} = 0V or V_{DDIO}		-20		20	µA
C_{IN}	Input Capacitance					10	pF
1.8V LVCMOS I/O (V_{DDIO} = 1.8V ± 5%)							
V_{IH}	High Level Input Voltage		PDB, BISTEN, BISTC, GPIO[3:0], D_GPIO[3:0], I2S_DA, I2S_DB, I2S_DC, I2S_DD, I2S_CLK, I2S_WC, LOCK, PASS	0.65 * V_{DDIO}		V_{DDIO}	V
V_{IL}	Low Level Input Voltage			0		0.35 * V_{DDIO}	V
I_{IN}	Input Current	V_{IN} = 0V or V_{DDIO}		-10		10	µA
V_{OH}	High Level Output Voltage	I_{OH} = -4mA		V_{DDIO}-0.45		V_{DDIO}	V
V_{OL}	Low Level Output Voltage	I_{OL} = +4mA		0		0.45	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V			-35		mA
I_{OZ}	Tri-state Output Current	PDB = 0V V_{OUT} = 0V or V_{DDIO}		-20		20	µA
C_{IN}	Input Capacitance					10	pF
SERIAL CONTROL BUS (V_{DDIO} = 1.8V ± 5% OR 3.3V ± 10%)							
V_{IH}	Input High Level		I2C_SDA, I2C_SCL	0.7 * V_{DDIO}		V_{DD33}	V
V_{IL}	Input Low Level			GND		0.3 * V_{DDIO}	V
V_{HY}	Input Hysteresis				>50		mV
V_{OL}	Output Low Level	I_{OL} = +4mA		0		0.4	V
I_{IN}	Input Current	V_{IN} = 0V or V_{DDIO}		-10		+10	µA
FPD-LINK III CML INPUT							
V_{TH}	Differential Threshold High Voltage	V_{CM} = 2.1V (Internal V_{BIAS})	RIN0+, RIN0- RIN1+, RIN1-			+50	mV
V_{TL}	Differential Threshold Low Voltage			-50			mV
V_{ID}	Input Differential Threshold			100			mV
V_{CM}	Differential Common-mode Voltage				2.1		V
R_T	Internal Termination Resistor - Differential			80	100	120	Ω

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DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
LVDS DRIVER							
V_{OD}	Output voltage swing (differential)	R_L = 100Ω. VOD Setting 1. See Figure 10. See Table 10 Register 0x4B for configuration details.	D0±, D1±, D2±, D3±, D4±, D5±, D6±, D7±, CLK1±, CLK2±	220	380	540	mV_{P-P}
		R_L = 100Ω. VOD Setting 2. See Figure 10. See Table 10 Register 0x4B for configuration details.		370	550	730	mV_{P-P}
		R_L = 100Ω. VOD Setting 3. See Figure 10. See Table 10 Register 0x4B for configuration details.		460	650	840	mV_{P-P}
		R_L = 100Ω. VOD Setting 4. See Figure 10. See Table 10 Register 0x4B for configuration details.		530	750	970	mV_{P-P}
ΔV_{OD}	Change in V_{OD} between complimentary Output States	R_L = 100Ω			1	50	mV
V_{OS}	Offset Voltage	R_L = 100Ω. See Figure 10.		1.0	1.2	1.5	V
ΔV_{OS}	Change in V_{OS} between complimentary Output States	R_L = 100Ω			1	50	mV
I_{OS}	Output Short Circuit Current				-20		mA
I_{OZ}	Output Tri-state LVDS Driver Current	PDB = 0V		-500		+500	µA
LOOP-THROUGH MONITOR OUTPUT							
V_{ODp-p}	Differential Output Voltage	R_L = 100Ω	CMLOUTP, CMLOUTN		360		mV
SUPPLY CURRENT							
P_T	Total Power Consumption, Normal Operation	Checkerboard Pattern, 170MHz. See Figure 1. 2-lane FPD-Link III Input, Dual Link OLDI Output	V_{DD}		858	1146	mW
P_Z	Total Power Consumption, Power-Down Mode	PDB = 0V			40	70	mW
I_{DD12}	Supply Current, Normal Operation	Checkerboard Pattern, 170MHz. See Figure 1. 2-lane FPD-Link III Input, Dual Link OLDI Output	V_{DD12} = 1.2V			223	mA
I_{DD33}			V_{DD33} = 3.6V			222	mA
I_{DDIO}			V_{DDIO} = 1.89V			19	mA
			V_{DDIO} = 3.6V			19	mA
I_{DD12}	Supply Current, Normal Operation	Random Pattern (PRBS7) 2-lane FPD-Link III Input, Dual Link OLDI Output	V_{DD12} = 1.2V		169		mA
I_{DD33}			V_{DD33} = 3.6V		168		mA
I_{DDIO}			V_{DDIO} = 1.89V		14		mA
			V_{DDIO} = 3.6V		14		mA
I_{DD12Z}	Supply Current, Power Down Mode	PDB = 0V	V_{DD12} = 1.2V		2	8	mA
I_{DD33Z}			V_{DD33} = 3.6V		2	8	mA
I_{DDIOZ}			V_{DDIO} = 1.89V		0.1	1	mA
			V_{DDIO} = 3.6V		0.1	1	mA

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7.6 AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
GPIO BIT RATE							
$R_{b,FC}$	Forward Channel Bit Rate	Single OLDI Output. OLDI Clock = 25 - 96MHz	GPIO[3:0]		0.25 * OLDI Clock		Mbps
		Dual OLDI Output. OLDI Clock = 25 - 85MHz			0.25 * OLDI Clock		Mbps
$R_{b,BC}$	Back Channel Bit Rate				133		kbps
$R_{b,BC}$	Back Channel Bit Rate	High Speed (2-lane Mode), 1 D_GPIO active. See Table 3.	D_GPIO[3:0]		2.0		Mbps
		High Speed (2-lane Mode), 2 D_GPIO's active. See Table 3.			1.33		Mbps
		High Speed (2-lane Mode), 4 D_GPIO's active. See Table 3.			800		kbps
		Normal mode. See Table 3.			133		kbps
$t_{GPIO,FC}$	GPIO Pulse Width, Forward Channel		GPIO[3:0]	>2 / OLDI Clock			s
$t_{GPIO,BC}$	GPIO Pulse Width, Back Channel		GPIO[3:0]	20			µs
RESET							
t_{LRST}	PDB Reset Low Pulse		PDB	2			ms
LOOP-THROUGH MONITOR OUTPUT							
E_W	Differential Output Eye Opening Width	RL = 100Ω, Jitter frequency >OLDI Clock / 40 See Figure 2.	CMLOUTP, CMLOUTN		0.4		UI
E_H	Differential Output Eye Height				>300		mV
FPD-LINK III CML INPUT							
t_{DDLT}	Lock Time	See Figure 6.	RIN0+, RIN0-, RIN1+, RIN1-		5	10 (1)	ms
I2S TRANSMITTER							
$t_{J,I2S}$	Clock Output Jitter		I2S_CLK		2		ns
t_{I2S}	I2S Clock Period (2)	See Figure 14.			>2 / OLDI Clock or >77		ns
$t_{HC,I2S}$	I2S Clock High Time (2)	See Figure 14.			0.48		t_{I2S}
$t_{LC,I2S}$	I2S Clock Low Time (2)	See Figure 14.			0.48		t_{I2S}
$t_{SR,I2S}$	I2S Set-up Time	See Figure 14.	I2S_DA, I2S_DB, I2S_DC, I2S_DD		0.4		t_{I2S}
$t_{HR,I2S}$	I2S Hold Time	See Figure 14.			0.4		t_{I2S}

(1) This parameter is specified by characterization and is not tested in production.
(2) I2S specifications for $t_{LC,I2S}$ and $t_{HC,I2S}$ pulses must each be greater than 1 OLDI clock period to ensure sampling and supersedes the $0.35*t_{I2S}$ requirement. $t_{LC,I2S}$ and $t_{HC,I2S}$ must be longer than the greater of either $0.35*t_{I2S}$ or 2 * OLDI Clock .

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7.7 Recommended Timing for the Serial Control Bus

Over I^2C supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	SCL Clock Frequency	Standard Mode	>0		100	kHz
		Fast Mode	>0		400	kHz
		Fast Plus Mode	>0		1	MHz
t_{LOW}	SCL Low Period	Standard Mode	4.7			µs
		Fast Mode	1.3			µs
		Fast Plus Mode	0.5			µs
t_{HIGH}	SCL High Period	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
		Fast Plus Mode	0.26			µs
$t_{HD;STA}$	Hold time for a start or a repeated start condition Figure 13	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
		Fast Plus Mode	0.26			µs
$t_{SU;STA}$	Set Up time for a start or a repeated start condition Figure 13	Standard Mode	4.7			µs
		Fast Mode	0.6			µs
		Fast Plus Mode	0.26			µs
$t_{HD;DAT}$	Data Hold Time Figure 13	Standard Mode	0			µs
		Fast Mode	0			µs
		Fast Plus Mode	0			µs
$t_{SU;DAT}$	Data Set Up Time Figure 13	Standard Mode	250			ns
		Fast Mode	100			ns
		Fast Plus Mode	50			ns
$t_{SU;STO}$	Set Up Time for STOP Condition Figure 13	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
		Fast Plus Mode	0.26			µs
t_{BUF}	Bus Free Time Between STOP and START Figure 13	Standard Mode	4.7			µs
		Fast Mode	1.3			µs
		Fast Plus Mode	0.5			µs
t_r	SCL & SDA Rise Time, Figure 13	Standard Mode			1000 (1)	ns
		Fast Mode			300 (1)	ns
		Fast Plus Mode			120 (1)	ns
t_f	SCL & SDA Fall Time, Figure 13	Standard Mode			300 (1)	ns
		Fast mode			300 (1)	ns
		Fast Plus Mode			120 (1)	ns
C_b	Capacitive Load for Each Bus Line	Standard Mode			400	pF
		Fast Mode			400	pF
		Fast Plus Mode			550	pF
t_{SP}	Input Filter	Fast Mode			50	ns
		Fast Plus Mode			20	ns

(1) Parameter is specified by bench characterization and is not tested in production.

7.8 Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
LVDS DRIVER SWITCHING CHARACTERISTICS							
t_{LVLHT}	LVDS Low-to-High Transition Time	20% to 80% transition. 5pF load. See Figure 9.	D0±, D1±, D2±, D3±, D4±, D5±, D6±, D7±, CLK1±, CLK2±		0.15	0.25 (1)	ns
t_{LVHLT}	LVDS High-to-Low Transition Time	80% to 20% transition. 5pF load. See Figure 9.			0.15	0.25 (1)	ns
t_{BIT}	Transmitter Output Bit Width	T = 1 / OLDI Clock frequency. See Figure 11.			1/7 * T		ns
t_{PPOS0}	Transmitter Output Pulse Positions Normalized for Bit 0				1		UI (2)
t_{PPOS1}	Transmitter Output Pulse Positions Normalized for Bit 1				2		UI (2)
t_{PPOS2}	Transmitter Output Pulse Positions Normalized for Bit 2				3		UI (2)
t_{PPOS3}	Transmitter Output Pulse Positions Normalized for Bit 3				4		UI (2)
t_{PPOS4}	Transmitter Output Pulse Positions Normalized for Bit 4				5		UI (2)
t_{PPOS5}	Transmitter Output Pulse Positions Normalized for Bit 5				6		UI (2)
t_{PPOS6}	Transmitter Output Pulse Positions Normalized for Bit 6				7		UI (2)
t_{PPOS}	Transmitter Output Pulse Positions (Bit 6 - Bit 0) Normalized				<0.1		UI (2)
t_{CCS}	Channel-to-Channel Skew				100		ps
t_{JCC}	Transmitter Jitter Cycle-to-Cycle	2-lane FPD-Link III Input, Dual OpenLDI Output			0.16		UI (2)
		2-lane FPD-Link III Input, Single OpenLDI Output			0.18		UI (2)
		1-lane FPD-Link III Input, Dual OpenLDI Output			0.04		UI (2)
		1-lane FPD-Link III Input, Single OpenLDI Output			0.04		UI (2)
t_{PDD}	Transmitter Power Down Delay	See Figure 5.			100		ns
t_{DD}	Deserializer Propagation Delay	T = 1 / OLDI Clock frequency. See Figure 4.			147 * T		ns

(1) Parameter is specified by bench characterization and is not tested in production.
(2) UI - Unit Interval is equal to 1 / (7 * OLDI Clock).

7.9 AC Timing Diagrams and Test Circuits

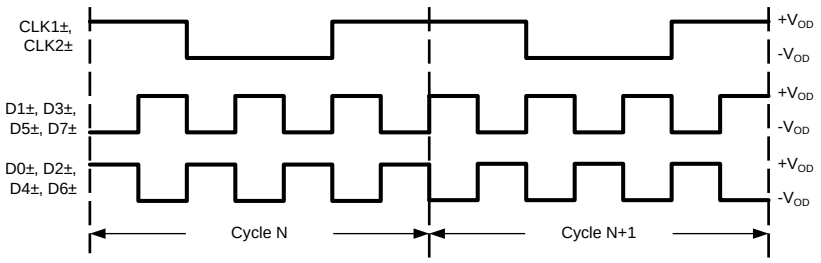

Figure 1. Checkerboard Data Pattern

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AC Timing Diagrams and Test Circuits (continued)

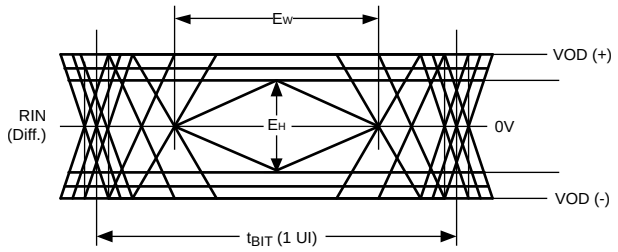

Figure 2. CML Output Driver

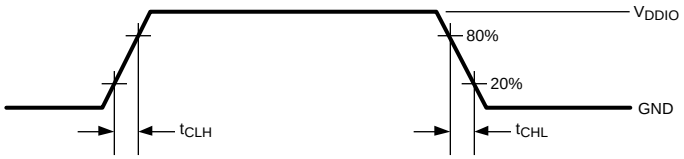

Figure 3. LVCMOS Transition Times

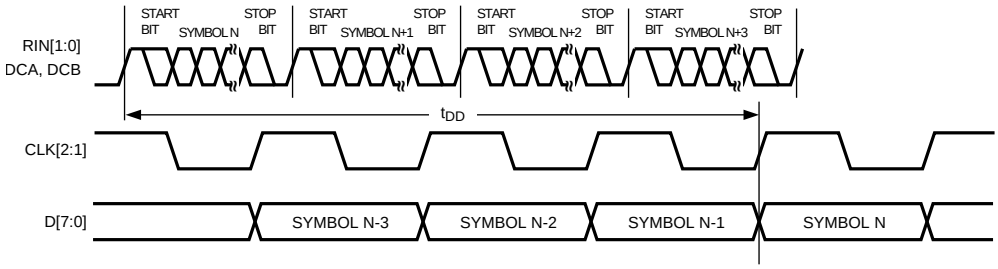

Figure 4. Latency Delay

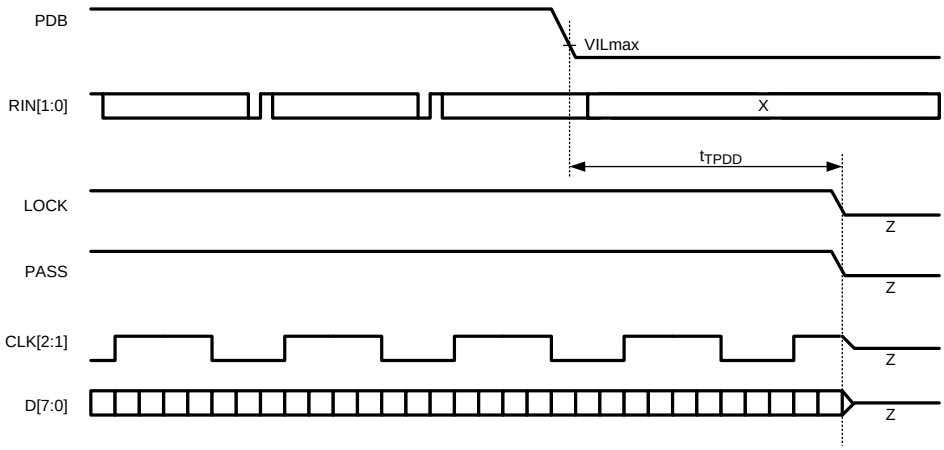

Figure 5. FPD-Link & LVCMOS Power Down Delay

AC Timing Diagrams and Test Circuits (continued)

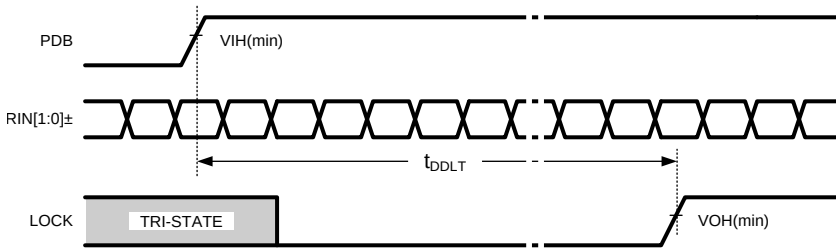

Figure 6. CML PLL Lock Time

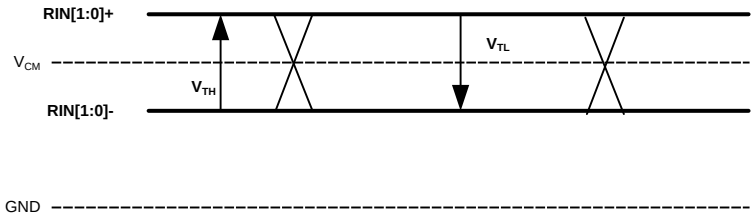

Figure 7. FPD-Link III Receiver DC V_{TH}/V_{TL} Definition

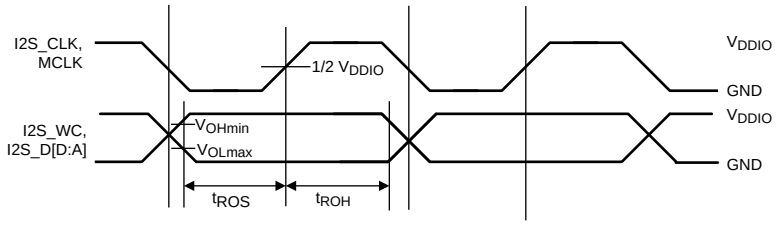

Figure 8. Output Data Valid (Setup and Hold) Times

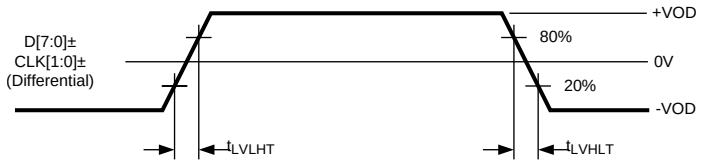

Figure 9. Input Transition Times

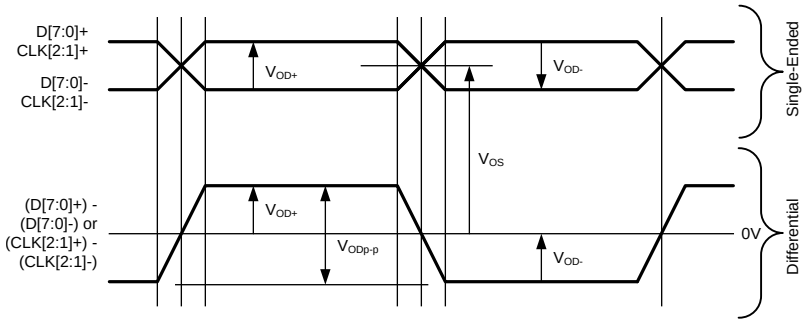

Figure 10. FPD-Link Single-Ended and Differential Waveforms

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AC Timing Diagrams and Test Circuits (continued)

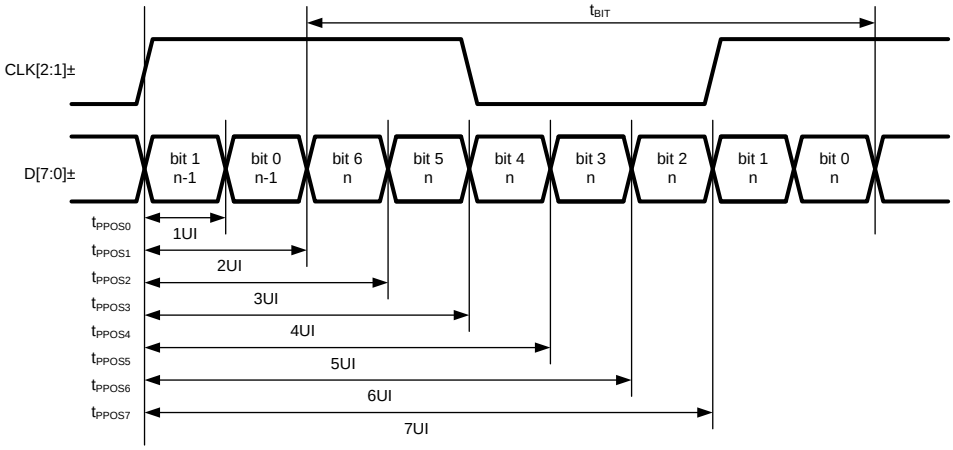

Figure 11. FPD-Link Transmitter Pulse Positions

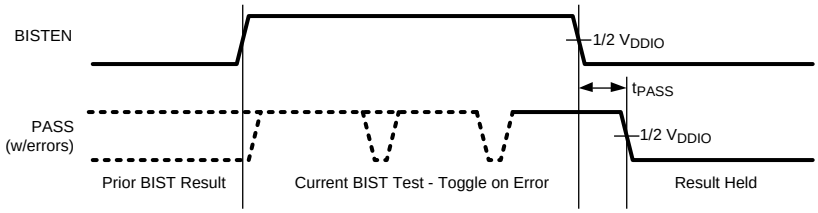

Figure 12. BIST PASS Waveform

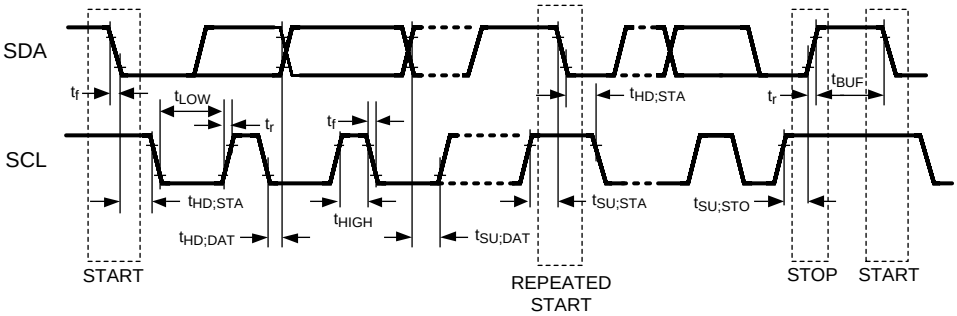

Figure 13. Serial Control Bus Timing Diagram

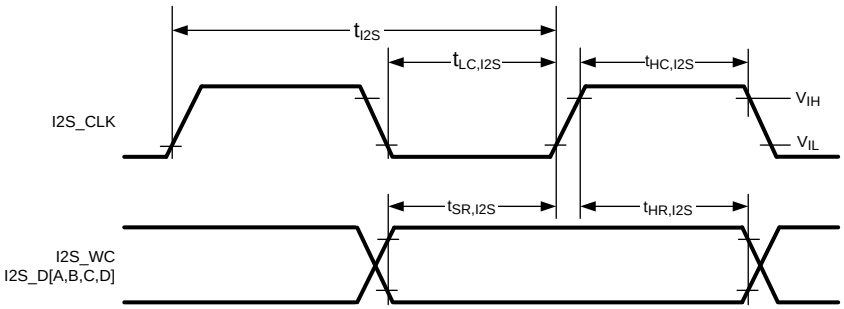

Figure 14. I2S Timing

7.10 Typical Characteristics

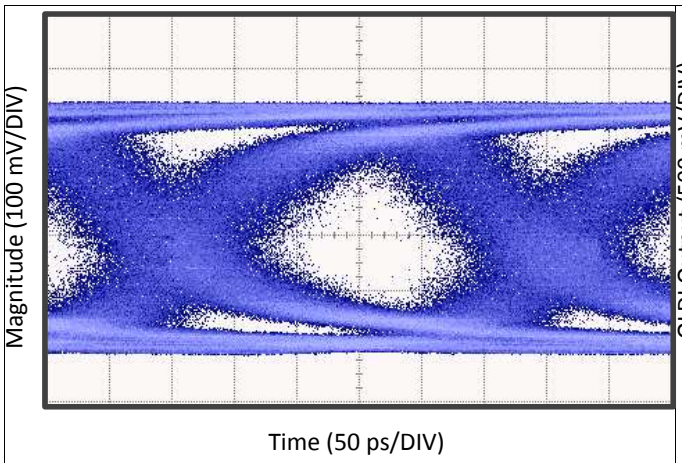

Figure 15. Deserializer Eye Diagram with 3.36 Gbps FPD-Link III Rate

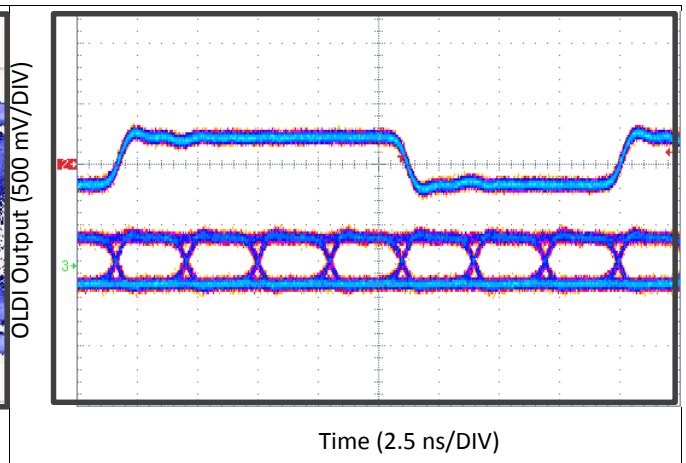

Figure 16. OpenLDI Output with 96 MHz Clock

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8 Detailed Description

8.1 Overview

The DS90UB948-Q1 receives a 35-bit symbol over single or dual serial FPD-Link III pairs operating at up to 3.36 Gbps line rate in 1-lane FPD-Link III mode and 2.975 Gbps per lane in 2-lane FPD-Link III mode. The DS90UB948-Q1 converts this stream into a single or dual FPD-Link Interface (4 LVDS data channels + 1 LVDS clock, or 8 LVDS data channels + 2 LVDS clocks). The FPD-Link III serial stream contains an embedded clock, video control signals, and the DC-balanced video data and audio data which enhance signal quality to support AC coupling.

The DS90UB948-Q1 is intended for use with the DS90UB949-Q1 or DS90UB947-Q1 Serializers, but is also backward compatible to the DS90UB925Q-Q1, DS90UB925AQ-Q1, and DS90UB927Q-Q1 FPD-Link III Serializers.

8.2 Functional Block Diagram

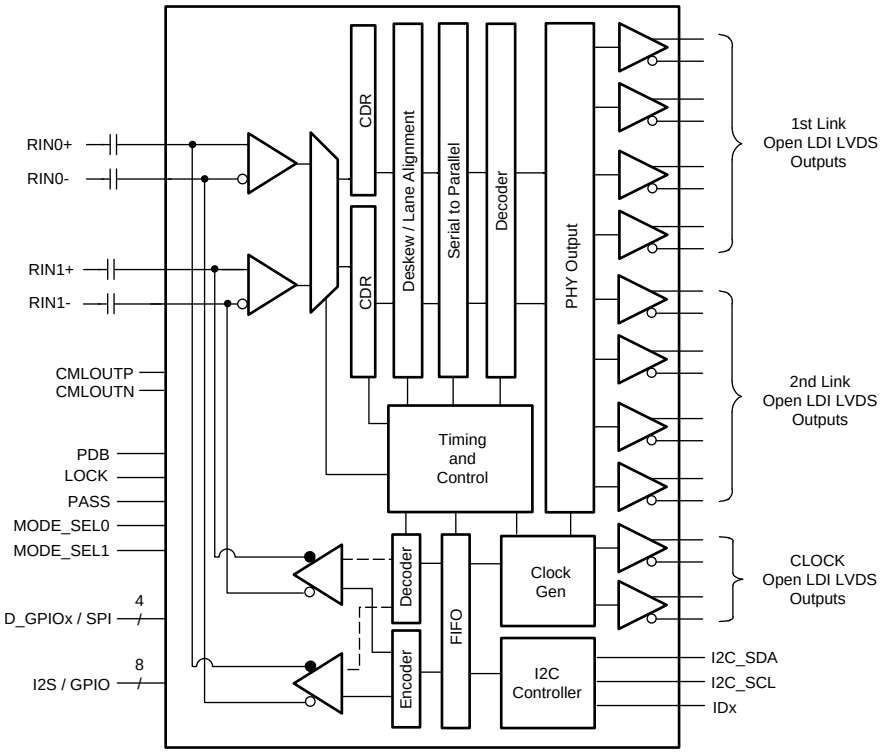

Figure 17. DS90UB948-Q1 Block Diagram

8.3 Feature Description

8.3.1 High Speed Forward Channel Data Transfer

The High Speed Forward Channel is composed of 35 bits of data containing RGB data, sync signals, I2C, GPIOs, and I2S audio transmitted from serializer to deserializer. Figure 18 illustrates the serial stream per clock cycle. This data payload is optimized for signal transmission over an AC coupled link. Data is randomized, balanced and scrambled.

Figure 18. FPD-Link III Serial Stream

Feature Description (continued)

The DS90UB948-Q1 supports clocks in the range of 25 MHz to 96 MHz over a 1-lane, or 50MHz to 170MHz over 2-lanes. The FPD-Link III serial stream rate is 3.36 Gbps maximum (875 Mbps minimum) or 2.975 Gbps maximum per lane (875 Mbps minimum) respectively.

8.3.2 Low Speed Back Channel Data Transfer

The Low-Speed Backward Channel provides bidirectional communication between the display and host processor. The information is carried from the deserializer to the serializer as serial frames. The back channel control data is transferred over both serial links along with the high-speed forward data, DC balance coding and embedded clock information. This architecture provides a backward path across the serial link together with a high speed forward channel. The back channel contains the I2C, CRC and 4 bits of standard GPIO information with 5 or 20 Mbps line rate (configured by MODE_SEL1).

8.3.3 Oscillator Output

The deserializer provides an optional CLK[2:1]± output when the input clock (serial stream) has been lost. This is based on an internal oscillator and may be controlled from register 0x02, bit 5 (OSC Clock Output Enable). See Table 10.

8.3.4 Clock and Output Status

When PDB is driven HIGH, the CDR PLL begins locking to the serial input and LOCK is tri-state or LOW (depending on the value of the OUTPUT ENABLE setting). After the deserializer completes its lock sequence to the input serial data, the LOCK output is driven HIGH, indicating valid data and clock recovered from the serial input is available on the LVCMOS and LVDS outputs. The State of the outputs is based on the OUTPUT ENABLE and OUTPUT SLEEP STATE SELECT register settings. See register 0x02 in Table 10.

Table 1. Output State Table

Inputs				Outputs			
Serial Input	**PDB**	**OUTPUT ENABLE Reg 0x02 [7]**	**OUTPUT SLEEP STATE SELECT Reg 0x02 [4]**	**LOCK**	**PASS**	**Data GPIO / D_GPIO I2S**	**D[7:0] / CLK[2:1]**
X	L	X	X	Z	Z	Z	Z
X	H	L	L	L or H	L	L	L
X	H	L	H	L or H	Z	Z	Z
Static	H	H	L	L	L	L	L/OSC (Register EN)
Static	H	H	H	L	Previous Status	L	L
Active	H	H	L	L	L	L	L
Active	H	H	H	H	Valid	Valid	Valid

8.3.5 LVCMOS VDDIO Option

The 1.8V or 3.3V Inputs and Outputs are powered from a separate V_{DDIO} supply to offer compatibility with external system interface signals.

NOTE

When configuring the V_{DDIO} power supplies, all the single-ended data and control input pins for device need to scale together with the same operating V_{DDIO} levels.

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8.3.6 Power Down (PDB)

The deserializer has a PDB input pin to ENABLE or POWER DOWN the device. This pin can be controlled by the host or through the V_{DDIO}, where V_{DDIO} = 3.0V to 3.6V or V_{DD33}. To save power, disable the link when the display is not needed (PDB = LOW). When the pin is driven by the host, make sure to release it after V_{DD33} and V_{DDIO} have reached final levels; no external components are required. In the case of driven by the V_{DDIO} = 3.0V to 3.6V or V_{DD33} directly, a 10kΩ resistor to the V_{DDIO} = 3.0V to 3.6V or V_{DD33}, and a >10 µF capacitor to the GND are required (see Figure 44 Typical Connection Diagram).

8.3.7 Interrupt Pin — Functional Description and Usage (INTB_IN)

The INTB_IN pin is an active low interrupt input pin. This interrupt signal, when configured, will propagate to the paired serializer. Consult the appropriate Serializer datasheet for details of how to configure this interrupt functionality.

1. On the Serializer, set register 0xC6[5] = 1 and 0xC6[0] = 1
2. Deserializer INTB_IN (pin 4) is set *LOW* by some downstream device.
3. Serializer pulls INTB pin *LOW*. The signal is active *LOW*, so a *LOW* indicates an interrupt condition.
4. External controller detects INTB = LOW; to determine interrupt source, read ISR register.
5. A read to ISR will clear the interrupt at the Serializer, releasing INTB.
6. The external controller typically must then access the remote device to determine downstream interrupt source and clear the interrupt driving the Deserializer INTB_IN. This would be when the downstream device releases the INTB_IN (pin 4) on the Deserializer. The system is now ready to return to step (2) at next falling edge of INTB_IN.

8.3.8 General-purpose I/O

8.3.8.1 GPIO[3:0] and D_GPIO[3:0] Configuration

In normal operation, GPIO[3:0] may be used as general purpose IOs in either forward channel (outputs) or back channel (inputs) mode. GPIO and D_GPIO modes may be configured from the registers (Table 9). The same registers configure either GPIO or D_GPIO, depending on the status of PORT1_SEL and PORT0_SEL bits (0x34[1:0]). D_GPIO operation requires 2-lane FPD-Link III mode. Consult the appropriate Serializer datasheet for details on D_GPIO configuration. Note: if paired with a DS90UH925Q-Q1 or DS90UB925Q-Q1 serializer, the devices must be configured into 18-bit mode to allow usage of GPIO pins on the serializer. To enable 18-bit mode, set serializer register 0x12[2] = 1. 18-bit mode will be auto-loaded into the deserializer from the serializer. See Table 2 for GPIO enable and configuration.

Table 2. GPIO Enable and Configuration

Description	Device	Forward Channel	Back Channel
GPIO3 / D_GPIO3	Serializer	0x0F[3:0] = 0x3	0x0F[3:0] = 0x5
	Deserializer	0x1F[3:0] = 0x5	0x1F[3:0] = 0x3
GPIO2 / D_GPIO2	Serializer	0x0E[7:4] = 0x3	0x0E[7:4] = 0x5
	Deserializer	0x1E[7:4] = 0x5	0x1E[7:4] = 0x3
GPIO1 / D_GPIO1	Serializer	0x0E[3:0] = 0x3	0x0E[3:0] = 0x5
	Deserializer	0x1E[3:0] = 0x5	0x1E[3:0] = 0x3
GPIO0 / D_GPIO0	Serializer	0x0D[3:0] = 0x3	0x0D[3:0] = 0x5
	Deserializer	0x1D[3:0] = 0x5	0x1D[3:0] = 0x3

The input value present on GPIO[3:0] or D_GPIO[3:0] may also be read from register, or configured to local output mode (Table 9).

8.3.8.2 Back Channel Configuration

The D_GPIO[3:0] pins can be configured to obtain different sampling rates depending on the mode as well as back channel frequency. The mode is controlled by register 0x43 (Table 9). The back channel frequency can be controlled several ways:

1. Register 0x23[6] sets the divider that controls the back channel frequency based on the internal oscillator. 0x23[6] = 0 sets the divider to 4 and 0x23[6] = 1 sets the divider to 2. As long as BC_HS_CTL (0x23[4]) is

set to 0, the back channel frequency would be either 5 Mbps or 10Mbps based on this bit.

2. Register 0x23[4] enables the high-speed back channel. This can also be pin-strapped via MODE_SEL1 (See Table 8). This bit overrides 0x23[6], and sets the divider for the back channel frequency to 1. Setting this bit to 1 sets the back channel frequency to 20 Mbps.

The back channel frequency has variation of ±20%. Note: The back channel frequency must be set to 5 Mbps when paired with a DS90UB925Q-Q1, DS90UB925AQ-Q1, or DS90UB927Q-Q1. See Table 3 for details about configuring the D_GPIOs in various modes.

Table 3. Back Channel D_GPIO Effective Frequency

HSCC_MODE (0x43[2:0])	Mode	Number of D_GPIOs	Samples per Frame	D_GPIO Effective Frequency(1) (kHz)			D_GPIOs Allowed
				5 Mbps BC(2)	10 Mbps BC(3)	20 Mbps BC(4)	
000	Normal	4	1	33	66	133	D_GPIO[3:0]
011	Fast	4	6	200	400	800	D_GPIO[3:0]
010	Fast	2	10	333	666	1333	D_GPIO[1:0]
001	Fast	1	15	500	1000	2000	D_GPIO0

(1) The effective frequency assumes the worst case back channel frequency (-20%) and a 4X sampling rate.
(2) 5 Mbps corresponds to BC FREQ SELECT = 0 & BC_HS_CTL = 0
(3) 10 Mbps corresponds to BC FREQ SELECT = 1 & BC_HS_CTL = 0
(4) 20 Mbps corresponds to BC FREQ SELECT = X & BC_HS_CTL = 1

8.3.8.3 GPIO_REG[8:5] Configuration

GPIO_REG[8:5] are register-only GPIOs and may be programmed as outputs or read as inputs through local register bits only. Where applicable, these bits are shared with I2S pins and will override I2S input if enabled into GPIO_REG mode. See Table 4 for GPIO enable and configuration.

Note: Local GPIO value may be configured and read either through local register access, or remote register access through the Low-Speed Bidirectional Control Channel. Configuration and state of these pins are not transported from serializer to deserializer as is the case for GPIO[3:0].

Table 4. GPIO_REG and GPIO Local Enable and Configuration

Description	Register Configuration	Function
GPIO_REG8	0x21[7:4] = 0x1	Output, L
	0x21[7:4] = 0x9	Output, H
	0x21[7:4] = 0x3	Input, Read: 0x6F[0]
GPIO_REG7	0x21[3:0] = 0x1	Output, L
	0x21[3:0] = 0x9	Output, H
	0x21[3:0] = 0x3	Input, Read: 0x6E[7]
GPIO_REG6	0x20[7:4] = 0x1	Output, L
	0x20[7:4] = 0x9	Output, H
	0x20[7:4] = 0x3	Input, Read: 0x6E[6]
GPIO_REG5	0x20[3:0] = 0x1	Output, L
	0x20[3:0] = 0x9	Output, H
	0x20[3:0] = 0x3	Input, Read: 0x6E[5]
GPIO3	0x1F[3:0] = 0x1	Output, L
	0x1F[3:0] = 0x9	Output, H
	0x1F[3:0] = 0x3	Input, Read: 0x6E[3]
GPIO2	0x1E[7:4] = 0x1	Output, L
	0x1E[7:4] = 0x9	Output, H
	0x1E[7:4] = 0x3	Input, Read: 0x6E[2]
GPIO1	0x1E[3:0] = 0x1	Output, L
	0x1E[3:0] = 0x9	Output, H
	0x1E[3:0] = 0x3	Input, Read: 0x6E[1]

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Table 4. GPIO_REG and GPIO Local Enable and Configuration (continued)

Description	Register Configuration	Function
GPIO0	0x1D[3:0] = 0x1	Output, L
	0x1D[3:0] = 0x9	Output, H
	0x1D[3:0] = 0x3	Input, Read: 0x6E[0]

8.3.9 SPI Communication

The SPI Control Channel utilizes the secondary link in a 2-lane FPD-Link III implementation. Two possible modes are available, Forward Channel and Reverse Channel modes. In Forward Channel mode, the SPI Master is located at the Serializer, such that the direction of sending SPI data is in the same direction as the video data. In Reverse Channel mode, the SPI Master is located at the Deserializer, such that the direction of sending SPI data is in the opposite direction as the video data.

The SPI Control Channel can operate in a high speed mode when writing data, but must operate at lower frequencies when reading data. During SPI reads, data is clocked from the slave to the master on the SPI clock falling edge. Thus, the SPI read must operate with a clock period that is greater than the round trip data latency. On the other hand, for SPI writes, data can be sent at much higher frequencies where the MISO pin can be ignored by the master.

SPI data rates are not symmetrical for the two modes of operation. Data over the forward channel can be sent much faster than data over the reverse channel.

Note: SPI cannot be used to access Serializer / Deserializer registers.

8.3.9.1 SPI Mode Configuration

SPI is configured over I2C using the High-Speed Control Channel Configuration (HSCC_CONTROL) register, 0x43 (Table 10). HSCC_MODE (0x43[2:0]) must be configured for either High-Speed, Forward Channel SPI mode (110) or High-Speed, Reverse Channel SPI mode (111).

8.3.9.2 Forward Channel SPI Operation

In Forward Channel SPI operation, the SPI master located at the Serializer generates the SPI Clock (SPLK), Master Out / Slave In data (MOSI), and active low Slave Select (SS). The Serializer oversamples the SPI signals directly using the video pixel clock. The three sampled values for SPLK, MOSI, and SS are each sent on data bits in the forward channel frame. At the Deserializer, the SPI signals are regenerated using the pixel clock. In order to preserve setup and hold time, the Deserializer will hold MOSI data while the SPLK signal is high. In addition, it delays SPLK by one pixel clock relative to the MOSI data, increasing setup by one pixel clock.

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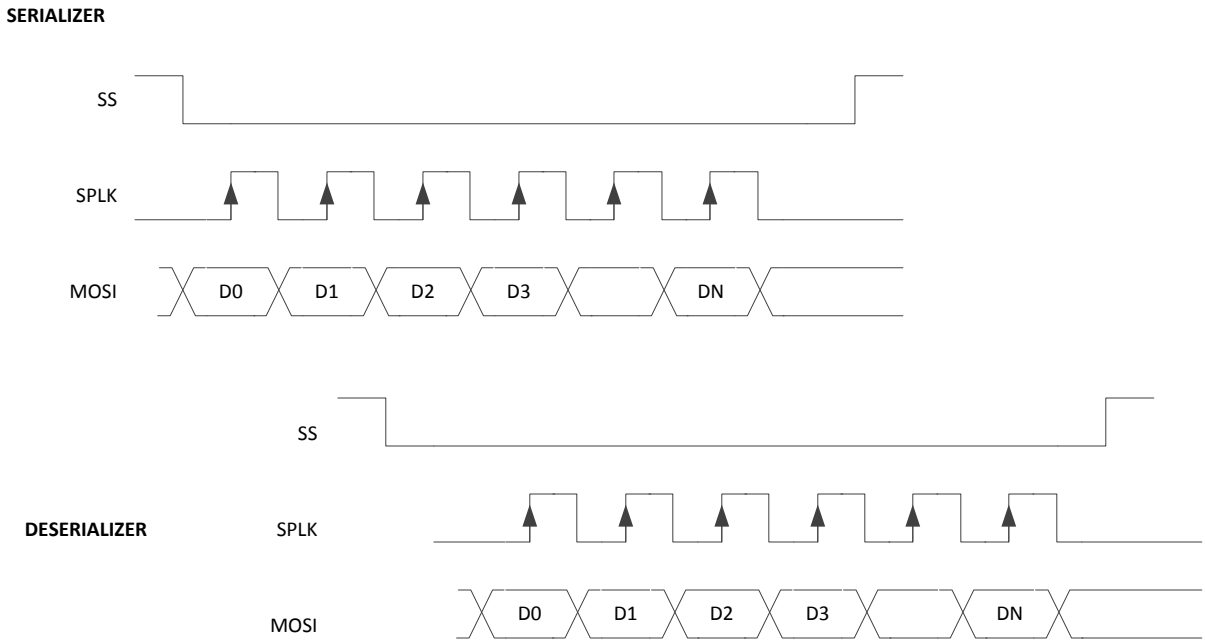

Figure 19. Forward Channel SPI Write

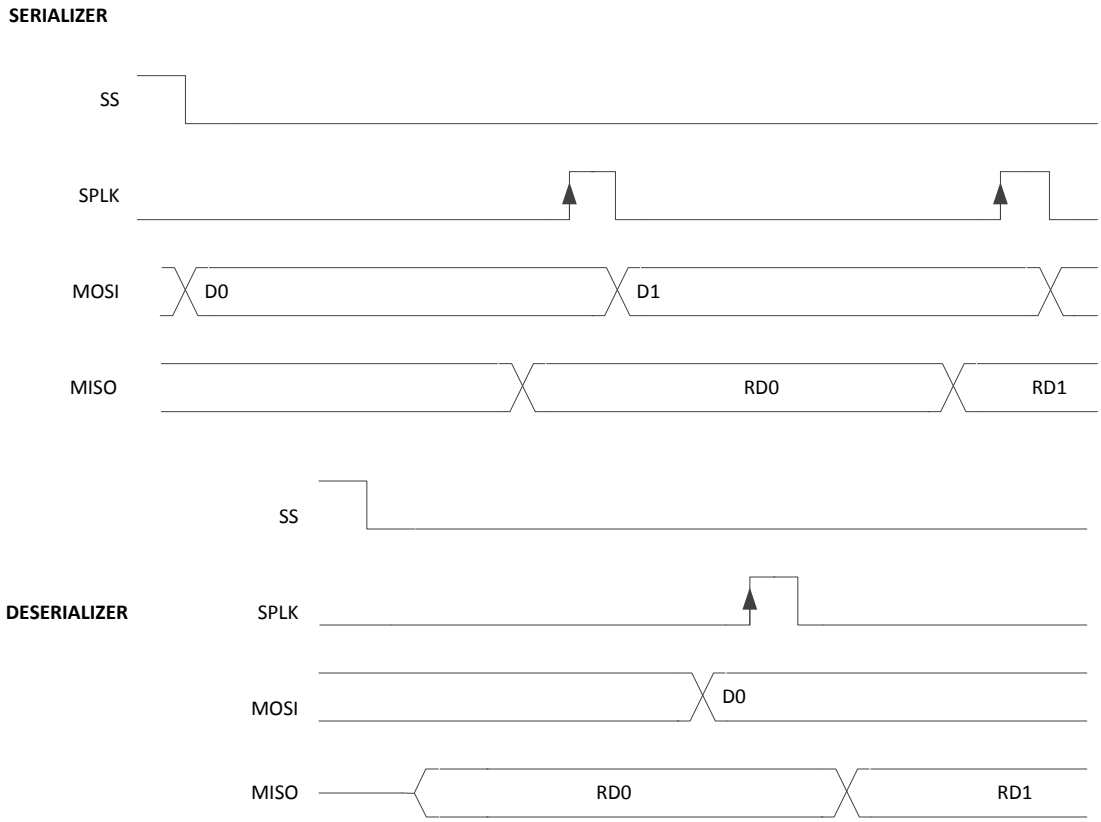

Figure 20. Forward Channel SPI Read

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8.3.9.3 Reverse Channel SPI Operation

In Reverse Channel SPI operation, the Deserializer samples the Slave Select (SS), SPI clock (SCLK) into the internal oscillator clock domain. In addition, upon detection of the active SPI clock edge, the Deserializer samples the SPI data (MOSI). The SPI data samples are stored in a buffer to be passed to the Serializer over the back channel. The Deserializer sends SPI information in a back channel frame to the Serializer. In each back channel frame, the Deserializer sends an indication of the Slave Select value. The Slave Select should be inactive (high) for at least one back-channel frame period to ensure propagation to the Serializer.

Because data is delivered in separate back channel frames and buffered, the data may be regenerated in bursts. The following figure (Figure 21) shows an example of the SPI data regeneration when the data arrives in three back channel frames. The first frame delivered the SS active indication, the second frame delivered the first three data bits, and the third frame delivers the additional data bits.

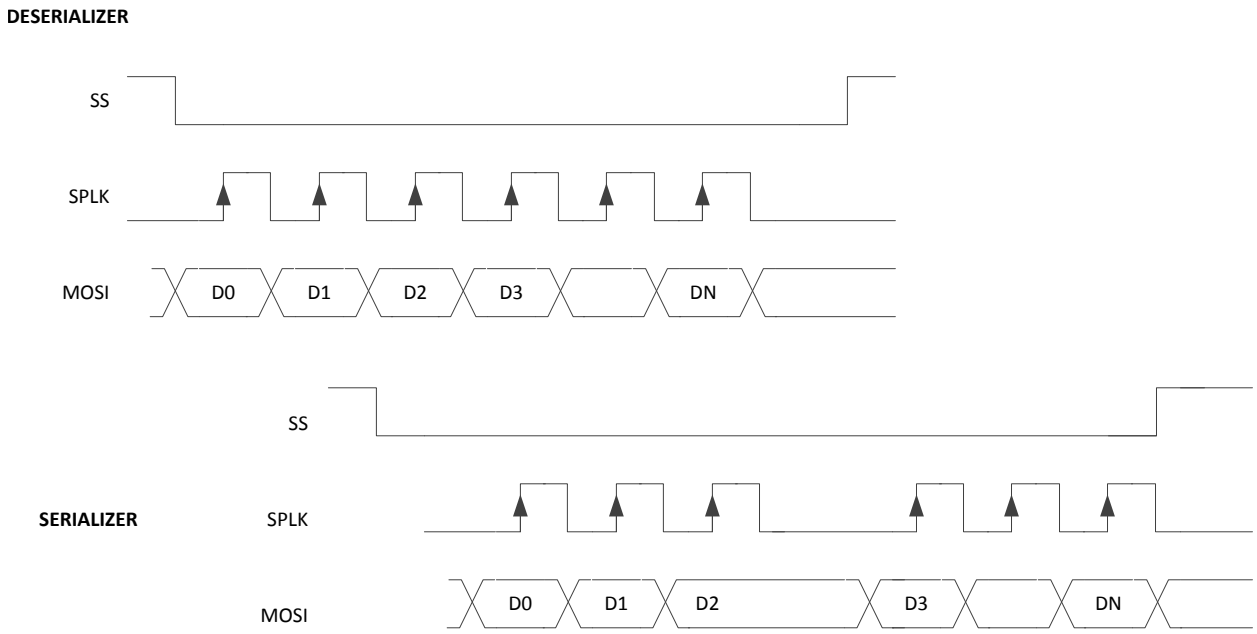

Figure 21. Reverse Channel SPI Write

For Reverse Channel SPI reads, the SPI master must wait for a round-trip response before generating the sampling edge of the SPI clock. This is similar to operation in Forward channel mode. Note that at most one data/clock sample will be sent per back channel frame.

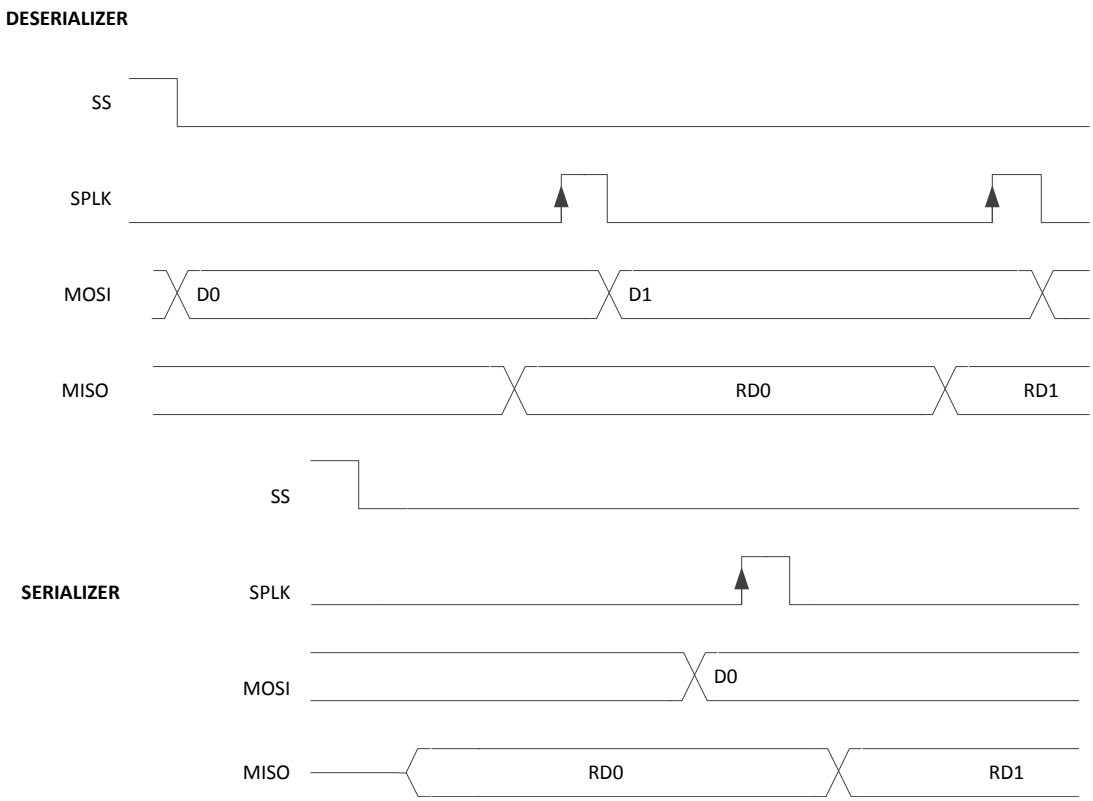

Figure 22. Reverse Channel SPI Read

For both Reverse Channel SPI writes and reads, the SPI_SS signal should be deasserted for at least one back channel frame period.

Table 5. SPI SS Deassertion Requirement

Back Channel Frequency	Deassertion Requirement
5 Mbps	7.5 µs
10 Mbps	3.75 µs
20 Mbps	1.875 µs

8.3.10 Backward Compatibility

The DS90UB948-Q1 is also backward compatible to the for PCLK frequencies ranging from 25MHz to 85MHz. Backward compatibility does not need to be enabled. When paired with a backward compatible device, the Deserializer will auto-detect to 1-lane FPD-Link III on the primary channel (RIN0±).

8.3.11 Input Equalization

An FPD-Link III input adaptive equalizer provides compensation for transmission medium losses and reduces medium-induced deterministic jitter. It equalizes up to 15m STP or 50Ω Coaxial cables with 3 connection breaks at maximum serializer stream payload of 3.36 Gbps.

8.3.12 I2S Audio Interface

This Deserializer features six I2S output pins that, when paired with a compatible serializer, supports surround sound audio applications. The bit clock (I2S_CLK) supports frequencies between 1MHz and the smaller of <PCLK/2 or <13MHz. Four I2S data outputs carry two channels of I2S-formatted digital audio each, with each channel delineated by the word select (I2C_WC) input.

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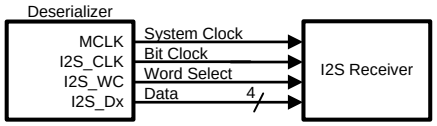

Figure 23. I2S Connection Diagram

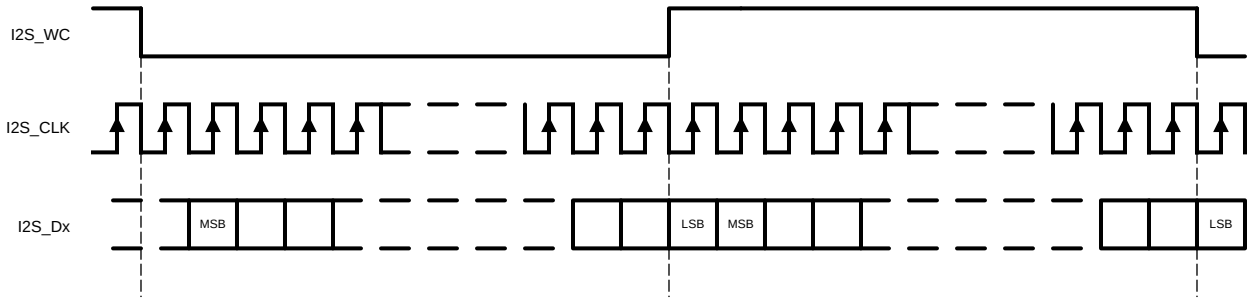

Figure 24. I2S Frame Timing Diagram

When paired with a DS90UB925Q, the Deserializer I2S interface supports a single I2S data output through I2S_DA (24-bit video mode), or two I2S data outputs through I2S_DA and I2S_DB (18-bit video mode).

8.3.12.1 I2S Transport Modes

By default, packetized audio is received during video blanking periods in dedicated Data Island Transport frames. The transport mode is set in the serializer and auto-loaded into the deserializer by default. The audio configuration may be disabled from control registers if Forward Channel Frame Transport of I2S data is desired. In frame transport, only I2S_DA is received to the Deserializer. Surround Sound Mode, which transmits all four I2S data inputs (I2S_D[D:A]), may only be operated in Data Island Transport mode. This mode is only available when connected to a DS90UH927Q, DS90UB927Q, DS90UH949-Q1, DS90UB949-Q1, DS90UH947-Q1, DS90UB947-Q1, DS90UH929-Q1, or DS90UB929-Q1 serializer. If connected to a DS90UH925Q or DS90UB925Q serializer, only I2S_DA and I2S_DB may be received.

8.3.12.2 I2S Repeater

I2S audio may be fanned-out and propagated in the repeater application. By default, data is propagated via Data Island Transport on the FPD-Link interface during the video blanking periods. If frame transport is desired, then the I2S pins should be connected from the deserializer to all serializers. Activating surround sound at the top-level serializer automatically configures downstream serializers and deserializers for surround sound transport utilizing Data Island Transport. If 4-channel operation utilizing I2S_DA and I2S_DB only is desired, this mode must be explicitly set in each serializer and deserializer control register throughout the repeater tree (Table 10).

A DS90UB948-Q1deserializer configured in repeater mode may also regenerate I2S audio from its I2S input pins in lieu of Data Island frames. See the Repeater Connection Diagram (Figure 27) and the I2C Control Registers (Table 10) for additional details.

8.3.12.3 I2S Jitter Cleaning

This device features a standalone PLL to clean the I2S data jitter, supporting high-end car audio systems. If I2S_CLK frequency is less than 1MHz, this feature must be disabled through register 0x2B[7]. See Table 10.

8.3.12.4 MCLK

The deserializer has an I2S Master Clock Output (MCLK). It supports x1, x2, or x4 of I2S CLK Frequency. When the I2S PLL is disabled, the MCLK output is off. Table 6 covers the range of I2S sample rates and MCLK frequencies. By default, all the MCLK output frequencies are x2 of the I2S CLK frequencies. The MCLK frequencies can also be enabled through the register bits 0x3A[6:4] (I2S DIVSEL), shown in Table 10. To select desired MCLK frequency, write 0x3A[7], then write to bit [6:4] accordingly.

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Table 6. Audio Interface Frequencies

Sample Rate (kHz)	I2S Data Word Size (bits)	I2S_CLK (MHz)	MCLK Output (MHz)	Register 0x3A[6:4]
32	16	1.024	I2S_CLK x1	000
			I2S_CLK x2	001
			I2S_CLK x4	010
44.1		1.4112	I2S_CLK x1	000
			I2S_CLK x2	001
			I2S_CLK x4	010
48		1.536	I2S_CLK x1	000
			I2S_CLK x2	001
			I2S_CLK x4	010
96		3.072	I2S_CLK x1	001
			I2S_CLK x2	010
			I2S_CLK x4	011
192		6.144	I2S_CLK x1	010
			I2S_CLK x2	011
			I2S_CLK x4	100
32	24	1.536	I2S_CLK x1	000
			I2S_CLK x2	001
			I2S_CLK x4	010
44.1		2.117	I2S_CLK x1	001
			I2S_CLK x2	010
			I2S_CLK x4	011
48		2.304	I2S_CLK x1	001
			I2S_CLK x2	010
			I2S_CLK x4	011
96		4.608	I2S_CLK x1	010
			I2S_CLK x2	011
			I2S_CLK x4	100
192		9.216	I2S_CLK x1	011
			I2S_CLK x2	100
			I2S_CLK x4	101
32	32	2.048	I2S_CLK x1	001
			I2S_CLK x2	010
			I2S_CLK x4	011
44.1		2.8224	I2S_CLK x1	001
			I2S_CLK x2	010
			I2S_CLK x4	011
48		3.072	I2S_CLK x1	001
			I2S_CLK x2	010
			I2S_CLK x4	011
96		6.144	I2S_CLK x1	010
			I2S_CLK x2	011
			I2S_CLK x4	100
192		12.288	I2S_CLK x1	011
			I2S_CLK x2	100
			I2S_CLK x4	110

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8.3.13 Repeater

The supported Repeater application provides a mechanism to extend transmission over multiple links to multiple display devices.

8.3.13.1 Repeater Configuration

In the repeater application, this document refers to the DS90UB947-Q1 Serializer or as the Transmitter (TX), and refers to the DS90UB948-Q1 as the Receiver (RX). Figure 25 shows the maximum configuration supported for Repeater implementations. Two levels of Repeaters are supported with a maximum of three Transmitters per Receiver.

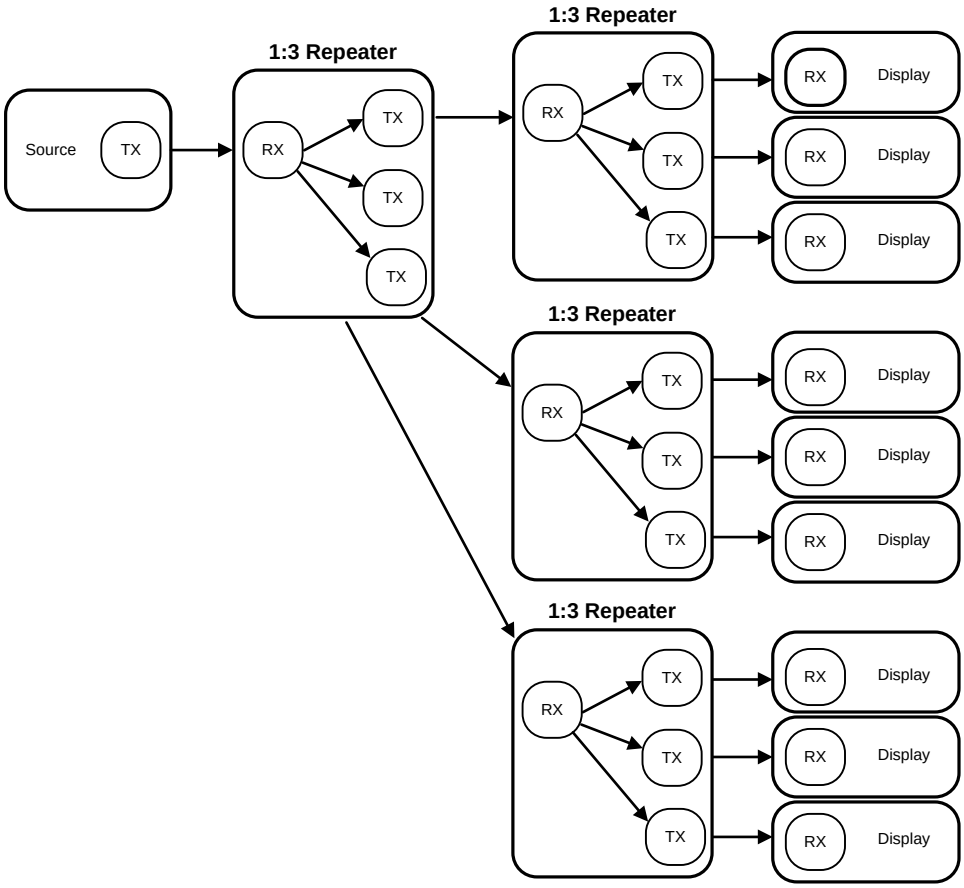

Figure 25. Maximum Repeater Application

In a repeater application, the I2C interface at each TX and RX is configured to transparently pass I2C communications upstream or downstream to any I2C device within the system. This includes a mechanism for assigning alternate IDs (Slave Aliases) to downstream devices in the case of duplicate addresses.

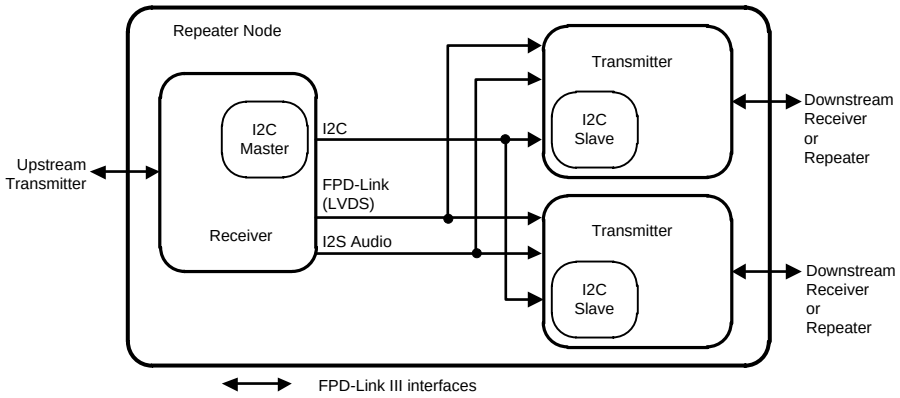

Figure 26. 1:2 Repeater Configuration

8.3.13.2 Repeater Connections

The Repeater requires the following connections between the Receiver and each Transmitter Figure 27.

1. Video Data – Connect all FPD-Link data and clock pairs. Single FPD-Link (D[3:0]) or Dual FPD-Link (D[7:0]) are both possible, provided the Deserializer and all Serializers are configured in the same mode.
2. I2C – Connect SCL and SDA signals. Both signals should be pulled up to V_{DD33} or V_{DDIO} = 3.0V to 3.6V with 4.7kΩ resistors.
3. Audio (optional) – Connect I2S_CLK, I2S_WC, and I2S_Dx signals. Audio is normally transported on the FPD-Link interface.
4. IDx pin – Each Transmitter and Receiver must have an unique I2C address.
5. REPEAT & MODE_SEL pins — All Transmitters and Receivers must be set into Repeater Mode.
6. Interrupt pin – Connect DS90UB948-Q1 INTB_IN pin to the DS90UB947-Q1 INTB pin. The signal must be pulled up to V_{DDIO} with a 10kΩ resistor.

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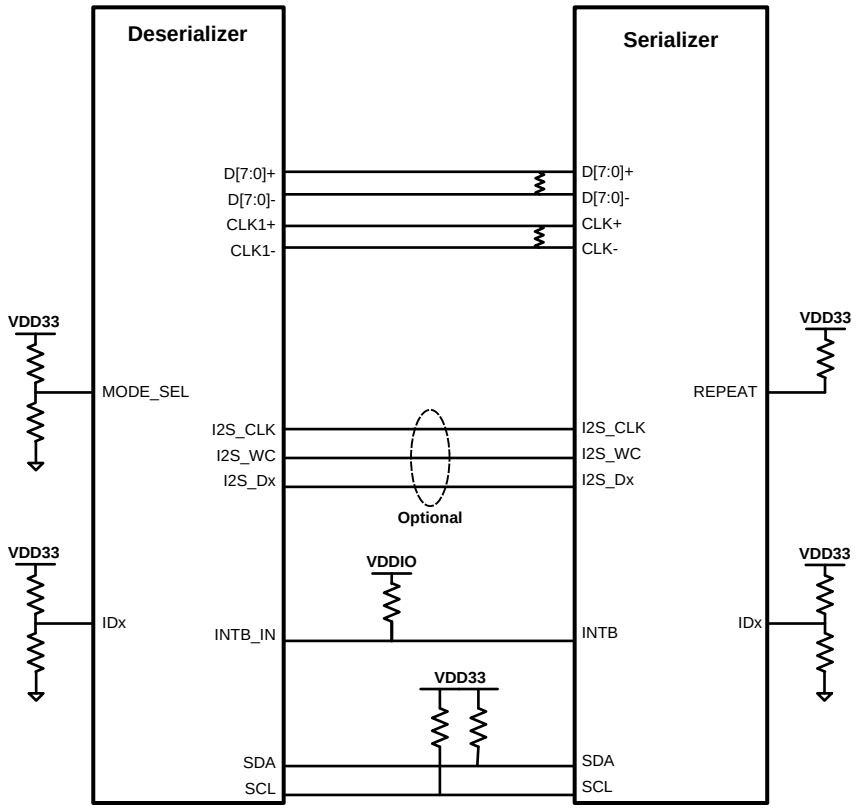

Figure 27. Repeater Connection Diagram

8.3.13.2.1 Repeater Fan-out Electrical Requirements

Repeater applications requiring fan-out from one DS90UB948-Q1 Deserializer to up to three DS90UB947-Q1 Serializers requires special considerations for routing and termination of the FPD-Link differential traces. Figure 28 details the requirements that must be met for each signal pair:

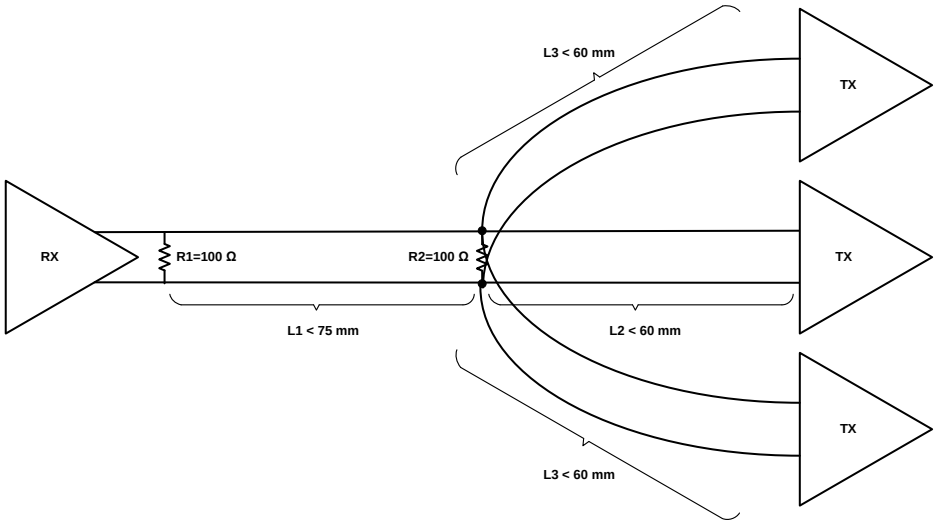

Figure 28. FPD-Link Fan-Out Electrical Requirements

8.3.14 Built-In Self Test (BIST)

An optional At-Speed Built-In Self Test (BIST) feature supports testing of the high speed serial link and the low-speed back channel without external data connections. This is useful in the prototype stage, equipment production, in-system test, and system diagnostics.

8.3.14.1 BIST Configuration And Status

The BIST mode is enabled at the deserializer by pin (BISTEN) or BIST configuration register. The test may select either an external PCLK or the 33 MHz internal Oscillator clock (OSC) frequency in the Serializer. In the absence of PCLK, the user can select the internal OSC frequency at the deserializer through the BISTC pin or BIST configuration register.

When BIST is activated at the deserializer, a BIST enable signal is sent to the serializer through the Back Channel. The serializer outputs a test pattern and drives the link at speed. The deserializer detects the test pattern and monitors it for errors. The deserializer PASS output pin toggles to flag each frame received containing one or more errors. The serializer also tracks errors indicated by the CRC fields in each back channel frame.

The BIST status can be monitored real time on the deserializer PASS pin, with each detected error resulting in a half pixel clock period toggled LOW. After BIST is deactivated, the result of the last test is held on the PASS output until reset (new BIST test or Power Down). A high on PASS indicates NO ERRORS were detected. A Low on PASS indicates one or more errors were detected. The duration of the test is controlled by the pulse width applied to the deserializer BISTEN pin. LOCK status is valid throughout the entire duration of BIST.

See Figure 29 for the BIST mode flow diagram.

8.3.14.1.1 Sample BIST Sequence

Note: Before BIST can be enabled, D_GPIO0 (pin 19) must be strapped HIGH and D_GPIO[3:1] (pins 16, 17, and 18) must be strapped LOW.

1. BIST Mode is enabled via the BISTEN pin of Deserializer. The desired clock source is selected through the deserializer BISTC pin.
2. The serializer is awakened through the back channel if it is not already on. An all-zeros pattern is balanced, scrambled, randomized, and sent through the FPD-Link III interface to the deserializer. Once the serializer and the deserializer are in BIST mode and the deserializer acquires LOCK, the PASS pin of the deserializer goes high and BIST starts checking the data stream. If an error in the payload (1 to 35) is detected, the PASS pin will switch low for one half of the clock period. During the BIST test, the PASS output can be monitored and counted to determine the payload error rate per 35 bits.
3. To Stop BIST mode, set the BISTEN pin LOW. The deserializer stops checking the data, and the final test result is held on the PASS pin. If the test ran error free, the PASS output will remain HIGH. If there one or more errors were detected, the PASS output will output constant LOW. The PASS output state is held until a new BIST is run, the device is RESET, or the device is powered down. BIST duration is user-controlled and may be of any length.

The link returns to normal operation after the deserializer BISTEN pin is low. shows the waveform diagram of a typical BIST test for two cases. Case 1 is error free, and Case 2 shows one with multiple errors. In most cases it is difficult to generate errors due to the robustness of the link (differential data transmission etc.), thus they may be introduced by greatly extending the cable length, faulting the interconnect medium, or reducing signal condition enhancements (Rx Equalization).

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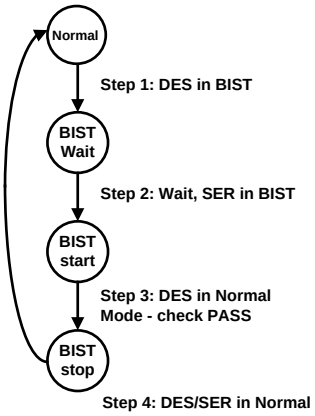
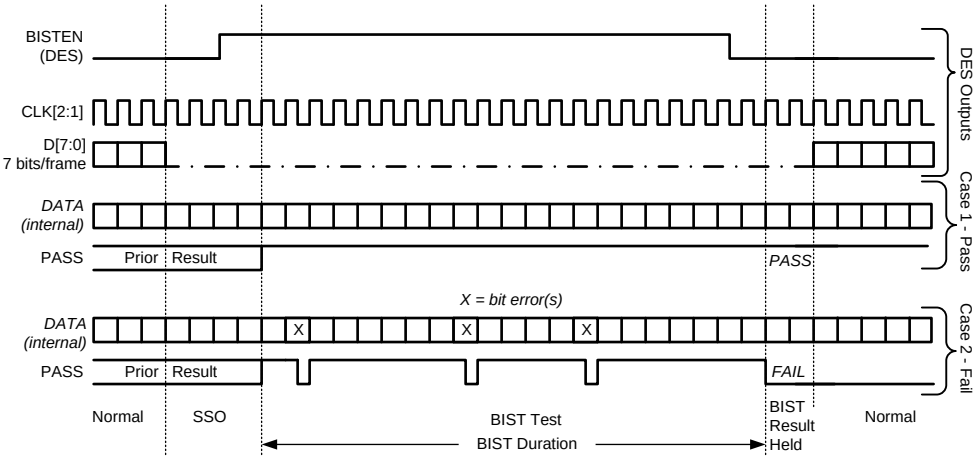


Figure 29. BIST Mode Flow Diagram

8.3.14.2 Forward Channel and Back Channel Error Checking

The Deserializer, on locking to the serial stream, compares the recovered serial stream with all-zeroes and records any errors in status registers. Errors are also dynamically reported on the PASS pin of the deserializer. Forward channel errors may also be read from register 0x25 (Table 10).

The back-channel data is checked for CRC errors once the serializer locks onto the back-channel serial stream, as indicated by link detect status (register bit 0x0C[0] - Table 10). CRC errors are recorded in an 8-bit register in the serializer. The register is cleared when the serializer enters the BIST mode. As soon as the serializer enters BIST mode, the functional mode CRC register starts recording any back channel CRC errors. The BIST mode CRC error register is active in BIST mode only and keeps the record of the last BIST run until cleared or the serializer enters BIST mode again.



BIST Waveforms

8.3.15 Internal Pattern Generation

The deserializer supports the internal pattern generation feature. It allows basic testing and debugging of an integrated panel. The test patterns are simple and repetitive and allow for a quick visual verification of panel operation. As long as the device is not in power down mode, the test pattern will be displayed even if no parallel input is applied. If no PCLK is received, the test pattern can be configured to use a programmed oscillator frequency. For detailed information, refer to Application Note AN-2198 (SNLA132).

8.4 Device Functional Modes

8.4.1 Configuration Select MODE_SEL[1:0]

The DS90UB948-Q1 is capable of operating in either in 1-lane or 2-lane mode for FPD-Link III. By default, the FPD-Link III receiver automatically configures the input based on 1- or 2-lane mode operation. Programming register 0x34 [4:3] settings will override the automatic detection. For each FPD-Link III pair, the serial datastream is composed of a 35-bit symbol.

The DS90UB948-Q1 recovers the FPD-Link III serial datastream(s) and produces video data driven to the OpenLDI (LVDS) interface. OpenLDI Single Link and Dual Link are supported with color depths of 18 bits per pixel or 24 bits per pixel. There are 8 differential data pairs (D0 through D7) and two clock pairs (CLK1 and CLK2) on the OpenLDI interface. The number of data lines may vary, depending on the pixel formats supported. For Single Link output the pixel clock is limited to 96 MHz. In the case of Dual Link, the pixel clock is limited to 170 MHz (or 85 MHz per LVDS port). When in a Dual Link configuration, LVDS channels D0 to D3 carry ODD pixel data, and LVDS channels D4 to D7 carry EVEN pixel data.

The device can be configured in following modes:

- 1-lane FPD-Link III Input, Single Link OpenLDI Output
- 1-lane FPD-Link III Input, Dual Link OpenLDI Output
- 2-lane FPD-Link III Input, Dual Link OpenLDI Output
- 2-lane FPD-Link III Input, Single Link OpenLDI Output
- 2-lane FPD-Link III Input, Single Link OpenLDI Output (Replicate)

8.4.1.1 1-lane FPD-Link III Input, Single Link OpenLDI Output

In this configuration the PCLK rate embedded within the 1-lane FPD-Link III frame can range from 25 MHz to 96 MHz, resulting in a link rate of 875 Mbps (35 bit * 25 MHz) to 3.36 Gbps (35 bit * 96 MHz). Each LVDS data lane will operate at a speed of 7 bits per LVDS clock cycle; resulting in a serial line rate of 175 Mbps to 672 Mbps. CLK1 will operate at the same rate as PCLK with a duty cycle ratio of 57:43.

8.4.1.2 1-lane FPD-Link III Input, Dual Link OpenLDI Output

The input RGB data is split into odd and even pixels starting with the ODD (first) pixel outputs D0 to D3 and then the EVEN (second) pixel outputs D4 to D7. The splitting of the data signals starts with DE (data enable) transitioning from logic LOW to HIGH indicating active data.

In this configuration the PCLK rate embedded within the 1-lane FPD-Link III frame can range from 50 MHz to 96 MHz, resulting in a link rate of 1.75 Gbps (35 bit * 50 MHz) to 3.36 Gbps (35 bit * 96 MHz). Each LVDS data lane will operate at a speed of 7 bits per 2 LVDS clock cycles, resulting in a serial line rate of 175 Mbps to 336 Mbps. CLK1 and CLK2 will operate at half the rate as PCLK with a duty cycle ratio of 57:43.

8.4.1.3 2-lane FPD-Link III Input, Dual Link OpenLDI Output

The input RGB data is split into odd and even pixels starting with the ODD (first) pixel outputs D0 to D3 and then the EVEN (second) pixel outputs D4 to D7. The splitting of the data signals starts with DE (data enable) transitioning from logic LOW to HIGH indicating active data.

In this configuration the PCLK rate embedded within 2-lane FPD-Link III frame can range from 50 MHz to 170 MHz, resulting in a link rate of 875 Mbps (35 bit * 25 MHz) to 2.975 Gbps (35 bit * 85 MHz). Each LVDS data lane will operate at a speed of 7 bits per 2 LVDS clock cycles, resulting in a serial line rate of 175 Mbps to 595 Mbps. CLK1 and CLK2 will operate at half the rate as PCLK with a duty cycle ratio of 57:43.

8.4.1.4 2-lane FPD-Link III Input, Single Link OpenLDI Output

In this configuration the PCLK rate embedded within 2-lane FPD-Link III frame can range from 50 MHz to 170 MHz, resulting in a link rate of 875 Mbps (35 bit * 25 MHz) to 2.975 Gbps (35 bit * 85 MHz). Each LVDS data lane will operate at a speed of 7 bits per LVDS clock cycle; resulting in a serial line rate of 350 Mbps to 1190 Mbps. CLK1 will operate at the twice the rate as PCLK with a duty cycle ratio of 57:43.

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Device Functional Modes (continued)

8.4.1.5 1-lane FPD-Link III Input, Single Link OpenLDI Output (Replicate)

Same as 1-lane FPD-Link III Input, Single Link OpenLDI Output mode and duplicates the LVDS signal on D4 to D7 outputs.

8.4.2 MODE_SEL[1:0]

Possible configurations are shown in Figure 30. These are described above (Configuration Select MODE_SEL[1:0]).

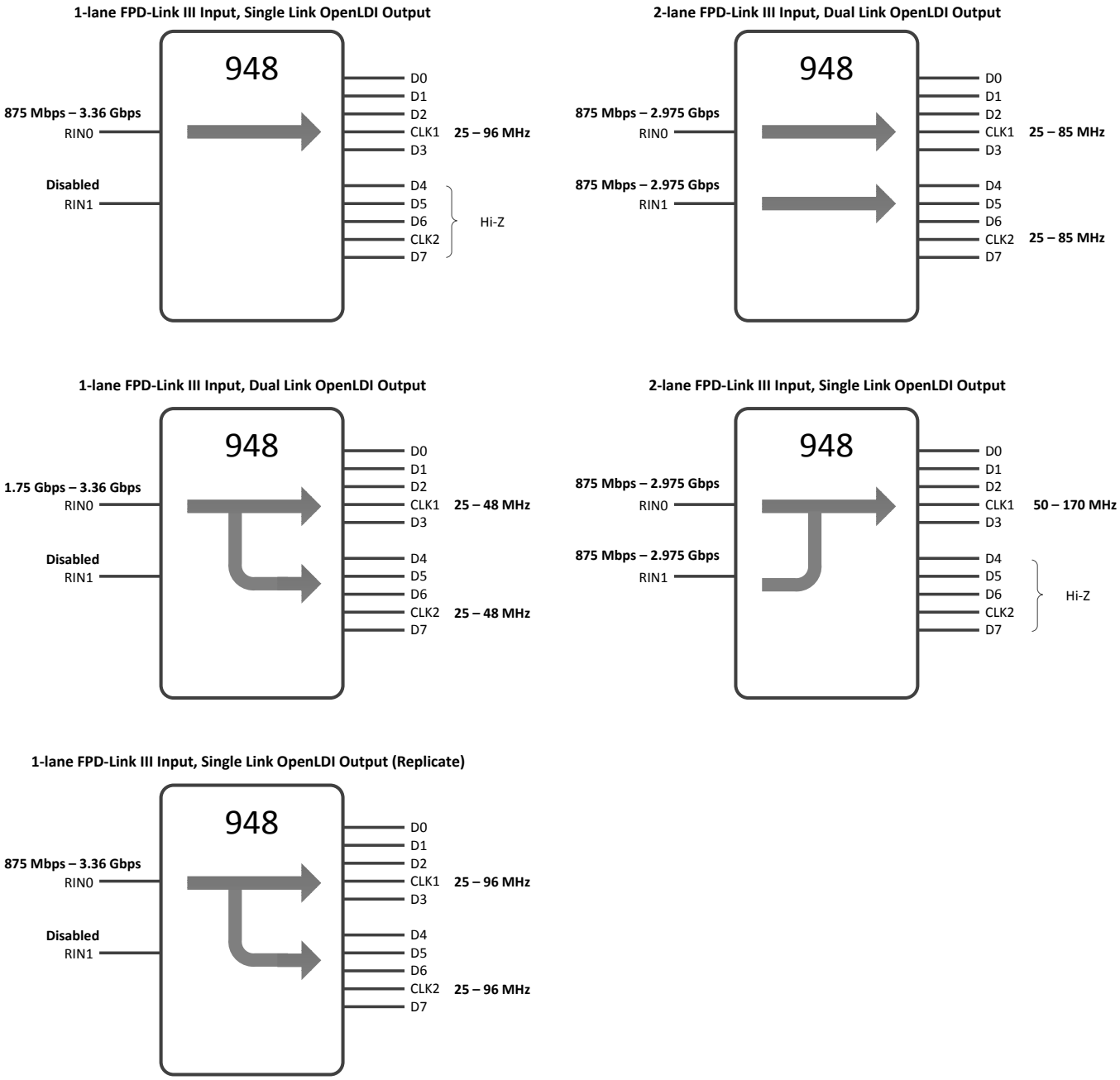

Figure 30. Datapath Configurations

Device Functional Modes (continued)

Configuration of the device may be done via the MODE_SEL[1:0] input pins, or via the configuration register bits. A pull-up resistor and a pull-down resistor of suggested values may be used to set the voltage ratio of the MODE_SEL[1:0] inputs (V_{R1}) and V_{DD33} to select one of the other 8 possible selected modes. See Table 7 and Table 8.

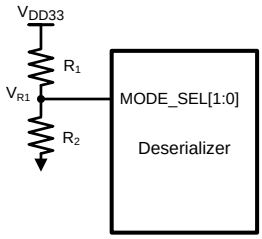

Figure 31. MODE_SEL[1:0] Connection Diagram

Table 7. Configuration Select (MODE_SEL0)

#	Ideal Ratio V_{R1}/V_{DD33}	Target V_{R1} (V)	Suggested Resistor R1 kΩ (1% tol)	Suggested Resistor R2 kΩ (1% tol)	MAP_SEL	OUTPUT_MODE [1:0]	Output Mode
1	0	0	Open	40.2 or Any	0	00	Dual OLDI output
2	0.169	0.559	232	47.5	0	01	Dual SWAP output
3	0.230	0.757	107	31.6	0	10	Single OLDI output
4	0.295	0.974	113	47.5	0	11	Replicate
5	0.376	1.241	113	68.1	1	00	Dual OLDI output
6	0.466	1.538	107	93.1	1	01	Dual SWAP output
7	0.556	1.835	90.9	113	1	10	Single OLDI output
8	0.801	2.642	45.3	182	1	11	Replicate

Table 8. Configuration Select (MODE_SEL1)

#	Ideal Ratio V_{R1}/V_{DD33}	Target V_{R1} (V)	Suggested Resistor R1 kΩ (1% tol)	Suggested Resistor R2 kΩ (1% tol)	Repeater	MODE	High Speed Back Channel	Input Mode
1	0	0	Open	40.2 or Any	0	00	5 Mbps	STP
2	0.169	0.559	232	47.5	0	01	5 Mbps	Coax
3	0.230	0.757	107	31.6	0	10	20 Mbps	STP
4	0.295	0.974	113	47.5	0	11	20 Mbps	Coax
5	0.376	1.241	113	68.1	1	00	5 Mbps	STP
6	0.466	1.538	107	93.1	1	01	5 Mbps	Coax
7	0.556	1.835	90.9	113	1	10	20 Mbps	STP
8	0.801	2.642	45.3	182	1	11	20 Mbps	Coax

8.4.3 OpenLDI Output Frame and Color Bit Mapping Select

The DS90UB948-Q1 can be configured to output 24-bit color (RGB888) or 18-bit color (RGB666) with 2 different mapping schemes, shown in Figure 32 and Figure 33. Each frame corresponds to a single pixel clock (PCLK) cycle. The LVDS clock output from CLK1± and CLK2± follows a 4:3 duty cycle scheme, with each 28-bit pixel frame starting with two LVDS bit clock periods high, three low, and ending with two high. The mapping scheme is controlled by MODE_SEL0 pin or by Register (Table 10).

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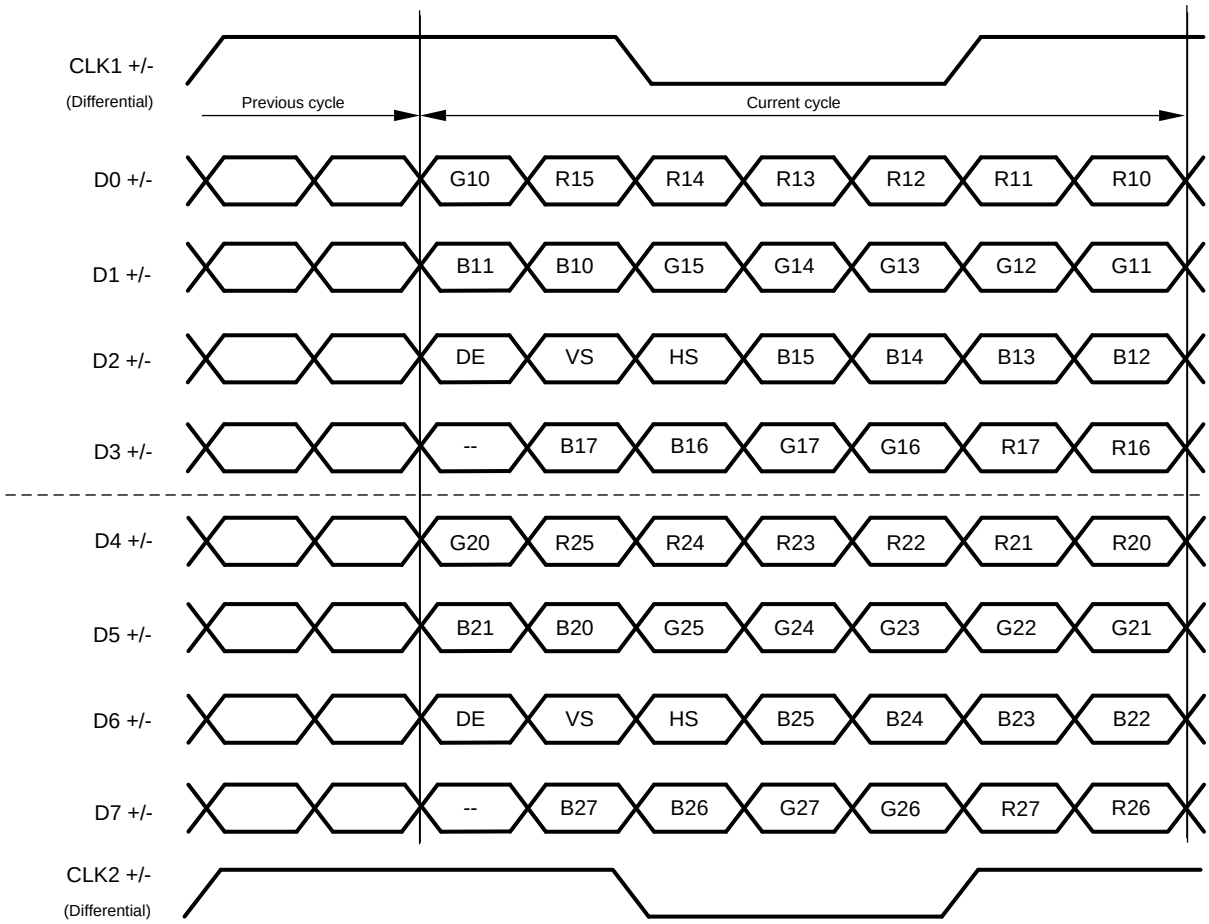

Figure 32. 24-bit Color Dual FPD-Link Mapping: MSBs on D3/D7 (MAPSEL=H)

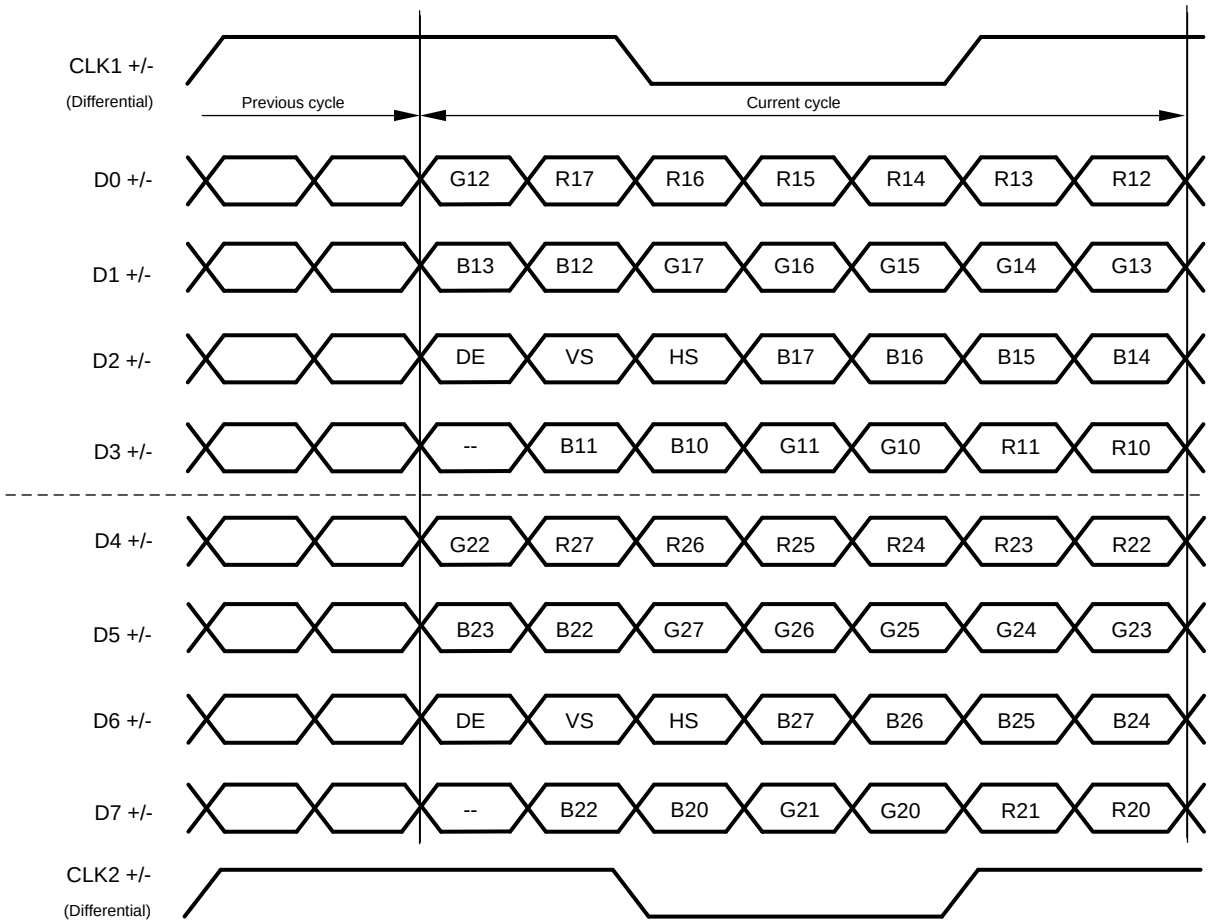

Figure 33. 24-bit Color Dual FPD-Link Mapping: LSBs on D3/D7 (MAPSEL=L)

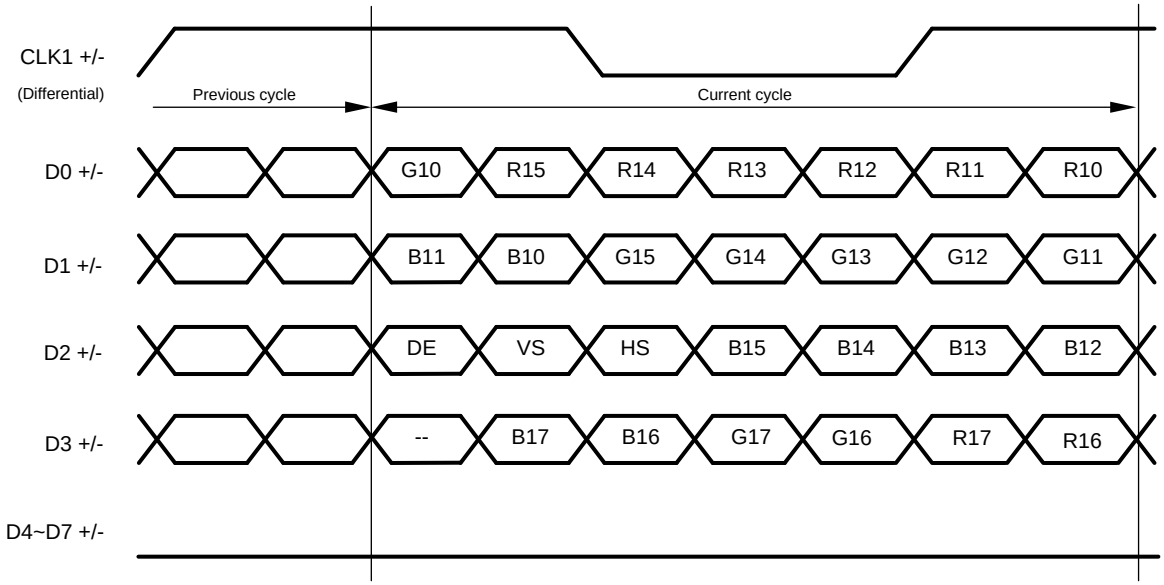

Figure 34. 24-bit Color Single FPD-Link Mapping: MSBs on D3 (MAPSEL=H)

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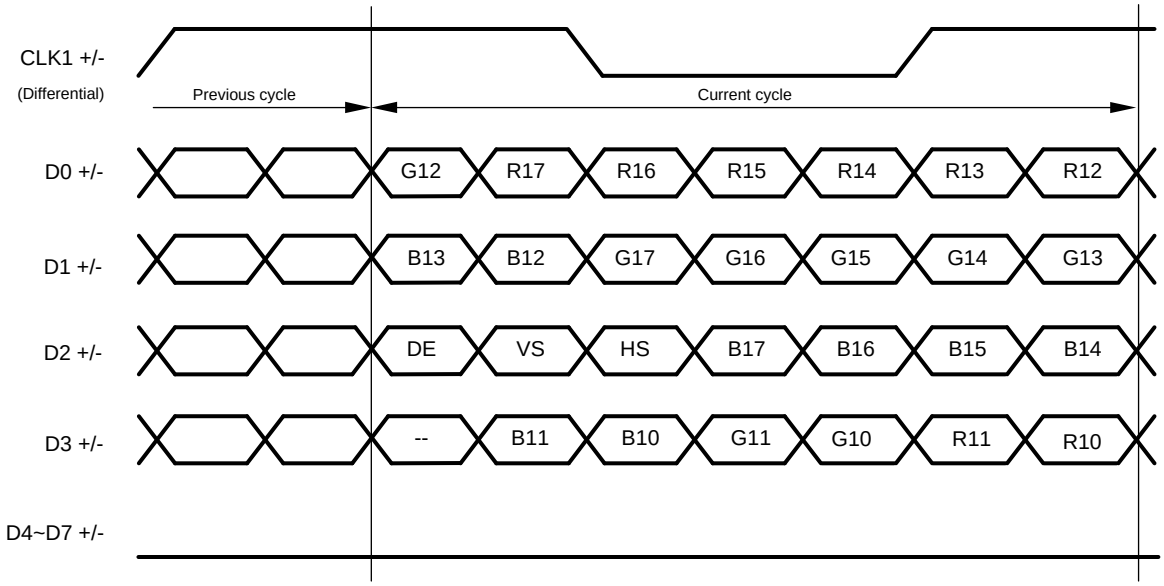

Figure 35. 24-bit Color Single FPD-Link Mapping: LSBs on D3 (MAPSEL=L)

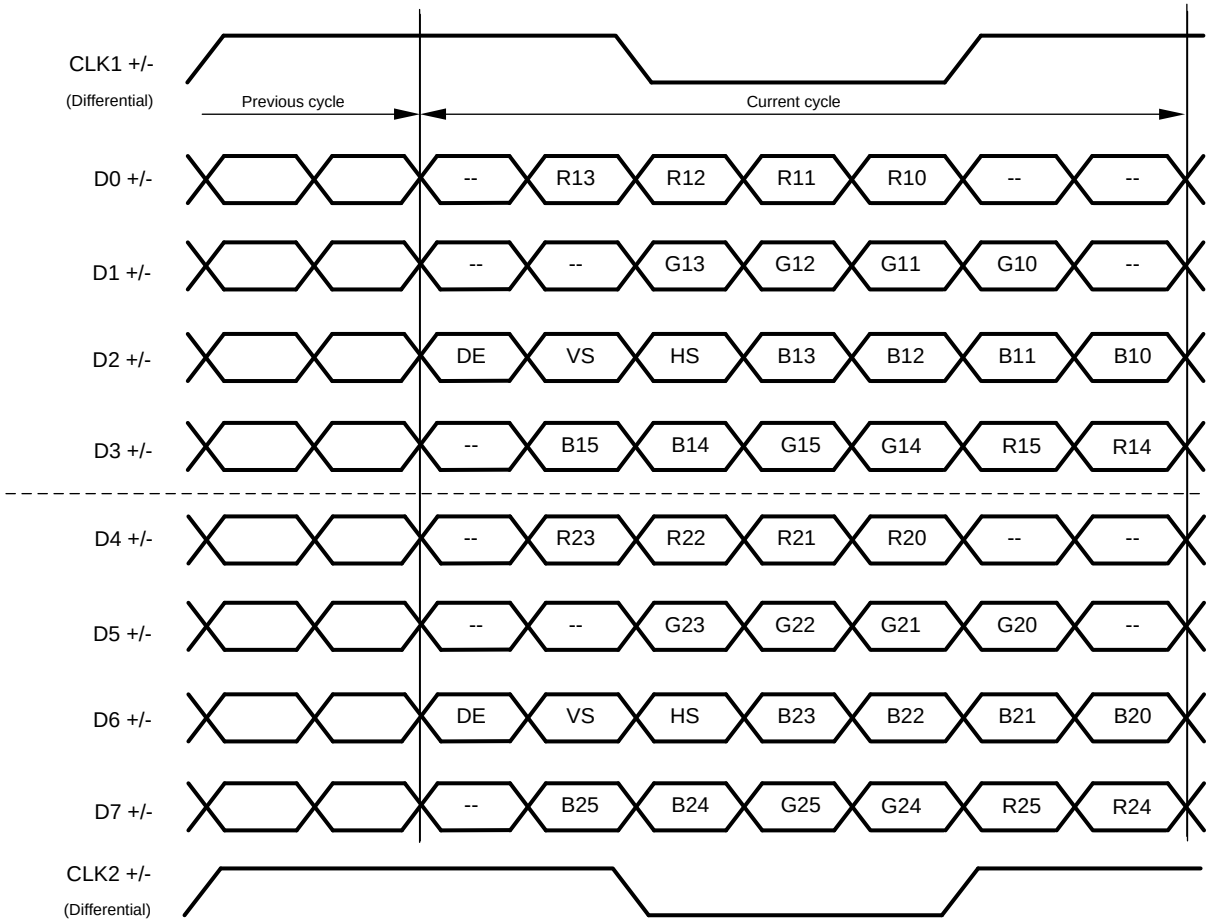

Figure 36. 18-bit Color Dual FPD-Link Mapping (MAPSEL=H)

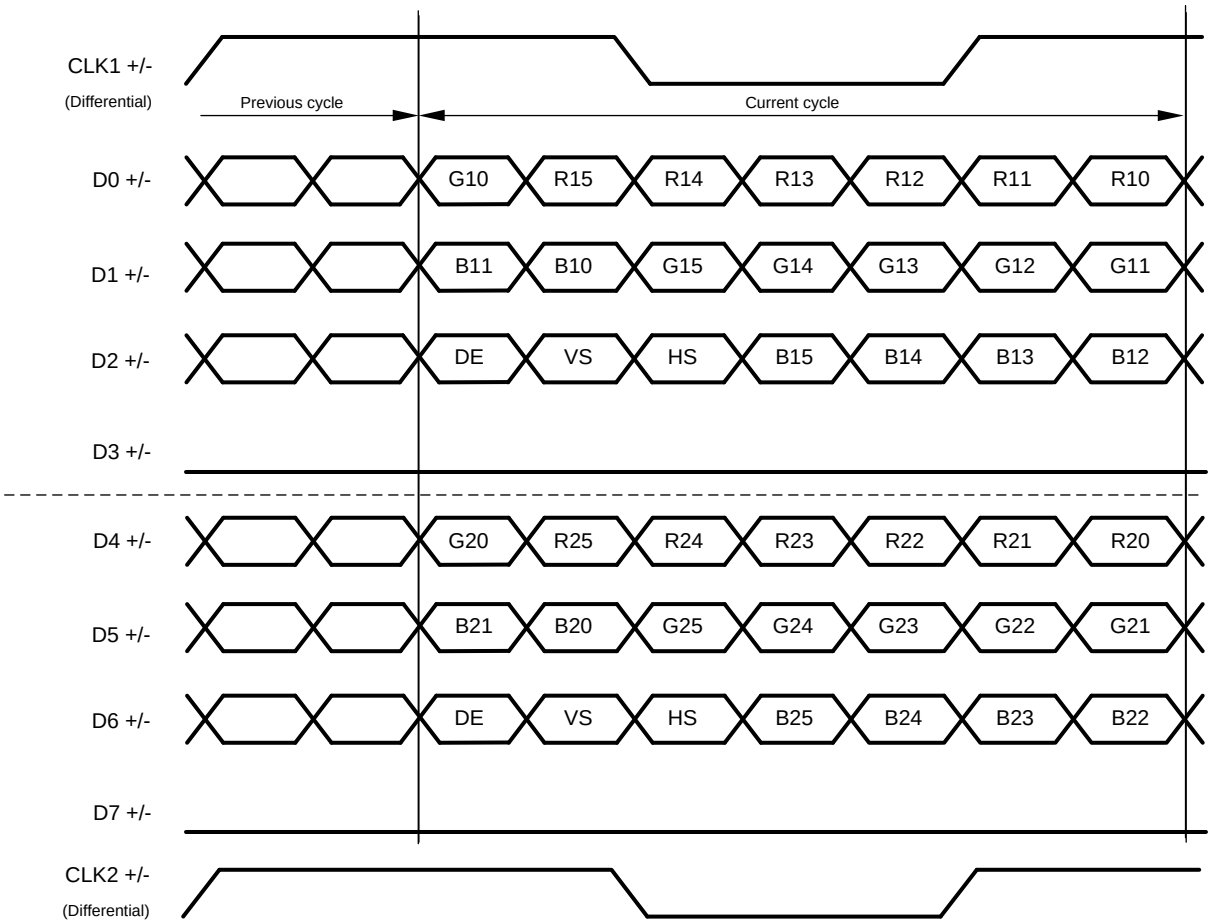

Figure 37. 18-bit Color Dual FPD-Link Mapping (MAPSEL=L)

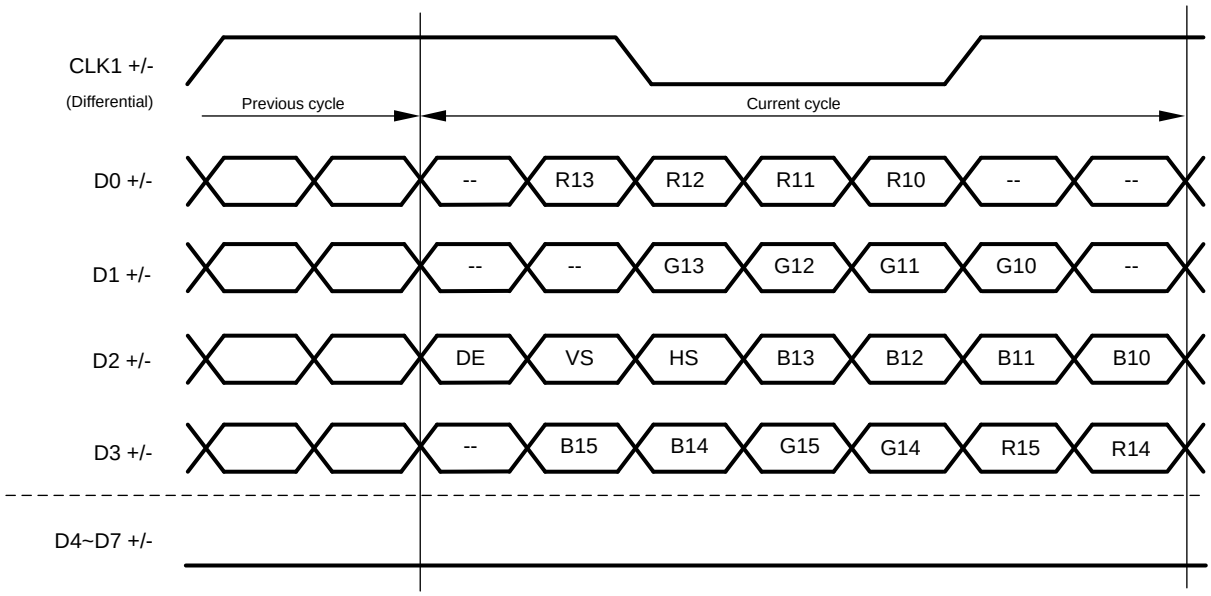

Figure 38. 18-bit Color Single FPD-Link Mapping (MAPSEL=H)

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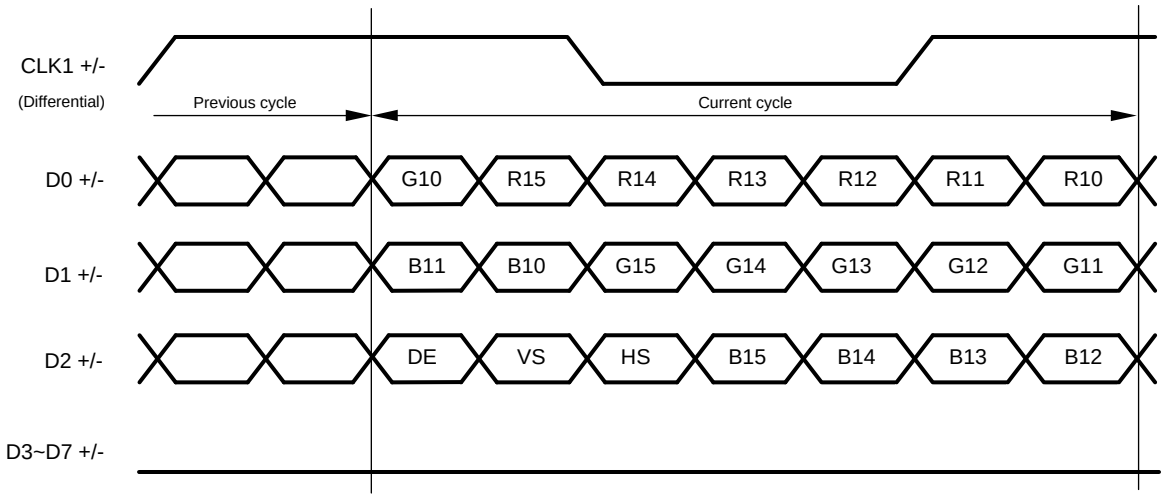

Figure 39. 18-bit Color Single FPD-Link Mapping (MAPSEL=L)

8.5 Programming

8.5.1 Serial Control Bus

The device may also be configured by the use of a I2C compatible serial control bus. Multiple devices may share the serial control bus (up to 8 device addresses supported). The device address is set via a resistor divider (R1 and R2 — see Figure 40 below) connected to the IDx pin.

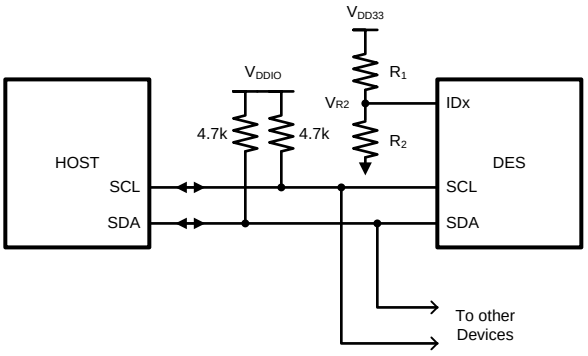

Figure 40. Serial Control Bus Connection

The serial control bus consists of two signals, SCL and SDA. SCL is a Serial Bus Clock Input. SDA is the Serial Bus Data Input / Output signal. Both SCL and SDA signals require an external pull-up resistor to 1.8V or 3.3V V_{DDIO}. For most applications, a 4.7kΩ pull-up resistor to V_{DD33} is recommended. However, the pull-up resistor value may be adjusted for capacitive loading and data rate requirements. The signals are either pulled High, or driven Low.

The IDx pin configures the control interface to one of 8 possible device addresses. A pull-up resistor and a pull-down resistor may be used to set the appropriate voltage ratio between the IDx input pin (V_{R2}) and V_{DD33}, each ratio corresponding to a specific device address. See Table 9 below.

Table 9. Serial Control Bus Addresses for IDx

#	Ideal Ratio V_{R2} / V_{DD33}	Ideal V_{R2} (V)	Suggested Resistor R1 kΩ (1% tol)	Suggested Resistor R2 kΩ (1% tol)	7-bit Address	8-bit Address
1	0	0	Open	40.2 or >10	0x2C	0x58
2	0.169	0.559	232	47.5	0x2E	0x5C
3	0.230	0.757	107	31.6	0x30	0x60
4	0.295	0.974	113	47.5	0x32	0x64
5	0.376	1.241	113	68.1	0x34	0x68
6	0.466	1.538	107	93.1	0x36	0x6C
7	0.556	1.835	90.9	113	0x38	0x70
8	0.801	2.642	45.3	182	0x3C	0x78

The Serial Bus protocol is controlled by START, START-Repeated, and STOP phases. A START occurs when SCL transitions Low while SDA is High. A STOP occurs when SDA transitions High while SCL is also HIGH. See Figure 41

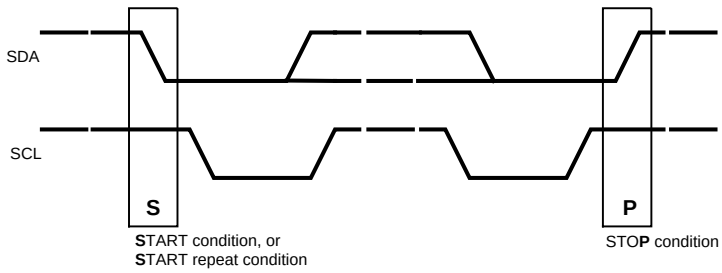

Figure 41. START and STOP Conditions

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To communicate with a remote device, the host controller (master) sends the slave address and listens for a response from the slave. This response is referred to as an acknowledge bit (ACK). If a slave on the bus is addressed correctly, it Acknowledges (ACKs) the master by driving the SDA bus low. If the address doesn't match a device's slave address, it Not-acknowledges (NACKs) the master by letting SDA be pulled High. ACKs also occur on the bus when data is being transmitted. When the master is writing data, the slave ACKs after every data byte is successfully received. When the master is reading data, the master ACKs after every data byte is received to let the slave know it wants to receive another data byte. When the master wants to stop reading, it NACKs after the last data byte and creates a stop condition on the bus. All communication on the bus begins with either a Start condition or a Repeated Start condition. All communication on the bus ends with a Stop condition. A READ is shown in Figure 42 and a WRITE is shown in Figure 43.

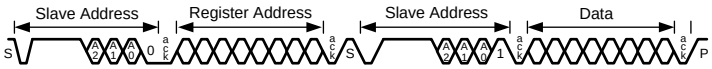

Figure 42. Serial Control Bus — READ

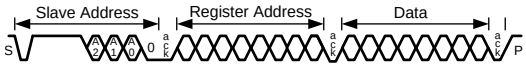

Figure 43. Serial Control Bus — WRITE

The I2C Master located at the Deserializer must support I2C clock stretching. For more information on I2C interface requirements and throughput considerations, please refer to TI Application Note SNLA131.

8.6 Register Maps

Table 10. Serial Control Bus Registers

ADD (hex)	Register Name	Bit(s)	Function	Type	Default Value (hex)	Description
0x00	I2C Device ID	7:1	DEVICE ID	RW	Strap	7-bit address of Deserializer; Defaults to the address configured by the IDx strap pin. See Table 9.
		0	DES ID	RW	0	0: Device ID is from IDx strap 1: Register I2C Device ID overrides IDx strap
0x01	Reset	7:2	RESERVED	RW	0	Reserved
		1	DIGITAL RESET0	RW	0	Digital Reset. Resets the entire digital block including registers. This bit is self-clearing. 1: Reset 0: Normal operation
		0	DIGITAL RESET1	RW	0	Digital Reset. Resets the entire digital block except registers. This bit is self-clearing. 1: Reset 0: Normal operation
0x02	General Configuration 0	7	OUTPUT ENABLE	RW	0	Output Enable Override Value (in conjunction with Output Sleep State Select) If the Override control is not set, the Output Enable will be set to 1.
		6	OUTPUT ENABLE OVERRIDE	RW	0	Overrides Output Enable and Output Sleep State default 0: Disable override 1: Enable override
		5	OSC CLOCK OUTPUT ENABLE (AUTO_CLOCK_EN)	RW	0	OSC clock output enable If loss of lock OSC clock is output onto PCLK. The frequency is selected in register 0x24. 1: Enable 0: Disable
		4	OUTPUT SLEEP STATE SELECT	RW	0	OSS Select Override value to control output state when LOCK is low (used in conjunction with Output Enable) If the Override control is not set, the Output Sleep State Select will be set to 1.
		3:0	RESERVED	RW	0	Reserved

Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (hex)	Register Name	Bit(s)	Function	Type	Default Value (hex)	Description
0x03	General Configuration 1	7	RESERVED	RW	1	Reserved
		6	BC CRC GENERATOR ENABLE	RW	1	Back Channel CRC Generator Enable 0: Enable 1: Disable (Default)
		5	FAILSAFE LOW	RW	1	Controls the pull direction for undriven LVCMOS inputs 1: Pull down 0: Pull up
		4	FILTER ENABLE	RW	1	HS,VS,DE two clock filter When enabled, pulses less than two full PCLK cycles on the DE, HS, and VS inputs will be rejected. 1: Filtering enable 0: Filtering disable
		3	I2C PASS-THROUGH	RW	0	I2C Pass-Through to Serializer if decode matches 0: Pass-Through Disabled 1: Pass-Through Enabled
		2	AUTO ACK	RW	0	Automatically Acknowledge I2C writes independent of the forward channel lock state 1: Enable 0: Disable
		1	DE GATE RGB	RW	0	Gate RGB data with DE signal. RGB data is gated with DE in order to allow packetized audio and block unencrypted data when paired with a serializer that supports HDCP. When paired with a serializer that does not support HDCP, RGB data is not gated with DE by default. However, to enable packetized autio this bit must be set. 1: Gate RGB data with DE (has no effect when paired with a serializer that supports HDCP) 0: Pass RGB data independent of DE (has no effect when paired with a serializer that does not support HDCP)
		0	RESERVED	RW	0	Reserved
0x04	BCC Watchdog Control	7:1	BCC WATCHDOG TIMER	RW	0x7F	The watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time. This field sets the Bidirectional Control Channel Watchdog Timeout value in units of 2 milliseconds. This field should not be set to 0.
		0	BCC WATCHDOG TIMER DISABLE	RW	0	Disable Bidirectional Control Channel Watchdog Timer 1: Disables BCC Watchdog Timer operation 0: Enables BCC Watchdog Timer operation
0x05	I2C Control 1	7	I2C PASS THROUGH ALL	RW	0	I2C Pass-Through All Transactions 0: Disabled 1: Enabled
		6:4	I2C SDA HOLD		0x1	Internal SDA Hold Time This field configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 50 nanoseconds.
		3:0	I2C FILTER DEPTH		0xE	I2C Glitch Filter Depth This field configures the maximum width of glitch pulses on the SCL and SDA inputs that will be rejected. Units are 5 nanoseconds.

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (hex)	Register Name	Bit(s)	Function	Type	Default Value (hex)	Description
0x06	I2C Control 2	7	FORWARD CHANNEL SEQUENCE ERROR	R	0	Control Channel Sequence Error Detected This bit indicates a sequence error has been detected in forward control channel. If this bit is set, an error may have occurred in the control channel operation.
		6	CLEAR SEQUENCE ERROR	RW	0	Clears the Sequence Error Detect bit
		5	RESERVED	R	0	Reserved.
		4:3	SDA Output Delay	RW	0	SDA Output Delay This field configures output delay on the SDA output. Setting this value will increase output delay in units of 50ns. Nominal output delay values for SCL to SDA are: 00 : 250ns 01: 300ns 10: 350ns 11: 400ns
		2	LOCAL WRITE DISABLE	RW	0	Disable Remote Writes to Local Registers Setting this bit to a 1 will prevent remote writes to local device registers from across the control channel. This prevents writes to the Deserializer registers from an I2C master attached to the Serializer. Setting this bit does not affect remote access to I2C slaves at the Deserializer.
		1	I2C BUS TIMER SPEEDUP	RW	0	Speed up I2C Bus Watchdog Timer 1: Watchdog Timer expires after approximately 50 microseconds 0: Watchdog Timer expires after approximately 1 second.
		0	I2C BUS TIMER DISABLE	RW	0	Disable I2C Bus Watchdog Timer When the I2C Watchdog Timer may be used to detect when the I2C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signalling occurs for approximately 1 second, the I2C bus will assumed to be free. If SDA is low and no signaling occurs, the device will attempt to clear the bus by driving 9 clocks on SCL
0x07	REMOTE ID	7:1	REMOTE ID	RW	0x00	7-bit Serializer Device ID Configures the I2C Slave ID of the remote Serializer. A value of 0 in this field disables I2C access to the remote Serializer. This field is automatically loaded from the Serializer once RX Lock has been detected. Software may overwrite this value, but should also assert the FREEZE DEVICE ID bit to prevent loading by the Bidirectional Control Channel.
		0	FREEZE DEVICE ID	RW	0	Freeze Serializer Device ID Prevent auto-loading of the Serializer Device ID from the Forward Channel. The ID will be frozen at the value written.
0x08	SlaveID[0]	7:1	SLAVE ID0	RW	0	7-bit Remote Slave Device ID 0 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID0, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
		0	RESERVED	R/W	0	Reserved.
0x09	SlaveID[1]	7:01	SLAVE ID1	RW	0	7-bit Remote Slave Device ID 1 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID1, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
		0	RESERVED	R/W	0	Reserved.

Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (hex)	Register Name	Bit(s)	Function	Type	Default Value (hex)	Description
0x0A	SlaveID[2]	7:1	SLAVE ID2	RW	0	7-bit Remote Slave Device ID 2 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID2, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
		0	RESERVED	R/W	0	Reserved.
0x0B	SlaveID[3]	7:1	SLAVE ID3	RW	0	7-bit Remote Slave Device ID 3 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID3, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
		0	RESERVED	R/W	0	Reserved.
0x0C	SlaveID[4]	7:1	SLAVE ID4	RW	0	7-bit Remote Slave Device ID 4 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID4, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
		0	RESERVED	R/W	0	Reserved.
0x0D	SlaveID[5]	7:1	SLAVE ID5	RW	0	7-bit Remote Slave Device ID 5 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID5, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
		0	RESERVED	R/W	0	Reserved.
0x0E	SlaveID[6]	7:1	SLAVE ID6	RW	0	7-bit Remote Slave Device ID 6 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID6, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
		0	RESERVED	R/W	0	Reserved.
0x0F	SlaveID[7]	7:1	SLAVE ID7	RW	0	7-bit Remote Slave Device ID 7 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID7, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
		0	RESERVED	R/W	0	Reserved.
0x10	SlaveAlias[0]	7:1	SLAVE ALIAS ID0	RW	0	7-bit Remote Slave Device Alias ID 0 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID0 register. A value of 0 in this field disables access to the remote I2C Slave.
		0	RESERVED		0	Reserved.
0x11	SlaveAlias[1]	7:1	SLAVE ALIAS ID1	RW	0	7-bit Remote Slave Device Alias ID 1 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID1 register. A value of 0 in this field disables access to the remote I2C Slave.
		0	RESERVED		0	Reserved.

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (hex)	Register Name	Bit(s)	Function	Type	Default Value (hex)	Description
0x12	SlaveAlias[2]	7:1	SLAVE ALIAS ID2	RW	0	7-bit Remote Slave Device Alias ID 2 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID2 register. A value of 0 in this field disables access to the remote I2C Slave.
		0	RESERVED		0	Reserved.
0x13	SlaveAlias[3]	7:1	SLAVE ALIAS ID3	RW	0	7-bit Remote Slave Device Alias ID 3 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID3 register. A value of 0 in this field disables access to the remote I2C Slave.
		0	RESERVED		0	Reserved.
0x14	SlaveAlias[4]	7:1	SLAVE ALIAS ID4	RW	0	7-bit Remote Slave Device Alias ID 4 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID4 register. A value of 0 in this field disables access to the remote I2C Slave.
		0	RESERVED		0	Reserved.
0x15	SlaveAlias[5]	7:1	SLAVE ALIAS ID5	RW	0	7-bit Remote Slave Device Alias ID 5 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID5 register. A value of 0 in this field disables access to the remote I2C Slave.
		0	RESERVED		0	Reserved
0x16	SlaveAlias[6]	7:1	SLAVE ALIAS ID6	RW	0	7-bit Remote Slave Device Alias ID 6 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID6 register. A value of 0 in this field disables access to the remote I2C Slave.
		0	RESERVED		0	Reserved.
0x17	SlaveAlias[7]	7:1	SLAVE ALIAS ID7	RW	0	7-bit Remote Slave Device Alias ID 7 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID7 register. A value of 0 in this field disables access to the remote I2C Slave.
		0	RESERVED		0	Reserved.
0x18	MAILBOX_18	7:0	MAILBOX_18	RW	0	Mailbox Register This register is an unused read/write register that can be used for any purpose such as passing messages between I2C masters on opposite ends of the link.
0x19	MAILBOX_19	7:0	MAILBOX_19	RW	0x01	Mailbox Register This register is an unused read/write register that can be used for any purpose such as passing messages between I2C masters on opposite ends of the link.

Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (hex)	Register Name	Bit(s)	Function	Type	Default Value (hex)	Description
0x1A	GPIO[9] and Global GPIO Config	7	GLOBAL GPIO OUTPUT VALUE	RW	0	Global GPIO Output Value This value is output on each GPIO pin when the individual pin is not otherwise enabled as a GPIO and the global GPIO direction is Output
		6	RESERVED	RW	0	Reserved
		5	GLOBAL GPIO FORCE DIR	RW	0	The GLOBAL GPIO DIR and GLOBAL GPIO EN bits configure the pad in input direction or output direction for functional mode or GPIO mode. The GLOBAL bits are overridden by the individual GPIO DIR and GPIO EN bits. {GLOBAL GPIO DIR, GLOBAL GPIO EN} 00: Functional mode; output 10: Tri-state 01: Force mode; output 11: Force mode; input
		4	GLOBAL GPIO FORCE EN	RW	0	
		3	GPIO9 OUTPUT VALUE	RW	0	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
		2	RESERVED	RW	0	Reserved
		1	GPIO9 DIR	RW	0	The GPIO DIR and GPIO EN bits configure the pad in input direction or output direction for functional mode or GPIO mode. {GPIO DIR, GPIO EN} 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input
		0	GPIO9 EN	RW	0	
0x1B	Frequency Counter	7:0	Frequency Count	RW	0	Frequency Counter control A write to this register will enable a frequency counter to count the number of pixel clock during a specified time interval. The time interval is equal to the value written multiplied by the oscillator clock period (nominally 50ns). A read of the register returns the number of pixel clock edges seen during the enabled interval. The frequency counter will freeze at 0xff if it reaches the maximum value. The frequency counter will provide a rough estimate of the pixel clock period. If the pixel clock frequency is known, the frequency counter may be used to determine the actual oscillator clock frequency.

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (hex)	Register Name	Bit(s)	Function	Type	Default Value (hex)	Description
0x1C	General Status	7:6	RESERVED	R	0	Reserved.
		5	DUAL_TX_STS	R	0	Transmitter Dual Link Status: This bit indicates the current operating mode of the FPD-Link Transmit port 1: Dual Link mode active 0: Single Link mode active
		4	DUAL_RX_STS	R	0	Receiver Dual Link Status: This bit indicates the current operating mode of the FPD-Link III Receive port 1: 2-lane mode active 0: 1-lane mode active
		3	I2S LOCKED	R	0	I2S LOCK STATUS 0: I2S PLL controller not locked 1: I2S PLL controller locked to input I2S clock
		2	RESERVED	R	0	Reserved.
		1	SIGNAL DETECT	R	0	1: Serial input detected 0: Serial input not detected
		0	LOCK	R	0	De-Serializer CDR, PLL's clock to recovered clock frequency 1: De-Serializer locked to recovered clock 0: De-Serializer not locked In Dual Link mode, this indicates both channels are locked.
0x1D	GPIO0 Config					GPIO0 and D_GPIO0 Configuration If PORT1_SEL is set, this register controls the D_GPIO0 pin
		7:4	RESERVED	R	0x1	Reserved.
		3	GPIO0 OUTPUT VALUE D_GPIO0 OUTPUT VALUE	RW	0	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
		2	GPIO0 REMOTE ENABLE D_GPIO0 REMOTE ENABLE	RW	0	Remote GPIO Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Serializer. 0: Disable GPIO control from remote Serializer.
		1	GPIO0 DIR D_GPIO0 DIR	RW	0	The GPIO DIR and GPIO EN configures the pad in input direction or output direction for functional mode or GPIO mode. {GPIO DIR, GPIO EN} 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input
		0	GPIO0 EN D_GPIO0 EN	RW	0	

Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (hex)	Register Name	Bit(s)	Function	Type	Default Value (hex)	Description
0x1E	GPIO1_2 Config					GPIO1/GPIO2 and D_GPIO1/D_GPIO2 Configuration If PORT1_SEL is set, this register controls the D_GPIO1 and D_GPIO2 pins
		7	GPIO2 OUTPUT VALUE D_GPIO2 OUTPUT VALUE	RW	0	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
		6	GPIO2 REMOTE ENABLE D_GPIO2 REMOTE ENABLE	RW	0	Remote GPIO Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Serializer. 0: Disable GPIO control from remote Serializer.
		5	GPIO2 DIR D_GPIO2 DIR	RW	0	The GPIO DIR and GPIO EN configures the pad in input direction or output direction for functional mode or GPIO mode. {GPIO DIR, GPIO EN} 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input
		4	GPIO2 EN D_GPIO2 EN	RW	0	
		3	GPIO1 OUTPUT VALUE D_GPIO1 OUTPUT VALUE	RW	0	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
		2	GPIO1 REMOTE ENABLE D_GPIO1 REMOTE ENABLE	RW	0	Remote GPIO Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Serializer. 0: Disable GPIO control from remote Serializer.
		1	GPIO1 DIR D_GPIO1 DIR	RW	0	The GPIO DIR and GPIO EN configures the pad in input direction or output direction for functional mode or GPIO mode. {GPIO DIR, GPIO EN} 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input
		0	GPIO1 EN D_GPIO1 EN	RW	0	
0x1F	GPIO3 Config					GPIO3 and D_GPIO3 Configuration If PORT1_SEL is set, this register controls the D_GPIO3 pin
		7:4	RESERVED	RW	0	Reserved (No GPIO 4)
		3	GPIO3 OUTPUT VALUE D_GPIO3 OUTPUT VALUE	RW	0	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
		2	GPIO3 REMOTE ENABLE D_GPIO3 REMOTE ENABLE	RW	0	Remote GPIO Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Serializer. 0: Disable GPIO control from remote Serializer.
		1	GPIO3 DIR D_GPIO3 DIR	RW	0	The GPIO DIR and GPIO EN configures the pad in input direction or output direction for functional mode or GPIO mode. {GPIO DIR, GPIO EN} 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input
		0	GPIO3 EN D_GPIO3 EN	RW	0	

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (hex)	Register Name	Bit(s)	Function	Type	Default Value (hex)	Description
0x20	GPIO5_6 Config	7	GPIO6 OUTPUT VALUE	RW	0	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
		6	GPIO6 REMOTE ENABLE	RW	0	Remote GPIO Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Serializer. 0: Disable GPIO control from remote Serializer.
		5	GPIO6 DIR	RW	0	The GPIO DIR and GPIO EN configures the pad in input direction or output direction for functional mode or GPIO mode. {GPIO DIR, GPIO EN} 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input
		4	GPIO6 EN	RW	0	
		3	GPIO5 OUTPUT VALUE	RW	0	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
		2	GPIO5 REMOTE ENABLE	RW	0	Remote GPIO Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Serializer. 0: Disable GPIO control from remote Serializer.
		1	GPIO5 DIR	RW	0	The GPIO DIR and GPIO EN configures the pad in input direction or output direction for functional mode or GPIO mode. {GPIO DIR, GPIO EN} 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input
		0	GPIO5 EN	RW	0	

Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (hex)	Register Name	Bit(s)	Function	Type	Default Value (hex)	Description
0x21	GPIO7_8 Config	7	GPIO8 OUTPUT VALUE	RW	0	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
		6	GPIO8 REMOTE ENABLE	RW	0	Remote GPIO Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Serializer. 0: Disable GPIO control from remote Serializer.
		5	GPIO8 DIR	RW	0	The GPIO DIR and GPIO EN configures the pad in input direction or output direction for functional mode or GPIO mode. {GPIO DIR, GPIO EN} 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input
		4	GPIO8 EN	RW	0	
		3	GPIO7 OUTPUT VALUE	RW	0	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
		2	GPIO7 REMOTE ENABLE	RW	0	Remote GPIO Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Serializer. 0: Disable GPIO control from remote Serializer.
		1	GPIO7 DIR	RW	0	The GPIO DIR and GPIO EN configures the pad in input direction or output direction for functional mode or GPIO mode. {GPIO DIR, GPIO EN} 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input
		0	GPIO7 EN	RW	0	

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (hex)	Register Name	Bit(s)	Function	Type	Default Value (hex)	Description
0x22	Datapath Control	7	OVERRIDE FC CONFIG	RW	0	1: Disable loading of this register from the forward channel, keeping locally written values intact 0: Allow forward channel loading of this register
		6	PASS RGB	RW	0	Setting this bit causes RGB data to be sent independent of DE. This allows operation in systems which may not use DE to frame video data or send other data when DE is deasserted. Note that this bit prevents HDCP operation and blocks packetized audio. This bit has no effect when paired with a serializer that does not support HDCP. 1: Pass RGB independent of DE 0: Normal operation Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.
		5	DE POLARITY	RW	0	This bit indicates the polarity of the DE (Data Enable) signal. 1: DE is inverted (active low, idle high) 0: DE is positive (active high, idle low) Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.
		4	I2S_RPTR_REG EN	RW	0	Regenerate I2S Data from Repeater I2S pins. 1: Don't output packetized audio data on RGB video output pins 0: Output packetized audio on RGB video output pins (Default). Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.
		3	I2S 4-CHANNEL ENABLE OVERRIDE	RW	0	1: Set I2S 4-Channel Enable from bit of of this register 0: Set I2S 4-Channel disabled Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.
		2	18-BIT VIDEO SELECT	RW	0	1: Select 18-bit video mode 0: Select 24-bit video mode Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.
		1	I2S TRANSPORT SELECT	RW	0	1: Enable I2S In-Band Transport 0: Enable I2S Data Island Transport Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.
		0	I2S 4-CHANNEL ENABLE	RW	0	I2S 4-Channel Enable 1: Enable I2S 4-Channel 0: Disable I2S 4-Channel Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.

Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (hex)	Register Name	Bit(s)	Function	Type	Default Value (hex)	Description
0x23	RX Mode Status	7	RESERVED	RW	0	Reserved
		6	BC FREQ SELECT	RW	0	Back Channel Frequency Select 0: Divide-by-4 frequency based on the internal oscillator 1: Divide-by-2 frequency based on the internal oscillator This bit will be ignored if BC_HIGH_SPEED is set to a 1. Note that changing this setting will result in some errors on the back channel for a short period of time. If set over the control channel, the Serializer should first be programmed to Auto-Ack operation (Serializer register 0x03, bit 5) to avoid a control channel timeout due to lack of response from the Deserializer.
		5	AUTO_I2S	RW	1	Auto I2S Determine I2S mode from the AUX data codes.
		4	BC_HS_CTL	RW	0	Back-Channel High-Speed control Enables high-speed back-channel at 20Mbps. This bit will override the BC_FREQ_SELECT setting. Note that changing this setting will result in some errors on the back channel for a short period of time. If set over the control channel, the Serializer should first be programmed to Auto-Ack operation (Serializer register 0x03, bit 5) to avoid a control channel timeout due to lack of response from the Deserializer. BC_HIGH_SPEED is loaded from the MODE_SEL1 pin strap options.
		3	COAX_MODE	RW	0	Coax Mode Configures the FPD3 Receiver for operation over Coax or STP cabling: 0 : Shielded Twisted pair (STP) 1 : Coax Coax Mode is loaded from the MODE_SEL1 pin strap options.
		2	REPEATER_MODE	RW	0	Repeater Mode Indicates device is strapped to repeater mode. Repeater Mode is loaded from the MODE_SEL1 pin strap options.
		1	RESERVED	RW	0	Reserved
		0	RESERVED	RW	0	Reserved
0x24	BIST Control	7:6	BIST_OUT_MODE	RW	0	BIST Output Mode 00 : No toggling 01 : Alternating 1/0 toggling 1x : Toggle based on BIST data
		5:4	AUTO_OSC_FREQ	RW	0	When register 0x02 bit 5 (AUTO)CLOCK_EN) is set, this field controls the nominal frequency of the oscillator-based receive clock. 00: 50 MHz 01: 25 MHz 10: 10 MHz 11: Reserved
		3	BIST PIN CONFIG	RW	1	Bist Configured through Pin. 1: Bist configured through pin. 0: Bist configured through bit 0 in this register
		2:1	BIST CLOCK SOURCE	RW	0	BIST Clock Source 00: External Pixel Clock 01: 33 MHz Oscillator 1x: 33 MHz Oscillator
		0	BIST_EN	RW	0	BIST Control 1: Enabled 0: Disabled

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (hex)	Register Name	Bit(s)	Function	Type	Default Value (hex)	Description
0x25	BIST ERROR COUNT	7:0	BIST ERROR COUNT	R	0	Bist Error Count Returns BIST error count for selected port. Port selected is based on the PORT_SEL control in the DUAL_RX_CTL register 0x34 [1:0].
0x26	SCL High Time	7:0	SCL HIGH TIME	RW	0x83	I2C Master SCL High Time This field configures the high pulse width of the SCL output when the De-Serializer is the Master on the local I2C bus. Units are 50 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL high time with the internal oscillator clock running at 26MHz rather than the nominal 20MHz.
0x27	SCL Low Time	7:0	SCL LOW TIME	RW	0x84	I2C SCL Low Time This field configures the low pulse width of the SCL output when the De-Serializer is the Master on the local I2C bus. This value is also used as the SDA setup time by the I2C Slave for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 50 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL low time with the internal oscillator clock running at 26MHz rather than the nominal 20MHz.
0x28	Datapath Control 2	7	OVERRIDE FC CONFIG	RW	0	1: Disable loading of this register from the forward channel, keeping locally witten values intact 0: Allow forward channel loading of this register
		6	RESERVED	RW	0	Reserved
		5	VIDEO_DISABLED	RW	0	Forward channel video disabled 0 : Normal operation 1 : Video is disabled, control channel is enabled This is a status bit only, indicating the forward channel is not sending active video. In this mode, the control channel and GPIO functions are enabled. Setting OVERRIDE_FC_CONFIG will prevent this bit from changing.
		4	DUAL_LINK	R		1: Dual Link mode enabled 0: Single Link mode enabled This bit will always be loaded from forward channel and cannot be written locally. To force DUAL_LINK receive mode, use the RX_PORT_SEL register (address 0x34)
		3	ALTERNATE I2S ENABLE	RW	0	1: Enable alternate I2S output on GPIO1 (word clock) and GPIO0 (data) 0: Normal Operation
		2	I2S DISABLED	RW	0	1: I2S DISABLED 0: Normal Operation
		1	28BIT VIDEO	RW	0	1: 28 bit Video enable. i.e. HS, VS, DE are present in forward channel. 0: Normal Operation
		0	I2S SURROUND	RW	0	1: I2S Surround enabled 0: I2S Surround disabled

Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (hex)	Register Name	Bit(s)	Function	Type	Default Value (hex)	Description
0x29	FRC Control	7	Timing Mode Select	RW	0	Select display timing mode 0: DE only Mode 1: Sync Mode (VS,HS)
		6	HS Polarity	RW	0	0: Active High 1: Active Low
		5	VS Polarity	RW	0	0: Active High 1: Active Low
		4	DE Polarity	RW	0	0: Active High 1: Active Low
		3	FRC2 Enable	RW	0	0: FRC2 disable 1: FRC2 enable
		2	FRC1 Enable	RW	0	0: FRC1 disable 1: FRC1 enable
		1	Hi-FRC2 Disable	RW	0	0: Hi-FRC2 enable 1: Hi-FRC2 disable
		0	Hi-FRC1 Disable	RW	0	0: Hi-FRC1 enable 1: Hi-FRC1 disable
0x2A	White Balance Control	7:6	Page Setting	RW	0	Page setting 00: Configuration Registers 01: Red LUT 10: Green LUT 11: Blue LUT
		5	White Balance Enable	RW	0	0: White Balance Disable 1: White Balance Enable
		4	LUT Reload Enable	RW	0	0: Reload Disable 1: Reload Enable
		3:0	RESERVED	RW	0	Reserved
0x2B	I2S Control	7:4	RESERVED	RW	0	Reserved
		3	I2S FIFO OVERRUN STATUS	R	0	I2S FIFO Overrun Status
		2	I2S FIFO UNDERRUN STATUS	R	0	I2S FIFO Underrun Status
		1	I2S FIFO ERROR RESET	RW	0	I2S Fifo Error Reset 1: Clears FIFO Error
		0	I2S DATA FALLING EDGE	RW	0	I2S Clock Edge Select 1: I2S Data is strobed on the Rising Clock Edge. 0: I2S Data is strobed on the Falling Clock Edge.
0x2E	PCLK Test Mode	7	EXTERNAL PCLK	RW	0	Select pixel clock from BISTC input
		6:0	RESERVED	RW	0	Reserved

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (hex)	Register Name	Bit(s)	Function	Type	Default Value (hex)	Description
0x34	DUAL_RX_CTL	7	RESERVED	R	0	Reserved
		6	RX_LOCK_MODE	RW	0	RX Lock Mode: Determines operating conditions for indication of RX_LOCK and generation of video data. 0 : RX_LOCK asserted only when receiving active video (Forward channel VIDEO_DISABLED bit is 0) 1 : RX_LOCK asserted when device is linked to a Serializer even if active video is not being sent. This allows indication of valid link where Bidirectional Control Channel is enabled, but Deserializer is not receiving Audio/Video data.
		5	RAW_2ND_BC	RW	0	Enable Raw Secondary Back channel If this bit is set to a 1, the secondary back channel will operate in a raw mode, passing D_GPIO0 from the Deserializer to the Serializer, without any oversampling or filtering.
		4:3	FPD3 INPUT MODE	RW	0	FPD-Link III Input Mode Determines operating mode of FPD-Link III Receive interface 00: Auto-detect based on received data 01: Forced Mode: 2-lane 10: Forced Mode: 1-lane, primary input 11: Forced Mode: 1-lane, secondary input
		2	RESERVED	RW	0	Reserved
		1	PORT1_SEL	RW	0	Selects Port 1 for Register Access from primary I2C Address For writes, port1 registers and shared registers will both be written. For reads, port1 registers and shared registers will be read. This bit must be cleared to read port0 registers.
		0	PORT0_SEL	RW	1	Selects Port 0 for Register Access from primary I2C Address For writes, port0 registers and shared registers will both be written. For writes, port0 registers and shared registers will both be written.
0x35	AEQ TEST					AEQ Test register If PORT1_SEL is set, this register sets port1 AEQ controls
		7	RESERVED	RO	0	Reserved
		6	AEQ_RESTART	RW	0	Set high to restart AEQ adaptation from initial value. Method is write HIGH then write LOW - not self clearing. Adaption will be restarted on both ports.
		5	OVERRIDE_AEQ_FLOOR	RW	0	Enable operation of SET_AEQ_FLOOR
		4	SET_AEQ_FLOOR	RW	0	AEQ adaptation starts from a pre-set floor value rather than from zero - recommended for long cable situations
		3:0	RESERVED	RW	0x0	Reserved
0x37	MODE_SEL	7	MODE1_DONE	RW	0	MODE_SEL1 Done: If set, indicates the MODE_SEL1 decode has completed and latched into the MODE_SEL1 status bits.
		6:4	MODE_SEL1	RW	0	MODE_SEL1 Decode 3-bit decode from MODE_SEL1 pin
		3	MODE0_DONE	RW	0	MODE_SEL0 Done: If set, indicates the MODE_SEL0 decode has completed and latched into the MODE_SEL0 status bits.
		2:0	MODE_SEL0	RW	0	MODE_SEL0 Decode 3-bit decode from MODE_SEL0 pin

Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (hex)	Register Name	Bit(s)	Function	Type	Default Value (hex)	Description
0x3A	I2S_DIVSEL	7	reg_ov_mdiv	RW	0x0	0: No override for MCLK divider 1: Override divider select for MCLK
		6:4	reg_mdiv	RW	0x0	Divide ratio select for VCO output (32*REF/M) 000: Divide by 32 (=REF/M) 001: Divide by 16 (=2*REF/M) 010: Divide by 8 (=4*REF/M) 011: Divide by 4 (=8*REF/M) 100: Reserved 101: Divide by 2 (=16*REF/M) 110: Reserved 111: Divide by 1 (32*REF/M)
		3	RESERVED	R	0x0	
		2	reg_ov_mselect	RW	0x0	0: Divide ratio of reference clock VCO selected by PLL-SM 1: Override divide ratio of clock to VCO
		1:0	reg_mselect	RW	0x0	Divide ratio select for VCO input (M) 00: Divide by 1 01: Divide by 2 10: Divide by 4 11: Divide by 8
0x41	LINK ERROR COUNT	7:5	RESERVED	RW	0	Reserved
		4	LINK ERROR COUNT ENABLE	RW	0	Enable serial link data integrity error count 1: Enable error count 0: DISABLE
		3:0	LINK ERROR COUNT	RW	0x3	Link error count threshold. Counter is pixel clock based. clk0, clk1 and DCA are monitored for link errors, if error count is enabled, deserializer loose lock once error count reaches threshold. If disabled deserilizer loose lock with one error.
0x43	HSCC_CONTROL	7:5	RESERVED	RW	0	Reserved
		4	SPI_MISO_MODE	RW	0	SPI MISO pin mode during Reverse SPI mode During Reverse SPI mode, SPI_MISO is typically an output signal. For bused SPI applications, it may be necessary to tri-state the SPI_MISO output if the device is not selected (SPI_SS = 0). 0 : Always enable SPI_MISO output driver 1 : Tri-state SPI_MISO output if SPI_SS is not asserted (low)
		3	SPI_CPOL	RW	0	SPI Clock Polarity Control 0 : SPI Data driven on Falling clock edge, sampled on Rising clock edge 1 : SPI Data driven on Rising clock edge, sampled on Falling clock edge
		2:0	HSCC_MODE	RW	0	High-Speed Control Channel Mode Enables high-speed modes for the secondary link back-channel, allowing higher speed signaling of GPIOs or SPI interface: These bits indicates the High Speed Control Channel mode of operation: 000: Normal frame, GPIO mode 001: High Speed GPIO mode, 1 GPIO 010: High Speed GPIO mode, 2 GPIOs 011: High Speed GPIO mode: 4 GPIOs 100: Reserved 101: Reserved 110: High Speed, Forward Channel SPI mode 111: High Speed, Reverse Channel SPI mode

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (hex)	Register Name	Bit(s)	Function	Type	Default Value (hex)	Description
0x44	ADAPTIVE EQ BYPASS					Adaptive Equalizer Bypass register If PORT1_SEL is set, this register sets port1 AEQ controls
		7:5	EQ STAGE 1 SELECT VALUE	RW	0x3	EQ select value[5:3] - Used if adaptive EQ is bypassed.
		4	RESERVED	RW	0	Reserved
		3:1	EQ STAGE 2 SELECT VALUE	RW	0	EQ select value [2:0] - Used if adaptive EQ is bypassed.
		0	ADAPTIVE EQ BYPASS	RW	0	1: Disable adaptive EQ 0: Enable adaptive EQ
0x45	ADAPTIVE EQ MIN MAX					Adaptive Equalizer Configuration If PORT1_SEL is set, this register sets port1 AEQ configuration
		7:4	RESERVED	RW	0	Reserved
		3:0	ADAPTIVE EQ FLOOR VALUE	RW	0x8	When AEQ floor is enabled by mode-sel pin or register {reg_35[5:4]} the starting setting is given by this register.
0x49	FPD_TX_MODE	7	MAPSEL MODE	R	Strap	Mapsel Pin Status Strap option on the MODE_SEL0 pin
		6	MAPSEL OVER WRITE	RW	0	Mapsel Over Write enable from register configuration
		5	MAPSEL REG BIT	RW	0	Register setting of MAPSEL mode if MAPSEL OVER WRITE is set
		4:2	RESERVED	R	0	Reserved
		1:0	FPD_OUT_MODE	R/W	Strap	FPD/OLDI output mode Controls single/dual operation of the FPD Transmit ports 00 : Dual FPD/OLDI output 01 : Dual SWAP FPD/OLDI output 10 : Single FPD/OLDI output 11 : Replicate FPD/OLDI output The FPD_OUT_MODE register bits are loaded at reset from the MODE_SEL0 pin strap options.
0x4B	LVDS CONTROL	7:2	RESERVED	RW	0x02	Reserved
		1:0	LVDS VOD CONTROL	RW	0	FPD/OLDI Output VOD Setting 00: Setting 1 - 190mV typical voltage swing (single-ended) 01: Setting 2 - 275mV typical voltage swing (single-ended) 10: Setting 3 - 325mV typical voltage swing (single-ended) 11: Setting 4 - 375mV typical voltage swing (single-ended)
0x52	CML OUTPUT CTL1	7	CML CHANNEL SELECT 1	RW	0	Selects between PORT0 and PORT1 to output onto CMLOUT±. 0: Recovered forward channel data from RIN0± is output on CMLOUT± 1: Recovered forward channel data from RIN1± is output on CMLOUT± CMLOUT driver must be enabled by setting 0x56[3] = 1. Note: This bit must match 0x57[2:1] setting for PORT0 or PORT1.
		6:0	RESERVED	RW	0	Reserved
0x56	CML OUTPUT ENABLE	7:4	RESERVED	RW	0	Reserved
		3	CMLOUT ENABLE	RW	0	Enable CMLOUT± Loop-through Driver 0: Disabled (Default) 1: Enabled
		2:0	RESERVED	RW	0	Reserved

Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (hex)	Register Name	Bit(s)	Function	Type	Default Value (hex)	Description
0x57	CML OUTPUT CTL2	7:3	RESERVED	RW	0	Reserved
		2:1	CML CHANNEL SELECT 2	RW	0	Selects between PORT0 and PORT1 to output onto CMLOUT±. 01: Recovered forward channel data from RIN0± is output on CMLOUT± 10: Recovered forward channel data from RIN1± is output on CMLOUT± CMLOUT driver must be enabled by setting 0x56[3] = 1. Note: This must match 0x52[7] setting for PORT0 or PORT1.
		0	RESERVED	RW	0	Reserved
0x64	PGCTL	7:4	PATGEN_SEL	RW	1	Fixed Pattern Select This field selects the pattern to output when in Fixed Pattern Mode. Scaled patterns are evenly distributed across the horizontal or vertical active regions. This field is ignored when Auto-Scrolling Mode is enabled. The following table shows the color selections in non-inverted followed by inverted color mode: 0000: Reserved 0001: White/Black 0010: Black/White 0011: Red/Cyan 0100: Green/Magenta 0101: Blue/Yellow 0110: Horizontally Scaled Black to White/White to Black 0111: Horizontally Scaled Black to Red/White to Cyan 1000: Horizontally Scaled Black to Green/White to Magenta 1001: Horizontally Scaled Black to Blue/White to Yellow 1010: Vertically Scaled Black to White/White to Black 1011: Vertically Scaled Black to Red/White to Cyan 1100: Vertically Scaled Black to Green/White to Magenta 1101: Vertically Scaled Black to Blue/White to Yellow 1110: Custom color (or its inversion) configured in PGRS, PGGS, PGBS registers 1111: Reserved See TI App Note AN-2198
		3	PATGEN_UNH	RW	0	Enables the UNH-IOL compliance test pattern: 0: Pattern type selected by PATGEN_SEL 1: Compliance test pattern is selected. Value of PATGEN_SEL is ignored.
		2	PATGEN_COLOR	RW	0	Enable Color Bars Pattern 0: Color Bars disabled (default) 1: Color bars enabled Overides the selection from bits [7:4]
		1	PATGEN_VCOM_REV	RW	0	Reverse the order of color bands in VCOM pattern 0: Color sequence from top left is (YCBR) (default) 1: Color sequence from top left is (RBCY)
		0	PATGEN_EN	RW	0	Pattern Generator Enable: 1: Enable Pattern Generator 0: Disable Pattern Generator

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (hex)	Register Name	Bit(s)	Function	Type	Default Value (hex)	Description
0x65	PGCFG	7:5	RESERVED	R	0	Reserved
		4	PATGEN_18B	RW	0	18-bit Mode Select: 1: Enable 18-bit color pattern generation. Scaled patterns will have 64 levels of brightness and the R, G, and B outputs use the six most significant color bits. 0: Enable 24-bit pattern generation. Scaled patterns use 256 levels of brightness. This bit has no effect in external timing mode (PATGEN_TSEL = 0).
		2	PATGEN_TSEL	RW	0	Timing Select Control: 1: The Pattern Generator creates its own video timing as configured in the Pattern Generator Total Frame Size, Active Frame Size, Horizontal Sync Width, Vertical Sync Width, Horizontal Back Porch, Vertical Back Porch, and Sync Configuration registers. 0: the Pattern Generator uses external video timing from the pixel clock, Data Enable, Horizontal Sync, and Vertical Sync signals.
		1	PATGEN_INV	RW	0	Enable Inverted Color Patterns: 1: Invert the color output. 0: Do not invert the color output.
		0	PATGEN_ASCRL	RW	0	Auto-Scroll Enable: 1: The Pattern Generator will automatically move to the next enabled pattern after the number of frames specified in the Pattern Generator Frame Time (PGFT) register. 0: The Pattern Generator retains the current pattern.
0x66	PGIA	7:0	PATGEN_IA	RW	0	Indirect Address: This 8-bit field sets the indirect address for accesses to indirectly-mapped registers. It should be written prior to reading or writing the Pattern Generator Indirect Data register. See TI App Note AN-2198.
0x67	PGID	7:0	PATGEN_ID	RW	0	Indirect Data: When writing to indirect registers, this register contains the data to be written. When reading from indirect registers, this register contains the readback value. See TI App Note AN-2198.
0x68	PGDBG	7:4	RESERVED	RW	0	Reserved
		3	PATGEN_BIST_EN	RW	0	Pattern Generator BIST Enable: Enables Pattern Generator in BIST mode. Pattern Generator will compare received video data with local generator pattern. Upstream device must be programmed to the same pattern.
		2:0	RESERVED	RW	0	Reserved
0x69	PGTSTDAT	7	PATGEN_BIST_ERR	R	0	Pattern Generator BIST Error Flag During Pattern Generator BIST mode, this bit indicates if the BIST engine has detected errors. If the BIST Error Count (available in the Pattern Generator indirect registers) is non-zero, this flag will be set.
		6:0	RESERVED	R	0	

Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (hex)	Register Name	Bit(s)	Function	Type	Default Value (hex)	Description
0x6E	GPI Pin Status 1	7	GPI7 Pin Status	R	0	GPI7/I2S_WC pin status
		6	GPI6 Pin Status	R	0	GPI6/I2S_DA pin status
		5	GPI5 Pin Status	R	0	GPI5/I2S_DB pin status
		4	RESERVED	R	0	Reserved for future use
		3	GPI3 Pin Status	R	0	GPI3 / I2S_DD pin status
		2	GPI2 Pin Status	R	0	GPI2 / I2S_DC pin status
		1	GPI1 Pin Status	R	0	GPI1 pin status
		0	GPI0 Pin Status	R	0	GPI0 pin status
0x6F	GPI Pin Status 2	7:1	RESERVED	R	0	Reserved for future use
		0	GPI8 Pin Status	R	0	GPI8/I2S_CLK pin status
0xF0	RX ID	7:0	ID0	R	0x5F	First byte ID code, '_'
0xF1		7:0	ID1	R	0x55	2nd byte of ID code, 'U'
0xF2		7:0	ID2	R	0x48	3rd byte of ID code. Value will be either 'B' or 'H'. 'H' indicates an HDCP capable device.
0xF3		7:0	ID3	R	0x39	4th byte of ID code: '9'
0xF4		7:0	ID4	R	0x34	5th byte of ID code: '4'
0xF5		7:0	ID5	R	0x38	6th byte of ID code: '8'

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DS90UB948-Q1 is a FPD-Link III Deserializer which, in conjunction with the DS90UB949/947-Q1 Serializers, converts 1-lane or 2-lane FPD-Link III streams into a FPD-Link (OpenLDI) interface. The Deserializer is capable of operating over cost-effective 50Ω single-ended coaxial or 100Ω differential shielded twisted-pair (STP) cables. It recovers the data from two FPD-Link III serial streams and translates it into dual pixel FPD-Link (data lanes + clock) supporting video resolutions up to WUXGA and 1080p60 with 24-bit color depth. This provides a bridge between HDMI enabled sources such as GPUs to connect to existing LVDS displays or Application Processors.

9.2 Typical Applications

Bypass capacitors should be placed near the power supply pins. At a minimum, four (4) 10µF capacitors should be used for local device bypassing. Ferrite beads are placed on the two sets of supply pins (VDD33 and VDDIO) for effective noise suppression. The interface to the graphics source is LVDS. The VDDIO pins may be connected to 3.3V or 1.8V. A capacitor and resistor are placed on the PDB pin to delay the enabling of the device until power is stable. See Figure 44 for a typical STP connection diagram and Figure 45 for a typical coax connection diagram.

Typical Applications (continued)

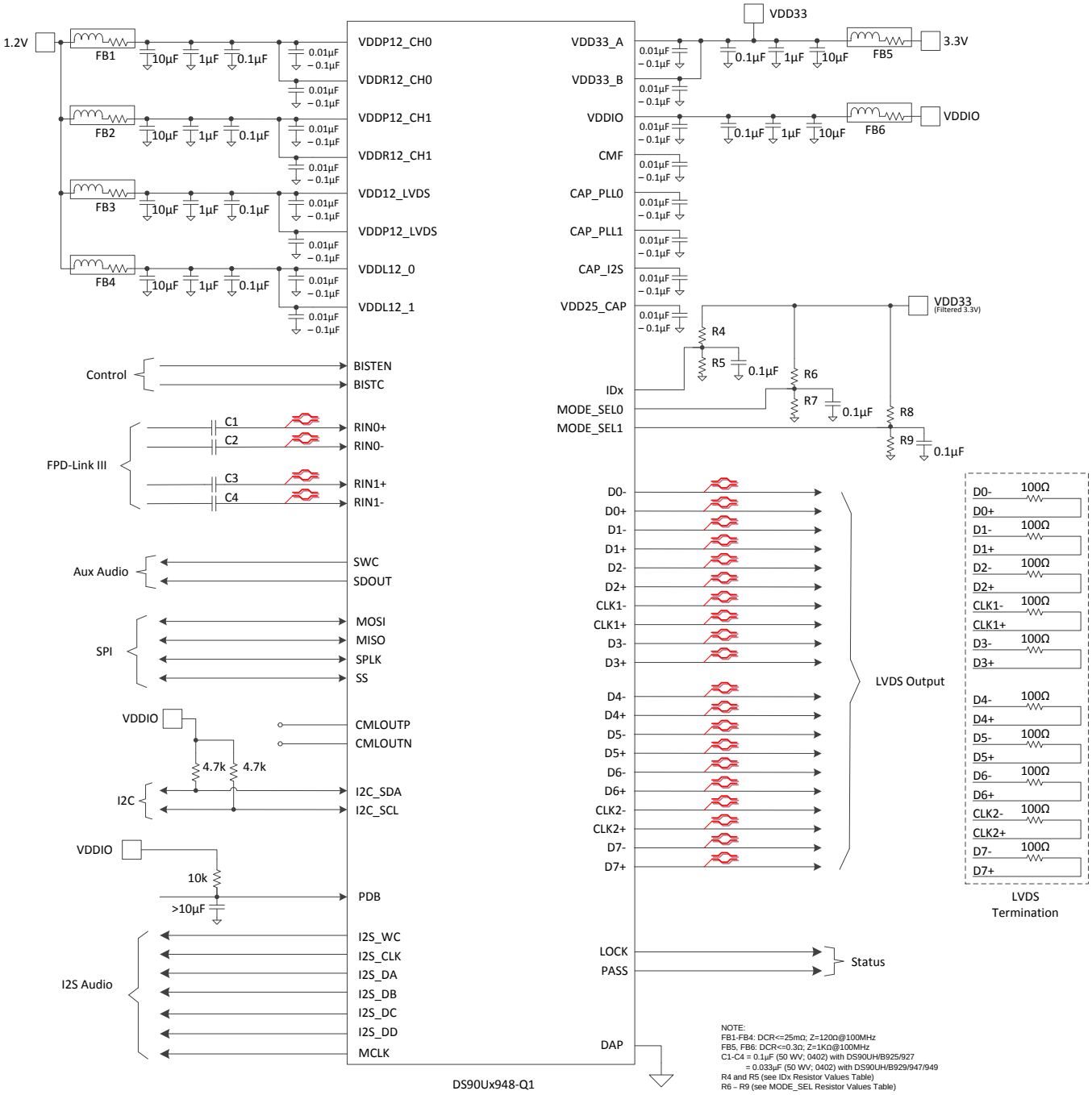

Figure 44. Typical Connection Diagram (STP)

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Typical Applications (continued)

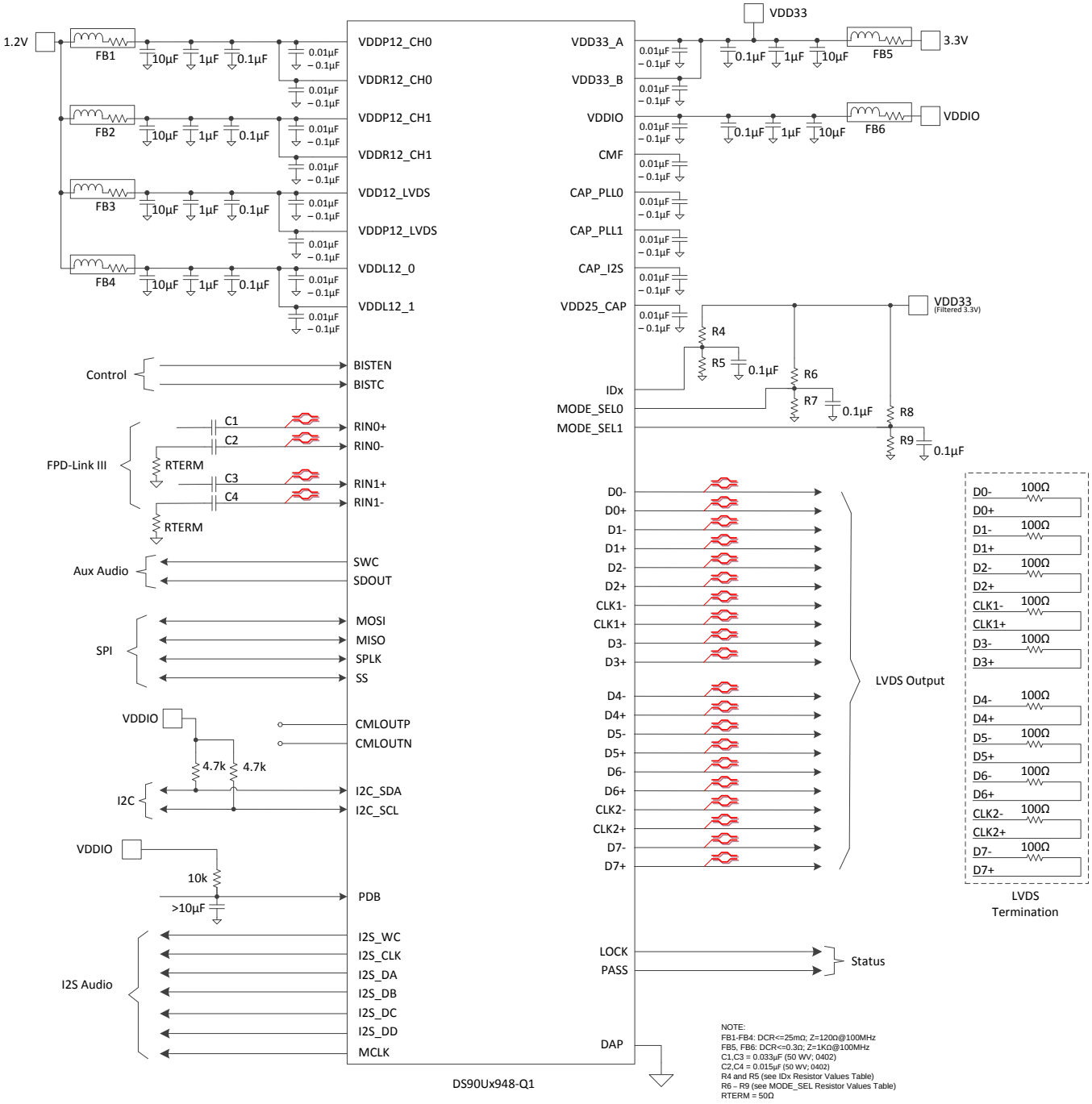

Figure 45. Typical Connection Diagram (Coax)

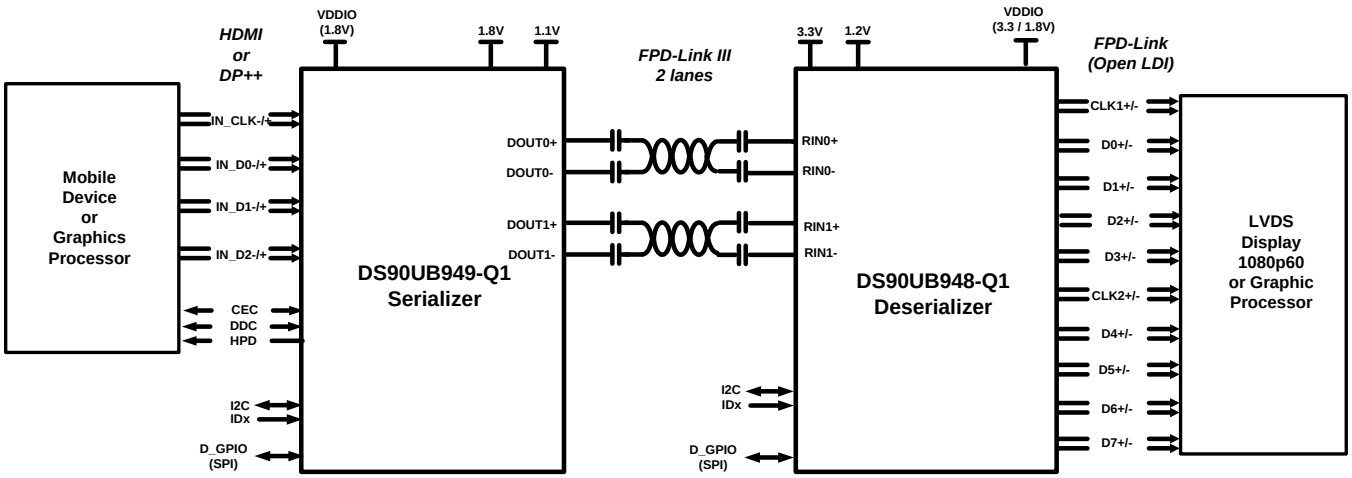

Figure 46. Typical Display System Diagram

9.2.1 Design Requirements

For the typical design application, use the following as input parameters.

Table 11. Design Parameters

Design Parameter	Example Value
VDDIO	1.8V or 3.3V
VDD12	1.2V
VDD33	3.3V
AC Coupling Capacitor for RIN0± and RIN1±	33nF

The SER/DES supports only AC-coupled interconnects through an integrated DC-balanced decoding scheme. External AC coupling capacitors must be placed in series in the FPD-Link III signal path as illustrated in Figure 47. For applications utilizing single-ended 50Ω coaxial cable, the unused data pins (RIN0-, RIN1-) should utilize a 15nF capacitor and should be terminated with a 50Ω resistor.

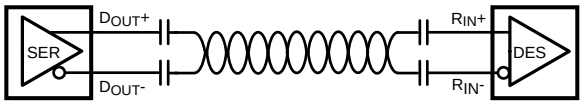

Figure 47. AC-Coupled Connection (STP)

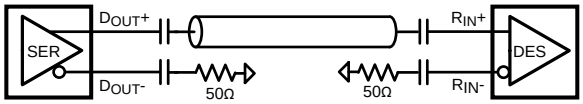

Figure 48. AC-Coupled Connection (Coaxial)

For high-speed FPD–Link III transmissions, the smallest available package should be used for the AC coupling capacitor. This will help minimize degradation of signal quality due to package parasitics. The I/O's require 33nF AC coupling capacitors to the line.

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9.2.2 Detailed Design Procedure

9.2.2.1 PCB Layout and Power System Considerations

Circuit board layout and stack-up for the LVDS serializer and deserializer devices should be designed to provide low-noise power to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mil) for power / ground sandwiches. This arrangement utilizes the plane capacitance for the PCB power system and has low-inductance, which has proven effectiveness especially at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01µF to 10µF. Tantalum capacitors may be in the 2.2µF to 10µF range. The voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

MLCC surface mount capacitors are recommended due to their smaller parasitic properties. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommended at the point of power entry. This is typically in the 50µF to 100µF range and will smooth low frequency switching noise. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path. A small body size X7R chip capacitor, such as 0603 or 0805, is recommended for external bypass. A small body sized capacitor has less inductance. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20MHz-30MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the LVDS lines to prevent coupling from the LVCMOS lines to the LVDS lines. Closely coupled differential lines of 100Ω are typically recommended for LVDS interconnect. The closely coupled lines help to ensure that coupled noise will appear as common mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

At least 32 thermal vias are necessary from the device center DAP to the ground plane. They connect the device ground to the PCB ground plane, as well as conduct heat from the exposed pad of the package to the PCB ground plane. More information on the WQFN style package, including PCB design and manufacturing requirements, is provided in TI Application Note: AN-1187.

9.2.2.2 CML Interconnect Guidelines

See AN-1108 and AN-905 for full details.

- Use 100Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  - – S = space between the pair
  - – 2S = space between pairs
  - – 3S = space to LVCMOS signal
- Minimize the number of Vias
- Use differential connectors when operating above 500Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair
- Terminate as close to the TX outputs and RX inputs as possible

Additional general guidance can be found in the LVDS Owner's Manual - available in PDF format from the Texas Instruments web site at: SNLA187

9.2.3 Application Performance Plots

The plots below correspond to 1080p60 video application with 2-lane FPD-Link III input and dual OpenLDI output.

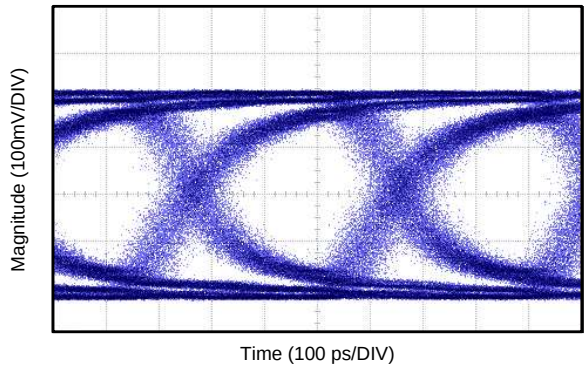

Figure 49. Loop-through CML Output at 2.6 Gbps Serial Line Rate

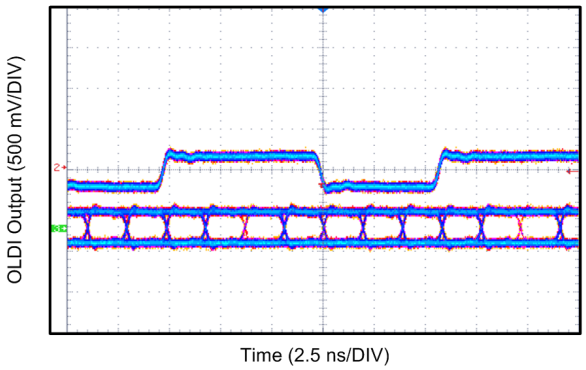

Figure 50. OpenLDI Clock and Data Output at 74.25 MHz Pixel Clock

10 Power Supply Recommendations

This device provides separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description table () provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

10.1 Power Up Requirements and PDB Pin

When power is applied, power from the highest voltage rail to the lowest voltage rail on any of the supply pins. For 3.3V IO operation, VDDIO and VDD33 can be powered by the same supply and ramped simultaneously. The power supply ramp (V_{DD12}, V_{DD33}, and V_{DDIO}) should be faster than 1.5ms with a monotonic rise. A large capacitor on the PDB pin is needed to ensure PDB arrives after all the supply pins have settled to the recommended operating voltage. When PDB pin is pulled up to V_{DD33}, a 10kΩ pull-up and a >10µF capacitor to GND are required to delay the PDB input signal rise. All inputs must not be driven until both V_{DD33} and V_{DDIO} has reached steady state. Pins V_{DD33_A} and V_{DD33_B} should both be externally connected, bypassed, and driven to the same potential (they are not internally connected).

11 Layout

11.1 Layout Guidelines

Circuit board layout and stack-up for the FPD-Link III devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power/ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 µF to 0.1 µF. Tantalum capacitors may be in the 2.2 µF to 10 µF range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50 µF to 100 µF range and will smooth low frequency switching noise. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path.

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Layout Guidelines (continued)

A small body size X7R chip capacitor, such as 0603 or 0402, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20 to 30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the CML lines to prevent coupling from the LVCMOS lines to the CML lines. Closely-coupled differential lines of 100Ω are typically recommended for CML interconnect. The closely coupled lines help to ensure that coupled noise will appear as common-mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

Information on the WQFN style package is provided in TI Application Note: AN-1187.

11.2 Layout Example

Stencil parameters such as aperture area ratio and the fabrication process have a significant impact on paste deposition. Inspection of the stencil prior to placement of the WQFN package is highly recommended to improve board assembly yields. If the via and aperture openings are not carefully monitored, the solder may flow unevenly through the DAP. Stencil parameters for aperture opening and via locations are shown in Figure 51:

Table 12. No Pullback WQFN Stencil Aperture Summary

Device	Pin Count	Mkt Dwg	PCB I/O Pad Size (mm)	PCB Pitch (mm)	PCB DAP Size(mm)	Stencil I/O Aperture (mm)	Stencil DAP Aperture (mm)	Number OF DAP Aperture Openings	Gap between DAP Aperture (Dim A mm)
DS90UB948-Q1	64	NKD	0.25 x 0.6	0.5	7.2 x 7.2	0.25 x 0.6	1.16 x 1.16	25	0.2

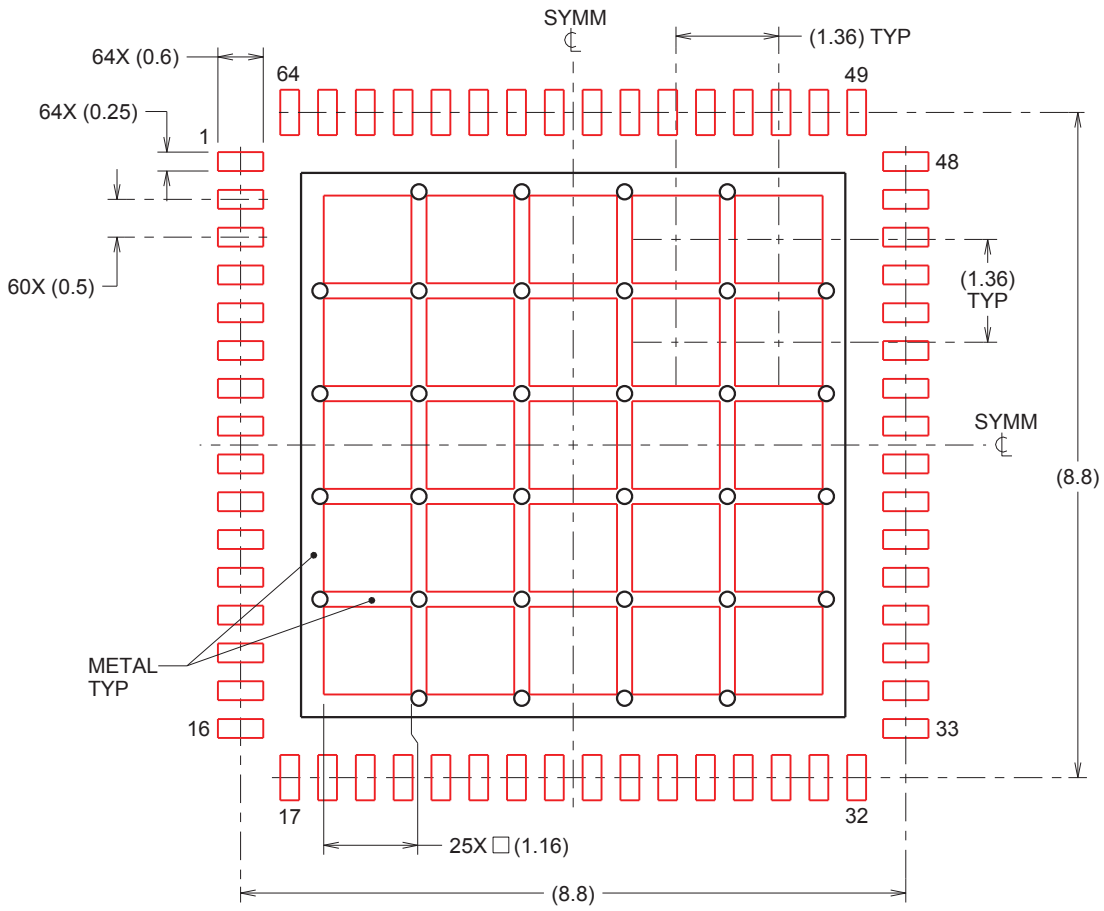

Figure 51. 64-Pin WQFN Stencil Example of Via and Opening Placement (dimensions in mm)

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Figure 52 (PCB layout example) is derived from a layout design of the DS90UB948-Q1 . This graphic and additional layout description are used to demonstrate both proper routing and proper solder techniques when designing in the Deserializer.

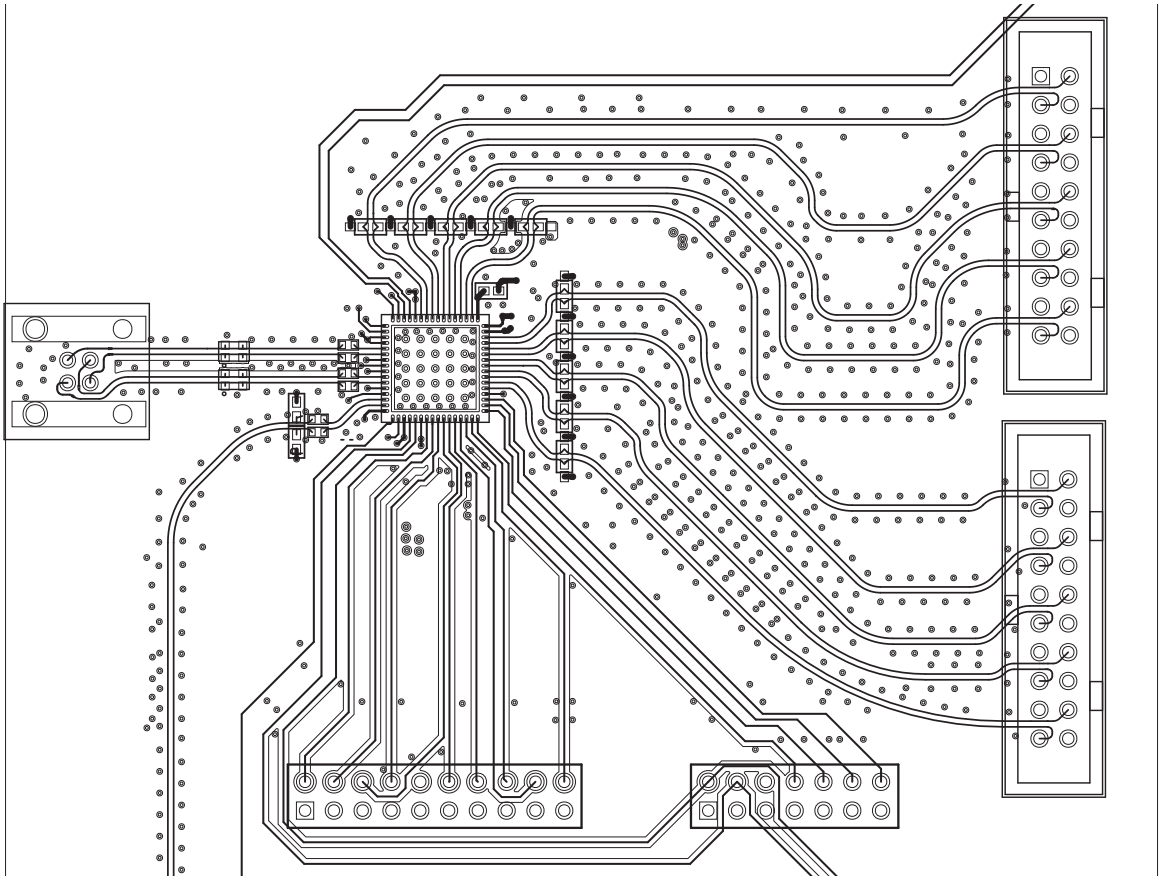

Figure 52. DS90UB948-Q1 Deserializer Example Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Soldering Specifications Application Report, SNOA549
- IC Package Thermal Metrics Application Report, SPRA953
- Channel-Link PCB and Interconnect Design-In Guidelines, SNLA008
- Transmission Line RAPIDESIGNER Operation and Application Guide, SNLA035
- Leadless Leadframe Package (LLP) Application Report, SNOA401
- LVDS Owner's Manual, SNLA187
- I2C Communication Over FPD-Link III with Bidirectional Control Channel, SNLA131A
- Using the I2S Audio Interface of DS90Ux92x FPD-Link III Devices, SNLA221
- Exploring the Internal Test Pattern Generation Feature of 720p FPD-Link III Devices, SNLA132

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90UB948TNKDRQ1	PREVIEW	WQFN	NKD	64	2000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 105	90UB948Q1	
DS90UB948TNKDTQ1	PREVIEW	WQFN	NKD	64	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 105	90UB948Q1	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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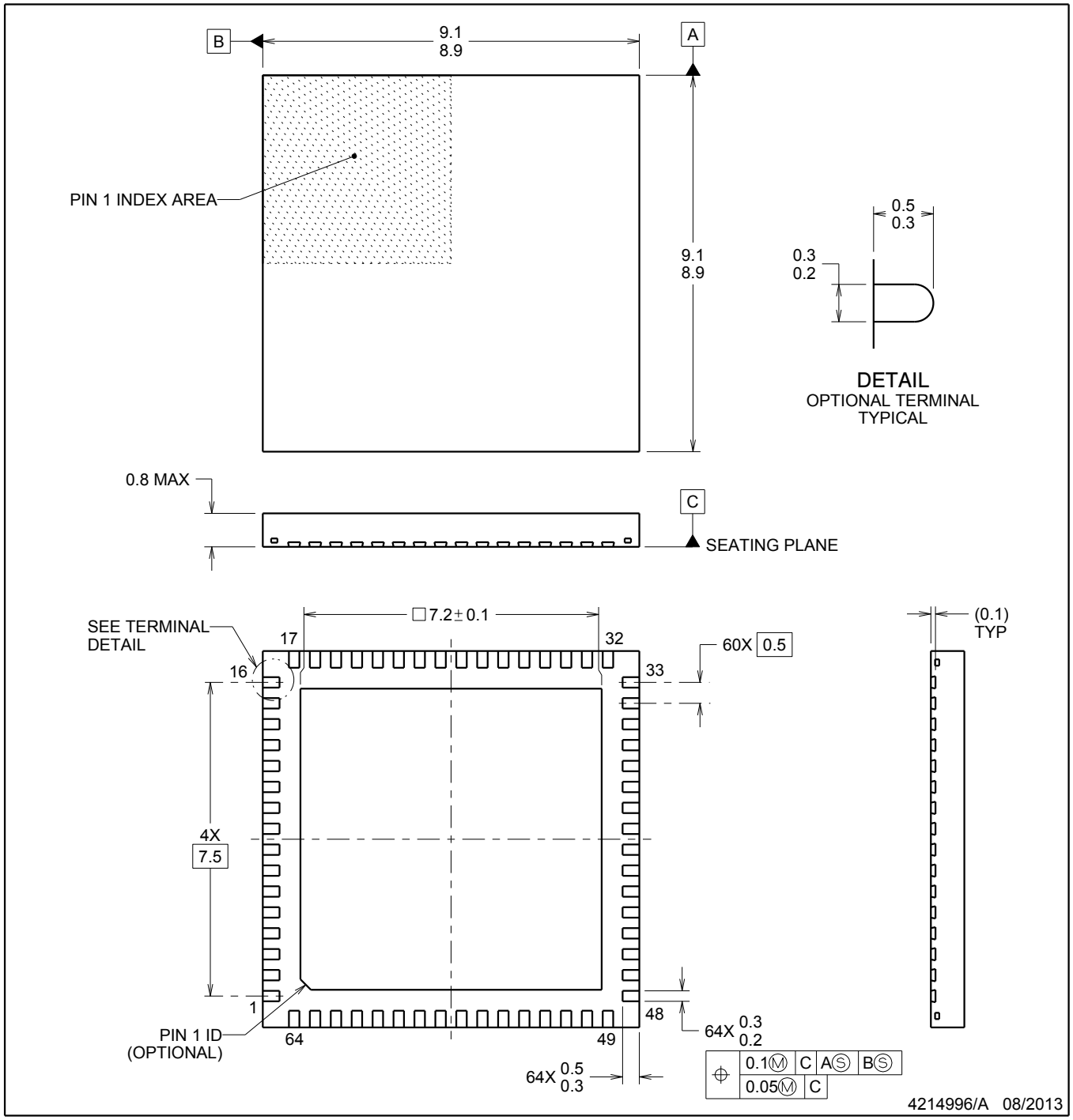
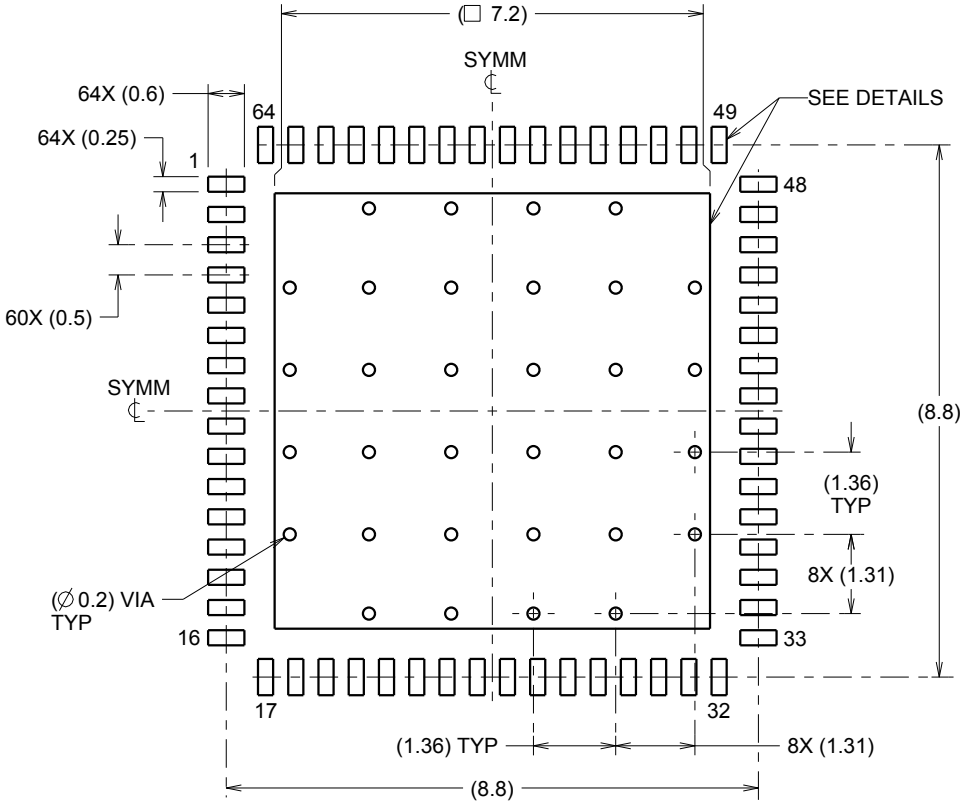
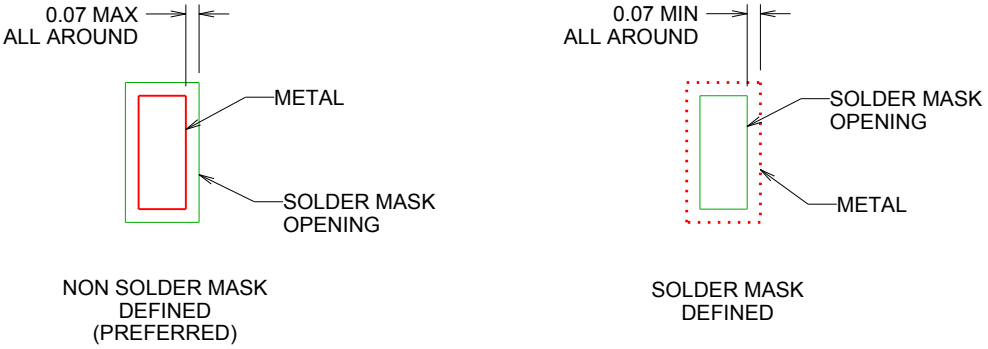


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:8X

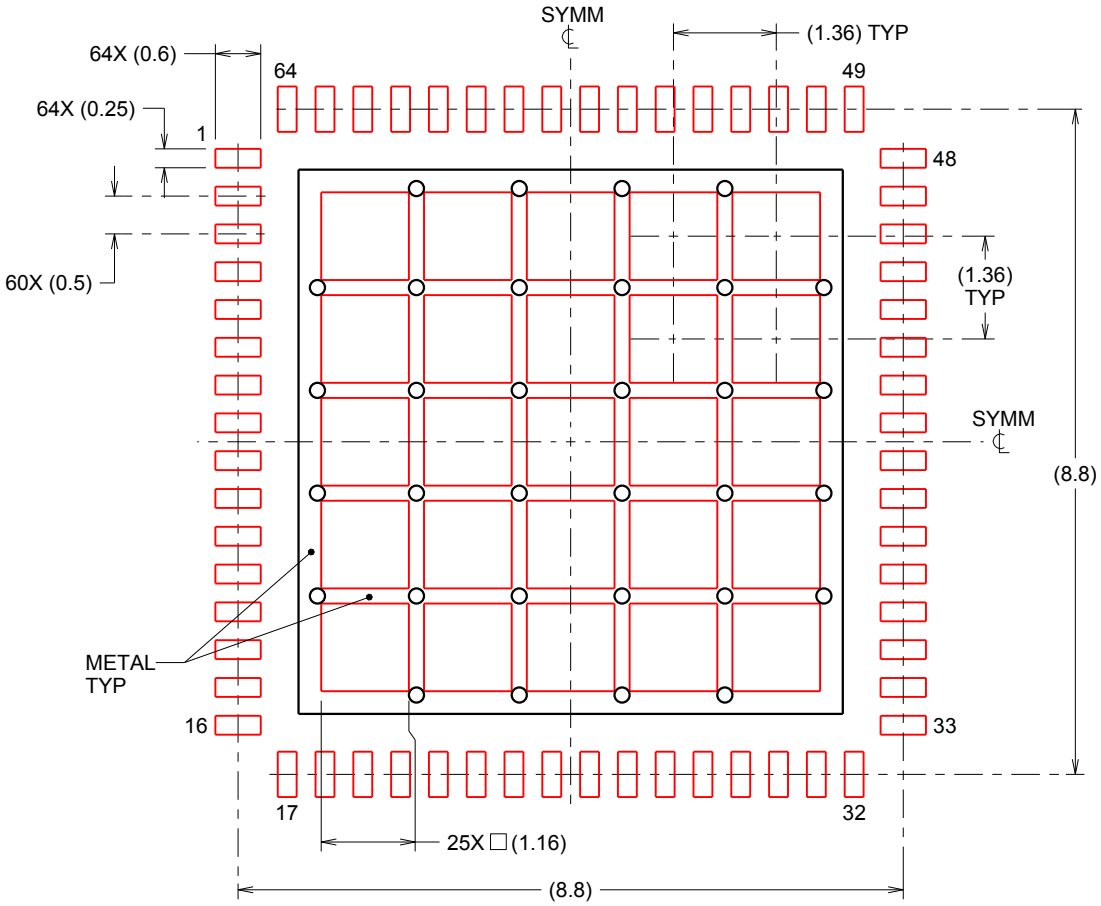


SOLDER MASK DETAILS

4214996/A 08/2013

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDERPASTE EXAMPLE
BASED ON 0.125mm THICK STENCIL

EXPOSED PAD
65% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

4214996/A 08/2013

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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