



# 50Ω, Low-Voltage, Quad SPST/Dual SPDT Analog Switches in UCSP

MAX4747-MAX4750

## General Description

The MAX4747-MAX4750 low-voltage, quad single-pole single-throw (SPST)/dual single-pole/double-throw (SPDT) analog switches operate from a single +2V to +11V supply and handle rail-to-rail analog signals. These switches exhibit low leakage current (0.1nA) and consume less than 0.5nW (typ) of quiescent power, making them ideal for battery-powered applications.

When powered from a +3V supply, these switches feature 50Ω (max) on-resistance (RON), with 3.5Ω (max) matching between channels and 9Ω (max) flatness over the specified signal range.

The MAX4747 has four normally open (NO) switches, the MAX4748 has four normally closed (NC) switches, and the MAX4749 has two NO and two NC switches. The MAX4750 has two SPDT switches. These switches are available in 14-pin TSSOP, 16-pin thin QFN (4mm x 4mm), and 16-bump chip-scale packages (UCSP™). This tiny chip-scale package occupies a 2mm x 2mm area and significantly reduces the required PC board area.

## Applications

- Battery-Powered Systems
- Audio/Video-Signal Routing
- Low-Voltage Data-Acquisition Systems
- Cell Phones
- Communications Circuits
- Glucose Meters
- PDA's

## Features

- ◆ 2mm x 2mm UCSP
- ◆ Guaranteed On-Resistance (RON)  
25Ω (max) at +5V  
50Ω (max) at +3V
- ◆ On-Resistance Matching  
3Ω (max) at +5V  
3.5Ω (max) at +3V
- ◆ Guaranteed < 0.1nA Leakage Current at  
TA = +25°C
- ◆ Single-Supply Operation from +2.0V to +11V
- ◆ TTL/CMOS-Logic Compatible
- ◆ -84dB Crosstalk (1MHz)
- ◆ -72dB Off-Isolation (1MHz)
- ◆ Low Power Consumption: 0.5nW (typ)
- ◆ Rail-to-Rail Signal Handling

## Ordering Information

PART	TEMP RANGE	PIN-/BUMP-PACKAGE	TOP MARK
MAX4747EUD	-40°C to +85°C	14 TSSOP	—
MAX4747ETE	-40°C to +85°C	16 Thin QFN-EP*	—
MAX4747EBE-T	-40°C to +85°C	16 UCSP-16	4747

\*EP = Exposed paddle.

Ordering Information continued at end of data sheet.

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## Pin Configurations/Truth Tables

TOP VIEW

THIN QFN

TOP VIEW  
(BUMPS SIDE DOWN)

TSSOP

UCSP

INPUT	SWITCH STATE
LOW	OFF
HIGH	ON

Pin Configurations/Truth Tables continued at end of data sheet.



**For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at [www.maxim-ic.com](http://www.maxim-ic.com).**

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## ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)

V+	.....-0.3V to +12V
IN_, COM_, NO_, NC_ (Note 1)	.....-0.3V to (V+ + 0.3V)
Continuous Current (any pin)	.....±10mA
Peak Current (any pin, pulsed at 1ms, 10% duty cycle)	...±20mA
Continuous Power Dissipation (T <sub>A</sub> = +70°C)	
14-Pin TSSOP (derate 6.3mW/°C above +70°C)	.....500mW
16-Pin Thin QFN (derate 16.9mW/°C above +70°C)	.....1349mW
16-Bump UCSP (derate 8.3mW/°C above +70°C)	.....659mW

Operating Temperature Range	.....-40°C to +85°C
Storage Temperature Range	.....-65°C to +150°C
Maximum Junction Temperature	.....+150°C
Bump Temperature (soldering)	
Infrared (15s)	.....+220°C
Vapor Phase (60s)	.....+215°C
Lead Temperature (soldering, 10s)	.....+300°C

**Note 1:** Signals on IN\_, NO\_, NC\_, or COM\_ exceeding V+ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +3V ±10%, V<sub>IH</sub> = +2.0V, V<sub>IL</sub> = +0.8V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at V+ = +3V, T<sub>A</sub> = +25°C.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNITS
<b>ANALOG SWITCH</b>							
Analog Signal Range	V <sub>COM_</sub> , V <sub>NO_</sub> , V <sub>NC_</sub>			0		V+	V
On-Resistance	R <sub>ON</sub>	V+ = +2.7V, I <sub>COM_</sub> = 5mA, V <sub>NO_</sub> or V <sub>NC_</sub> = +1.5V	+25°C		17	50	Ω
			T <sub>MIN</sub> to T <sub>MAX</sub>			60	
On-Resistance Matching Between Channels (Notes 5, 6)	ΔR <sub>ON</sub>	V+ = +2.7V, I <sub>COM_</sub> = 5mA, V <sub>NO_</sub> or V <sub>NC_</sub> = +1.5V	+25°C		0.2	3.5	Ω
			T <sub>MIN</sub> to T <sub>MAX</sub>			4.5	
On-Resistance Flatness (Note 7)	R <sub>FLAT(ON)</sub>	V+ = +2.7V, I <sub>COM_</sub> = 5mA, V <sub>NO_</sub> or V <sub>NC_</sub> = +1V, +1.5V, +2V	+25°C		2.7	9	Ω
			T <sub>MIN</sub> to T <sub>MAX</sub>			11	
NO_ or NC_ Off-Leakage Current (Note 8)	I <sub>NO_(OFF)</sub> , I <sub>NC_(OFF)</sub>	V+ = +3.6V, V <sub>COM_</sub> = +0.3V, +3V, V <sub>NO_</sub> or V <sub>NC_</sub> = +3V, +0.3V	+25°C	-0.1		+0.1	nA
			T <sub>MIN</sub> to T <sub>MAX</sub>	-2		+2	
COM_ Off-Leakage Current (Note 8)	I <sub>COM_(OFF)</sub>	V+ = +3.6V, V <sub>COM_</sub> = +0.3V, +3V, V <sub>NO_</sub> or V <sub>NC_</sub> = +3V, +0.3V	+25°C	-0.1		+0.1	nA
			T <sub>MIN</sub> to T <sub>MAX</sub>	-2		+2	
COM_ On-Leakage Current (Note 8)	I <sub>COM_(ON)</sub>	V+ = +3.6V, V <sub>COM_</sub> = +0.3V, +3.0V, V <sub>NO_</sub> or V <sub>NC_</sub> = +0.3V, +3V, or floating	+25°C	-0.2		+0.2	nA
			T <sub>MIN</sub> to T <sub>MAX</sub>	-4		+4	

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## ELECTRICAL CHARACTERISTICS—Single +3V Supply (continued)

(V+ = +3V ±10%, V<sub>IH</sub> = +2.0V, V<sub>IL</sub> = +0.8V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at V+ = +3V, T<sub>A</sub> = +25°C.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNITS
<b>DYNAMIC</b>							
Turn-On Time	t <sub>ON</sub>	V <sub>NO_</sub> or V <sub>NC_</sub> = +1.5V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Figure 2	+25°C	57	150		ns
			T <sub>MIN</sub> to T <sub>MAX</sub>			170	
Turn-Off Time	t <sub>OFF</sub>	V <sub>NO_</sub> or V <sub>NC_</sub> = +1.5V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Figure 2	+25°C	24	60		ns
			T <sub>MIN</sub> to T <sub>MAX</sub>			70	
Break-Before-Make (MAX4749/MAX4750 Only) (Note 8)	t <sub>BBM</sub>	V <sub>NO_</sub> or V <sub>NC_</sub> = +1.5V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Figure 3	+25°C		33		ns
			T <sub>MIN</sub> to T <sub>MAX</sub>	1			
Charge Injection	Q	V <sub>GEN</sub> = 0V, R <sub>GEN</sub> = 0, C <sub>L</sub> = 1.0nF, Figure 4	+25°C		7		pC
On-Channel -3dB Bandwidth	BW	Signal = 0dBm, 50Ω in and out	+25°C		250		MHz
Off-Isolation (Note 9)	V <sub>ISO</sub>	f = 1MHz, V <sub>NO_</sub> = 1V <sub>RMS</sub> , R <sub>L</sub> = 50Ω, C <sub>L</sub> = 5pF, Figure 5	+25°C		-72		dB
Crosstalk (Note 10)	V <sub>CT</sub>	f = 1MHz, V <sub>NO_</sub> = 1V <sub>RMS</sub> , R <sub>L</sub> = 50Ω, C <sub>L</sub> = 5pF, Figure 6	+25°C		84		dB
NO_ or NC_ Off-Capacitance	C <sub>OFF</sub>	f = 1MHz, Figure 7	+25°C		20		pF
COM_ Off-Capacitance	C <sub>COM_(OFF)</sub>	f = 1MHz, Figure 7	+25°C		20		pF
COM_ On-Capacitance	C <sub>COM_(ON)</sub>	f = 1MHz, Figure 7	+25°C		40		pF
<b>LOGIC INPUT</b>							
Input Logic High	V <sub>IH</sub>			1.4			V
Input Logic Low	V <sub>IL</sub>					0.8	V
Input Leakage Current	I <sub>IN</sub>	V <sub>IN_</sub> = 0V or V+		-1	+0.005	+1	μA
<b>POWER SUPPLY</b>							
Power-Supply Range	V+			2		11	V
Positive Supply Current	I+	V+ = +5.5V, V <sub>IN_</sub> = 0V or V+, all switches on or off			0.0001	1	μA

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## ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +5V ±10%, V<sub>IH</sub> = +2.0V, V<sub>IL</sub> = +0.8V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at V+ = +5V, T<sub>A</sub> = +25°C.)  
(Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNITS
<b>ANALOG SWITCH</b>							
Analog Signal Range	V <sub>COM_</sub> , V <sub>NO_</sub> , V <sub>NC_</sub>			0		V+	V
On-Resistance	R <sub>ON</sub>	V+ = +4.5V, I <sub>COM_</sub> = 5mA, V <sub>NO_</sub> or V <sub>NC_</sub> = +3.0V	+25°C	8.2	25		Ω
			T <sub>MIN</sub> to T <sub>MAX</sub>		30		
On-Resistance Matching Between Channels (Notes 5, 6)	ΔR <sub>ON</sub>	V+ = +4.5V, I <sub>COM_</sub> = 5mA, V <sub>NO_</sub> or V <sub>NC_</sub> = +3.0V	+25°C	0.1	3		Ω
			T <sub>MIN</sub> to T <sub>MAX</sub>		4		
On-Resistance Flatness (Notes 7)	R <sub>FLAT(ON)</sub>	V+ = +4.5V, I <sub>COM_</sub> = 5mA, V <sub>NO_</sub> or V <sub>NC_</sub> = +1V, +2V, +3V	+25°C	2.2	5		Ω
			T <sub>MIN</sub> to T <sub>MAX</sub>		7		
NO_ or NC_ Off-Leakage Current (Note 8)	I <sub>NO_(OFF)</sub> , I <sub>NC_(OFF)</sub>	V+ = +5.5V, V <sub>COM_</sub> = +1V, +4.5V, V <sub>NO_</sub> or V <sub>NC_</sub> = +4.5V, +1V	+25°C	-0.1		+0.1	nA
			T <sub>MIN</sub> to T <sub>MAX</sub>	-2		+2	
COM_ Off-Leakage Current (Note 8)	I <sub>COM_(OFF)</sub>	V+ = +5.5V, V <sub>COM_</sub> = +1V, +4.5V, V <sub>NO_</sub> or V <sub>NC_</sub> = +4.5V, +1V	+25°C	-0.1		+0.1	nA
			T <sub>MIN</sub> to T <sub>MAX</sub>	-2		+2	
COM_ On-Leakage Current (Note 8)	I <sub>COM_(ON)</sub>	V+ = +5.5V, V <sub>COM_</sub> = +1V, +4.5V, V <sub>NO_</sub> or V <sub>NC_</sub> = +1V, +4.5V, or floating	+25°C	-0.2		+0.2	nA
			T <sub>MIN</sub> to T <sub>MAX</sub>	-4		+4	
<b>DYNAMIC</b>							
Turn-On Time	t <sub>ON</sub>	V <sub>NO_</sub> or V <sub>NC_</sub> = +3.0V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Figure 2	+25°C	36	85		ns
			T <sub>MIN</sub> to T <sub>MAX</sub>		95		
Turn-Off Time	t <sub>OFF</sub>	V <sub>NO_</sub> or V <sub>NC_</sub> = +3.0V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Figure 2	+25°C	19	45		ns
			T <sub>MIN</sub> to T <sub>MAX</sub>		55		
Break-Before-Make (MAX4749/MAX4750 Only) (Note 8)	t <sub>BBM</sub>	V <sub>NO_</sub> or V <sub>NC_</sub> = +3.0V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Figure 3	+25°C	14			ns
			T <sub>MIN</sub> to T <sub>MAX</sub>	1			
Charge Injection	Q	V <sub>GEN</sub> = 0V, R <sub>GEN</sub> = 0, C <sub>L</sub> = 1.0nF, Figure 4	+25°C	9			pC
On-Channel -3dB Bandwidth	BW	Signal = 0dBm, 50Ω in and out	+25°C	250			MHz
Off-Isolation (Note 9)	V <sub>ISO</sub>	f = 1MHz, V <sub>NO_</sub> = 1V <sub>RMS</sub> , R <sub>L</sub> = 50Ω, C <sub>L</sub> = 5pF, Figure 5	+25°C	-72			dB

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## ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

( $V_+ = +5V \pm 10\%$ ,  $V_{IH} = +2.0V$ ,  $V_{IL} = +0.8V$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $V_+ = +5V$ ,  $T_A = +25^\circ C$ .) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNITS
Crosstalk (Note 10)	V <sub>CT</sub>	f = 1MHz, V <sub>NO_</sub> = 1V <sub>RMS</sub> , R <sub>L</sub> = 50Ω, C <sub>L</sub> = 5pF, Figure 6	+25°C		-84		dB
NO_ or NC_ Off-Capacitance	C <sub>OFF</sub>	f = 1MHz, Figure 7	+25°C		20		pF
COM_ Off-Capacitance	C <sub>COM_(OFF)</sub>	f = 1MHz, Figure 7	+25°C		20		pF
COM_ On-Capacitance	C <sub>COM_(ON)</sub>	f = 1MHz, Figure 7	+25°C		40		pF
<b>LOGIC INPUT</b>							
Input Logic High	V <sub>IH</sub>			2			V
Input Logic Low	V <sub>IL</sub>					0.8	V
Input Leakage Current	I <sub>IN</sub>	V <sub>IN_</sub> = 0V or V <sub>+</sub>		-1	+0.005	+1	μA
<b>POWER SUPPLY</b>							
Power-Supply Range	V <sub>+</sub>			2		11	V
Positive Supply Current	I <sub>+</sub>	V <sub>+</sub> = +5.5V, V <sub>IN_</sub> = 0V or V <sub>+</sub> , all switches on or off			0.0001	1	μA

**Note 3:** The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

**Note 4:** UCSP parts are 100% tested at +25°C only, and are guaranteed by design over temperature. TSSOP and Thin QFN parts are 100% tested at +85°C and guaranteed by design over temperature.

**Note 5:**  $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$ .

**Note 6:** UCSP and Thin QFN on-resistance matching between channels is guaranteed by design.

**Note 7:** Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.

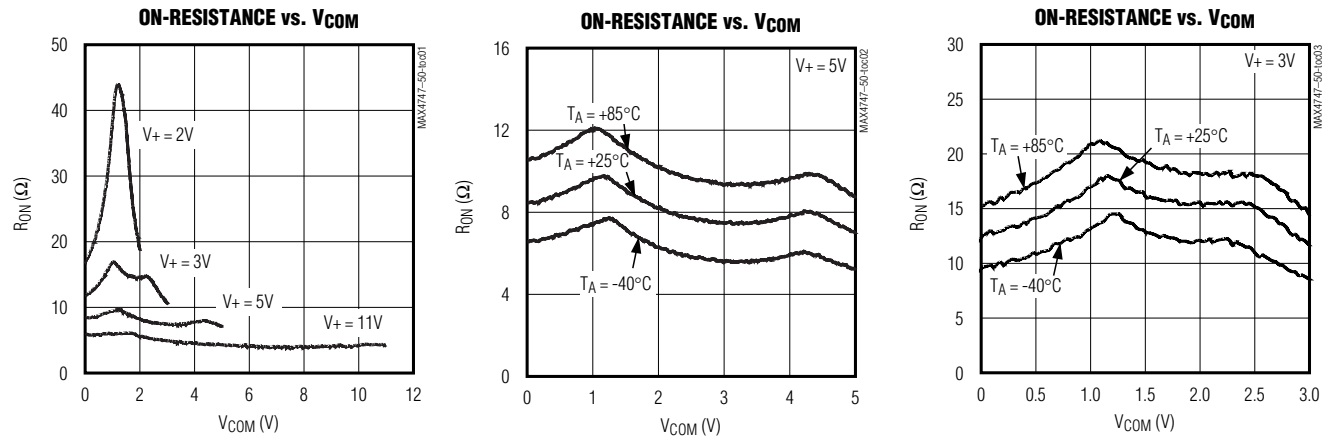
**Note 8:** Guaranteed by design.

**Note 9:** Off-isolation =  $20 \log_{10}(V_{NO\_}/V_{COM\_})$ , V<sub>NO\_</sub> = output, V<sub>COM\_</sub> = input to off switch.

**Note 10:** Between any two switches.

## Typical Operating Characteristics

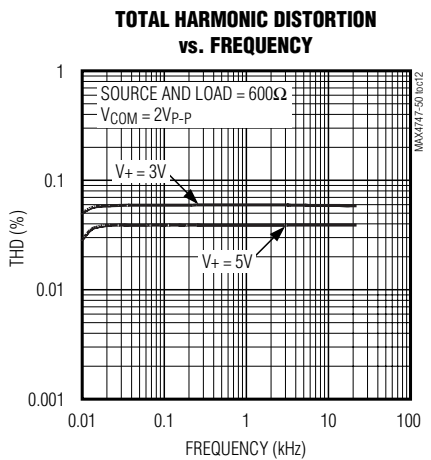
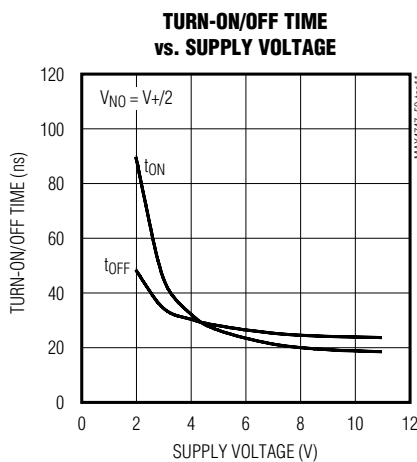
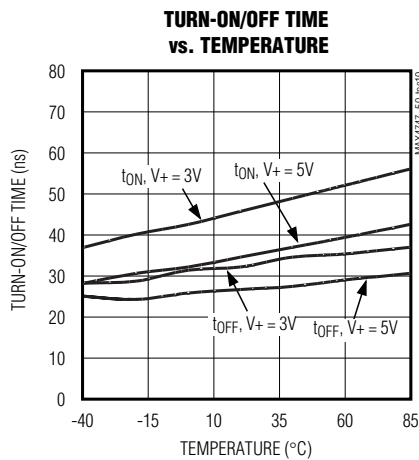
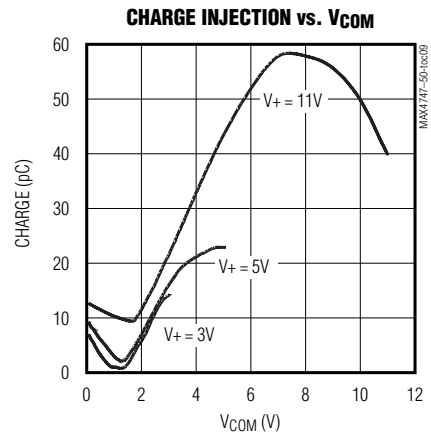
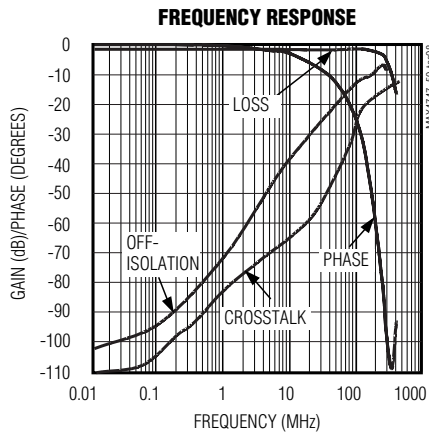
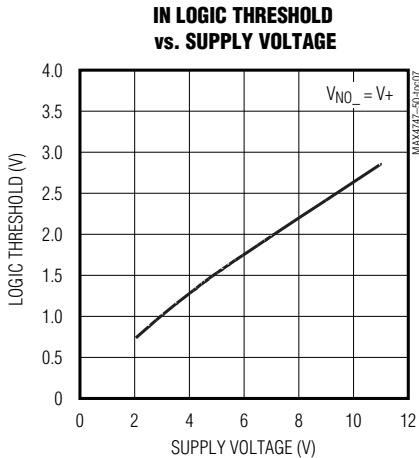
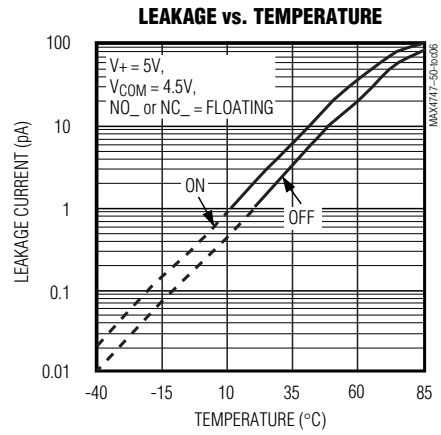
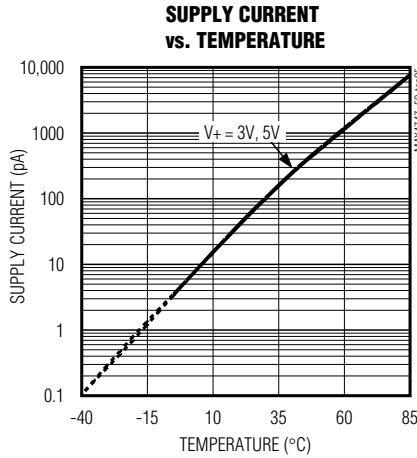
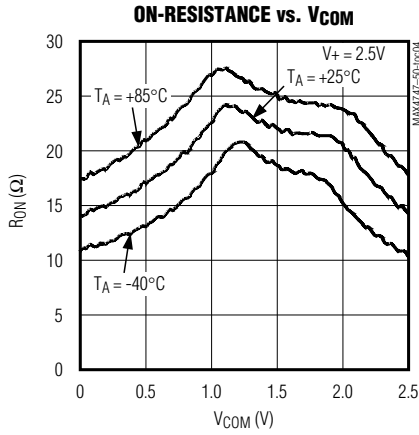
(T<sub>A</sub> = +25°C, unless otherwise noted.)



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## Typical Operating Characteristics (continued)

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



# 50Ω, Low-Voltage, Quad SPST/Dual SPDT Analog Switches in UCSP

**MAX4747-MAX4750**

## Pin Description—TSSOP

PIN				NAME	FUNCTION
MAX4747	MAX4748	MAX4749	MAX4750		
1, 3, 8, 11	—	—	—	NO1–NO4	Analog-Switch Normally Open Terminals
—	1, 3, 8, 11	—	—	NC1–NC4	Analog-Switch Normally Closed Terminals
—	—	1, 8	—	NO1, NO3	Analog-Switch Normally Open Terminals
—	—	—	1, 8	NO1, NO2	Analog-Switch Normally Open Terminals
—	—	—	4, 11	NC1, NC2	Analog-Switch Normally Closed Terminals
—	—	3, 11	—	NC2, NC4	Analog-Switch Normally Closed Terminals
2, 4, 9, 10	2, 4, 9, 10	2, 4, 9, 10	—	COM1–COM4	Analog-Switch Common Terminal
—	—	—	2, 9	COM1, COM2	Analog-Switch Common Terminal
13, 5, 6, 12	13, 5, 6, 12	13, 5, 6, 12	—	IN1–IN4	Logic-Control Digital Input
—	—	—	13, 6	IN1, IN2	Logic-Control Digital Input
7	7	7	7	GND	Ground. Connect to digital ground.
14	14	14	14	V+	Positive Analog and Digital Supply Voltage Input. Internally connected to substrate.
—	—	—	3, 5, 10, 12	N.C.	No Connection. Not internally connected.

## Pin Description—UCSP

PIN				NAME	FUNCTION
MAX4747	MAX4748	MAX4749	MAX4750		
B1, A2, C4, D2	—	—	—	NO1–NO4	Analog-Switch Normally Open Terminals
—	B1, A2, C4, D2	—	—	NC1–NC4	Analog-Switch Normally Closed Terminals
—	—	B1, C4	—	NO1, NO3	Analog-Switch Normally Open Terminals
—	—	—	B1, C4	NO1, NO2	Analog-Switch Normally Open Terminals
—	—	—	A3, D2	NC1, NC2	Analog-Switch Normally Closed Terminals
—	—	A2, D2	—	NC2, NC4	Analog-Switch Normally Closed Terminals
A1, A3, D4, D3	A1, A3, D4, D3	A1, A3, D4, D3	—	COM1–COM4	Analog-Switch Common Terminal
—	—	—	A1, D4	COM1, COM2	Analog-Switch Common Terminal
C1, A4, B4, D1	C1, A4, B4, D1	C1, A4, B4, D1	—	IN1–IN4	Logic-Control Digital Input
—	—	—	C1, B4	IN1, IN2	Logic-Control Digital Input
C3	C3	C3	C3	GND	Ground. Connect to digital ground.
B2	B2	B2	B2	V+	Positive Analog and Digital Supply Voltage Input. Internally connected to substrate.
—	—	—	A2, A4, D1, D3	N.C.	No Connection. Not internally connected.

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**MAX4747-MAX4750**

## Pin Description—Thin QFN

PIN				NAME	FUNCTION
MAX4747	MAX4748	MAX4749	MAX4750		
1, 3	1, 3	1, 3	4, 12	COM1, COM2	Analog-Switch Common Terminals
2	—	—	3	NO2	Analog-Switch Normally Open Terminal
4, 13	4, 13	4, 13	2, 10	IN2, IN1	Logic-Control Digital Inputs
5, 12	5, 12	5, 12	—	IN3, IN4	Logic-Control Digital Inputs
6	6	6	6	GND	Ground. Connect to digital ground.
7	—	7	—	NO3	Analog-Switch Normally Open Terminal
8, 14	8, 14	8, 14	1, 5, 8, 9, 13, 14	N.C.	No Connection. Not internally connected.
9, 10	9, 10	9, 10	—	COM3, COM4	Analog-Switch Common Terminals
11	—	—	—	NO4	Analog-Switch Normally Open Terminal
15	15	15	15	V+	Positive Supply-Voltage Input
16	—	16	11	NO1	Analog-Switch Normally Open Terminal
—	2	2	7	NC2	Analog-Switch Normally Closed Terminal
—	7	—	—	NC3	Analog-Switch Normally Closed Terminal
—	11	11	—	NC4	Analog-Switch Normally Closed Terminal
—	16	—	16	NC1	Analog-Switch Normally Closed Terminal
EP	EP	EP	EP	EP	Exposed Paddle. Connect exposed paddle to V+.



# 50Ω, Low-Voltage, Quad SPST/Dual SPDT Analog Switches in UCSP

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## Applications Information

### Operating Considerations for High-Voltage Supply

The MAX4747–MAX4750 operate to +11V with some precautions. The absolute maximum rating for V+ is +12V (referenced to GND). When operating near this region, bypass V+ with a minimum 0.1μF capacitor to ground as close to the IC as possible.

### Logic Levels

The MAX4747–MAX4750 are TTL compatible when powered from a single +3V supply. When powered from other supply voltages, the logic inputs should be driven rail-to-rail. For example, with a +11V supply, IN<sub>-</sub> should be driven low to 0V and high to 11V. With a +3.3V supply, IN<sub>-</sub> should be driven low to 0V and high to 3.3V. Driving IN<sub>-</sub> rail-to-rail minimizes power consumption.

### Analog Signal Levels

Analog signals that range over the entire supply voltage (GND to V+) pass with very little change in R<sub>ON</sub> (see the *Typical Operating Characteristics*). The bidirectional switches allow NO<sub>-</sub>, NC<sub>-</sub>, and COM<sub>-</sub> connections to be used as either inputs or outputs.

### Power-Supply Sequencing and Overvoltage Protection

**CAUTION: Do not exceed the absolute maximum ratings. Stresses beyond the listed ratings can cause permanent damage to the devices.**

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V+ before applying analog signals, especially if the analog signal is not current limited. If this sequencing is not possible, and if the analog inputs are not current limited to < 20mA, add small-signal diode D1 as shown in Figure 1. If the analog signal can dip below GND, add D2. Adding protection diodes reduces the analog signal range to a diode drop (about 0.7V) below V+ (for D1), and to a diode drop above ground (for D2). Leakage is unaffected by adding the diodes. On-resistance increases slightly at low supply voltages. Maximum supply voltage (V+) must not exceed +11V.

## Test Circuits/Timing Diagrams

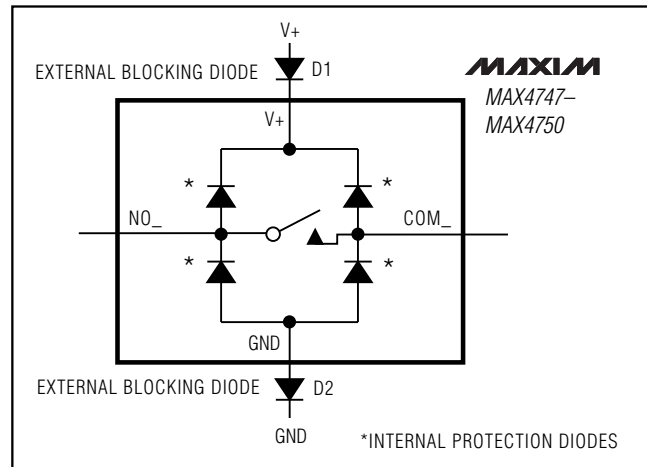


Figure 1. Overvoltage Protection Using External Blocking Diodes

Adding protection diodes causes the logic thresholds to be shifted relative to the power-supply rails. The most significant shift occurs when using low supply voltages (+5V or less). With a +5V supply, TTL compatibility is not guaranteed when protection diodes are added. Driving IN<sub>-</sub> and IN<sub>-</sub> all the way to the supply rails (i.e., to a diode drop higher than the V+ pin, or to a diode drop lower than the GND pin) is always acceptable.

Protection diodes D1 and D2 also protect against some overvoltage situations. Using the circuit in Figure 1, no damage results if the supply voltage is below the absolute maximum rating (+12V) and if a fault voltage up to the absolute maximum rating (V+ + 0.3V) is applied to an analog signal terminal.

## UCSP Applications Information

For the latest application details on UCSP construction, dimensions, tape carrier information, PC board techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to the Application Note: UCSP—A Wafer-Level Chip-Scale Package on Maxim's web site at [www.maxim-ic.com/ucsp](http://www.maxim-ic.com/ucsp).

# 50Ω, Low-Voltage, Quad SPST/Dual SPDT Analog Switches in UCSP

## Test Circuits/Timing Diagrams (continued)

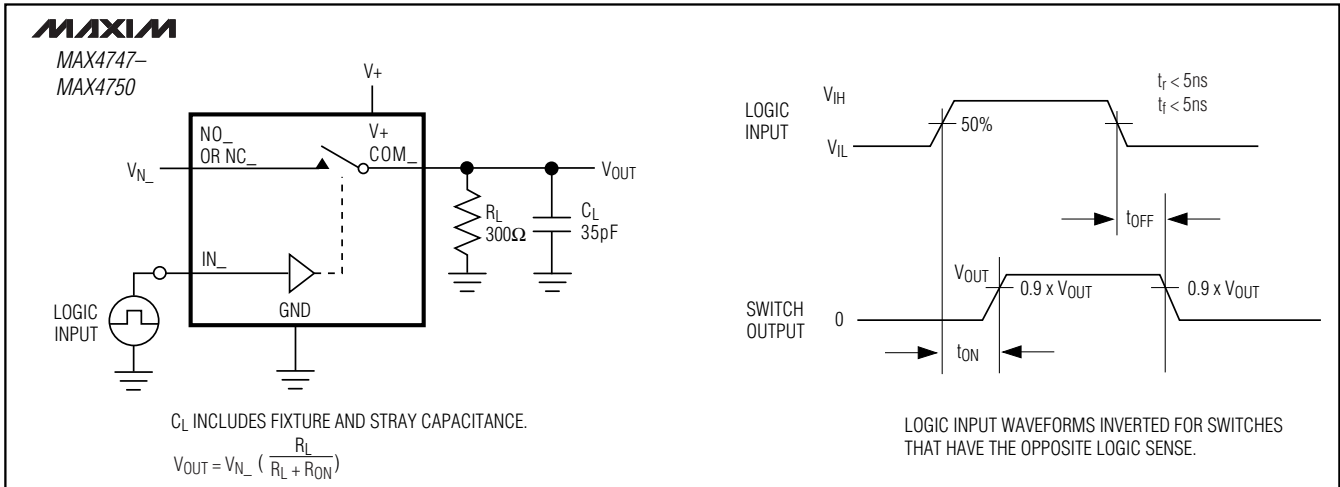


Figure 2. Switching Time

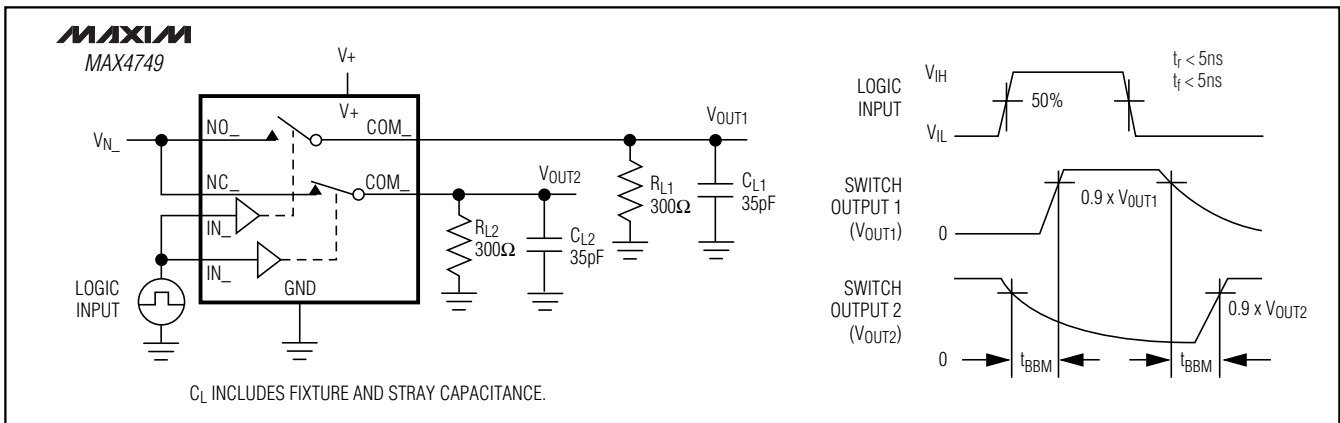


Figure 3. Break-Before-Make Interval

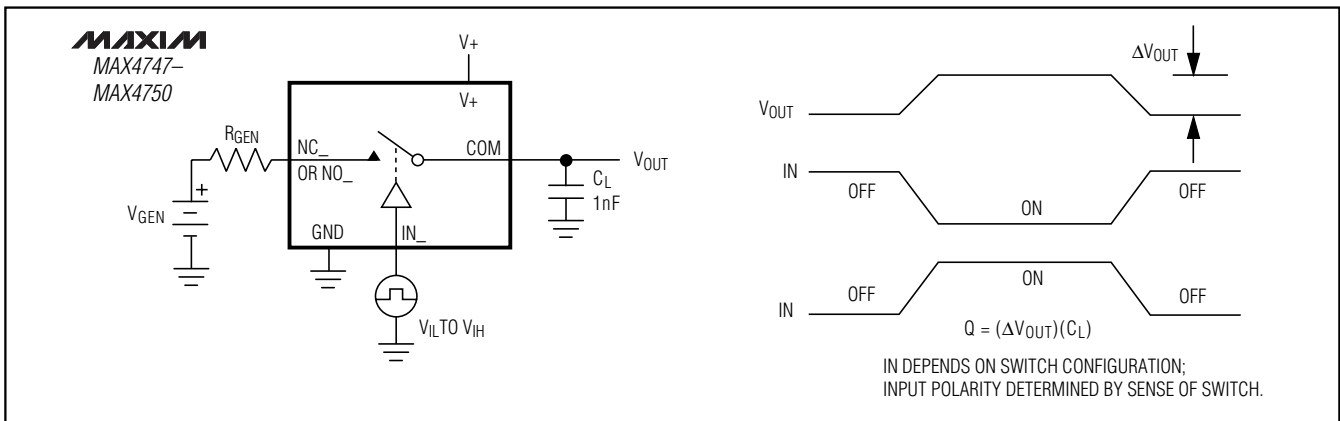


Figure 4. Charge Injection

# 50Ω, Low-Voltage, Quad SPST/Dual SPDT Analog Switches in UCSP

## Test Circuits/Timing Diagrams (continued)

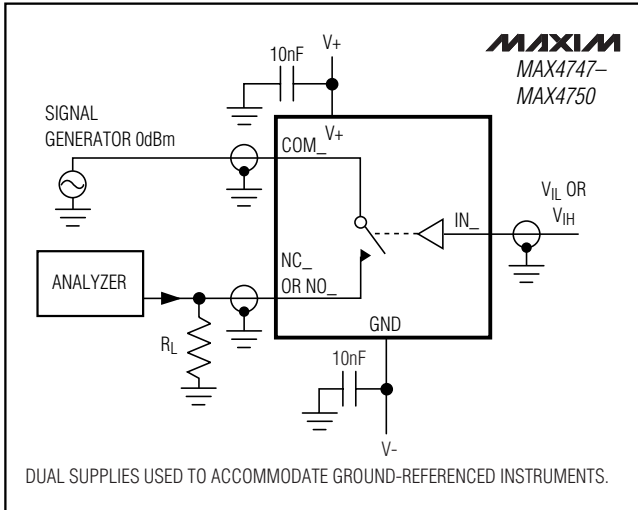


Figure 5. Off-Isolation/On-Channel Bandwidth

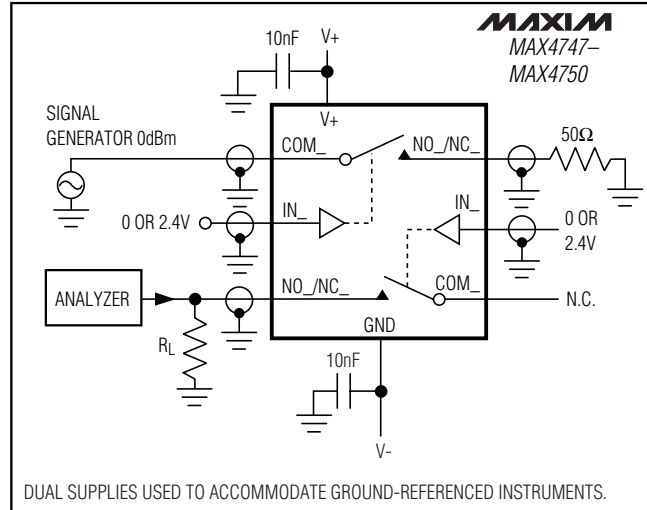


Figure 6. Crosstalk

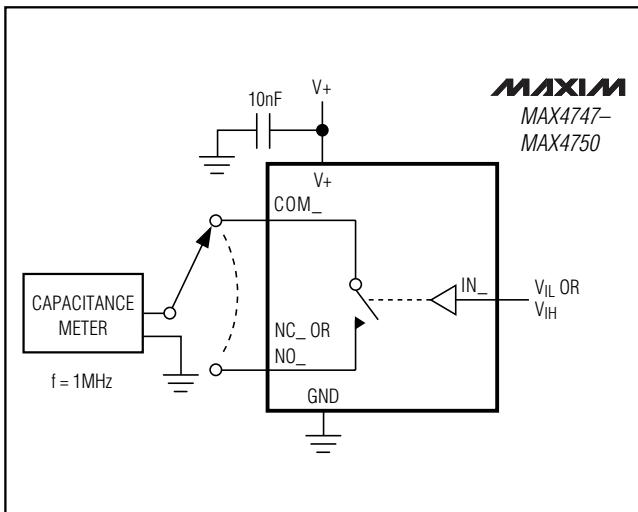


Figure 7. Channel Off-/On-Capacitance

## Ordering Information (continued)

PART	TEMP RANGE	PIN-/BUMP-PACKAGE	TOP MARK
<b>MAX4748</b> EUD	-40°C to +85°C	14 TSSOP	—
MAX4748ETE	-40°C to +85°C	16 Thin QFN-EP*	—
MAX4748EBE-T	-40°C to +85°C	16 UCSP-16	4748
<b>MAX4749</b> EUD	-40°C to +85°C	14 TSSOP	—
MAX4749ETE	-40°C to +85°C	16 Thin QFN-EP*	—
MAX4749EBE-T	-40°C to +85°C	16 UCSP-16	4749
<b>MAX4750</b> EUD	-40°C to +85°C	14 TSSOP	—
MAX4750ETE	-40°C to +85°C	16 Thin QFN-EP*	—
MAX4750EBE-T	-40°C to +85°C	16 UCSP-16	4750

\*EP = Exposed paddle.

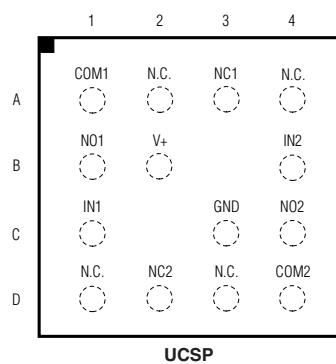
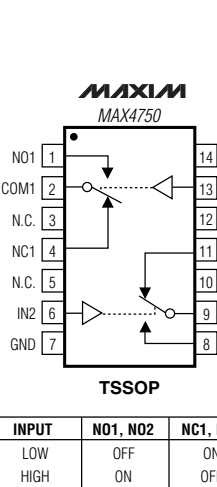
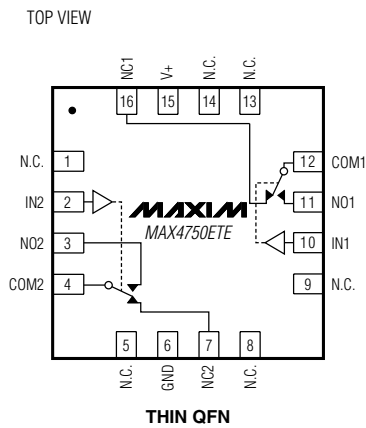
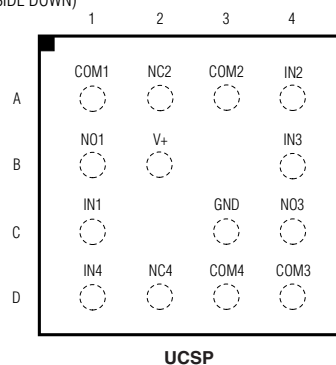
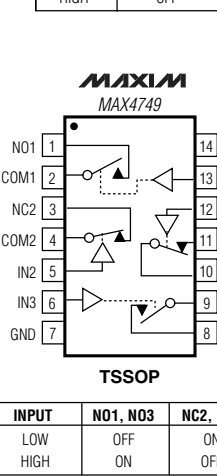
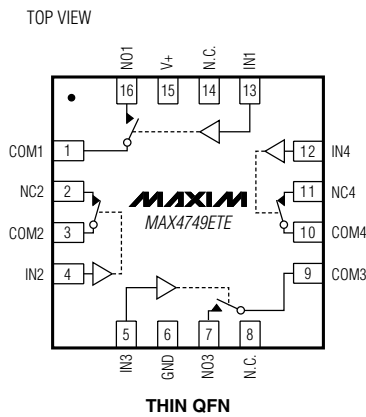
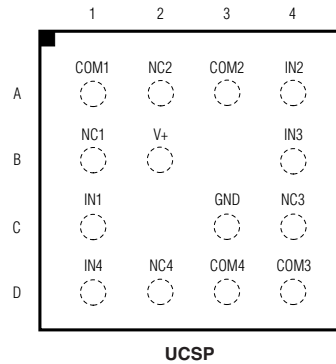
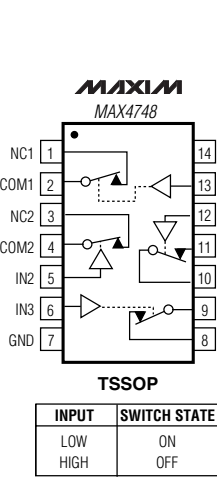
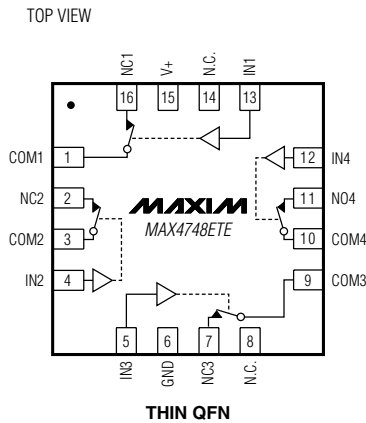
## Chip Information

TRANSISTOR COUNT: 130

PROCESS: CMOS

# 50Ω, Low-Voltage, Quad SPST/Dual SPDT Analog Switches in UCSP

## Pin Configurations/Truth Tables (continued)



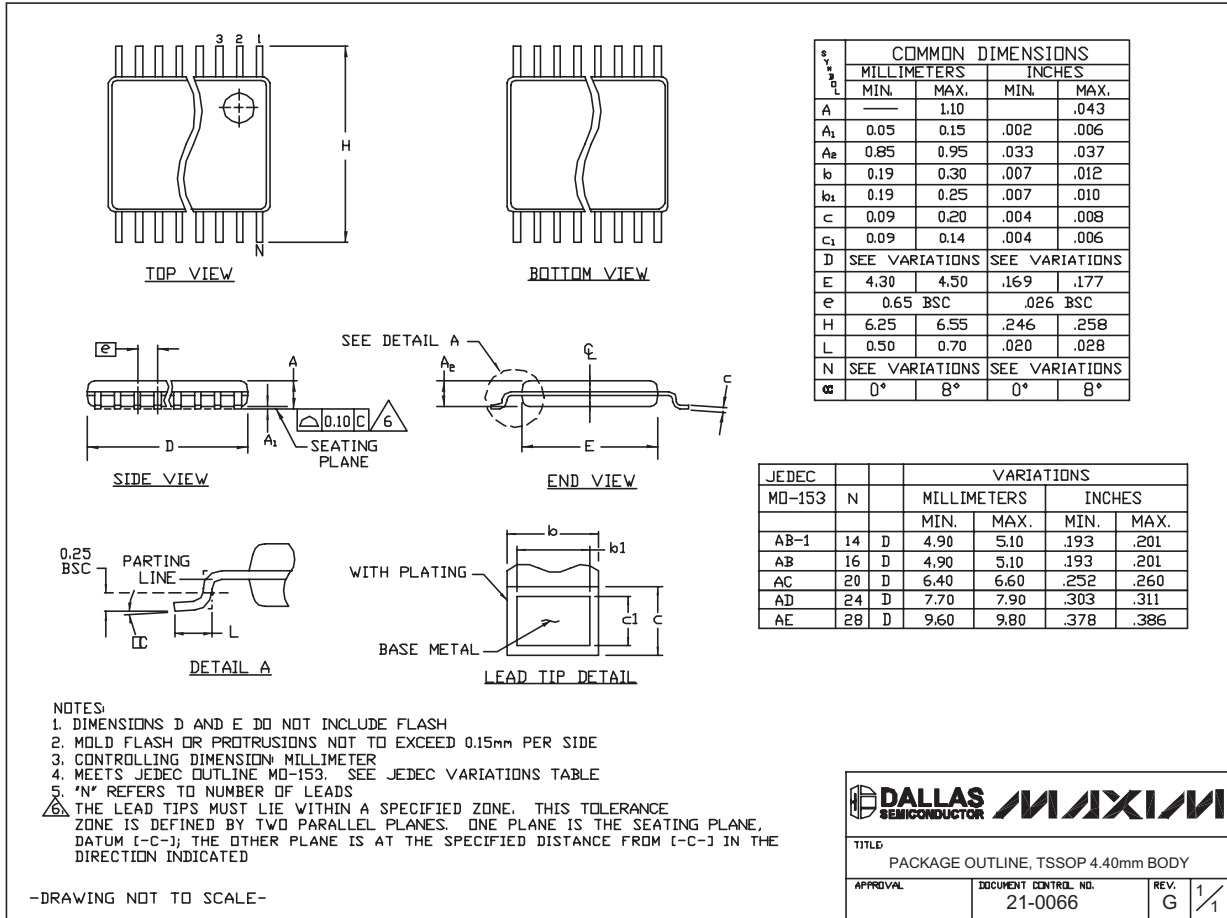
# 50Ω, Low-Voltage, Quad SPST/Dual SPDT Analog Switches in UCSP

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

MAX4747-MAX4750

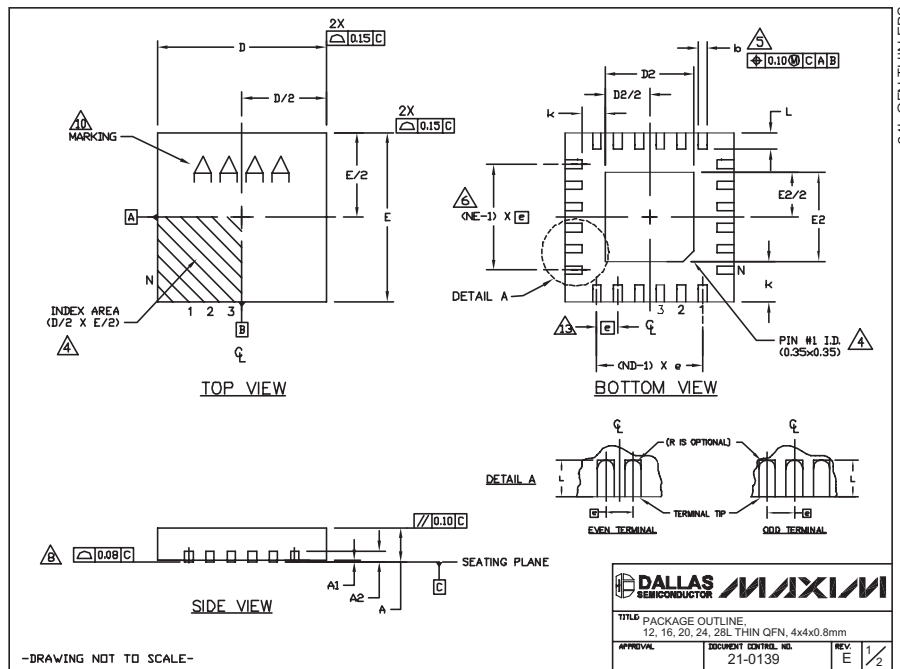
TSSOP4\_40mm.EPS



# 50Ω, Low-Voltage, Quad SPST/Dual SPDT Analog Switches in UCSP

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



COMMON DIMENSIONS													EXPOSED PAD VARIATIONS										
PKG REF.	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4			PKG CODES	D2			E2			DOWN BIRDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	ND
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF			T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.40	0.23	0.30	0.15	0.20	0.25	T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	ND
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.			T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	YES
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50	T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	ND
N	12			16			20			24			28			T2844-1	2.50	2.60	2.70	2.50	2.60	2.70	ND
ND	3			4			5			6			7										
NE	3			4			5			6			7										
VGGB	VGGB			VGGB			VGGB-1			VGGB-2			VGGB										

-DRAWING NOT TO SCALE-

	<b>TITLE</b> PACKAGE OUTLINE 12, 16, 20, 24, 28L THIN QFN, 4x4x0.8mm <b>APPROVAL</b> <b>DOCUMENT CONTROL NO.</b> 21-0139 <b>REV.</b> E <b>2/2</b>
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- NOTES:
- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
  - ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
  - N IS THE TOTAL NUMBER OF TERMINALS.
- △ THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- △ DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
- △ ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
- △ COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC M0220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
- △ MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm
12. WARPAGE SHALL NOT EXCEED 0.10mm
- △ LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "a", ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY

# 50Ω, Low-Voltage, Quad SPST/Dual SPDT Analog Switches in UCSP

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

MAX4747-MAX4750

**TOP VIEW**

COMMON DIMENSIONS	
A	0.62±0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	∅0.35±0.03
D1	1.50 BASIC
E1	1.50 BASIC
e	0.50 BASIC
SD	0.25 BASIC
SE	0.25 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B16-1	2.02±0.05	2.02±0.05	NONE
B16-2	2.02±0.05	2.02±0.05	B3, C3
B16-3	2.02±0.05	2.02±0.05	B3, C2
B16-4	2.02±0.05	2.02±0.05	B2, C3
B16-5	2.02±0.05	2.02±0.05	B2, B3, C2, C3
B16-6	2.02±0.05	2.02±0.05	C3

NOTES:

- ALL DIMENSIONS ARE IN MILLIMETERS.
- PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.

**BOTTOM VIEW**

**SIDE VIEW**

<b>DALLAS SEMICONDUCTOR</b>			
<b>MAXIM</b>			
<small>PROPRIETARY INFORMATION</small>			
<small>TITLE:</small>			
PACKAGE OUTLINE, 4x4 UCSP			
<small>APPROVAL</small>	<small>DOCUMENT CTRL. NO.</small>	<small>REV.</small>	<small>1/1</small>
	21-0101	H	

## Revision History

Pages changed at Rev 2: 1, 2, 8, 9, 11, 13, 14, 15

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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