**Freescale Semiconductor**
Data Sheet: Technical Data

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# K10P100M72SF1

# K10 Sub-Family

## Supports: MK10DX128VLL7, MK10DX256VLL7, MK10DX64VMC7, MK10DX128VMC7, MK10DX256VMC7

### Features

- Operating Characteristics
  - Voltage range: 1.71 to 3.6 V
  - Flash write voltage range: 1.71 to 3.6 V
  - Temperature range (ambient): -40 to 105°C
- Clocks
  - 3 to 32 MHz crystal oscillator
  - 32 kHz crystal oscillator
  - Multi-purpose clock generator
- System peripherals
  - Multiple low-power modes to provide power optimization based on application requirements
  - 16-channel DMA controller, supporting up to 63 request sources
  - External watchdog monitor
  - Software watchdog
  - Low-leakage wakeup unit
- Security and integrity modules
  - Hardware CRC module to support fast cyclic redundancy checks
  - 128-bit unique identification (ID) number per chip
- Human-machine interface
  - Low-power hardware touch sensor interface (TSI)
  - General-purpose input/output
- Analog modules
  - Two 16-bit SAR ADCs
  - Programmable gain amplifier (PGA) (up to x64) integrated into each ADC
  - 12-bit DAC
  - Three analog comparators (CMP) containing a 6-bit DAC and programmable reference input
  - Voltage reference
- Timers
  - Programmable delay block
  - Eight-channel motor control/general purpose/PWM timer
  - Two 2-channel quadrature decoder/general purpose timers
  - Periodic interrupt timers
  - 16-bit low-power timer
  - Carrier modulator transmitter
  - Real-time clock
- Communication interfaces
  - Controller Area Network (CAN) module
  - Two SPI modules
  - Two I2C modules
  - Five UART modules
  - I2S module

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# 1 Ordering parts

## 1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to www.freescale.com and perform a part number search for the following device numbers: PK10 and MK10 .

# 2 Part identification

## 2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

## 2.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

## 2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

| Field | Description | Values |
|---|---|---|
| Q | Qualification status | • M = Fully qualified, general market flow<br>• P = Prequalification |
| K## | Kinetis family | • K10 |
| A | Key attribute | • D = Cortex-M4 w/ DSP<br>• F = Cortex-M4 w/ DSP and FPU |
| M | Flash memory type | • N = Program flash only<br>• X = Program flash and FlexMemory |

*Table continues on the next page...*

| Field | Description | Values |
|---|---|---|
| FFF | Program flash memory size | • 32 = 32 KB<br>• 64 = 64 KB<br>• 128 = 128 KB<br>• 256 = 256 KB<br>• 512 = 512 KB<br>• 1M0 = 1 MB |
| R | Silicon revision | • Z = Initial<br>• (Blank) = Main<br>• A = Revision after main |
| T | Temperature range (°C) | • V = –40 to 105<br>• C = –40 to 85 |
| PP | Package identifier | • FM = 32 QFN (5 mm x 5 mm)<br>• FT = 48 QFN (7 mm x 7 mm)<br>• LF = 48 LQFP (7 mm x 7 mm)<br>• LH = 64 LQFP (10 mm x 10 mm)<br>• MP = 64 MAPBGA (5 mm x 5 mm)<br>• LK = 80 LQFP (12 mm x 12 mm)<br>• LL = 100 LQFP (14 mm x 14 mm)<br>• MC = 121 MAPBGA (8 mm x 8 mm)<br>• LQ = 144 LQFP (20 mm x 20 mm)<br>• MD = 144 MAPBGA (13 mm x 13 mm)<br>• MJ = 256 MAPBGA (17 mm x 17 mm) |
| CC | Maximum CPU frequency (MHz) | • 5 = 50 MHz<br>• 7 = 72 MHz<br>• 10 = 100 MHz<br>• 12 = 120 MHz<br>• 15 = 150 MHz |
| N | Packaging type | • R = Tape and reel<br>• (Blank) = Trays |

## 2.4 Example

This is an example part number:

MK10DN512ZVMD10

# 3 Terminology and guidelines

## 3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

### 3.1.1 Example

This is an example of an operating requirement, which you must meet for the accompanying operating behaviors to be guaranteed:

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | 1.0 V core supply voltage | 0.9 | 1.1 | V |

## 3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

### 3.2.1 Example

This is an example of an operating behavior, which is guaranteed if you meet the accompanying operating requirements:

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $I_{WP}$ | Digital I/O weak pullup/ pulldown current | 10 | 130 | µA |

## 3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

### 3.3.1 Example

This is an example of an attribute:

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| CIN_D | Input capacitance: digital pins | — | 7 | pF |

## 3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

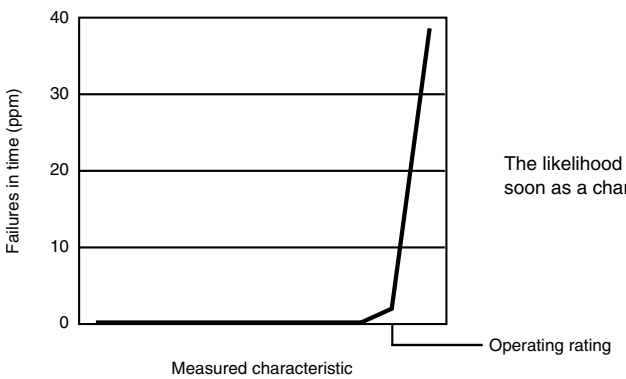
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

### 3.4.1 Example

This is an example of an operating rating:

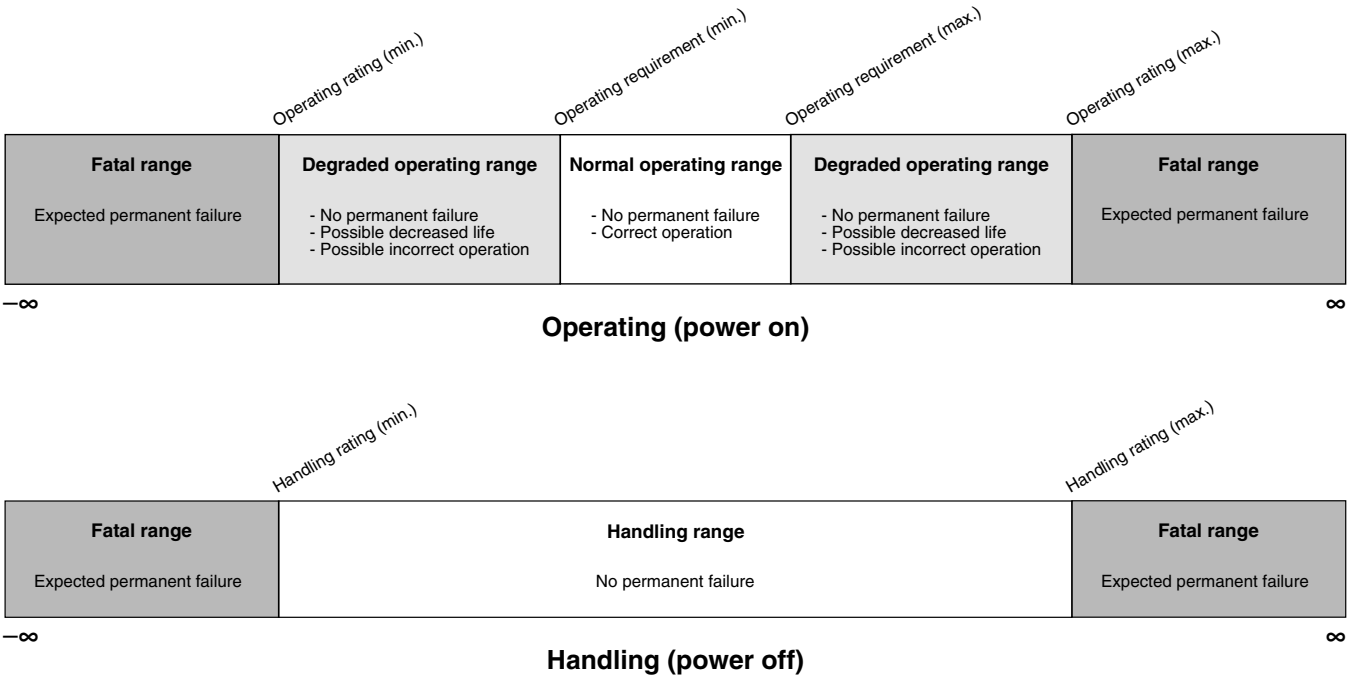
| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | 1.0 V core supply voltage | –0.3 | 1.2 | V |

## 3.5 Result of exceeding a rating




The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

## 3.6 Relationship between ratings and operating requirements




## 3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

## 3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

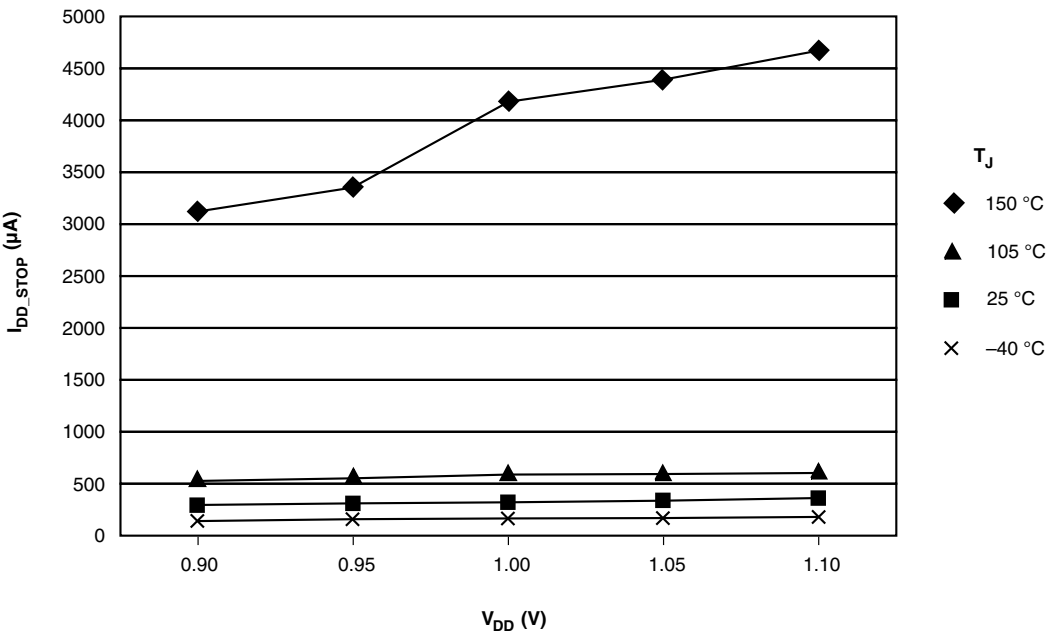
### 3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{WP}$ | Digital I/O weak pullup/pulldown current | 10 | 70 | 130 | µA |

### 3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:




## 3.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

| Symbol | Description | Value | Unit |
|---|---|---|---|
| $T_A$ | Ambient temperature | 25 | °C |
| $V_{DD}$ | 3.3 V supply voltage | 3.3 | V |

# 4 Ratings

## 4.1 Thermal handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $T_{STG}$ | Storage temperature | –55 | 150 | °C | 1 |
| $T_{SDR}$ | Solder temperature, lead-free | — | 260 | °C | 2 |

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 4.2 Moisture handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| MSL | Moisture sensitivity level | — | 3 | — | 1 |

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 4.3 ESD handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{HBM}$ | Electrostatic discharge voltage, human body model | -2000 | +2000 | V | 1 |
| $V_{CDM}$ | Electrostatic discharge voltage, charged-device model | -500 | +500 | V | 2 |
| $I_{LAT}$ | Latch-up current at ambient temperature of 105°C | -100 | +100 | mA | |

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

## 4.4 Voltage and current operating ratings

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Digital supply voltage | –0.3 | 3.8 | V |

*Table continues on the next page...*

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $I_{DD}$ | Digital supply current | — | 185 | mA |
| $V_{DIO}$ | Digital input voltage (except $\overline{RESET}$, EXTAL, and XTAL) | –0.3 | 5.5 | V |
| $V_{AIO}$ | Analog[1], $\overline{RESET}$, EXTAL, and XTAL input voltage | –0.3 | $V_{DD}$ + 0.3 | V |
| $I_D$ | Maximum current single pin limit (applies to all digital pins) | –25 | 25 | mA |
| $V_{DDA}$ | Analog supply voltage | $V_{DD}$ – 0.3 | $V_{DD}$ + 0.3 | V |
| $V_{BAT}$ | RTC battery supply voltage | –0.3 | 3.8 | V |

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

# 5 General

## 5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

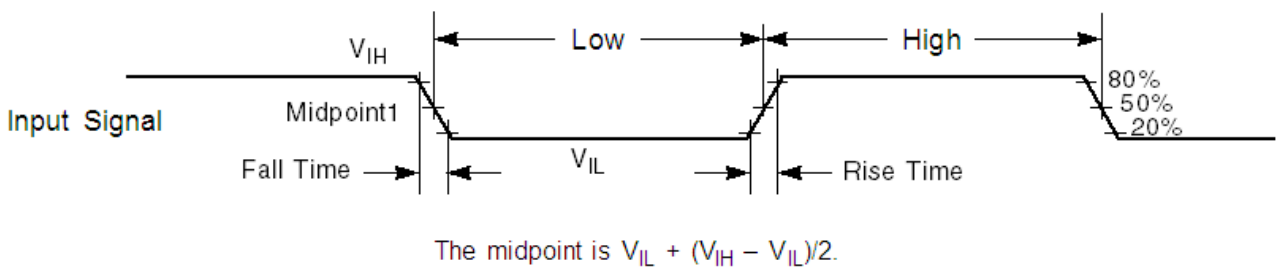



**Figure 1. Input signal measurement reference**

All digital I/O switching characteristics assume:

1. output pins
   - have $C_L$=30pF loads,
   - are configured for fast slew rate (PORTx_PCRn[SRE]=0), and
   - are configured for high drive strength (PORTx_PCRn[DSE]=1)
2. input pins
   - have their passive filter disabled (PORTx_PCRn[PFE]=0)

## 5.2 Nonswitching electrical specifications

## 5.2.1 Voltage and current operating requirements

**Table 1. Voltage and current operating requirements**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.71 | 3.6 | V | |
| $V_{DDA}$ | Analog supply voltage | 1.71 | 3.6 | V | |
| $V_{DD} – V_{DDA}$ | $V_{DD}$-to-$V_{DDA}$ differential voltage | –0.1 | 0.1 | V | |
| $V_{SS} – V_{SSA}$ | $V_{SS}$-to-$V_{SSA}$ differential voltage | –0.1 | 0.1 | V | |
| $V_{BAT}$ | RTC battery supply voltage | 1.71 | 3.6 | V | |
| $V_{IH}$ | Input high voltage<br>• 2.7 V ≤ $V_{DD}$ ≤ 3.6 V<br>• 1.7 V ≤ $V_{DD}$ ≤ 2.7 V | <br>0.7 × $V_{DD}$<br>0.75 × $V_{DD}$ | <br>—<br>— | <br>V<br>V | |
| $V_{IL}$ | Input low voltage<br>• 2.7 V ≤ $V_{DD}$ ≤ 3.6 V<br>• 1.7 V ≤ $V_{DD}$ ≤ 2.7 V | <br>—<br>— | <br>0.35 × $V_{DD}$<br>0.3 × $V_{DD}$ | <br>V<br>V | |
| $V_{HYS}$ | Input hysteresis | 0.06 × $V_{DD}$ | — | V | |
| $I_{ICDIO}$ | Digital pin negative DC injection current — single pin<br>• $V_{IN}$ < $V_{SS}$-0.3V | -5 | — | mA | 1 |
| $I_{ICAIO}$ | Analog[2], EXTAL, and XTAL pin DC injection current — single pin<br>• $V_{IN}$ < $V_{SS}$-0.3V (Negative current injection)<br>• $V_{IN}$ > $V_{DD}$+0.3V (Positive current injection) | <br>-5<br>— | <br>—<br>+5 | mA | 3 |
| $I_{ICcont}$ | Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins<br>• Negative current injection<br>• Positive current injection | <br>-25<br>— | <br>—<br>+25 | mA | |
| $V_{RAM}$ | $V_{DD}$ voltage required to retain RAM | 1.2 | — | V | |
| $V_{RFVBAT}$ | $V_{BAT}$ voltage required to retain the VBAT register file | $V_{POR_VBAT}$ | — | V | |

1. All 5 V tolerant digital I/O pins are internally clamped to $V_{SS}$ through a ESD protection diode. There is no diode connection to $V_{DD}$. If $V_{IN}$ greater than $V_{DIO_MIN}$ (=$V_{SS}$-0.3V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R=($V_{DIO_MIN}$-$V_{IN}$)/|$I_{IC}$|.
2. Analog pins are defined as pins that do not have an associated general purpose I/O port function.
3. All analog pins are internally clamped to $V_{SS}$ and $V_{DD}$ through ESD protection diodes. If $V_{IN}$ is greater than $V_{AIO_MIN}$ (=$V_{SS}$-0.3V) and $V_{IN}$ is less than $V_{AIO_MAX}$(=$V_{DD}$+0.3V) is observed, then there is no need to provide current limiting resistors at the pads. If these limits cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R=($V_{AIO_MIN}$-$V_{IN}$)/|$I_{IC}$|. The positive injection current limiting resistor is calculated as R=($V_{IN}$-$V_{AIO_MAX}$)/|$I_{IC}$|. Select the larger of these two calculated resistances.

## 5.2.2 LVD and POR operating requirements

### Table 2. $V_{DD}$ supply LVD and POR operating requirements

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{POR}$ | Falling VDD POR detect voltage | 0.8 | 1.1 | 1.5 | V | |
| $V_{LVDH}$ | Falling low-voltage detect threshold — high range (LVDV=01) | 2.48 | 2.56 | 2.64 | V | |
| | Low-voltage warning thresholds — high range | | | | | 1 |
| $V_{LVW1H}$ | • Level 1 falling (LVWV=00) | 2.62 | 2.70 | 2.78 | V | |
| $V_{LVW2H}$ | • Level 2 falling (LVWV=01) | 2.72 | 2.80 | 2.88 | V | |
| $V_{LVW3H}$ | • Level 3 falling (LVWV=10) | 2.82 | 2.90 | 2.98 | V | |
| $V_{LVW4H}$ | • Level 4 falling (LVWV=11) | 2.92 | 3.00 | 3.08 | V | |
| $V_{HYSH}$ | Low-voltage inhibit reset/recover hysteresis — high range | — | ±80 | — | mV | |
| $V_{LVDL}$ | Falling low-voltage detect threshold — low range (LVDV=00) | 1.54 | 1.60 | 1.66 | V | |
| | Low-voltage warning thresholds — low range | | | | | 1 |
| $V_{LVW1L}$ | • Level 1 falling (LVWV=00) | 1.74 | 1.80 | 1.86 | V | |
| $V_{LVW2L}$ | • Level 2 falling (LVWV=01) | 1.84 | 1.90 | 1.96 | V | |
| $V_{LVW3L}$ | • Level 3 falling (LVWV=10) | 1.94 | 2.00 | 2.06 | V | |
| $V_{LVW4L}$ | • Level 4 falling (LVWV=11) | 2.04 | 2.10 | 2.16 | V | |
| $V_{HYSL}$ | Low-voltage inhibit reset/recover hysteresis — low range | — | ±60 | — | mV | |
| $V_{BG}$ | Bandgap voltage reference | 0.97 | 1.00 | 1.03 | V | |
| $t_{LPO}$ | Internal low power oscillator period — factory trimmed | 900 | 1000 | 1100 | µs | |

1. Rising thresholds are falling threshold + hysteresis voltage

### Table 3. VBAT power operating requirements

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{POR_VBAT}$ | Falling VBAT supply POR detect voltage | 0.8 | 1.1 | 1.5 | V | |

## 5.2.3 Voltage and current operating behaviors

**Table 4. Voltage and current operating behaviors**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{OH}$ | Output high voltage — high drive strength | | | | |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OH}$ = -9mA | $V_{DD}$ – 0.5 | — | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OH}$ = -3mA | $V_{DD}$ – 0.5 | — | V | |
| | Output high voltage — low drive strength | | | | |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OH}$ = -2mA | $V_{DD}$ – 0.5 | — | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OH}$ = -0.6mA | $V_{DD}$ – 0.5 | — | V | |
| $I_{OHT}$ | Output high current total for all ports | — | 100 | mA | |
| $V_{OL}$ | Output low voltage — high drive strength | | | | |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OL}$ = 9mA | — | 0.5 | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OL}$ = 3mA | — | 0.5 | V | |
| | Output low voltage — low drive strength | | | | |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OL}$ = 2mA | — | 0.5 | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OL}$ = 0.6mA | — | 0.5 | V | |
| $I_{OLT}$ | Output low current total for all ports | — | 100 | mA | |
| $I_{IN}$ | Input leakage current (per pin) for full temperature range | — | 1 | µA | 1 |
| $I_{IN}$ | Input leakage current (per pin) at 25°C | — | 0.025 | µA | 1 |
| $I_{OZ}$ | Hi-Z (off-state) leakage current (per pin) | — | 1 | µA | |
| $R_{PU}$ | Internal pullup resistors | 20 | 50 | kΩ | 2 |
| $R_{PD}$ | Internal pulldown resistors | 20 | 50 | kΩ | 3 |

1. Measured at VDD=3.6V
2. Measured at $V_{DD}$ supply voltage = $V_{DD}$ min and Vinput = $V_{SS}$
3. Measured at $V_{DD}$ supply voltage = $V_{DD}$ min and Vinput = $V_{DD}$

## 5.2.4 Power mode transition operating behaviors

All specifications except $t_{POR}$, and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 72 MHz
- Bus clock = 36 MHz
- FlexBus clock = 36 MHz
- Flash clock = 24 MHz

**Table 5. Power mode transition operating behaviors**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $t_{POR}$ | After a POR event, amount of time from the point $V_{DD}$ reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip. | — | 300 | µs | 1 |
| | • VLLS1 → RUN | — | 112 | µs | |
| | • VLLS2 → RUN | — | 74 | µs | |
| | • VLLS3 → RUN | — | 73 | µs | |
| | • LLS → RUN | — | 5.9 | µs | |
| | • VLPS → RUN | — | 5.8 | µs | |
| | • STOP → RUN | — | 4.2 | µs | |

1. Normal boot (FTFL_OPT[LPBOOT]=1)

## 5.2.5 Power consumption operating behaviors

**Table 6. Power consumption operating behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DDA}$ | Analog supply current | — | — | See note | mA | 1 |
| $I_{DD_RUN}$ | Run mode current — all peripheral clocks disabled, code executing from flash | | | | | 2 |
| | • @ 1.8V | — | 21.5 | 25 | mA | |
| | • @ 3.0V | — | 21.5 | 30 | mA | |
| $I_{DD_RUN}$ | Run mode current — all peripheral clocks enabled, code executing from flash | | | | | 3, 4 |
| | • @ 1.8V | — | 31 | 34 | mA | |
| | • @ 3.0V | | | | | |
| | • @ 25°C | — | 31 | 34 | mA | |
| | • @ 125°C | — | 32 | 39 | mA | |
| $I_{DD_WAIT}$ | Wait mode high frequency current at 3.0 V — all peripheral clocks disabled | — | 12.5 | — | mA | 2 |
| $I_{DD_WAIT}$ | Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled | — | 7.2 | — | mA | 5 |
| $I_{DD_VLPR}$ | Very-low-power run mode current at 3.0 V — all peripheral clocks disabled | — | 0.996 | — | mA | 6 |
| $I_{DD_VLPR}$ | Very-low-power run mode current at 3.0 V — all peripheral clocks enabled | — | 1.46 | — | mA | 7 |

*Table continues on the next page...*

## Table 6. Power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DD_VLPW}$ | Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled | — | 0.61 | — | mA | 8 |
| $I_{DD_STOP}$ | Stop mode current at 3.0 V | | | | | |
| | • @ –40 to 25°C | — | 0.35 | 0.567 | mA | |
| | • @ 70°C | — | 0.384 | 0.793 | mA | |
| | • @ 105°C | — | 0.628 | 1.2 | mA | |
| $I_{DD_VLPS}$ | Very-low-power stop mode current at 3.0 V | | | | | |
| | • @ –40 to 25°C | — | 5.9 | 32.7 | µA | |
| | • @ 70°C | — | 26.1 | 59.8 | µA | |
| | • @ 105°C | — | 98.1 | 188 | µA | |
| $I_{DD_LLS}$ | Low leakage stop mode current at 3.0 V | | | | | 9 |
| | • @ –40 to 25°C | — | 2.6 | 8.6 | µA | |
| | • @ 70°C | — | 10.3 | 29.1 | µA | |
| | • @ 105°C | — | 42.5 | 92.5 | µA | |
| $I_{DD_VLLS3}$ | Very low-leakage stop mode 3 current at 3.0 V | | | | | 9 |
| | • @ –40 to 25°C | — | 1.9 | 5.8 | µA | |
| | • @ 70°C | — | 6.9 | 12.1 | µA | |
| | • @ 105°C | — | 28.1 | 41.9 | µA | |
| $I_{DD_VLLS2}$ | Very low-leakage stop mode 2 current at 3.0 V | | | | | |
| | • @ –40 to 25°C | — | 1.59 | 5.5 | µA | |
| | • @ 70°C | — | 4.3 | 9.5 | µA | |
| | • @ 105°C | — | 17.5 | 34 | µA | |
| $I_{DD_VLLS1}$ | Very low-leakage stop mode 1 current at 3.0 V | | | | | |
| | • @ –40 to 25°C | — | 1.47 | 5.4 | µA | |
| | • @ 70°C | — | 2.97 | 8.1 | µA | |
| | • @ 105°C | — | 12.41 | 32 | µA | |
| $I_{DD_VBAT}$ | Average current with RTC and 32kHz disabled at 3.0 V | | | | | |
| | • @ –40 to 25°C | — | 0.19 | 0.22 | µA | |
| | • @ 70°C | — | 0.49 | 0.64 | µA | |
| | • @ 105°C | — | 2.2 | 3.2 | µA | |

*Table continues on the next page...*

**Table 6. Power consumption operating behaviors (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DD_VBAT}$ | Average current when CPU is not accessing RTC registers | | | | | 10 |
| | • @ 1.8V | | | | | |
| | • @ –40 to 25°C | — | 0.57 | 0.67 | µA | |
| | • @ 70°C | — | 0.90 | 1.2 | µA | |
| | • @ 105°C | — | 2.4 | 3.5 | µA | |
| | • @ 3.0V | | | | | |
| | • @ –40 to 25°C | — | 0.67 | 0.94 | µA | |
| | • @ 70°C | — | 1.0 | 1.4 | µA | |
| | • @ 105°C | — | 2.7 | 3.9 | µA | |

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 72MHz core and system clock, 36MHz bus and FlexBus clock, and 24MHz flash clock. MCG configured for FEE mode. All peripheral clocks disabled.
3. 72MHz core and system clock, 36MHz bus and FlexBus clock, and 24MHz flash clock. MCG configured for FEE mode. All peripheral clocks enabled.
4. Max values are measured with CPU executing DSP instructions.
5. 25MHz core, system, bus, FlexBus and flash clock. MCG configured for FEI mode.
6. 4 MHz core and system clock, 4 MHz FlexBus and bus clock, and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
7. 4 MHz core and system clock, 4 MHz FlexBus and bus clock, and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
8. 4 MHz core and system clock, 4 MHz FlexBus and bus clock, and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
9. Data reflects devices with 128 KB of RAM.
10. Includes 32kHz oscillator current and RTC operation.

### 5.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode for 50 MHz and lower frequencies. MCG in FEE mode at greater than 50 MHz frequencies.
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFL

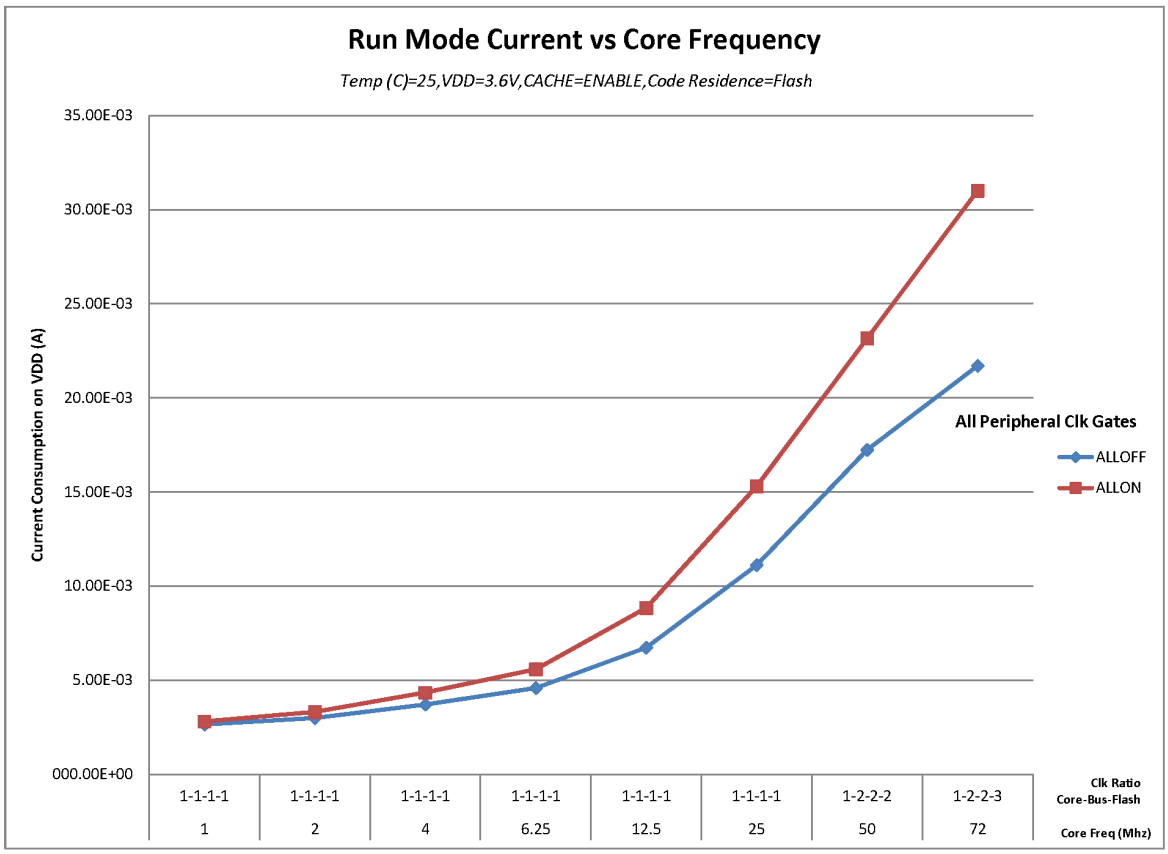



**Figure 2. Run mode supply current vs. core frequency**

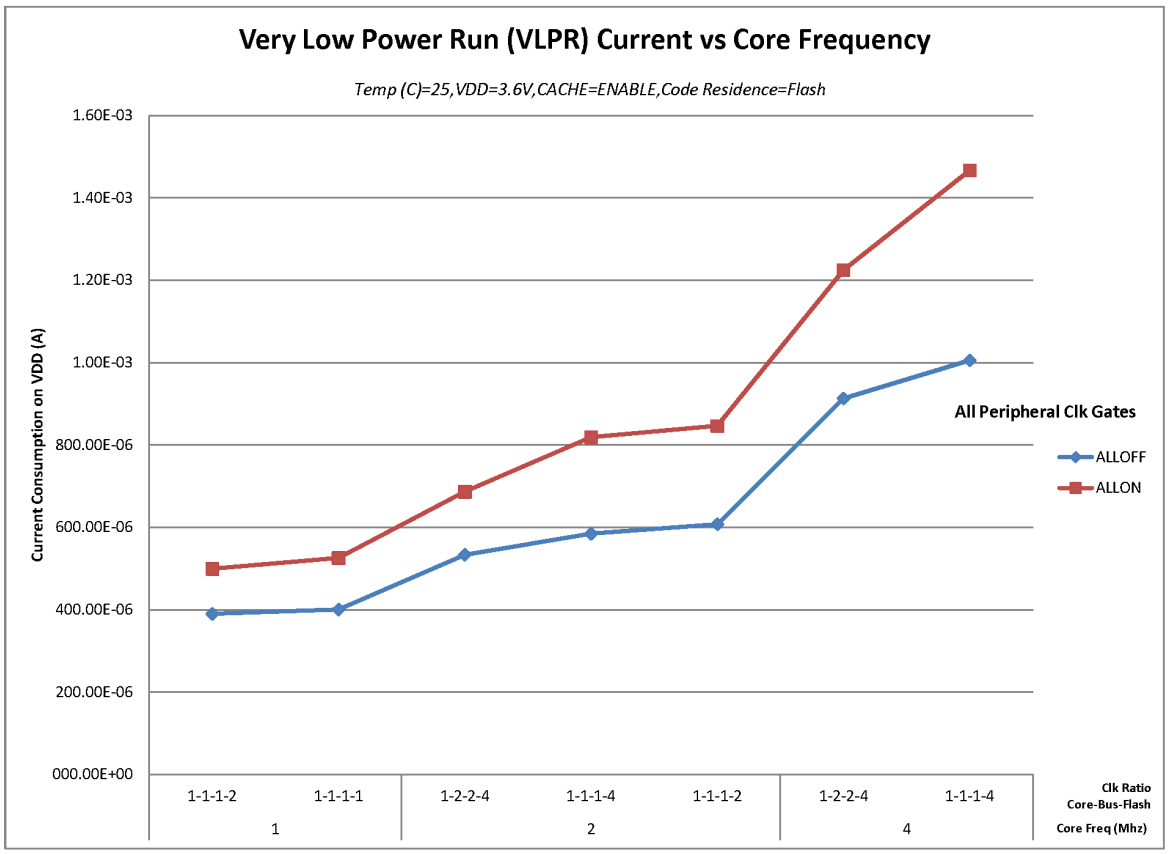



**Figure 3. VLPR mode supply current vs. core frequency**

## 5.2.6 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

## 5.2.7 Capacitance attributes

**Table 7. Capacitance attributes**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $C_{IN_A}$ | Input capacitance: analog pins | — | 7 | pF |
| $C_{IN_D}$ | Input capacitance: digital pins | — | 7 | pF |

# 5.3 Switching specifications

## 5.3.1 Device clock specifications

**Table 8. Device clock specifications**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| Normal run mode | | | | | |
| $f_{SYS}$ | System and core clock | — | 72 | MHz | |
| $f_{BUS}$ | Bus clock | — | 50 | MHz | |
| FB_CLK | FlexBus clock | — | 50 | MHz | |
| $f_{FLASH}$ | Flash clock | — | 25 | MHz | |
| $f_{LPTMR}$ | LPTMR clock | — | 25 | MHz | |
| VLPR mode[1] | | | | | |
| $f_{SYS}$ | System and core clock | — | 4 | MHz | |
| $f_{BUS}$ | Bus clock | — | 4 | MHz | |
| FB_CLK | FlexBus clock | — | 4 | MHz | |
| $f_{FLASH}$ | Flash clock | — | 0.5 | MHz | |
| $f_{ERCLK}$ | External reference clock | — | 16 | MHz | |
| $f_{LPTMR_pin}$ | LPTMR clock | — | 25 | MHz | |
| $f_{LPTMR_ERCLK}$ | LPTMR external reference clock | — | 16 | MHz | |
| $f_{FlexCAN_ERCLK}$ | FlexCAN external reference clock | — | 8 | MHz | |
| $f_{I2S_MCLK}$ | I2S master clock | — | 12.5 | MHz | |
| $f_{I2S_BCLK}$ | I2S bit clock | — | 4 | MHz | |

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

## 5.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, CAN, CMT, and $I^2C$ signals.

**Table 9. General switching specifications**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| | GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path | 1.5 | — | Bus clock cycles | 1, 2 |
| | GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path | 100 | — | ns | 3 |

*Table continues on the next page...*

**Table 9. General switching specifications (continued)**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| | GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path | 16 | — | ns | 3 |
| | External reset pulse width (digital glitch filter disabled) | 100 | — | ns | 3 |
| | Mode select ($\overline{\text{EZP_CS}}$) hold time after reset deassertion | 2 | — | Bus clock cycles | |
| | Port rise and fall time (high drive strength)<br>• Slew disabled<br>• $1.71 \le V_{DD} \le 2.7V$<br>• $2.7 \le V_{DD} \le 3.6V$<br>• Slew enabled<br>• $1.71 \le V_{DD} \le 2.7V$<br>• $2.7 \le V_{DD} \le 3.6V$ | <br><br>—<br>—<br><br>—<br>— | <br><br>12<br>6<br><br>36<br>24 | <br><br>ns<br>ns<br><br>ns<br>ns | 4 |
| | Port rise and fall time (low drive strength)<br>• Slew disabled<br>• $1.71 \le V_{DD} \le 2.7V$<br>• $2.7 \le V_{DD} \le 3.6V$<br>• Slew enabled<br>• $1.71 \le V_{DD} \le 2.7V$<br>• $2.7 \le V_{DD} \le 3.6V$ | <br><br>—<br>—<br><br>—<br>— | <br><br>12<br>6<br><br>36<br>24 | <br><br>ns<br>ns<br><br>ns<br>ns | 5 |

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 75pF load
5. 15pF load

# 5.4 Thermal specifications

## 5.4.1 Thermal operating requirements

**Table 10. Thermal operating requirements**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $T_J$ | Die junction temperature | –40 | 125 | °C |
| $T_A$ | Ambient temperature | –40 | 105 | °C |

## 5.4.2 Thermal attributes

| Board type | Symbol | Description | 121 MAPBGA | 100 LQFP | Unit | Notes |
|---|---|---|---|---|---|---|
| Single-layer (1s) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 74 | 52 | °C/W | 1, 2 |
| Four-layer (2s2p) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 42 | 40 | °C/W | 1, 3 |
| Single-layer (1s) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./ min. air speed) | 62 | 42 | °C/W | 1,3 |
| Four-layer (2s2p) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./ min. air speed) | 38 | 34 | °C/W | 1,3 |
| — | $R_{\theta JB}$ | Thermal resistance, junction to board | 23 | 25 | °C/W | 4 |
| — | $R_{\theta JC}$ | Thermal resistance, junction to case | 19 | 12 | °C/W | 5 |
| — | $\Psi_{JT}$ | Thermal characterization parameter, junction to package top outside center (natural convection) | 4 | 2 | °C/W | 6 |

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. For the LQFP, the board meets the JESD51-3 specification. For the MAPBGA, the board meets the JESD51-9 specification.
3. Determined according to JEDEC Standard JESD51-6, *Integrated Circuits Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)* with the board horizontal. For the LQFP, the board meets the JESD51-7 specification.
4. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*. Board temperature is measured on the top surface of the board near the package.

5. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
6. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

# 6 Peripheral operating requirements and behaviors

## 6.1 Core modules

### 6.1.1 Debug trace timing specifications

**Table 11. Debug trace operating behaviors**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $T_{cyc}$ | Clock period | Frequency dependent | | MHz |
| $T_{wl}$ | Low pulse width | 2 | — | ns |
| $T_{wh}$ | High pulse width | 2 | — | ns |
| $T_r$ | Clock and data rise time | — | 3 | ns |
| $T_f$ | Clock and data fall time | — | 3 | ns |
| $T_s$ | Data setup | 3 | — | ns |
| $T_h$ | Data hold | 2 | — | ns |

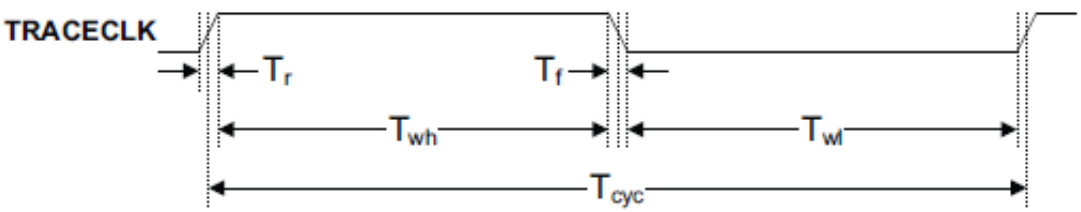



**Figure 4. TRACE_CLKOUT specifications**

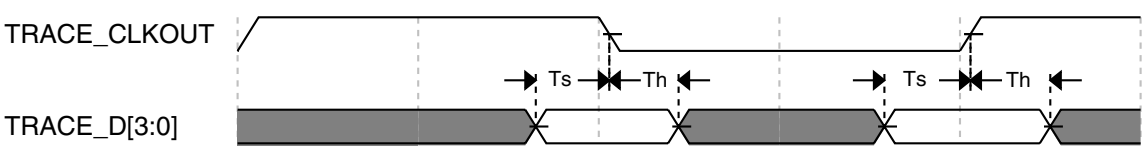



**Figure 5. Trace data specifications**

## 6.1.2 JTAG electricals

### Table 12. JTAG limited voltage range electricals

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 2.7 | 3.6 | V |
| J1 | TCLK frequency of operation | | | MHz |
| | • Boundary Scan | 0 | 10 | |
| | • JTAG and CJTAG | 0 | 25 | |
| | • Serial Wire Debug | 0 | 50 | |
| J2 | TCLK cycle period | 1/J1 | — | ns |
| J3 | TCLK clock pulse width | | | |
| | • Boundary Scan | 50 | — | ns |
| | • JTAG and CJTAG | 20 | — | ns |
| | • Serial Wire Debug | 10 | — | ns |
| J4 | TCLK rise and fall times | — | 3 | ns |
| J5 | Boundary scan input data setup time to TCLK rise | 20 | — | ns |
| J6 | Boundary scan input data hold time after TCLK rise | 0 | — | ns |
| J7 | TCLK low to boundary scan output data valid | — | 25 | ns |
| J8 | TCLK low to boundary scan output high-Z | — | 25 | ns |
| J9 | TMS, TDI input data setup time to TCLK rise | 8 | — | ns |
| J10 | TMS, TDI input data hold time after TCLK rise | 1 | — | ns |
| J11 | TCLK low to TDO data valid | — | 17 | ns |
| J12 | TCLK low to TDO high-Z | — | 17 | ns |
| J13 | $\overline{\text{TRST}}$ assert time | 100 | — | ns |
| J14 | $\overline{\text{TRST}}$ setup time (negation) to TCLK high | 8 | — | ns |

### Table 13. JTAG full voltage range electricals

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V |
| J1 | TCLK frequency of operation | | | MHz |
| | • Boundary Scan | 0 | 10 | |
| | • JTAG and CJTAG | 0 | 20 | |
| | • Serial Wire Debug | 0 | 40 | |
| J2 | TCLK cycle period | 1/J1 | — | ns |
| J3 | TCLK clock pulse width | | | |
| | • Boundary Scan | 50 | — | ns |
| | • JTAG and CJTAG | 25 | — | ns |
| | • Serial Wire Debug | 12.5 | — | ns |
| J4 | TCLK rise and fall times | — | 3 | ns |

*Table continues on the next page...*

**Table 13. JTAG full voltage range electricals (continued)**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| J5 | Boundary scan input data setup time to TCLK rise | 20 | — | ns |
| J6 | Boundary scan input data hold time after TCLK rise | 0 | — | ns |
| J7 | TCLK low to boundary scan output data valid | — | 25 | ns |
| J8 | TCLK low to boundary scan output high-Z | — | 25 | ns |
| J9 | TMS, TDI input data setup time to TCLK rise | 8 | — | ns |
| J10 | TMS, TDI input data hold time after TCLK rise | 1.4 | — | ns |
| J11 | TCLK low to TDO data valid | — | 22.1 | ns |
| J12 | TCLK low to TDO high-Z | — | 22.1 | ns |
| J13 | $\overline{\text{TRST}}$ assert time | 100 | — | ns |
| J14 | $\overline{\text{TRST}}$ setup time (negation) to TCLK high | 8 | — | ns |

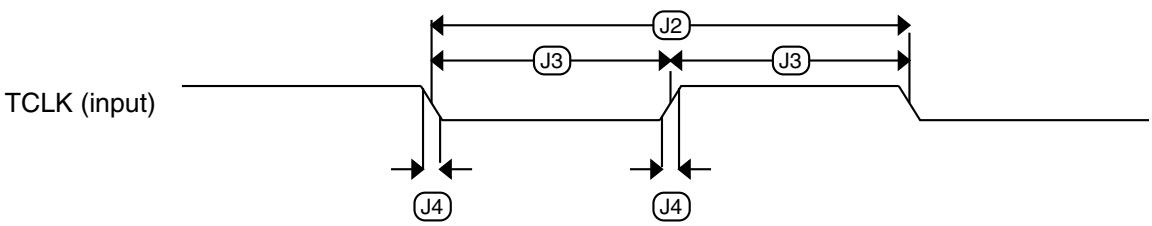



**Figure 6. Test clock input timing**

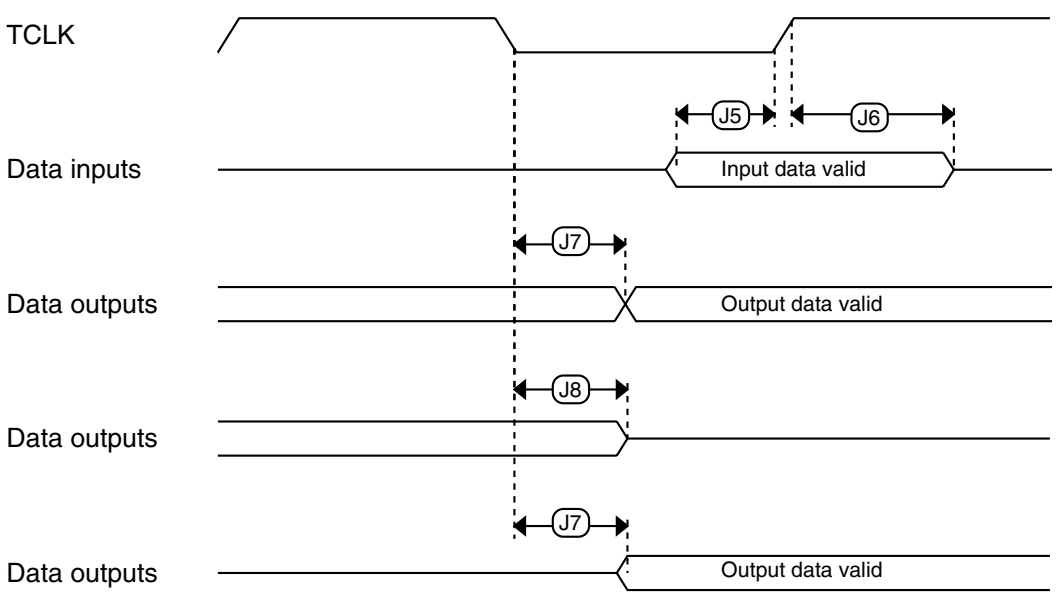



**Figure 7. Boundary scan (JTAG) timing**

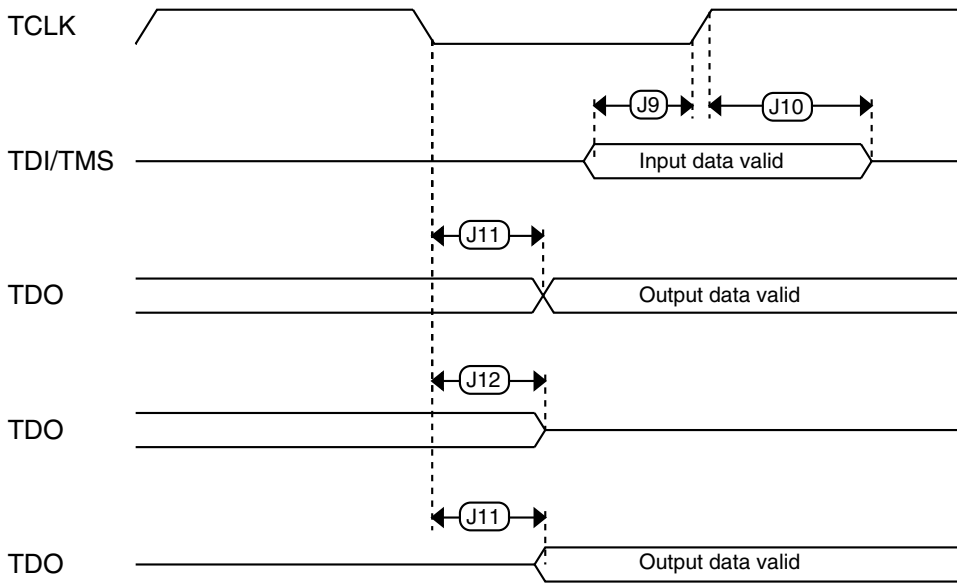



**Figure 8. Test Access Port timing**

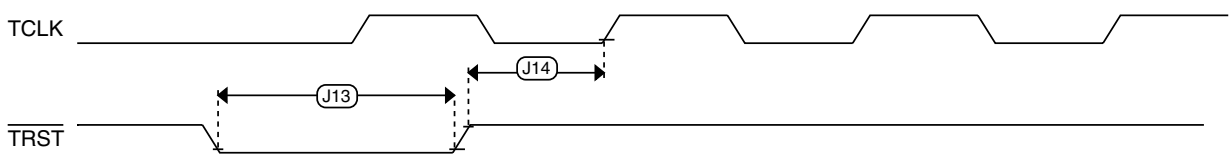



**Figure 9. $\overline{\text{TRST}}$ timing**

## 6.2 System modules

There are no specifications necessary for the device's system modules.

## 6.3 Clock modules

## 6.3.1 MCG specifications

**Table 14. MCG specifications**

| Symbol | Description | | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $f_{ints_ft}$ | Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C | | — | 32.768 | — | kHz | |
| $f_{ints_t}$ | Internal reference frequency (slow clock) — user trimmed | | 31.25 | — | 39.0625 | kHz | |
| $\Delta_{fdco_res_t}$ | Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM | | — | ± 0.3 | ± 0.6 | $\%f_{dco}$ | 1 |
| $\Delta f_{dco_res_t}$ | Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only | | — | ± 0.2 | ± 0.5 | $\%f_{dco}$ | 1 |
| $\Delta f_{dco_t}$ | Total deviation of trimmed average DCO output frequency over voltage and temperature | | — | +0.5/-0.7 | — | $\%f_{dco}$ | 1 |
| $\Delta f_{dco_t}$ | Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C | | — | ± 0.3 | ± 0.3 | $\%f_{dco}$ | 1 |
| $f_{intf_ft}$ | Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C | | — | 4 | — | MHz | |
| $f_{intf_t}$ | Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C | | 3 | — | 5 | MHz | |
| $f_{loc_low}$ | Loss of external clock minimum frequency — RANGE = 00 | | (3/5) x $f_{ints_t}$ | — | — | kHz | |
| $f_{loc_high}$ | Loss of external clock minimum frequency — RANGE = 01, 10, or 11 | | (16/5) x $f_{ints_t}$ | — | — | kHz | |
| FLL | | | | | | | |
| $f_{fll_ref}$ | FLL reference frequency range | | 31.25 | — | 39.0625 | kHz | |
| $f_{dco}$ | DCO output frequency range | Low range (DRS=00) 640 × $f_{fll_ref}$ | 20 | 20.97 | 25 | MHz | 2, 3 |
| | | Mid range (DRS=01) 1280 × $f_{fll_ref}$ | 40 | 41.94 | 50 | MHz | |
| | | Mid-high range (DRS=10) 1920 × $f_{fll_ref}$ | 60 | 62.91 | 75 | MHz | |
| | | High range (DRS=11) 2560 × $f_{fll_ref}$ | 80 | 83.89 | 100 | MHz | |
| $f_{dco_t_DMX32}$ | DCO output frequency | Low range (DRS=00) 732 × $f_{fll_ref}$ | — | 23.99 | — | MHz | 4, 5 |
| | | Mid range (DRS=01) 1464 × $f_{fll_ref}$ | — | 47.97 | — | MHz | |
| | | Mid-high range (DRS=10) 2197 × $f_{fll_ref}$ | — | 71.99 | — | MHz | |
| | | High range (DRS=11) 2929 × $f_{fll_ref}$ | — | 95.98 | — | MHz | |

*Table continues on the next page...*

**Table 14. MCG specifications (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $J_{cyc_fll}$ | FLL period jitter<br>• $f_{VCO}$ = 48 MHz<br>• $f_{VCO}$ = 98 MHz | —<br>— | 180<br>150 | —<br>— | ps | |
| $t_{fll_acquire}$ | FLL target frequency acquisition time | — | — | 1 | ms | 6 |
| PLL | | | | | | |
| $f_{vco}$ | VCO operating frequency | 48.0 | — | 100 | MHz | |
| $I_{pll}$ | PLL operating current<br>• PLL @ 96 MHz ($f_{osc_hi_1}$ = 8 MHz, $f_{pll_ref}$ = 2 MHz, VDIV multiplier = 48) | — | 1060 | — | µA | 7 |
| $I_{pll}$ | PLL operating current<br>• PLL @ 48 MHz ($f_{osc_hi_1}$ = 8 MHz, $f_{pll_ref}$ = 2 MHz, VDIV multiplier = 24) | — | 600 | — | µA | 7 |
| $f_{pll_ref}$ | PLL reference frequency range | 2.0 | — | 4.0 | MHz | |
| $J_{cyc_pll}$ | PLL period jitter (RMS)<br>• $f_{vco}$ = 48 MHz<br>• $f_{vco}$ = 100 MHz | <br>—<br>— | <br>120<br>50 | <br>—<br>— | <br>ps<br>ps | 8 |
| $J_{acc_pll}$ | PLL accumulated jitter over 1µs (RMS)<br>• $f_{vco}$ = 48 MHz<br>• $f_{vco}$ = 100 MHz | <br>—<br>— | <br>1350<br>600 | <br>—<br>— | <br>ps<br>ps | 8 |
| $D_{lock}$ | Lock entry frequency tolerance | ± 1.49 | — | ± 2.98 | % | |
| $D_{unl}$ | Lock exit frequency tolerance | ± 4.47 | — | ± 5.97 | % | |
| $t_{pll_lock}$ | Lock detector detection time | — | — | $150 \times 10^{-6} + 1075(1/f_{pll_ref})$ | s | 9 |

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation ($\Delta f_{dco_t}$) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Excludes any oscillator currents that are also consuming power while PLL is in operation.
8. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
9. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

## 6.3.2 Oscillator electrical specifications

This section provides the electrical characteristics of the module.

### 6.3.2.1 Oscillator DC electrical specifications

**Table 15. Oscillator DC electrical specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.71 | — | 3.6 | V | |
| $I_{DDOSC}$ | Supply current — low-power mode (HGO=0) | | | | | 1 |
| | • 32 kHz | — | 500 | — | nA | |
| | • 4 MHz | — | 200 | — | µA | |
| | • 8 MHz (RANGE=01) | — | 300 | — | µA | |
| | • 16 MHz | — | 950 | — | µA | |
| | • 24 MHz | — | 1.2 | — | mA | |
| | • 32 MHz | — | 1.5 | — | mA | |
| $I_{DDOSC}$ | Supply current — high gain mode (HGO=1) | | | | | 1 |
| | • 32 kHz | — | 25 | — | µA | |
| | • 4 MHz | — | 400 | — | µA | |
| | • 8 MHz (RANGE=01) | — | 500 | — | µA | |
| | • 16 MHz | — | 2.5 | — | mA | |
| | • 24 MHz | — | 3 | — | mA | |
| | • 32 MHz | — | 4 | — | mA | |
| $C_x$ | EXTAL load capacitance | — | — | — | | 2, 3 |
| $C_y$ | XTAL load capacitance | — | — | — | | 2, 3 |
| $R_F$ | Feedback resistor — low-frequency, low-power mode (HGO=0) | — | — | — | MΩ | 2, 4 |
| | Feedback resistor — low-frequency, high-gain mode (HGO=1) | — | 10 | — | MΩ | |
| | Feedback resistor — high-frequency, low-power mode (HGO=0) | — | — | — | MΩ | |
| | Feedback resistor — high-frequency, high-gain mode (HGO=1) | — | 1 | — | MΩ | |
| $R_S$ | Series resistor — low-frequency, low-power mode (HGO=0) | — | — | — | kΩ | |
| | Series resistor — low-frequency, high-gain mode (HGO=1) | — | 200 | — | kΩ | |
| | Series resistor — high-frequency, low-power mode (HGO=0) | — | — | — | kΩ | |
| | Series resistor — high-frequency, high-gain mode (HGO=1) | — | 0 | — | kΩ | |

*Table continues on the next page...*

**Table 15. Oscillator DC electrical specifications (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{pp}$[5] | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1) | — | $V_{DD}$ | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1) | — | $V_{DD}$ | — | V | |

1. $V_{DD}$=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. $C_x$,$C_y$ can be provided by using either the integrated capacitors or by using external components.
4. When low power mode is selected, $R_F$ is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

## 6.3.2.2 Oscillator frequency specifications

**Table 16. Oscillator frequency specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $f_{osc_lo}$ | Oscillator crystal or resonator frequency — low frequency mode (MCG_C2[RANGE]=00) | 32 | — | 40 | kHz | |
| $f_{osc_hi_1}$ | Oscillator crystal or resonator frequency — high frequency mode (low range) (MCG_C2[RANGE]=01) | 3 | — | 8 | MHz | |
| $f_{osc_hi_2}$ | Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x) | 8 | — | 32 | MHz | |
| $f_{ec_extal}$ | Input clock frequency (external clock mode) | — | — | 50 | MHz | 1, 2 |
| $t_{dc_extal}$ | Input clock duty cycle (external clock mode) | 40 | 50 | 60 | % | |
| $t_{cst}$ | Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0) | — | 750 | — | ms | 3, 4 |
| | Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1) | — | 250 | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0) | — | 0.6 | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1) | — | 1 | — | ms | |

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FBE to FEI mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.

4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

**NOTE**

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

## 6.3.3 32 kHz Oscillator Electrical Characteristics

This section describes the module electrical characteristics.

### 6.3.3.1 32 kHz oscillator DC electrical specifications

**Table 17. 32kHz oscillator DC electrical specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{BAT}$ | Supply voltage | 1.71 | — | 3.6 | V |
| $R_F$ | Internal feedback resistor | — | 100 | — | MΩ |
| $C_{para}$ | Parasitical capacitance of EXTAL32 and XTAL32 | — | 5 | 7 | pF |
| $V_{pp}$[1] | Peak-to-peak amplitude of oscillation | — | 0.6 | — | V |

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

### 6.3.3.2 32kHz oscillator frequency specifications

**Table 18. 32kHz oscillator frequency specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $f_{osc_lo}$ | Oscillator crystal | — | 32.768 | — | kHz | |
| $t_{start}$ | Crystal start-up time | — | 1000 | — | ms | 1 |
| $v_{ec_extal32}$ | Externally provided input clock amplitude | 700 | — | $V_{BAT}$ | mV | 2, 3 |

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and $V_{IH}$ and $V_{IL}$ specifications do not apply. The voltage of the applied clock must be within the range of $V_{SS}$ to $V_{BAT}$.

# 6.4 Memories and memory interfaces

## 6.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

### 6.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

**Table 19. NVM program/erase timing specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{hvpgm4}$ | Longword Program high-voltage time | — | 7.5 | 18 | µs | |
| $t_{hversscr}$ | Sector Erase high-voltage time | — | 13 | 113 | ms | 1 |
| $t_{hversblk32k}$ | Erase Block high-voltage time for 32 KB | — | 52 | 452 | ms | 1 |
| $t_{hversblk256k}$ | Erase Block high-voltage time for 256 KB | — | 104 | 904 | ms | 1 |

1. Maximum time based on expectations at cycling end-of-life.

### 6.4.1.2 Flash timing specifications — commands

**Table 20. Flash command timing specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | Read 1s Block execution time | | | | | |
| $t_{rd1blk32k}$ | • 32 KB data flash | — | — | 0.5 | ms | |
| $t_{rd1blk256k}$ | • 256 KB program flash | — | — | 1.7 | ms | |
| $t_{rd1sec1k}$ | Read 1s Section execution time (data flash sector) | — | — | 60 | µs | 1 |
| $t_{rd1sec2k}$ | Read 1s Section execution time (program flash sector) | — | — | 60 | µs | 1 |
| $t_{pgmchk}$ | Program Check execution time | — | — | 45 | µs | 1 |
| $t_{rdrsrc}$ | Read Resource execution time | — | — | 30 | µs | 1 |
| $t_{pgm4}$ | Program Longword execution time | — | 65 | 145 | µs | |
| | Erase Flash Block execution time | | | | | 2 |
| $t_{ersblk32k}$ | • 32 KB data flash | — | 55 | 465 | ms | |
| $t_{ersblk256k}$ | • 256 KB program flash | — | 122 | 985 | ms | |
| $t_{ersscr}$ | Erase Flash Sector execution time | — | 14 | 114 | ms | 2 |
| | Program Section execution time | | | | | |
| $t_{pgmsec512p}$ | • 512 B program flash | — | 2.4 | — | ms | |
| $t_{pgmsec512d}$ | • 512 B data flash | — | 4.7 | — | ms | |
| $t_{pgmsec1kp}$ | • 1 KB program flash | — | 4.7 | — | ms | |
| $t_{pgmsec1kd}$ | • 1 KB data flash | — | 9.3 | — | ms | |
| $t_{rd1all}$ | Read 1s All Blocks execution time | — | — | 1.8 | ms | |
| $t_{rdonce}$ | Read Once execution time | — | — | 25 | µs | 1 |
| $t_{pgmonce}$ | Program Once execution time | — | 65 | — | µs | |
| $t_{ersall}$ | Erase All Blocks execution time | — | 175 | 1500 | ms | 2 |

*Table continues on the next page...*

## Table 20. Flash command timing specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{vfykey}$ | Verify Backdoor Access Key execution time | — | — | 30 | µs | 1 |
| | Swap Control execution time | | | | | |
| $t_{swapx01}$ | • control code 0x01 | — | 200 | — | µs | |
| $t_{swapx02}$ | • control code 0x02 | — | 70 | 150 | µs | |
| $t_{swapx04}$ | • control code 0x04 | — | 70 | 150 | µs | |
| $t_{swapx08}$ | • control code 0x08 | — | — | 30 | µs | |
| | Program Partition for EEPROM execution time | | | | | |
| $t_{pgmpart32k}$ | • 32 KB FlexNVM | — | 70 | — | ms | |
| | Set FlexRAM Function execution time: | | | | | |
| $t_{setramff}$ | • Control Code 0xFF | — | 50 | — | µs | |
| $t_{setram8k}$ | • 8 KB EEPROM backup | — | 0.3 | 0.5 | ms | |
| $t_{setram32k}$ | • 32 KB EEPROM backup | — | 0.7 | 1.0 | ms | |
| | Byte-write to FlexRAM for EEPROM operation | | | | | |
| $t_{eewr8bers}$ | Byte-write to erased FlexRAM location execution time | — | 175 | 260 | µs | 3 |
| | Byte-write to FlexRAM execution time: | | | | | |
| $t_{eewr8b8k}$ | • 8 KB EEPROM backup | — | 340 | 1700 | µs | |
| $t_{eewr8b16k}$ | • 16 KB EEPROM backup | — | 385 | 1800 | µs | |
| $t_{eewr8b32k}$ | • 32 KB EEPROM backup | — | 475 | 2000 | µs | |
| | Word-write to FlexRAM for EEPROM operation | | | | | |
| $t_{eewr16bers}$ | Word-write to erased FlexRAM location execution time | — | 175 | 260 | µs | |
| | Word-write to FlexRAM execution time: | | | | | |
| $t_{eewr16b8k}$ | • 8 KB EEPROM backup | — | 340 | 1700 | µs | |
| $t_{eewr16b16k}$ | • 16 KB EEPROM backup | — | 385 | 1800 | µs | |
| $t_{eewr16b32k}$ | • 32 KB EEPROM backup | — | 475 | 2000 | µs | |
| | Longword-write to FlexRAM for EEPROM operation | | | | | |
| $t_{eewr32bers}$ | Longword-write to erased FlexRAM location execution time | — | 360 | 540 | µs | |
| | Longword-write to FlexRAM execution time: | | | | | |
| $t_{eewr32b8k}$ | • 8 KB EEPROM backup | — | 545 | 1950 | µs | |
| $t_{eewr32b16k}$ | • 16 KB EEPROM backup | — | 630 | 2050 | µs | |
| $t_{eewr32b32k}$ | • 32 KB EEPROM backup | — | 810 | 2250 | µs | |

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.

### 6.4.1.3 Flash high voltage current behaviors

**Table 21. Flash high voltage current behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{DD_PGM}$ | Average current adder during high voltage flash programming operation | — | 2.5 | 6.0 | mA |
| $I_{DD_ERS}$ | Average current adder during high voltage flash erase operation | — | 1.5 | 4.0 | mA |

### 6.4.1.4 Reliability specifications

**Table 22. NVM reliability specifications**

| Symbol | Description | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | Program Flash | | | | | |
| $t_{nvmretp10k}$ | Data retention after up to 10 K cycles | 5 | 50 | — | years | |
| $t_{nvmretp1k}$ | Data retention after up to 1 K cycles | 20 | 100 | — | years | |
| $n_{nvmcycp}$ | Cycling endurance | 10 K | 50 K | — | cycles | 2 |
| | Data Flash | | | | | |
| $t_{nvmretd10k}$ | Data retention after up to 10 K cycles | 5 | 50 | — | years | |
| $t_{nvmretd1k}$ | Data retention after up to 1 K cycles | 20 | 100 | — | years | |
| $n_{nvmcycd}$ | Cycling endurance | 10 K | 50 K | — | cycles | 2 |
| | FlexRAM as EEPROM | | | | | |
| $t_{nvmretee100}$ | Data retention up to 100% of write endurance | 5 | 50 | — | years | |
| $t_{nvmretee10}$ | Data retention up to 10% of write endurance | 20 | 100 | — | years | |
| | Write endurance | | | | | 3 |
| $n_{nvmwree16}$ | • EEPROM backup to FlexRAM ratio = 16 | 35 K | 175 K | — | writes | |
| $n_{nvmwree128}$ | • EEPROM backup to FlexRAM ratio = 128 | 315 K | 1.6 M | — | writes | |
| $n_{nvmwree512}$ | • EEPROM backup to FlexRAM ratio = 512 | 1.27 M | 6.4 M | — | writes | |
| $n_{nvmwree4k}$ | • EEPROM backup to FlexRAM ratio = 4096 | 10 M | 50 M | — | writes | |
| $n_{nvmwree8k}$ | • EEPROM backup to FlexRAM ratio = 8192 | 20 M | 100 M | — | writes | |

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40°C ≤ $T_j$ ≤ 125°C.
3. Write endurance represents the number of writes to each FlexRAM location at -40°C ≤Tj ≤ 125°C influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup per subsystem. Minimum and typical values assume all byte-writes to FlexRAM.

### 6.4.1.5 Write endurance to FlexRAM for EEPROM

When the FlexNVM partition code is not set to full data flash, the EEPROM data set size can be set to any of several non-zero values.

The bytes not assigned to data flash via the FlexNVM partition code are used by the flash memory module to obtain an effective endurance increase for the EEPROM data. The built-in EEPROM record management system raises the number of program/erase cycles that can be attained prior to device wear-out by cycling the EEPROM data through a larger EEPROM NVM storage space.

While different partitions of the FlexNVM are available, the intention is that a single choice for the FlexNVM partition code and EEPROM data set size is used throughout the entire lifetime of a given application. The EEPROM endurance equation and graph shown below assume that only one configuration is ever used.

$$\text{Writes_subsystem} = \frac{\text{EEPROM} - 2 \times \text{EEESPLIT} \times \text{EEESIZE}}{\text{EEESPLIT} \times \text{EEESIZE}} \times \text{Write_efficiency} \times n_{nvmcycd}$$

where

- Writes_subsystem — minimum number of writes to each FlexRAM location for subsystem (each subsystem can have different endurance)
- EEPROM — allocated FlexNVM for each EEPROM subsystem based on DEPART; entered with the Program Partition command
- EEESPLIT — FlexRAM split factor for subsystem; entered with the Program Partition command
- EEESIZE — allocated FlexRAM based on DEPART; entered with the Program Partition command
- Write_efficiency —
  - 0.25 for 8-bit writes to FlexRAM
  - 0.50 for 16-bit or 32-bit writes to FlexRAM
- $n_{nvmcycd}$ — data flash cycling endurance (the following graph assumes 10,000 cycles)

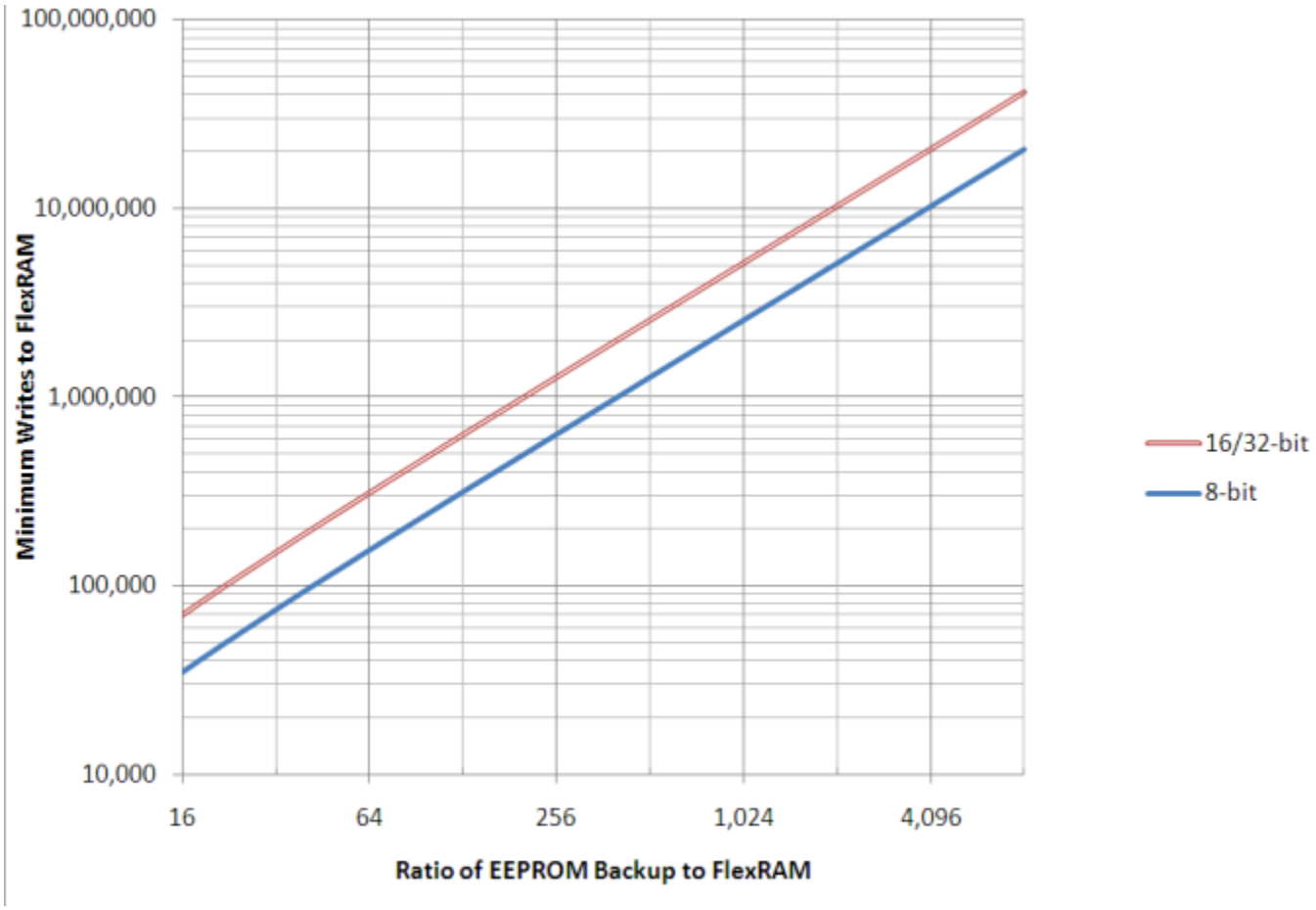



**Figure 10. EEPROM backup writes to FlexRAM**

## 6.4.2 EzPort Switching Specifications

**Table 23. EzPort switching specifications**

| Num | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V |
| EP1 | EZP_CK frequency of operation (all commands except READ) | — | $f_{SYS}/2$ | MHz |
| EP1a | EZP_CK frequency of operation (READ command) | — | $f_{SYS}/8$ | MHz |
| EP2 | $\overline{\text{EZP_CS}}$ negation to next $\overline{\text{EZP_CS}}$ assertion | 2 x $t_{EZP_CK}$ | — | ns |
| EP3 | $\overline{\text{EZP_CS}}$ input valid to EZP_CK high (setup) | 5 | — | ns |
| EP4 | EZP_CK high to $\overline{\text{EZP_CS}}$ input invalid (hold) | 5 | — | ns |
| EP5 | EZP_D input valid to EZP_CK high (setup) | 2 | — | ns |
| EP6 | EZP_CK high to EZP_D input invalid (hold) | 5 | — | ns |
| EP7 | EZP_CK low to EZP_Q output valid | — | 16 | ns |
| EP8 | EZP_CK low to EZP_Q output invalid (hold) | 0 | — | ns |
| EP9 | $\overline{\text{EZP_CS}}$ negation to EZP_Q tri-state | — | 12 | ns |

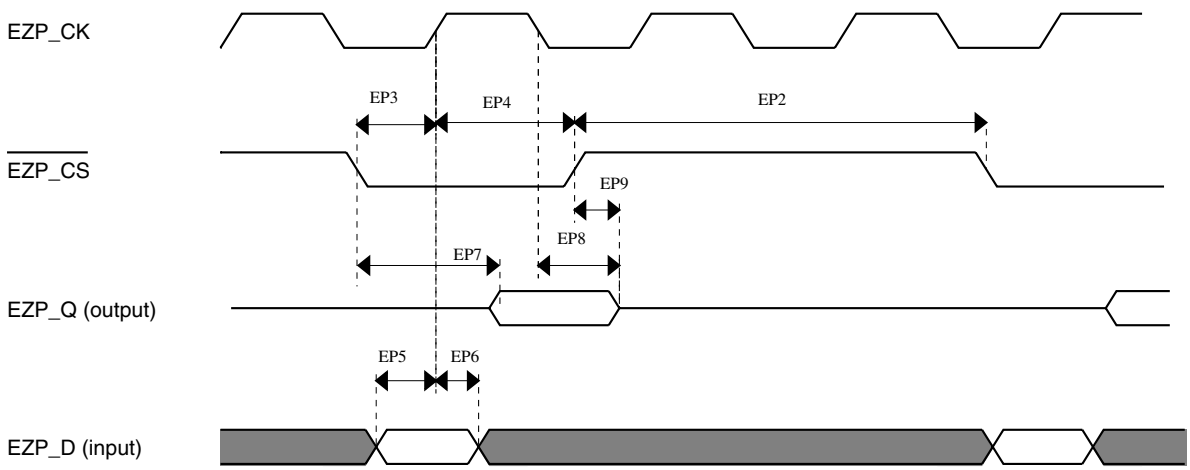



**Figure 11. EzPort Timing Diagram**

## 6.4.3 Flexbus Switching Specifications

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Flexbus output clock (FB_CLK). All other timing relationships can be derived from these values.

**Table 24. Flexbus limited voltage range switching specifications**

| Num | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| | Operating voltage | 2.7 | 3.6 | V | |
| | Frequency of operation | — | FB_CLK | MHz | |
| FB1 | Clock period | 20 | — | ns | |
| FB2 | Address, data, and control output valid | — | 11.5 | ns | 1 |
| FB3 | Address, data, and control output hold | 0.5 | — | ns | 1 |
| FB4 | Data and $\overline{\text{FB_TA}}$ input setup | 8.5 | — | ns | 2 |
| FB5 | Data and $\overline{\text{FB_TA}}$ input hold | 0.5 | — | ns | 2 |

1. Specification is valid for all FB_AD[31:0], $\overline{\text{FB_BE}}$/BWE*n*, $\overline{\text{FB_CS}}$*n*, $\overline{\text{FB_OE}}$, FB_R/$\overline{\text{W}}$,$\overline{\text{FB_TBST}}$, FB_TSIZ[1:0], FB_ALE, and $\overline{\text{FB_TS}}$.

2. Specification is valid for all FB_AD[31:0] and FB_TA.

## Table 25. Flexbus full voltage range switching specifications

| Num | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V | |
| | Frequency of operation | — | FB_CLK | MHz | |
| FB1 | Clock period | 1/FB_CLK | — | ns | |
| FB2 | Address, data, and control output valid | — | 13.5 | ns | 1 |
| FB3 | Address, data, and control output hold | 0 | — | ns | 1 |
| FB4 | Data and FB_TA input setup | 13.7 | — | ns | 2 |
| FB5 | Data and FB_TA input hold | 0.5 | — | ns | 2 |

1. Specification is valid for all FB_AD[31:0], FB_BE/BWE*n*, FB_CS*n*, FB_OE, FB_R/W,FB_TBST, FB_TSIZ[1:0], FB_ALE, and FB_TS.
2. Specification is valid for all FB_AD[31:0] and FB_TA.

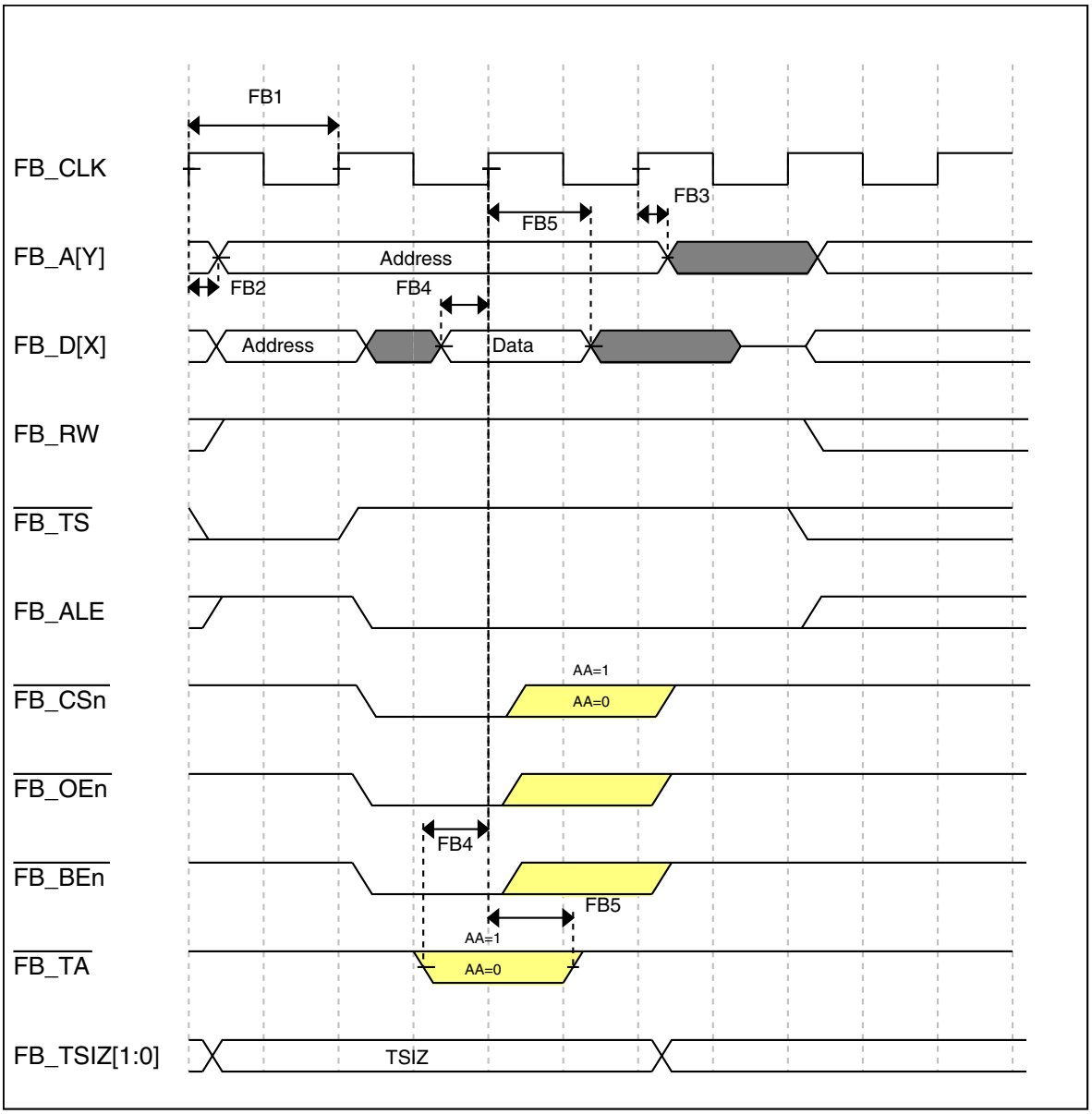



**Figure 12. FlexBus read timing diagram**

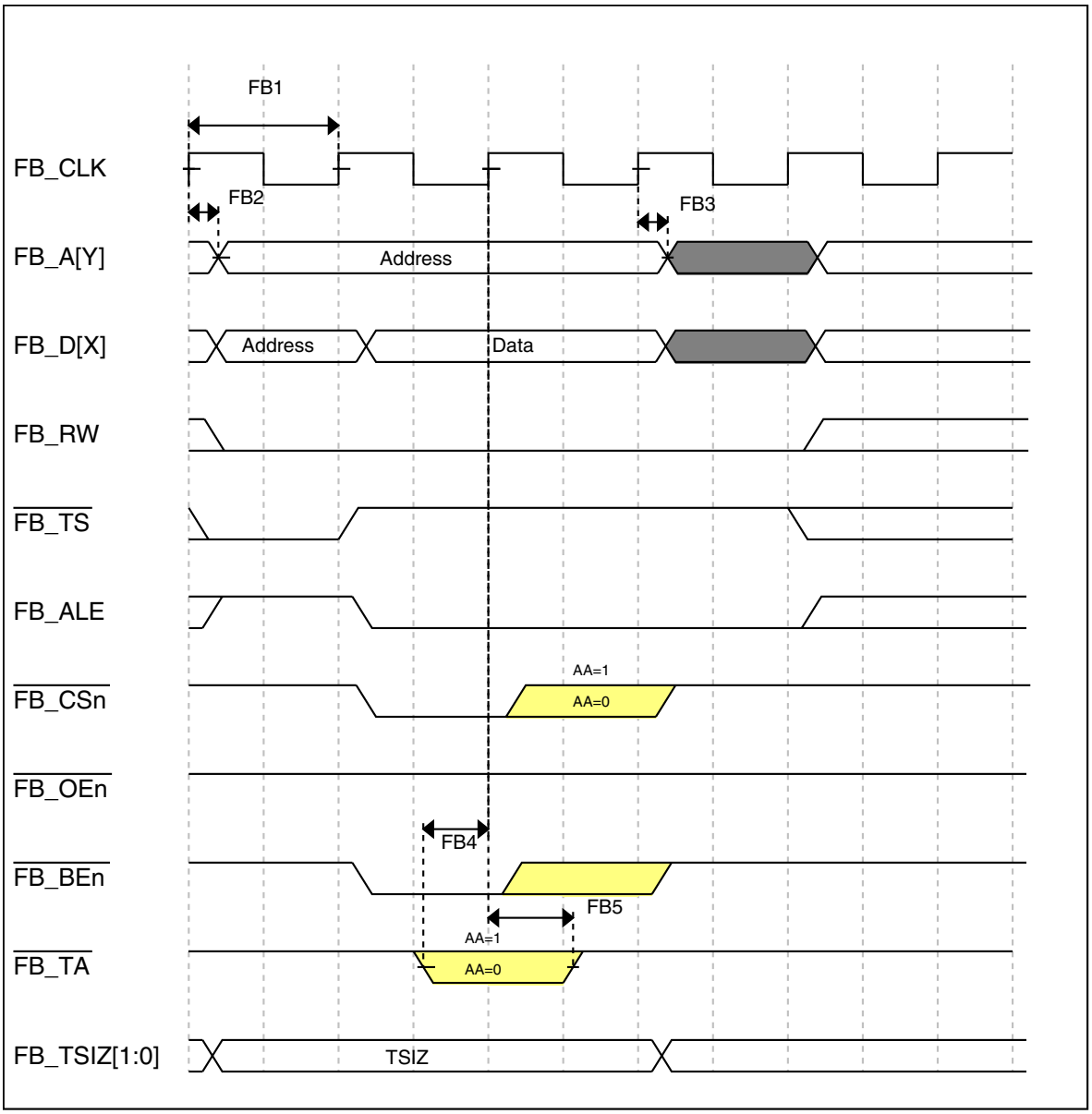



**Figure 13. FlexBus write timing diagram**

## 6.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

## 6.6 Analog

## 6.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in Table 26 and Table 27 are achievable on the differential pins ADCx_DP0, ADCx_DM0.

The ADCx_DP2 and ADCx_DM2 ADC inputs are connected to the PGA outputs and are not direct device pins. Accuracy specifications for these pins are defined in Table 28 and Table 29.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

### 6.6.1.1 16-bit ADC operating conditions

**Table 26. 16-bit ADC operating conditions**

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | Absolute | 1.71 | — | 3.6 | V | |
| $\Delta V_{DDA}$ | Supply voltage | Delta to $V_{DD}$ ($V_{DD}$ - $V_{DDA}$) | -100 | 0 | +100 | mV | 2 |
| $\Delta V_{SSA}$ | Ground voltage | Delta to $V_{SS}$ ($V_{SS}$ - $V_{SSA}$) | -100 | 0 | +100 | mV | 2 |
| $V_{REFH}$ | ADC reference voltage high | | 1.13 | $V_{DDA}$ | $V_{DDA}$ | V | |
| $V_{REFL}$ | ADC reference voltage low | | $V_{SSA}$ | $V_{SSA}$ | $V_{SSA}$ | V | |
| $V_{ADIN}$ | Input voltage | • 16-bit differential mode<br>• All other modes | VREFL<br>VREFL | —<br>— | 31/32 * VREFH<br>VREFH | V | |
| $C_{ADIN}$ | Input capacitance | • 16-bit mode<br>• 8-/10-/12-bit modes | —<br>— | 8<br>4 | 10<br>5 | pF | |
| $R_{ADIN}$ | Input resistance | | — | 2 | 5 | kΩ | |
| $R_{AS}$ | Analog source resistance | 13-/12-bit modes<br>$f_{ADCK}$ < 4 MHz | — | — | 5 | kΩ | 3 |
| $f_{ADCK}$ | ADC conversion clock frequency | ≤ 13-bit mode | 1.0 | — | 18.0 | MHz | 4 |
| $f_{ADCK}$ | ADC conversion clock frequency | 16-bit mode | 2.0 | — | 12.0 | MHz | 4 |
| $C_{rate}$ | ADC conversion rate | ≤ 13 bit modes<br>No ADC hardware averaging<br>Continuous conversions enabled, subsequent conversion time | 20.000 | — | 818.330 | Ksps | 5 |

*Table continues on the next page...*

**Table 26. 16-bit ADC operating conditions (continued)**

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $C_{rate}$ | ADC conversion rate | 16-bit mode<br>No ADC hardware averaging<br>Continuous conversions enabled, subsequent conversion time | 37.037 | — | 461.467 | Ksps | 5 |

1. Typical values assume $V_{DDA}$ = 3.0 V, Temp = 25 °C, $f_{ADCK}$ = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. The analog source resistance must be kept as low as possible to achieve the best results. The results in this data sheet were derived from a system which has < 8 Ω analog source resistance. The $R_{AS}/C_{AS}$ time constant should be kept to < 1ns.
4. To use the maximum ADC conversion clock frequency, the ADHSC bit must be set and the ADLPC bit must be clear.
5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool

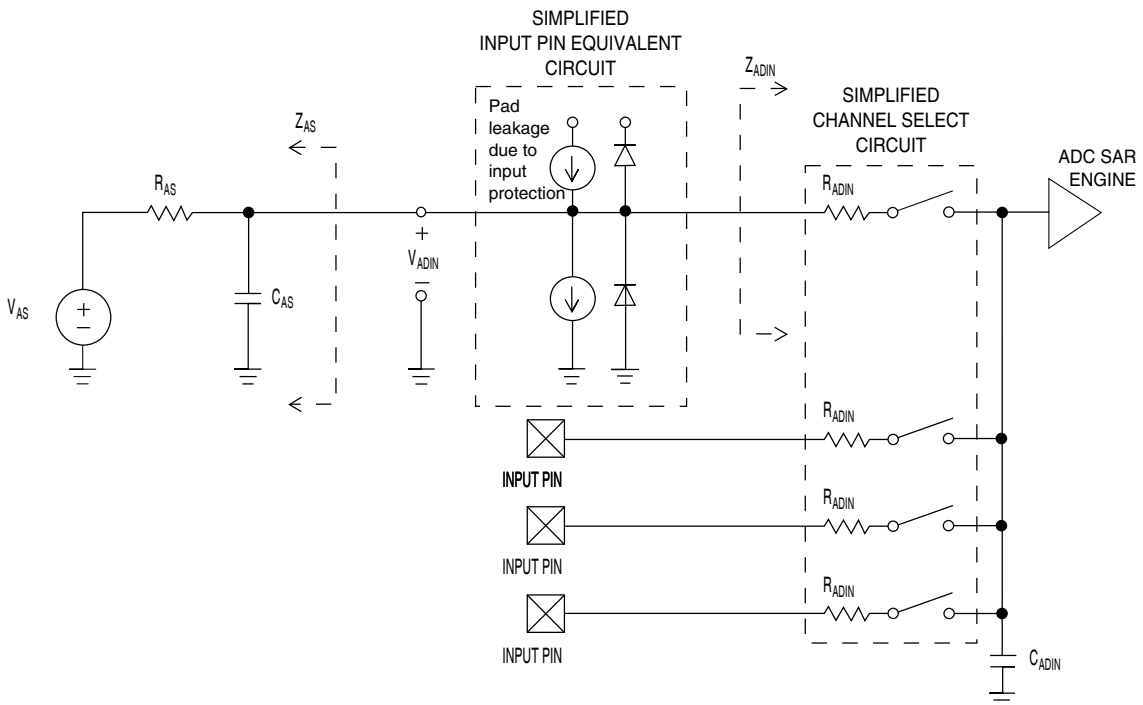



**Figure 14. ADC input impedance equivalency diagram**

## 6.6.1.2 16-bit ADC electrical characteristics

**Table 27. 16-bit ADC characteristics ($V_{REFH}$ = $V_{DDA}$, $V_{REFL}$ = $V_{SSA}$)**

| Symbol | Description | Conditions[1] | Min. | Typ.[2] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $I_{DDA_ADC}$ | Supply current | | 0.215 | — | 1.7 | mA | 3 |

*Table continues on the next page...*

## Table 27. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

| Symbol | Description | Conditions[1] | Min. | Typ.[2] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $f_{ADACK}$ | ADC asynchronous clock source | • ADLPC = 1, ADHSC = 0<br>• ADLPC = 1, ADHSC = 1<br>• ADLPC = 0, ADHSC = 0<br>• ADLPC = 0, ADHSC = 1 | 1.2<br>2.4<br>3.0<br>4.4 | 2.4<br>4.0<br>5.2<br>6.2 | 3.9<br>6.1<br>7.3<br>9.5 | MHz<br>MHz<br>MHz<br>MHz | $t_{ADACK} = 1/f_{ADACK}$ |
| | Sample Time | See Reference Manual chapter for sample times | | | | | |
| TUE | Total unadjusted error | • 12-bit modes<br>• <12-bit modes | —<br>— | ±4<br>±1.4 | ±6.8<br>±2.1 | LSB[4] | 5 |
| DNL | Differential non-linearity | • 12-bit modes<br>• <12-bit modes | —<br>— | ±0.7<br>±0.2 | -1.1 to +1.9<br>-0.3 to 0.5 | LSB[4] | 5 |
| INL | Integral non-linearity | • 12-bit modes<br>• <12-bit modes | —<br>— | ±1.0<br>±0.5 | -2.7 to +1.9<br>-0.7 to +0.5 | LSB[4] | 5 |
| $E_{FS}$ | Full-scale error | • 12-bit modes<br>• <12-bit modes | —<br>— | -4<br>-1.4 | -5.4<br>-1.8 | LSB[4] | $V_{ADIN} = V_{DDA}$<br>5 |
| $E_Q$ | Quantization error | • 16-bit modes<br>• ≤13-bit modes | —<br>— | -1 to 0<br>— | —<br>±0.5 | LSB[4] | |
| ENOB | Effective number of bits | 16-bit differential mode<br>• Avg = 32<br>• Avg = 4<br>16-bit single-ended mode<br>• Avg = 32<br>• Avg = 4 | <br>12.8<br>11.9<br><br>12.2<br>11.4 | <br>14.5<br>13.8<br><br>13.9<br>13.1 | <br>—<br>—<br><br>—<br>— | <br>bits<br>bits<br><br>bits<br>bits | 6 |
| SINAD | Signal-to-noise plus distortion | See ENOB | 6.02 × ENOB + 1.76 | | | dB | |
| THD | Total harmonic distortion | 16-bit differential mode<br>• Avg = 32<br>16-bit single-ended mode<br>• Avg = 32 | <br>—<br><br>— | <br>–94<br><br>-85 | <br>—<br><br>— | <br>dB<br><br>dB | 7 |
| SFDR | Spurious free dynamic range | 16-bit differential mode<br>• Avg = 32<br>16-bit single-ended mode<br>• Avg = 32 | <br>82<br><br>78 | <br>95<br><br>90 | <br>—<br><br>— | <br>dB<br><br>dB | 7 |

*Table continues on the next page...*

## Table 27. 16-bit ADC characteristics ($V_{REFH}$ = $V_{DDA}$, $V_{REFL}$ = $V_{SSA}$) (continued)

| Symbol | Description | Conditions[1] | Min. | Typ.[2] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $E_{IL}$ | Input leakage error | | | $I_{In} \times R_{AS}$ | | mV | $I_{In}$ = leakage current (refer to the MCU's voltage and current operating ratings) |
| | Temp sensor slope | Across the full temperature range of the device | — | 1.715 | — | mV/°C | |
| $V_{TEMP25}$ | Temp sensor voltage | 25 °C | — | 719 | — | mV | |

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH}$ = $V_{DDA}$
2. Typical values assume $V_{DDA}$ = 3.0 V, Temp = 25°C, $f_{ADCK}$ = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and the ADLPC bit (low power). For lowest power operation the ADLPC bit must be set, the HSC bit must be clear with 1 MHz ADC conversion clock speed.
4. 1 LSB = ($V_{REFH}$ - $V_{REFL}$)/$2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.

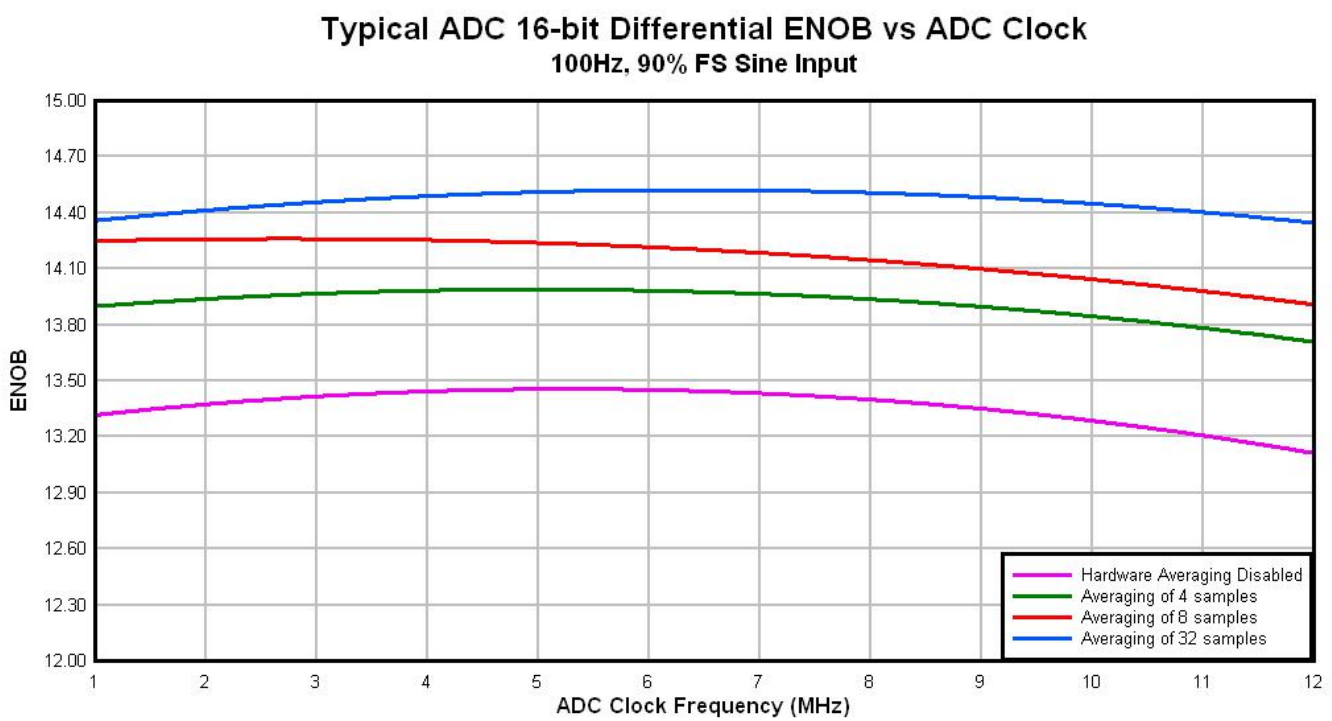



**Figure 15. Typical ENOB vs. ADC_CLK for 16-bit differential mode**

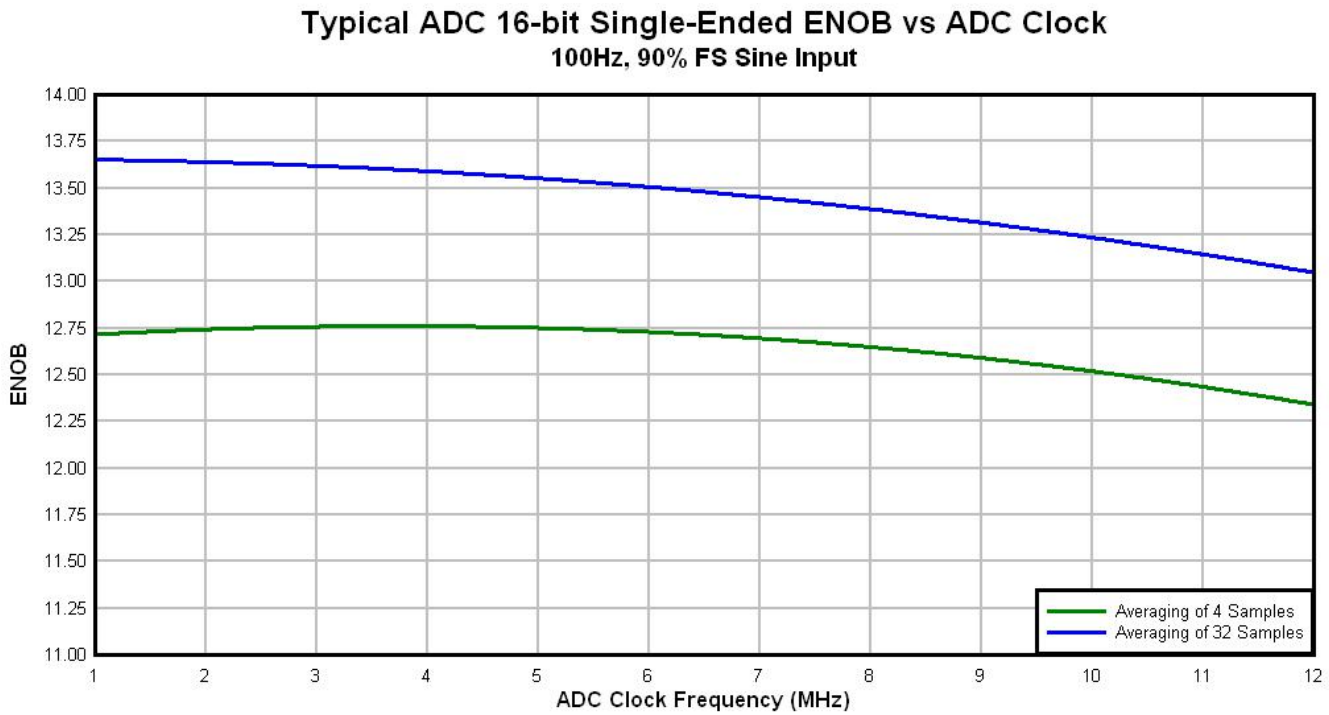



**Figure 16. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode**

### 6.6.1.3 16-bit ADC with PGA operating conditions

**Table 28. 16-bit ADC with PGA operating conditions**

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | Absolute | 1.71 | — | 3.6 | V | |
| $V_{REFPGA}$ | PGA ref voltage | | VREF_OUT | VREF_OUT | VREF_OUT | V | 2, 3 |
| $V_{ADIN}$ | Input voltage | | $V_{SSA}$ | — | $V_{DDA}$ | V | |
| $V_{CM}$ | Input Common Mode range | | $V_{SSA}$ | — | $V_{DDA}$ | V | |
| $R_{PGAD}$ | Differential input impedance | Gain = 1, 2, 4, 8 | — | 128 | — | kΩ | IN+ to IN-[4] |
| | | Gain = 16, 32 | — | 64 | — | | |
| | | Gain = 64 | — | 32 | — | | |
| $R_{AS}$ | Analog source resistance | | — | 100 | — | Ω | 5 |
| $T_S$ | ADC sampling time | | 1.25 | — | — | μs | 6 |

*Table continues on the next page...*

**Table 28. 16-bit ADC with PGA operating conditions (continued)**

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $C_{rate}$ | ADC conversion rate | ≤ 13 bit modes<br>No ADC hardware averaging<br>Continuous conversions enabled<br>Peripheral clock = 50 MHz | 18.484 | — | 450 | Ksps | 7 |
| | | 16 bit modes<br>No ADC hardware averaging<br>Continuous conversions enabled<br>Peripheral clock = 50 MHz | 37.037 | — | 250 | Ksps | 8 |

1. Typical values assume $V_{DDA}$ = 3.0 V, Temp = 25°C, $f_{ADCK}$ = 6 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. ADC must be configured to use the internal voltage reference (VREF_OUT)
3. PGA reference is internally connected to the VREF_OUT pin. If the user wishes to drive VREF_OUT with a voltage other than the output of the VREF module, the VREF module must be disabled.
4. For single ended configurations the input impedance of the driven input is $R_{PGAD}/2$
5. The analog source resistance ($R_{AS}$), external to MCU, should be kept as minimum as possible. Increased $R_{AS}$ causes drop in PGA gain without affecting other performances. This is not dependent on ADC clock frequency.
6. The minimum sampling time is dependent on input signal frequency and ADC mode of operation. A minimum of 1.25µs time should be allowed for $F_{in}$=4 kHz at 16-bit differential mode. Recommended ADC setting is: ADLSMP=1, ADLSTS=2 at 8 MHz ADC clock.
7. ADC clock = 18 MHz, ADLSMP = 1, ADLST = 00, ADHSC = 1
8. ADC clock = 12 MHz, ADLSMP = 1, ADLST = 01, ADHSC = 1

### 6.6.1.4 16-bit ADC with PGA characteristics with Chop enabled (ADC_PGA[PGACHPb] =0)

**Table 29. 16-bit ADC with PGA characteristics**

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $I_{DDA_PGA}$ | Supply current | Low power (ADC_PGA[PGALPb]=0) | — | 420 | 644 | µA | 2 |
| $I_{DC_PGA}$ | Input DC current | | $\frac{2}{R_{PGAD}}\left(\frac{(V_{REFPGA}\times 0.583)-V_{CM}}{(Gain+1)}\right)$ | | | A | 3 |
| | | Gain =1, $V_{REFPGA}$=1.2V, $V_{CM}$=0.5V | — | 1.54 | — | µA | |
| | | Gain =64, $V_{REFPGA}$=1.2V, $V_{CM}$=0.1V | — | 0.57 | — | µA | |

*Table continues on the next page...*

## Table 29. 16-bit ADC with PGA characteristics (continued)

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| G | Gain[4] | • PGAG=0<br>• PGAG=1<br>• PGAG=2<br>• PGAG=3<br>• PGAG=4<br>• PGAG=5<br>• PGAG=6 | 0.95<br>1.9<br>3.8<br>7.6<br>15.2<br>30.0<br>58.8 | 1<br>2<br>4<br>8<br>16<br>31.6<br>63.3 | 1.05<br>2.1<br>4.2<br>8.4<br>16.6<br>33.2<br>67.8 | | $R_{AS} < 100\Omega$ |
| BW | Input signal bandwidth | • 16-bit modes<br>• < 16-bit modes | —<br>— | —<br>— | 4<br>40 | kHz<br>kHz | |
| PSRR | Power supply rejection ratio | Gain=1 | — | -84 | — | dB | $V_{DDA}$= 3V ±100mV, $f_{VDDA}$= 50Hz, 60Hz |
| CMRR | Common mode rejection ratio | • Gain=1<br>• Gain=64 | —<br>— | -84<br>-85 | —<br>— | dB<br>dB | $V_{CM}$= 500mVpp, $f_{VCM}$= 50Hz, 100Hz |
| $V_{OFS}$ | Input offset voltage | | — | 0.2 | — | mV | Output offset = $V_{OFS}$*(Gain+1) |
| $T_{GSW}$ | Gain switching settling time | | — | — | 10 | µs | 5 |
| dG/dT | Gain drift over full temperature range | • Gain=1<br>• Gain=64 | —<br>— | 6<br>31 | 10<br>42 | ppm/°C<br>ppm/°C | |
| $dG/dV_{DDA}$ | Gain drift over supply voltage | • Gain=1<br>• Gain=64 | —<br>— | 0.07<br>0.14 | 0.21<br>0.31 | %/V<br>%/V | $V_{DDA}$ from 1.71 to 3.6V |
| $E_{IL}$ | Input leakage error | All modes | $I_{In} \times R_{AS}$ | | | mV | $I_{In}$ = leakage current<br>(refer to the MCU's voltage and current operating ratings) |
| $V_{PP,DIFF}$ | Maximum differential input signal swing | | $\left(\frac{(\min(V_X, V_{DDA}-V_X)-0.2)\times 4}{\text{Gain}}\right)$<br>where $V_X = V_{REFPGA} \times 0.583$ | | | V | 6 |
| SNR | Signal-to-noise ratio | • Gain=1<br>• Gain=64 | 80<br>52 | 90<br>66 | —<br>— | dB<br>dB | 16-bit differential mode, Average=32 |
| THD | Total harmonic distortion | • Gain=1<br>• Gain=64 | 85<br>49 | 100<br>95 | —<br>— | dB<br>dB | 16-bit differential mode, Average=32, $f_{in}$=100Hz |

*Table continues on the next page...*

**Table 29. 16-bit ADC with PGA characteristics (continued)**

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| SFDR | Spurious free dynamic range | • Gain=1<br>• Gain=64 | 85<br>53 | 105<br>88 | —<br>— | dB<br>dB | 16-bit differential mode, Average=32, $f_{in}$=100Hz |
| ENOB | Effective number of bits | • Gain=1, Average=4<br>• Gain=64, Average=4<br>• Gain=1, Average=32<br>• Gain=2, Average=32<br>• Gain=4, Average=32<br>• Gain=8, Average=32<br>• Gain=16, Average=32<br>• Gain=32, Average=32<br>• Gain=64, Average=32 | 11.6<br>7.2<br>12.8<br>11.0<br>7.9<br>7.3<br>6.8<br>6.8<br>7.5 | 13.4<br>9.6<br>14.5<br>14.3<br>13.8<br>13.1<br>12.5<br>11.5<br>10.6 | —<br>—<br>—<br>—<br>—<br>—<br>—<br>—<br>— | bits<br>bits<br>bits<br>bits<br>bits<br>bits<br>bits<br>bits<br>bits | 16-bit differential mode,$f_{in}$=100Hz |
| SINAD | Signal-to-noise plus distortion ratio | See ENOB | 6.02 × ENOB + 1.76 | | | dB | |

1. Typical values assume $V_{DDA}$ =3.0V, Temp=25°C, $f_{ADCK}$=6MHz unless otherwise stated.
2. This current is a PGA module adder, in addition to ADC conversion currents.
3. Between IN+ and IN-. The PGA draws a DC current from the input terminals. The magnitude of the DC current is a strong function of input common mode voltage ($V_{CM}$) and the PGA gain.
4. Gain = $2^{PGAG}$
5. After changing the PGA gain setting, a minimum of 2 ADC+PGA conversions should be ignored.
6. Limit the input signal swing so that the PGA does not saturate during operation. Input signal swing is dependent on the PGA reference voltage and gain setting.

## 6.6.2 CMP and 6-bit DAC electrical specifications

**Table 30. Comparator and 6-bit DAC electrical specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.71 | — | 3.6 | V |
| $I_{DDHS}$ | Supply current, High-speed mode (EN=1, PMODE=1) | — | — | 200 | µA |
| $I_{DDLS}$ | Supply current, low-speed mode (EN=1, PMODE=0) | — | — | 20 | µA |
| $V_{AIN}$ | Analog input voltage | $V_{SS}$ – 0.3 | — | $V_{DD}$ | V |
| $V_{AIO}$ | Analog input offset voltage | — | — | 20 | mV |
| $V_H$ | Analog comparator hysteresis[1]<br>• CR0[HYSTCTR] = 00<br>• CR0[HYSTCTR] = 01<br>• CR0[HYSTCTR] = 10<br>• CR0[HYSTCTR] = 11 | <br>—<br>—<br>—<br>— | <br>5<br>10<br>20<br>30 | <br>—<br>—<br>—<br>— | <br>mV<br>mV<br>mV<br>mV |

*Table continues on the next page...*

## Table 30. Comparator and 6-bit DAC electrical specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CMPOh}$ | Output high | $V_{DD}$ – 0.5 | — | — | V |
| $V_{CMPOl}$ | Output low | — | — | 0.5 | V |
| $t_{DHS}$ | Propagation delay, high-speed mode (EN=1, PMODE=1) | 20 | 50 | 200 | ns |
| $t_{DLS}$ | Propagation delay, low-speed mode (EN=1, PMODE=0) | 80 | 250 | 600 | ns |
| | Analog comparator initialization delay[2] | — | — | 40 | µs |
| $I_{DAC6b}$ | 6-bit DAC current adder (enabled) | — | 7 | — | µA |
| INL | 6-bit DAC integral non-linearity | –0.5 | — | 0.5 | LSB[3] |
| DNL | 6-bit DAC differential non-linearity | –0.3 | — | 0.3 | LSB |

1. Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD}$-0.6V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}$/64

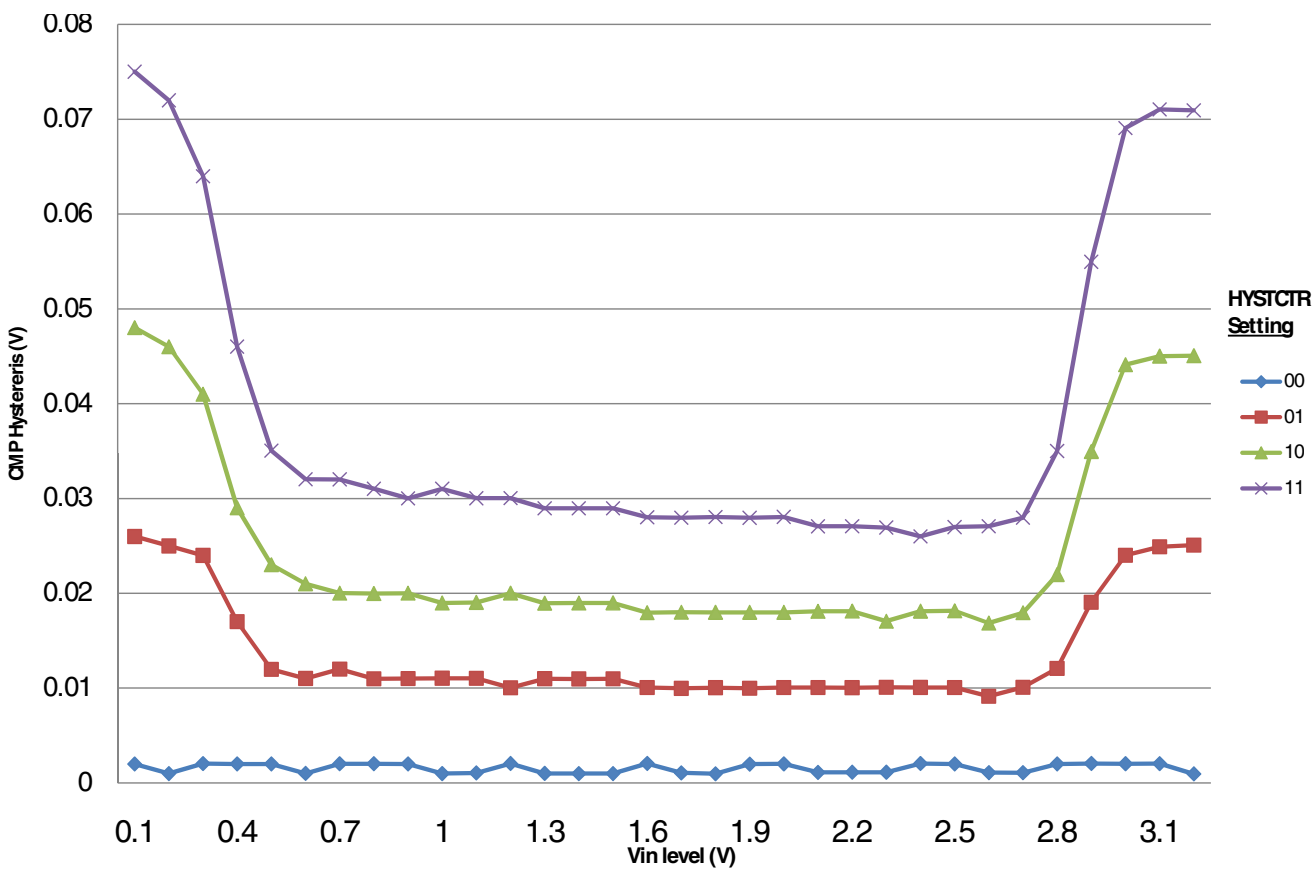



**Figure 17. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=0)**

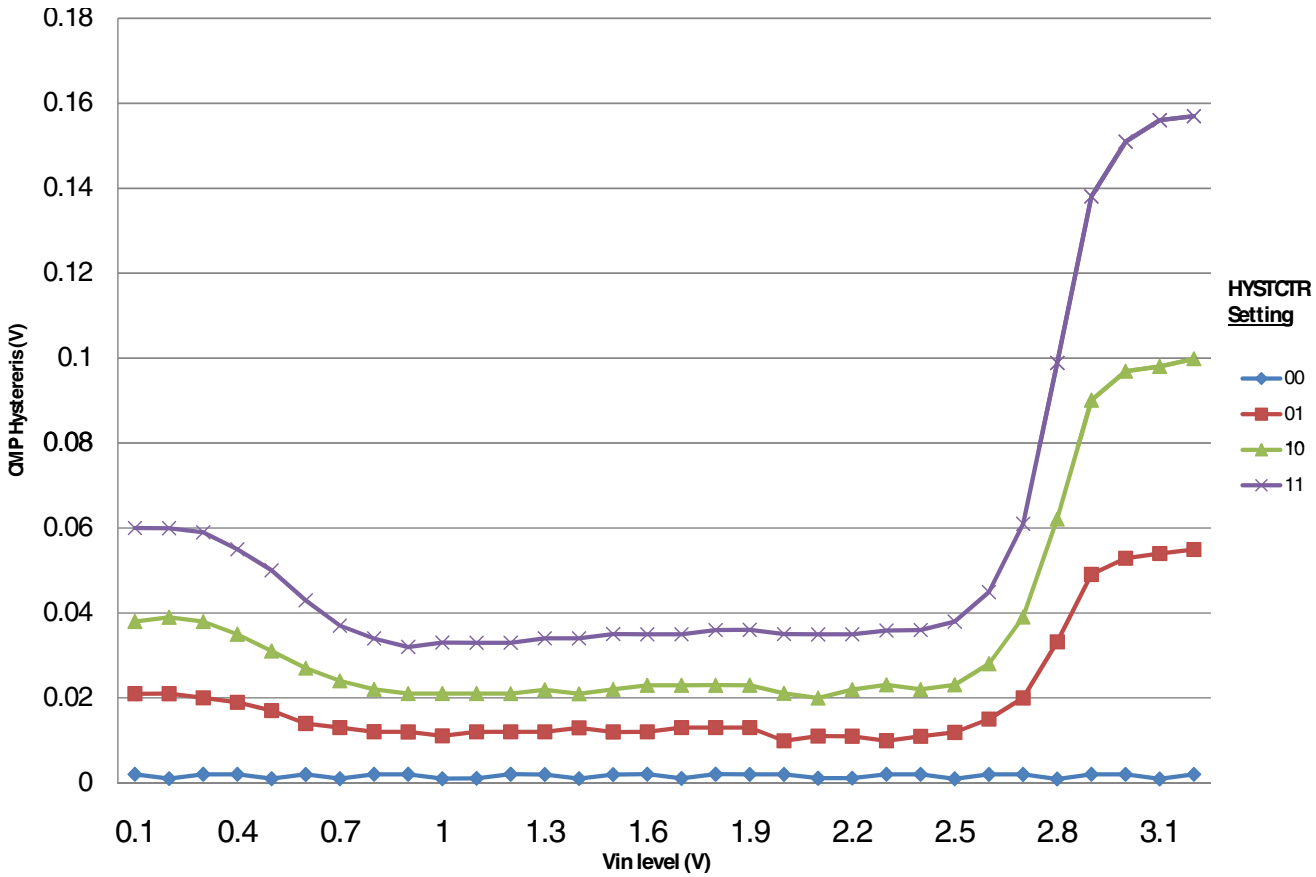



**Figure 18. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=1)**

## 6.6.3 12-bit DAC electrical characteristics

### 6.6.3.1 12-bit DAC operating requirements

**Table 31. 12-bit DAC operating requirements**

| Symbol | Desciption | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | 1.71 | 3.6 | V | |
| $V_{DACR}$ | Reference voltage | 1.13 | 3.6 | V | 1 |
| $T_A$ | Temperature | Operating temperature range of the device | | °C | |
| $C_L$ | Output load capacitance | — | 100 | pF | 2 |
| $I_L$ | Output load current | — | 1 | mA | |

1. The DAC reference can be selected to be $V_{DDA}$ or the voltage output of the VREF module (VREF_OUT)
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC

### 6.6.3.2 12-bit DAC operating behaviors

**Table 32. 12-bit DAC operating behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DDA_DACLP}$ | Supply current — low-power mode | — | — | 150 | µA | |
| $I_{DDA_DACHP}$ | Supply current — high-speed mode | — | — | 700 | µA | |
| $t_{DACLP}$ | Full-scale settling time (0x080 to 0xF7F) — low-power mode | — | 100 | 200 | µs | 1 |
| $t_{DACHP}$ | Full-scale settling time (0x080 to 0xF7F) — high-power mode | — | 15 | 30 | µs | 1 |
| $t_{CCDACLP}$ | Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode | — | 0.7 | 1 | µs | 1 |
| $V_{dacoutl}$ | DAC output voltage range low — high-speed mode, no load, DAC set to 0x000 | — | — | 100 | mV | |
| $V_{dacouth}$ | DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF | $V_{DACR}$ −100 | — | $V_{DACR}$ | mV | |
| INL | Integral non-linearity error — high speed mode | — | — | ±8 | LSB | 2 |
| DNL | Differential non-linearity error — $V_{DACR}$ > 2 V | — | — | ±1 | LSB | 3 |
| DNL | Differential non-linearity error — $V_{DACR}$ = VREF_OUT | — | — | ±1 | LSB | 4 |
| $V_{OFFSET}$ | Offset error | — | ±0.4 | ±0.8 | %FSR | 5 |
| $E_G$ | Gain error | — | ±0.1 | ±0.6 | %FSR | 5 |
| PSRR | Power supply rejection ratio, $V_{DDA}$ ≥ 2.4 V | 60 | — | 90 | dB | |
| $T_{CO}$ | Temperature coefficient offset voltage | — | 3.7 | — | µV/C | 6 |
| $T_{GE}$ | Temperature coefficient gain error | — | 0.000421 | — | %FSR/C | |
| Rop | Output resistance load = 3 kΩ | — | — | 250 | Ω | |
| SR | Slew rate -80h→ F7Fh→ 80h | | | | V/µs | |
| | • High power ($SP_{HP}$) | 1.2 | 1.7 | — | | |
| | • Low power ($SP_{LP}$) | 0.05 | 0.12 | — | | |
| CT | Channel to channel cross talk | — | — | -80 | dB | |
| BW | 3dB bandwidth | | | | kHz | |
| | • High power ($SP_{HP}$) | 550 | — | — | | |
| | • Low power ($SP_{LP}$) | 40 | — | — | | |

1. Settling within ±1 LSB
2. The INL is measured for 0 + 100 mV to $V_{DACR}$ −100 mV
3. The DNL is measured for 0 + 100 mV to $V_{DACR}$ −100 mV
4. The DNL is measured for 0 + 100 mV to $V_{DACR}$ −100 mV with $V_{DDA}$ > 2.4 V
5. Calculated by a best fit curve from $V_{SS}$ + 100 mV to $V_{DACR}$ − 100 mV
6. $V_{DDA}$ = 3.0 V, reference select set for $V_{DDA}$ (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

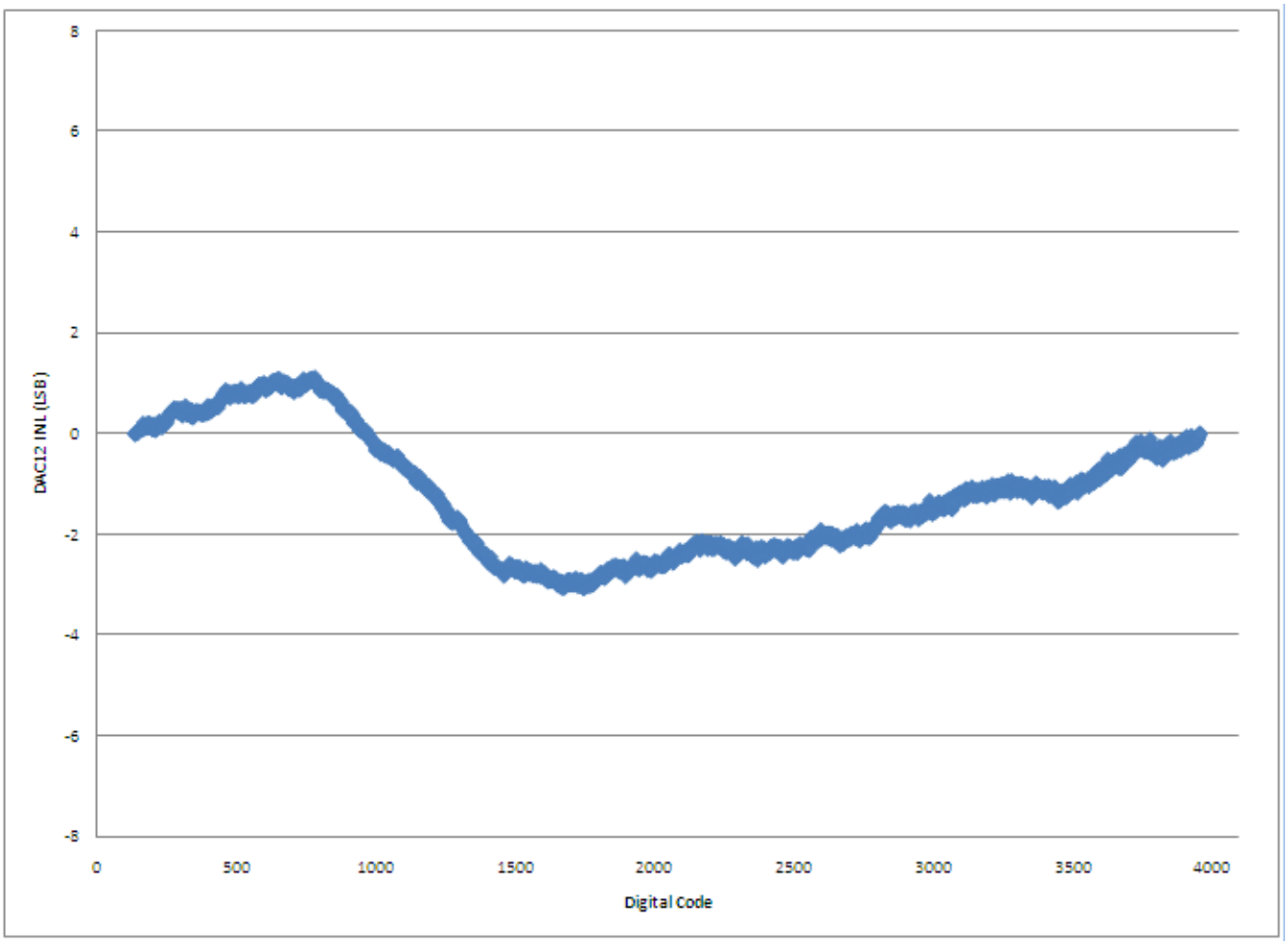



**Figure 19. Typical INL error vs. digital code**

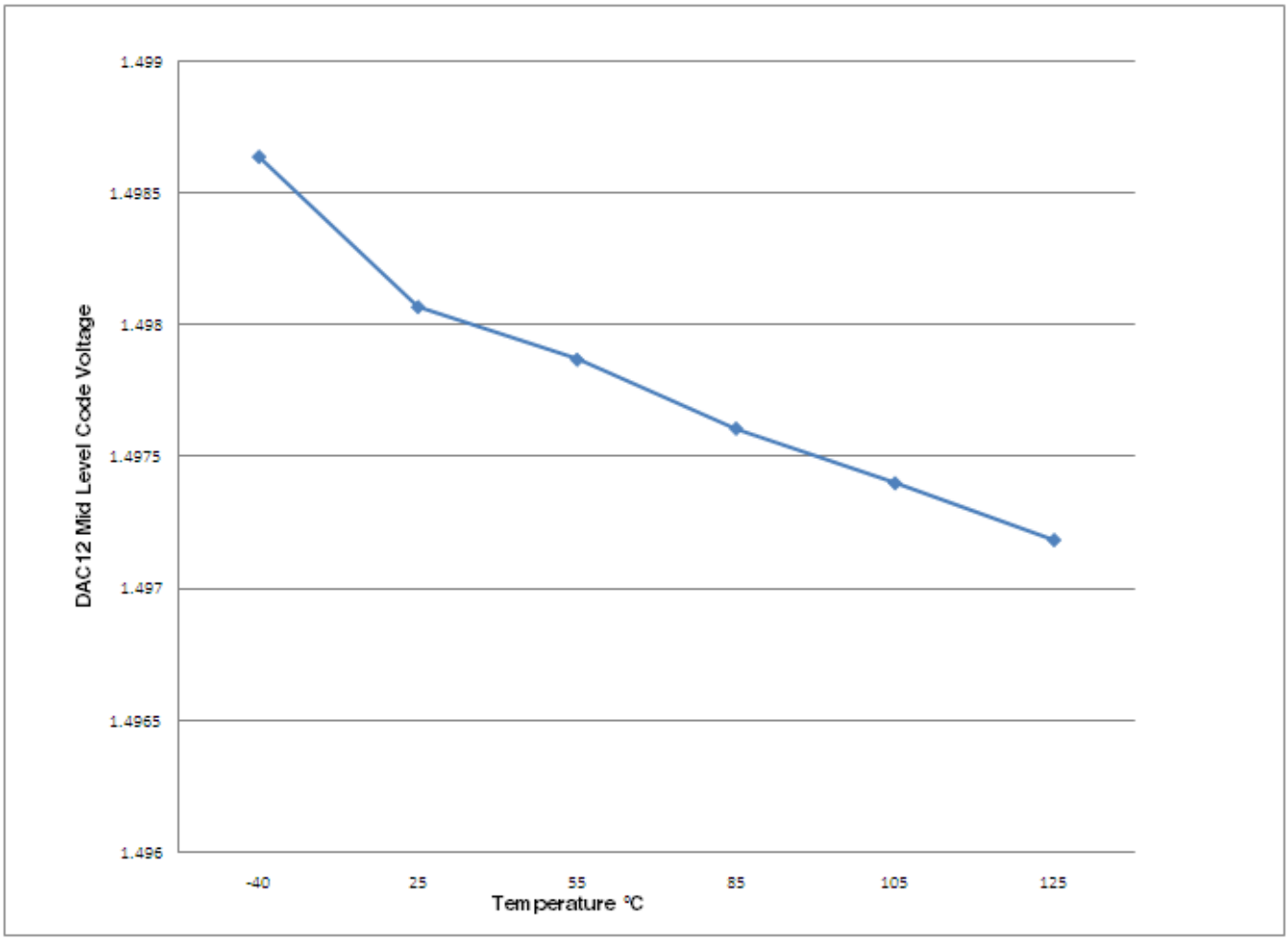



**Figure 20. Offset at half scale vs. temperature**

## 6.6.4 Voltage reference electrical specifications

**Table 33. VREF full-range operating requirements**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | 1.71 | 3.6 | V | |
| $T_A$ | Temperature | Operating temperature range of the device | | °C | |
| $C_L$ | Output load capacitance | 100 | | nF | 1, 2 |

1. $C_L$ must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified $C_L$ value over the operating temperature range of the device.

### Table 34. VREF full-range operating behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{out}$ | Voltage reference output with factory trim at nominal $V_{DDA}$ and temperature=25C | 1.1915 | 1.195 | 1.1977 | V | |
| $V_{out}$ | Voltage reference output — factory trim | 1.1584 | — | 1.2376 | V | |
| $V_{out}$ | Voltage reference output — user trim | 1.193 | — | 1.197 | V | |
| $V_{step}$ | Voltage reference trim step | — | 0.5 | — | mV | |
| $V_{tdrift}$ | Temperature drift (Vmax -Vmin across the full temperature range) | — | — | 80 | mV | |
| $I_{bg}$ | Bandgap only current | — | — | 80 | µA | 1 |
| $I_{lp}$ | Low-power buffer current | — | — | 360 | uA | 1 |
| $I_{hp}$ | High-power buffer current | — | — | 1 | mA | 1 |
| $\Delta V_{LOAD}$ | Load regulation<br>• current = ± 1.0 mA | —<br>— | <br>200 | <br>— | µV | 1, 2 |
| $T_{stup}$ | Buffer startup time | — | — | 100 | µs | |
| $V_{vdrift}$ | Voltage drift (Vmax -Vmin across the full voltage range) | — | 2 | — | mV | 1 |

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

### Table 35. VREF limited-range operating requirements

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $T_A$ | Temperature | 0 | 50 | °C | |

### Table 36. VREF limited-range operating behaviors

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{out}$ | Voltage reference output with factory trim | 1.173 | 1.225 | V | |

## 6.7 Timers

See General switching specifications.

## 6.8 Communication interfaces

### 6.8.1 CAN switching specifications

See General switching specifications.

### 6.8.2 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

**Table 37. Master mode DSPI timing (limited voltage range)**

| Num | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| | Operating voltage | 2.7 | 3.6 | V | |
| | Frequency of operation | — | 25 | MHz | |
| DS1 | DSPI_SCK output cycle time | 2 x $t_{BUS}$ | — | ns | |
| DS2 | DSPI_SCK output high/low time | ($t_{SCK}$/2) – 2 | ($t_{SCK}$/2) + 2 | ns | |
| DS3 | DSPI_PCS*n* valid to DSPI_SCK delay | ($t_{BUS}$ x 2) – 2 | — | ns | 1 |
| DS4 | DSPI_SCK to DSPI_PCS*n* invalid delay | ($t_{BUS}$ x 2) – 2 | — | ns | 2 |
| DS5 | DSPI_SCK to DSPI_SOUT valid | — | 8.5 | ns | |
| DS6 | DSPI_SCK to DSPI_SOUT invalid | –2 | — | ns | |
| DS7 | DSPI_SIN to DSPI_SCK input setup | 15 | — | ns | |
| DS8 | DSPI_SCK to DSPI_SIN input hold | 0 | — | ns | |

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

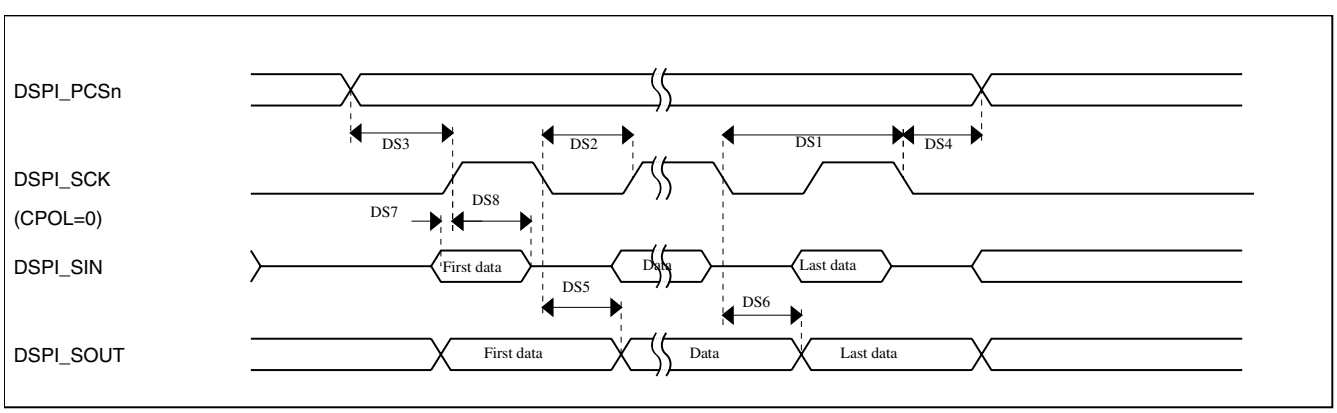



**Figure 21. DSPI classic SPI timing — master mode**

**Table 38. Slave mode DSPI timing (limited voltage range)**

| Num | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 2.7 | 3.6 | V |
| | Frequency of operation | | 12.5 | MHz |
| DS9 | DSPI_SCK input cycle time | 4 x $t_{BUS}$ | — | ns |
| DS10 | DSPI_SCK input high/low time | ($t_{SCK}$/2) – 2 | ($t_{SCK}$/2) + 2 | ns |
| DS11 | DSPI_SCK to DSPI_SOUT valid | — | 10 | ns |
| DS12 | DSPI_SCK to DSPI_SOUT invalid | 0 | — | ns |
| DS13 | DSPI_SIN to DSPI_SCK input setup | 2 | — | ns |
| DS14 | DSPI_SCK to DSPI_SIN input hold | 7 | — | ns |
| DS15 | $\overline{\text{DSPI_SS}}$ active to DSPI_SOUT driven | — | 14 | ns |
| DS16 | $\overline{\text{DSPI_SS}}$ inactive to DSPI_SOUT not driven | — | 14 | ns |

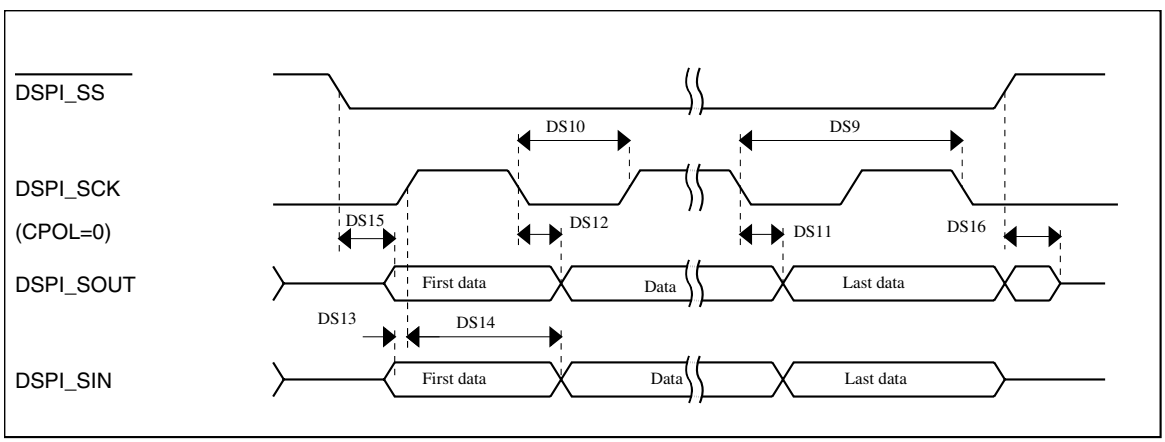



**Figure 22. DSPI classic SPI timing — slave mode**

## 6.8.3 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

**Table 39. Master mode DSPI timing (full voltage range)**

| Num | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V | 1 |
| | Frequency of operation | — | 12.5 | MHz | |
| DS1 | DSPI_SCK output cycle time | 4 x $t_{BUS}$ | — | ns | |

*Table continues on the next page...*

## Table 39. Master mode DSPI timing (full voltage range) (continued)

| Num | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| DS2 | DSPI_SCK output high/low time | ($t_{SCK}$/2) - 4 | ($t_{SCK/2}$) + 4 | ns | |
| DS3 | DSPI_PCS*n* valid to DSPI_SCK delay | ($t_{BUS}$ x 2) – 4 | — | ns | 2 |
| DS4 | DSPI_SCK to DSPI_PCS*n* invalid delay | ($t_{BUS}$ x 2) – 4 | — | ns | 3 |
| DS5 | DSPI_SCK to DSPI_SOUT valid | — | 10 | ns | |
| DS6 | DSPI_SCK to DSPI_SOUT invalid | -4.5 | — | ns | |
| DS7 | DSPI_SIN to DSPI_SCK input setup | 20.5 | — | ns | |
| DS8 | DSPI_SCK to DSPI_SIN input hold | 0 | — | ns | |

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

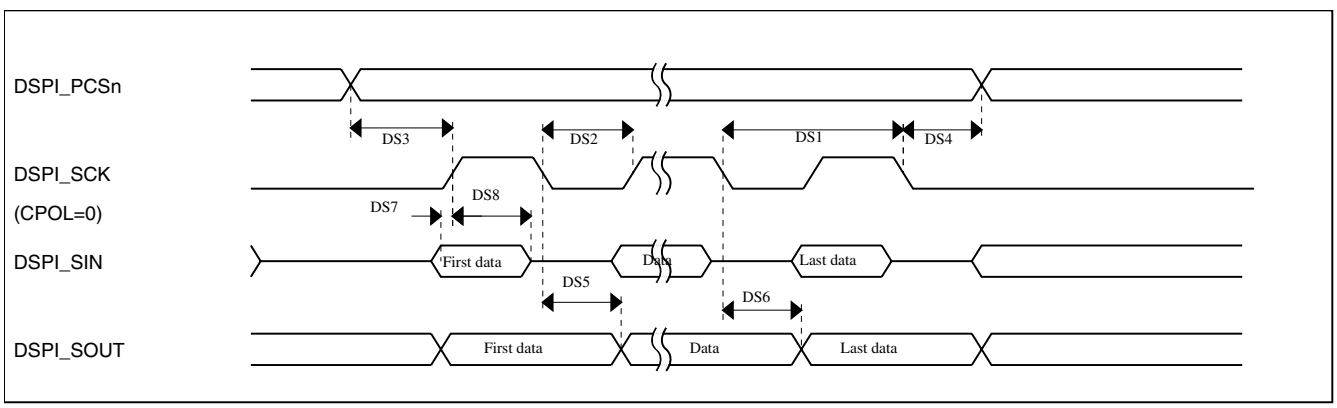



**Figure 23. DSPI classic SPI timing — master mode**

## Table 40. Slave mode DSPI timing (full voltage range)

| Num | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V |
| | Frequency of operation | — | 6.25 | MHz |
| DS9 | DSPI_SCK input cycle time | 8 x $t_{BUS}$ | — | ns |
| DS10 | DSPI_SCK input high/low time | ($t_{SCK}$/2) - 4 | ($t_{SCK/2}$) + 4 | ns |
| DS11 | DSPI_SCK to DSPI_SOUT valid | — | 20 | ns |
| DS12 | DSPI_SCK to DSPI_SOUT invalid | 0 | — | ns |
| DS13 | DSPI_SIN to DSPI_SCK input setup | 2 | — | ns |
| DS14 | DSPI_SCK to DSPI_SIN input hold | 7 | — | ns |
| DS15 | $\overline{\text{DSPI_SS}}$ active to DSPI_SOUT driven | — | 19 | ns |
| DS16 | $\overline{\text{DSPI_SS}}$ inactive to DSPI_SOUT not driven | — | 19 | ns |

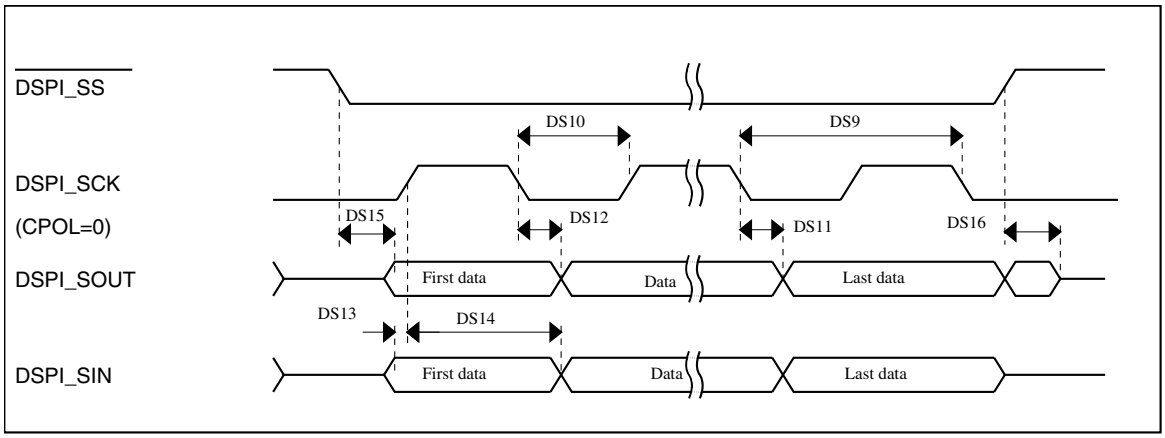



**Figure 24. DSPI classic SPI timing — slave mode**

## 6.8.4 I²C switching specifications

See General switching specifications.

## 6.8.5 UART switching specifications

See General switching specifications.

## 6.8.6 I2S/SAI Switching Specifications

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP] is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

### 6.8.6.1 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

### Table 41. I2S/SAI master mode timing in Normal Run, Wait and Stop modes (full voltage range)

| Num. | Characteristic | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V |
| S1 | I2S_MCLK cycle time | 40 | — | ns |
| S2 | I2S_MCLK pulse width high/low | 45% | 55% | MCLK period |
| S3 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (output) | 80 | — | ns |
| S4 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low | 45% | 55% | BCLK period |
| S5 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid | — | 15 | ns |
| S6 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid | -1.0 | — | ns |
| S7 | I2S_TX_BCLK to I2S_TXD valid | — | 15 | ns |
| S8 | I2S_TX_BCLK to I2S_TXD invalid | 0 | — | ns |
| S9 | I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK | 20.5 | — | ns |
| S10 | I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK | 0 | — | ns |

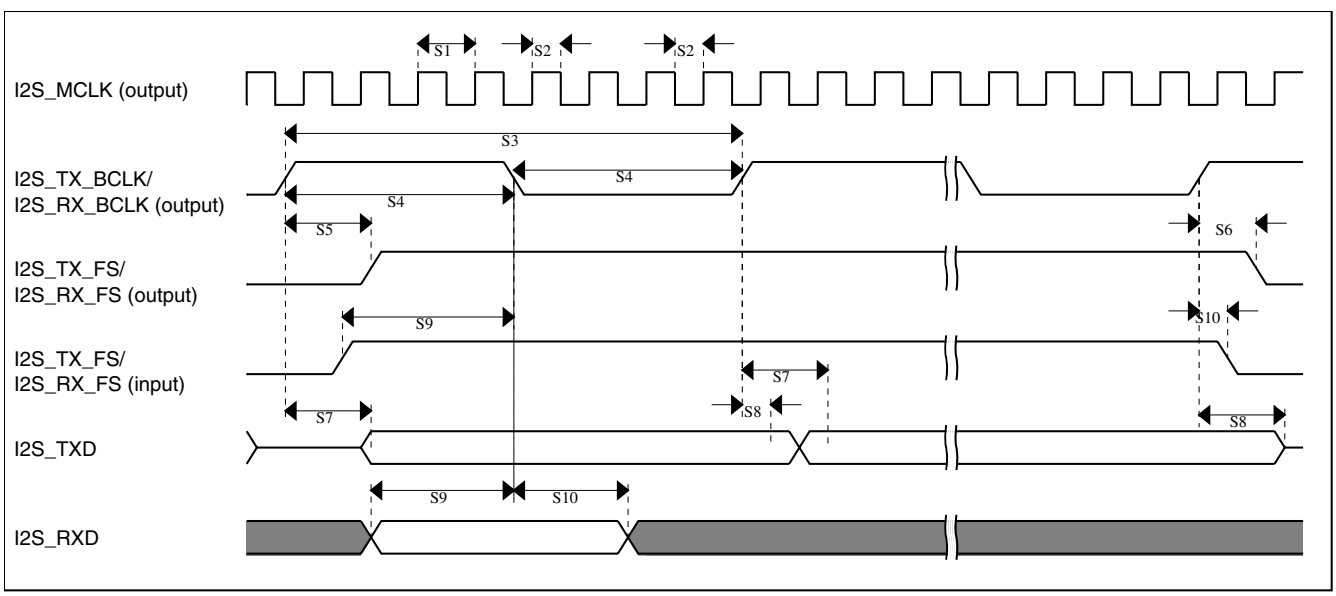



**Figure 25. I2S/SAI timing — master modes**

### Table 42. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (full voltage range)

| Num. | Characteristic | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V |
| S11 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (input) | 80 | — | ns |
| S12 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input) | 45% | 55% | MCLK period |

*Table continues on the next page...*

**Table 42. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (full voltage range) (continued)**

| Num. | Characteristic | Min. | Max. | Unit |
|---|---|---|---|---|
| S13 | I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK | 5.8 | — | ns |
| S14 | I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK | 2 | — | ns |
| S16 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid | 0 | — | ns |
| S17 | I2S_RXD setup before I2S_RX_BCLK | 5.8 | — | ns |
| S18 | I2S_RXD hold after I2S_RX_BCLK | 2 | — | ns |
| S19 | I2S_TX_FS input assertion to I2S_TXD output valid[1] | — | 25 | ns |

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

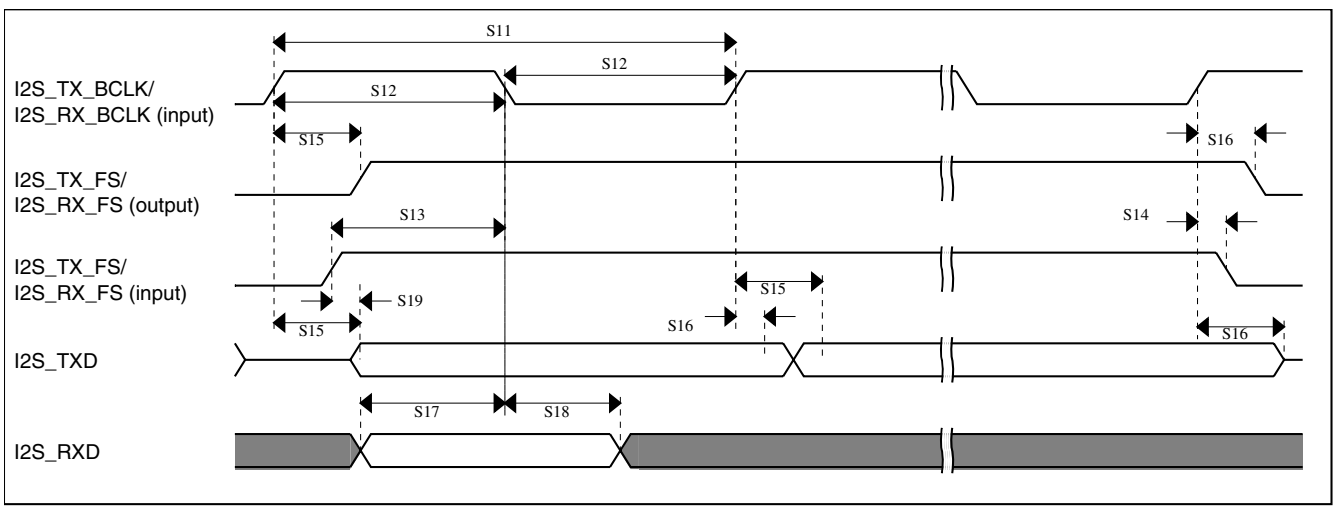



**Figure 26. I2S/SAI timing — slave modes**

## 6.8.6.2 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

**Table 43. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)**

| Num. | Characteristic | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V |
| S1 | I2S_MCLK cycle time | 62.5 | — | ns |
| S2 | I2S_MCLK pulse width high/low | 45% | 55% | MCLK period |
| S3 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (output) | 250 | — | ns |
| S4 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low | 45% | 55% | BCLK period |

*Table continues on the next page...*

**Table 43. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range) (continued)**

| Num. | Characteristic | Min. | Max. | Unit |
|---|---|---|---|---|
| S5 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid | — | 45 | ns |
| S6 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid | 0 | — | ns |
| S7 | I2S_TX_BCLK to I2S_TXD valid | — | 45 | ns |
| S8 | I2S_TX_BCLK to I2S_TXD invalid | 0 | — | ns |
| S9 | I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK | 53 | — | ns |
| S10 | I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK | 0 | — | ns |

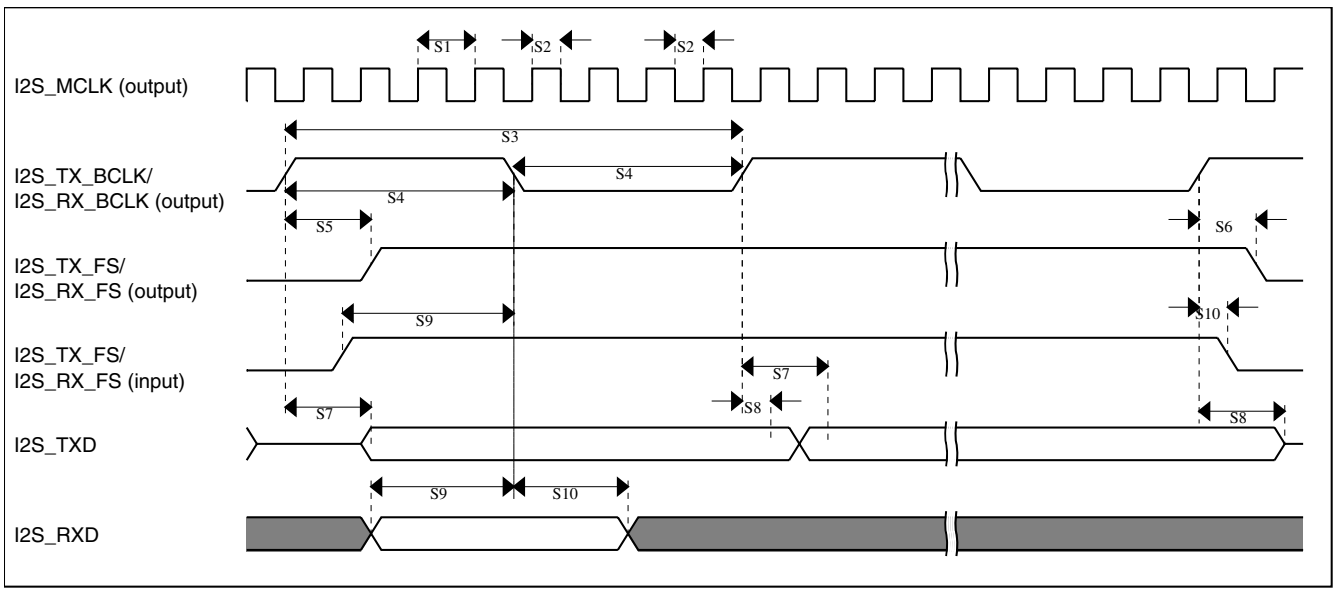



**Figure 27. I2S/SAI timing — master modes**

**Table 44. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)**

| Num. | Characteristic | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V |
| S11 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (input) | 250 | — | ns |
| S12 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input) | 45% | 55% | MCLK period |
| S13 | I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK | 30 | — | ns |
| S14 | I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK | 7.6 | — | ns |
| S15 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid | — | 67 | ns |
| S16 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid | 0 | — | ns |

*Table continues on the next page...*

**Table 44. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range) (continued)**

| Num. | Characteristic | Min. | Max. | Unit |
|---|---|---|---|---|
| S17 | I2S_RXD setup before I2S_RX_BCLK | 30 | — | ns |
| S18 | I2S_RXD hold after I2S_RX_BCLK | 6.5 | — | ns |
| S19 | I2S_TX_FS input assertion to I2S_TXD output valid[1] | — | 72 | ns |

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

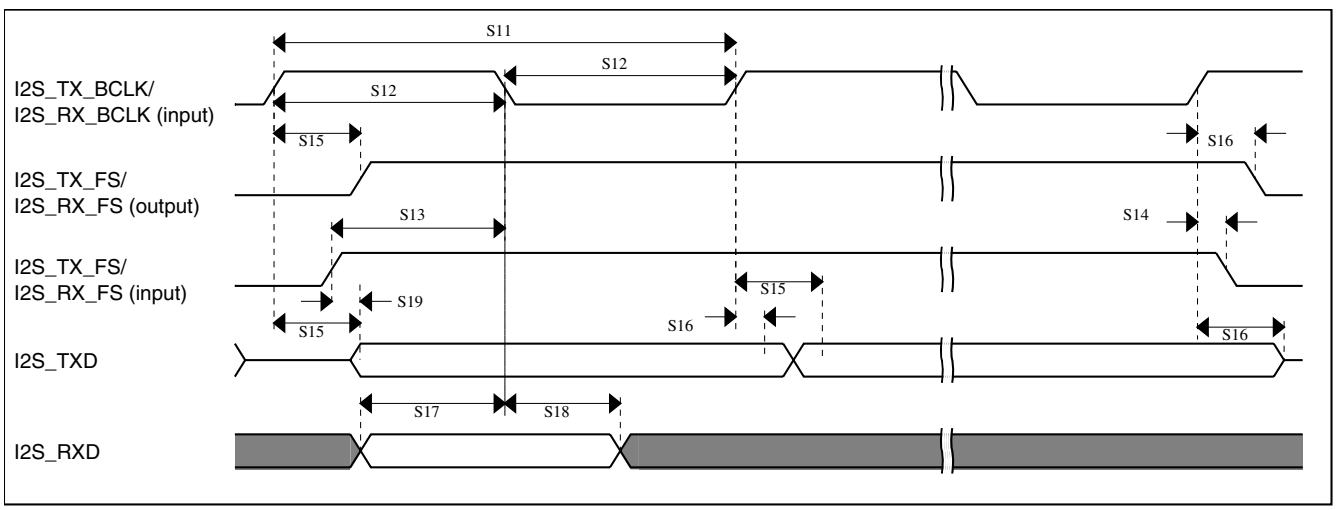



**Figure 28. I2S/SAI timing — slave modes**

# 6.9 Human-machine interfaces (HMI)

## 6.9.1 TSI electrical specifications

**Table 45. TSI electrical specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{DDTSI}$ | Operating voltage | 1.71 | — | 3.6 | V | |
| $C_{ELE}$ | Target electrode capacitance range | 1 | 20 | 500 | pF | 1 |
| $f_{REFmax}$ | Reference oscillator frequency | — | 8 | 15 | MHz | 2, 3 |
| $f_{ELEmax}$ | Electrode oscillator frequency | — | 1 | 1.8 | MHz | 2, 4 |
| $C_{REF}$ | Internal reference capacitor | — | 1 | — | pF | |
| $V_{DELTA}$ | Oscillator delta voltage | — | 500 | — | mV | 2, 5 |
| $I_{REF}$ | Reference oscillator current source base current<br>• 2 µA setting (REFCHRG = 0)<br>• 32 µA setting (REFCHRG = 15) | —<br>— | 2<br>36 | 3<br>50 | µA | 2, 6 |

*Table continues on the next page...*

**Table 45. TSI electrical specifications (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{ELE}$ | Electrode oscillator current source base current<br>• 2 µA setting (EXTCHRG = 0)<br>• 32 µA setting (EXTCHRG = 15) | —<br>— | 2<br>36 | 3<br>50 | µA | 2, 7 |
| Pres5 | Electrode capacitance measurement precision | — | 8.3333 | 38400 | fF/count | 8 |
| Pres20 | Electrode capacitance measurement precision | — | 8.3333 | 38400 | fF/count | 9 |
| Pres100 | Electrode capacitance measurement precision | — | 8.3333 | 38400 | fF/count | 10 |
| MaxSens | Maximum sensitivity | 0.008 | 1.46 | — | fF/count | 11 |
| Res | Resolution | — | — | 16 | bits | |
| $T_{Con20}$ | Response time @ 20 pF | 8 | 15 | 25 | µs | 12 |
| $I_{TSI_RUN}$ | Current added in run mode | — | 55 | — | µA | |
| $I_{TSI_LP}$ | Low power mode current adder | — | 1.3 | 2.5 | µA | 13 |

1. The TSI module is functional with capacitance values outside this range. However, optimal performance is not guaranteed.
2. Fixed external capacitance of 20 pF.
3. REFCHRG = 2, EXTCHRG=0.
4. REFCHRG = 0, EXTCHRG = 10.
5. $V_{DD}$ = 3.0 V.
6. The programmable current source value is generated by multiplying the SCANC[REFCHRG] value and the base current.
7. The programmable current source value is generated by multiplying the SCANC[EXTCHRG] value and the base current.
8. Measured with a 5 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 8; Iext = 16.
9. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 2; Iext = 16.
10. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 16, NSCN = 3; Iext = 16.
11. Sensitivity defines the minimum capacitance change when a single count from the TSI module changes. Sensitivity depends on the configuration used. The documented values are provided as examples calculated for a specific configuration of operating conditions using the following equation: $(C_{ref} * I_{ext})/( I_{ref} * PS * NSCN)$

    The typical value is calculated with the following configuration:

    $I_{ext} = 6$ µA (EXTCHRG = 2), PS = 128, NSCN = 2, $I_{ref} = 16$ µA (REFCHRG = 7), $C_{ref}$ = 1.0 pF

    The minimum value is calculated with the following configuration:

    $I_{ext} = 2$ µA (EXTCHRG = 0), PS = 128, NSCN = 32, $I_{ref} = 32$ µA (REFCHRG = 15), $C_{ref}$ = 0.5 pF

    The highest possible sensitivity is the minimum value because it represents the smallest possible capacitance that can be measured by a single count.
12. Time to do one complete measurement of the electrode. Sensitivity resolution of 0.0133 pF, PS = 0, NSCN = 0, 1 electrode, EXTCHRG = 7.
13. REFCHRG=0, EXTCHRG=4, PS=7, NSCN=0F, LPSCNITV=F, LPO is selected (1 kHz), and fixed external capacitance of 20 pF. Data is captured with an average of 7 periods window.

# 7 Dimensions

## 7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to www.freescale.com and perform a keyword search for the drawing's document number:

| If you want the drawing for this package | Then use this document number |
|---|---|
| 100-pin LQFP | 98ASS23308W |
| 121-pin MAPBGA | 98ASA00344D |

# 8 Pinout

## 8.1 K10 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

| 121 MAP BGA | 100 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E4 | 1 | PTE0 | ADC1_SE4a | ADC1_SE4a | PTE0 | SPI1_PCS1 | UART1_TX | | | I2C1_SDA | RTC_CLKOUT | |
| E3 | 2 | PTE1/ LLWU_P0 | ADC1_SE5a | ADC1_SE5a | PTE1/ LLWU_P0 | SPI1_SOUT | UART1_RX | | | I2C1_SCL | SPI1_SIN | |
| E2 | 3 | PTE2/ LLWU_P1 | ADC1_SE6a | ADC1_SE6a | PTE2/ LLWU_P1 | SPI1_SCK | UART1_CTS_ b | | | | | |
| F4 | 4 | PTE3 | ADC1_SE7a | ADC1_SE7a | PTE3 | SPI1_SIN | UART1_RTS_ b | | | | SPI1_SOUT | |
| E7 | — | VDD | VDD | VDD | | | | | | | | |
| F7 | — | VSS | VSS | VSS | | | | | | | | |
| H7 | 5 | PTE4/ LLWU_P2 | DISABLED | | PTE4/ LLWU_P2 | SPI1_PCS0 | UART3_TX | | | | | |
| G4 | 6 | PTE5 | DISABLED | | PTE5 | SPI1_PCS2 | UART3_RX | | | | | |
| F3 | 7 | PTE6 | DISABLED | | PTE6 | SPI1_PCS3 | UART3_CTS_ b | I2S0_MCLK | | | | |
| E6 | 8 | VDD | VDD | VDD | | | | | | | | |
| G7 | 9 | VSS | VSS | VSS | | | | | | | | |
| F1 | 10 | PTE16 | ADC0_SE4a | ADC0_SE4a | PTE16 | SPI0_PCS0 | UART2_TX | FTM_CLKIN0 | | FTM0_FLT3 | | |
| F2 | 11 | PTE17 | ADC0_SE5a | ADC0_SE5a | PTE17 | SPI0_SCK | UART2_RX | FTM_CLKIN1 | | LPTMR0_ ALT3 | | |
| G1 | 12 | PTE18 | ADC0_SE6a | ADC0_SE6a | PTE18 | SPI0_SOUT | UART2_CTS_ b | I2C0_SDA | | | | |
| G2 | 13 | PTE19 | ADC0_SE7a | ADC0_SE7a | PTE19 | SPI0_SIN | UART2_RTS_ b | I2C0_SCL | | | | |
| L6 | — | VSS | VSS | VSS | | | | | | | | |
| H1 | 14 | ADC0_DP1 | ADC0_DP1 | ADC0_DP1 | | | | | | | | |
| H2 | 15 | ADC0_DM1 | ADC0_DM1 | ADC0_DM1 | | | | | | | | |
| J1 | 16 | ADC1_DP1 | ADC1_DP1 | ADC1_DP1 | | | | | | | | |

| 121 MAP BGA | 100 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| J2 | 17 | ADC1_DM1 | ADC1_DM1 | ADC1_DM1 | | | | | | | | |
| K1 | 18 | PGA0_DP/ ADC0_DP0/ ADC1_DP3 | PGA0_DP/ ADC0_DP0/ ADC1_DP3 | PGA0_DP/ ADC0_DP0/ ADC1_DP3 | | | | | | | | |
| K2 | 19 | PGA0_DM/ ADC0_DM0/ ADC1_DM3 | PGA0_DM/ ADC0_DM0/ ADC1_DM3 | PGA0_DM/ ADC0_DM0/ ADC1_DM3 | | | | | | | | |
| L1 | 20 | PGA1_DP/ ADC1_DP0/ ADC0_DP3 | PGA1_DP/ ADC1_DP0/ ADC0_DP3 | PGA1_DP/ ADC1_DP0/ ADC0_DP3 | | | | | | | | |
| L2 | 21 | PGA1_DM/ ADC1_DM0/ ADC0_DM3 | PGA1_DM/ ADC1_DM0/ ADC0_DM3 | PGA1_DM/ ADC1_DM0/ ADC0_DM3 | | | | | | | | |
| F5 | 22 | VDDA | VDDA | VDDA | | | | | | | | |
| G5 | 23 | VREFH | VREFH | VREFH | | | | | | | | |
| G6 | 24 | VREFL | VREFL | VREFL | | | | | | | | |
| F6 | 25 | VSSA | VSSA | VSSA | | | | | | | | |
| L3 | 26 | VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18 | VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18 | VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18 | | | | | | | | |
| K5 | 27 | DAC0_OUT/ CMP1_IN3/ ADC0_SE23 | DAC0_OUT/ CMP1_IN3/ ADC0_SE23 | DAC0_OUT/ CMP1_IN3/ ADC0_SE23 | | | | | | | | |
| L7 | — | RTC_ WAKEUP_B | RTC_ WAKEUP_B | RTC_ WAKEUP_B | | | | | | | | |
| L4 | 28 | XTAL32 | XTAL32 | XTAL32 | | | | | | | | |
| L5 | 29 | EXTAL32 | EXTAL32 | EXTAL32 | | | | | | | | |
| K6 | 30 | VBAT | VBAT | VBAT | | | | | | | | |
| H5 | 31 | PTE24 | ADC0_SE17 | ADC0_SE17 | PTE24 | | UART4_TX | | | EWM_OUT_b | | |
| J5 | 32 | PTE25 | ADC0_SE18 | ADC0_SE18 | PTE25 | | UART4_RX | | | EWM_IN | | |
| H6 | 33 | PTE26 | DISABLED | | PTE26 | | UART4_CTS_ b | | | RTC_CLKOUT | | |
| J6 | 34 | PTA0 | JTAG_TCLK/ SWD_CLK/ EZP_CLK | TSI0_CH1 | PTA0 | UART0_CTS_ b/ UART0_COL_ b | FTM0_CH5 | | | | JTAG_TCLK/ SWD_CLK | EZP_CLK |
| H8 | 35 | PTA1 | JTAG_TDI/ EZP_DI | TSI0_CH2 | PTA1 | UART0_RX | FTM0_CH6 | | | | JTAG_TDI | EZP_DI |
| J7 | 36 | PTA2 | JTAG_TDO/ TRACE_SWO/ EZP_DO | TSI0_CH3 | PTA2 | UART0_TX | FTM0_CH7 | | | | JTAG_TDO/ TRACE_SWO | EZP_DO |
| H9 | 37 | PTA3 | JTAG_TMS/ SWD_DIO | TSI0_CH4 | PTA3 | UART0_RTS_ b | FTM0_CH0 | | | | JTAG_TMS/ SWD_DIO | |
| J8 | 38 | PTA4/ LLWU_P3 | NMI_b/ EZP_CS_b | TSI0_CH5 | PTA4/ LLWU_P3 | | FTM0_CH1 | | | | NMI_b | EZP_CS_b |

| 121 MAP BGA | 100 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| K7 | 39 | PTA5 | DISABLED | | PTA5 | | FTM0_CH2 | | CMP2_OUT | I2S0_TX_BCLK | JTAG_TRST_b | |
| E5 | 40 | VDD | VDD | VDD | | | | | | | | |
| G3 | 41 | VSS | VSS | VSS | | | | | | | | |
| K8 | 42 | PTA12 | CMP2_IN0 | CMP2_IN0 | PTA12 | CAN0_TX | FTM1_CH0 | | | I2S0_TXD0 | FTM1_QD_PHA | |
| L8 | 43 | PTA13/ LLWU_P4 | CMP2_IN1 | CMP2_IN1 | PTA13/ LLWU_P4 | CAN0_RX | FTM1_CH1 | | | I2S0_TX_FS | FTM1_QD_PHB | |
| K9 | 44 | PTA14 | DISABLED | | PTA14 | SPI0_PCS0 | UART0_TX | | | I2S0_RX_BCLK | I2S0_TXD1 | |
| L9 | 45 | PTA15 | DISABLED | | PTA15 | SPI0_SCK | UART0_RX | | | I2S0_RXD0 | | |
| J10 | 46 | PTA16 | DISABLED | | PTA16 | SPI0_SOUT | UART0_CTS_b/ UART0_COL_b | | | I2S0_RX_FS | I2S0_RXD1 | |
| H10 | 47 | PTA17 | ADC1_SE17 | ADC1_SE17 | PTA17 | SPI0_SIN | UART0_RTS_b | | | I2S0_MCLK | | |
| L10 | 48 | VDD | VDD | VDD | | | | | | | | |
| K10 | 49 | VSS | VSS | VSS | | | | | | | | |
| L11 | 50 | PTA18 | EXTAL0 | EXTAL0 | PTA18 | | FTM0_FLT2 | FTM_CLKIN0 | | | | |
| K11 | 51 | PTA19 | XTAL0 | XTAL0 | PTA19 | | FTM1_FLT0 | FTM_CLKIN1 | | LPTMR0_ALT1 | | |
| J11 | 52 | RESET_b | RESET_b | RESET_b | | | | | | | | |
| G11 | 53 | PTB0/ LLWU_P5 | ADC0_SE8/ ADC1_SE8/ TSI0_CH0 | ADC0_SE8/ ADC1_SE8/ TSI0_CH0 | PTB0/ LLWU_P5 | I2C0_SCL | FTM1_CH0 | | | FTM1_QD_PHA | | |
| G10 | 54 | PTB1 | ADC0_SE9/ ADC1_SE9/ TSI0_CH6 | ADC0_SE9/ ADC1_SE9/ TSI0_CH6 | PTB1 | I2C0_SDA | FTM1_CH1 | | | FTM1_QD_PHB | | |
| G9 | 55 | PTB2 | ADC0_SE12/ TSI0_CH7 | ADC0_SE12/ TSI0_CH7 | PTB2 | I2C0_SCL | UART0_RTS_b | | | FTM0_FLT3 | | |
| G8 | 56 | PTB3 | ADC0_SE13/ TSI0_CH8 | ADC0_SE13/ TSI0_CH8 | PTB3 | I2C0_SDA | UART0_CTS_b/ UART0_COL_b | | | FTM0_FLT0 | | |
| F11 | — | PTB6 | ADC1_SE12 | ADC1_SE12 | PTB6 | | | | FB_AD23 | | | |
| E11 | — | PTB7 | ADC1_SE13 | ADC1_SE13 | PTB7 | | | | FB_AD22 | | | |
| D11 | — | PTB8 | DISABLED | | PTB8 | | UART3_RTS_b | | FB_AD21 | | | |
| E10 | 57 | PTB9 | DISABLED | | PTB9 | SPI1_PCS1 | UART3_CTS_b | | FB_AD20 | | | |
| D10 | 58 | PTB10 | ADC1_SE14 | ADC1_SE14 | PTB10 | SPI1_PCS0 | UART3_RX | | FB_AD19 | FTM0_FLT1 | | |
| C10 | 59 | PTB11 | ADC1_SE15 | ADC1_SE15 | PTB11 | SPI1_SCK | UART3_TX | | FB_AD18 | FTM0_FLT2 | | |
| — | 60 | VSS | VSS | VSS | | | | | | | | |
| — | 61 | VDD | VDD | VDD | | | | | | | | |
| B10 | 62 | PTB16 | TSI0_CH9 | TSI0_CH9 | PTB16 | SPI1_SOUT | UART0_RX | | FB_AD17 | EWM_IN | | |

| 121 MAP BGA | 100 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E9 | 63 | PTB17 | TSI0_CH10 | TSI0_CH10 | PTB17 | SPI1_SIN | UART0_TX | | FB_AD16 | EWM_OUT_b | | |
| D9 | 64 | PTB18 | TSI0_CH11 | TSI0_CH11 | PTB18 | CAN0_TX | FTM2_CH0 | I2S0_TX_BCLK | FB_AD15 | FTM2_QD_PHA | | |
| C9 | 65 | PTB19 | TSI0_CH12 | TSI0_CH12 | PTB19 | CAN0_RX | FTM2_CH1 | I2S0_TX_FS | FB_OE_b | FTM2_QD_PHB | | |
| F10 | 66 | PTB20 | DISABLED | | PTB20 | | | | FB_AD31 | CMP0_OUT | | |
| F9 | 67 | PTB21 | DISABLED | | PTB21 | | | | FB_AD30 | CMP1_OUT | | |
| F8 | 68 | PTB22 | DISABLED | | PTB22 | | | | FB_AD29 | CMP2_OUT | | |
| E8 | 69 | PTB23 | DISABLED | | PTB23 | | SPI0_PCS5 | | FB_AD28 | | | |
| B9 | 70 | PTC0 | ADC0_SE14/ TSI0_CH13 | ADC0_SE14/ TSI0_CH13 | PTC0 | SPI0_PCS4 | PDB0_EXTRG | | FB_AD14 | I2S0_TXD1 | | |
| D8 | 71 | PTC1/ LLWU_P6 | ADC0_SE15/ TSI0_CH14 | ADC0_SE15/ TSI0_CH14 | PTC1/ LLWU_P6 | SPI0_PCS3 | UART1_RTS_b | FTM0_CH0 | FB_AD13 | I2S0_TXD0 | | |
| C8 | 72 | PTC2 | ADC0_SE4b/ CMP1_IN0/ TSI0_CH15 | ADC0_SE4b/ CMP1_IN0/ TSI0_CH15 | PTC2 | SPI0_PCS2 | UART1_CTS_b | FTM0_CH1 | FB_AD12 | I2S0_TX_FS | | |
| B8 | 73 | PTC3/ LLWU_P7 | CMP1_IN1 | CMP1_IN1 | PTC3/ LLWU_P7 | SPI0_PCS1 | UART1_RX | FTM0_CH2 | CLKOUT | I2S0_TX_BCLK | | |
| — | 74 | VSS | VSS | VSS | | | | | | | | |
| — | 75 | VDD | VDD | VDD | | | | | | | | |
| A8 | 76 | PTC4/ LLWU_P8 | DISABLED | | PTC4/ LLWU_P8 | SPI0_PCS0 | UART1_TX | FTM0_CH3 | FB_AD11 | CMP1_OUT | | |
| D7 | 77 | PTC5/ LLWU_P9 | DISABLED | | PTC5/ LLWU_P9 | SPI0_SCK | LPTMR0_ALT2 | I2S0_RXD0 | FB_AD10 | CMP0_OUT | | |
| C7 | 78 | PTC6/ LLWU_P10 | CMP0_IN0 | CMP0_IN0 | PTC6/ LLWU_P10 | SPI0_SOUT | PDB0_EXTRG | I2S0_RX_BCLK | FB_AD9 | I2S0_MCLK | | |
| B7 | 79 | PTC7 | CMP0_IN1 | CMP0_IN1 | PTC7 | SPI0_SIN | | I2S0_RX_FS | FB_AD8 | | | |
| A7 | 80 | PTC8 | ADC1_SE4b/ CMP0_IN2 | ADC1_SE4b/ CMP0_IN2 | PTC8 | | | I2S0_MCLK | FB_AD7 | | | |
| D6 | 81 | PTC9 | ADC1_SE5b/ CMP0_IN3 | ADC1_SE5b/ CMP0_IN3 | PTC9 | | | I2S0_RX_BCLK | FB_AD6 | FTM2_FLT0 | | |
| C6 | 82 | PTC10 | ADC1_SE6b | ADC1_SE6b | PTC10 | I2C1_SCL | | I2S0_RX_FS | FB_AD5 | | | |
| C5 | 83 | PTC11/ LLWU_P11 | ADC1_SE7b | ADC1_SE7b | PTC11/ LLWU_P11 | I2C1_SDA | | I2S0_RXD1 | FB_RW_b | | | |
| B6 | 84 | PTC12 | DISABLED | | PTC12 | | UART4_RTS_b | | FB_AD27 | | | |
| A6 | 85 | PTC13 | DISABLED | | PTC13 | | UART4_CTS_b | | FB_AD26 | | | |
| A5 | 86 | PTC14 | DISABLED | | PTC14 | | UART4_RX | | FB_AD25 | | | |
| B5 | 87 | PTC15 | DISABLED | | PTC15 | | UART4_TX | | FB_AD24 | | | |
| — | 88 | VSS | VSS | VSS | | | | | | | | |
| — | 89 | VDD | VDD | VDD | | | | | | | | |
| D5 | 90 | PTC16 | DISABLED | | PTC16 | | UART3_RX | | FB_CS5_b/ FB_TSIZ1/ FB_BE23_16_b | | | |

| 121 MAP BGA | 100 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C4 | 91 | PTC17 | DISABLED | | PTC17 | | UART3_TX | | FB_CS4_b/ FB_TSIZ0/ FB_BE31_24_ b | | | |
| B4 | 92 | PTC18 | DISABLED | | PTC18 | | UART3_RTS_ b | | FB_TBST_b/ FB_CS2_b/ FB_BE15_8_b | | | |
| A4 | — | PTC19 | DISABLED | | PTC19 | | UART3_CTS_ b | | FB_CS3_b/ FB_BE7_0_b | FB_TA_b | | |
| D4 | 93 | PTD0/ LLWU_P12 | DISABLED | | PTD0/ LLWU_P12 | SPI0_PCS0 | UART2_RTS_ b | | FB_ALE/ FB_CS1_b/ FB_TS_b | | | |
| D3 | 94 | PTD1 | ADC0_SE5b | ADC0_SE5b | PTD1 | SPI0_SCK | UART2_CTS_ b | | FB_CS0_b | | | |
| C3 | 95 | PTD2/ LLWU_P13 | DISABLED | | PTD2/ LLWU_P13 | SPI0_SOUT | UART2_RX | | FB_AD4 | | | |
| B3 | 96 | PTD3 | DISABLED | | PTD3 | SPI0_SIN | UART2_TX | | FB_AD3 | | | |
| A3 | 97 | PTD4/ LLWU_P14 | DISABLED | | PTD4/ LLWU_P14 | SPI0_PCS1 | UART0_RTS_ b | FTM0_CH4 | FB_AD2 | EWM_IN | | |
| A2 | 98 | PTD5 | ADC0_SE6b | ADC0_SE6b | PTD5 | SPI0_PCS2 | UART0_CTS_ b/ UART0_COL_ b | FTM0_CH5 | FB_AD1 | EWM_OUT_b | | |
| B2 | 99 | PTD6/ LLWU_P15 | ADC0_SE7b | ADC0_SE7b | PTD6/ LLWU_P15 | SPI0_PCS3 | UART0_RX | FTM0_CH6 | FB_AD0 | FTM0_FLT0 | | |
| A1 | 100 | PTD7 | DISABLED | | PTD7 | CMT_IRO | UART0_TX | FTM0_CH7 | | FTM0_FLT1 | | |
| A11 | — | NC | NC | NC | | | | | | | | |
| B11 | — | NC | NC | NC | | | | | | | | |
| C11 | — | NC | NC | NC | | | | | | | | |
| K3 | — | NC | NC | NC | | | | | | | | |
| H4 | — | NC | NC | NC | | | | | | | | |
| J3 | — | NC | NC | NC | | | | | | | | |
| H3 | — | NC | NC | NC | | | | | | | | |
| K4 | — | NC | NC | NC | | | | | | | | |
| J9 | — | NC | NC | NC | | | | | | | | |
| J4 | — | NC | NC | NC | | | | | | | | |
| H11 | — | NC | NC | NC | | | | | | | | |
| A10 | — | NC | NC | NC | | | | | | | | |
| A9 | — | NC | NC | NC | | | | | | | | |
| B1 | — | NC | NC | NC | | | | | | | | |
| C2 | — | NC | NC | NC | | | | | | | | |
| C1 | — | NC | NC | NC | | | | | | | | |
| D2 | — | NC | NC | NC | | | | | | | | |
| D1 | — | NC | NC | NC | | | | | | | | |
| E1 | — | NC | NC | NC | | | | | | | | |

## 8.2 K10 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

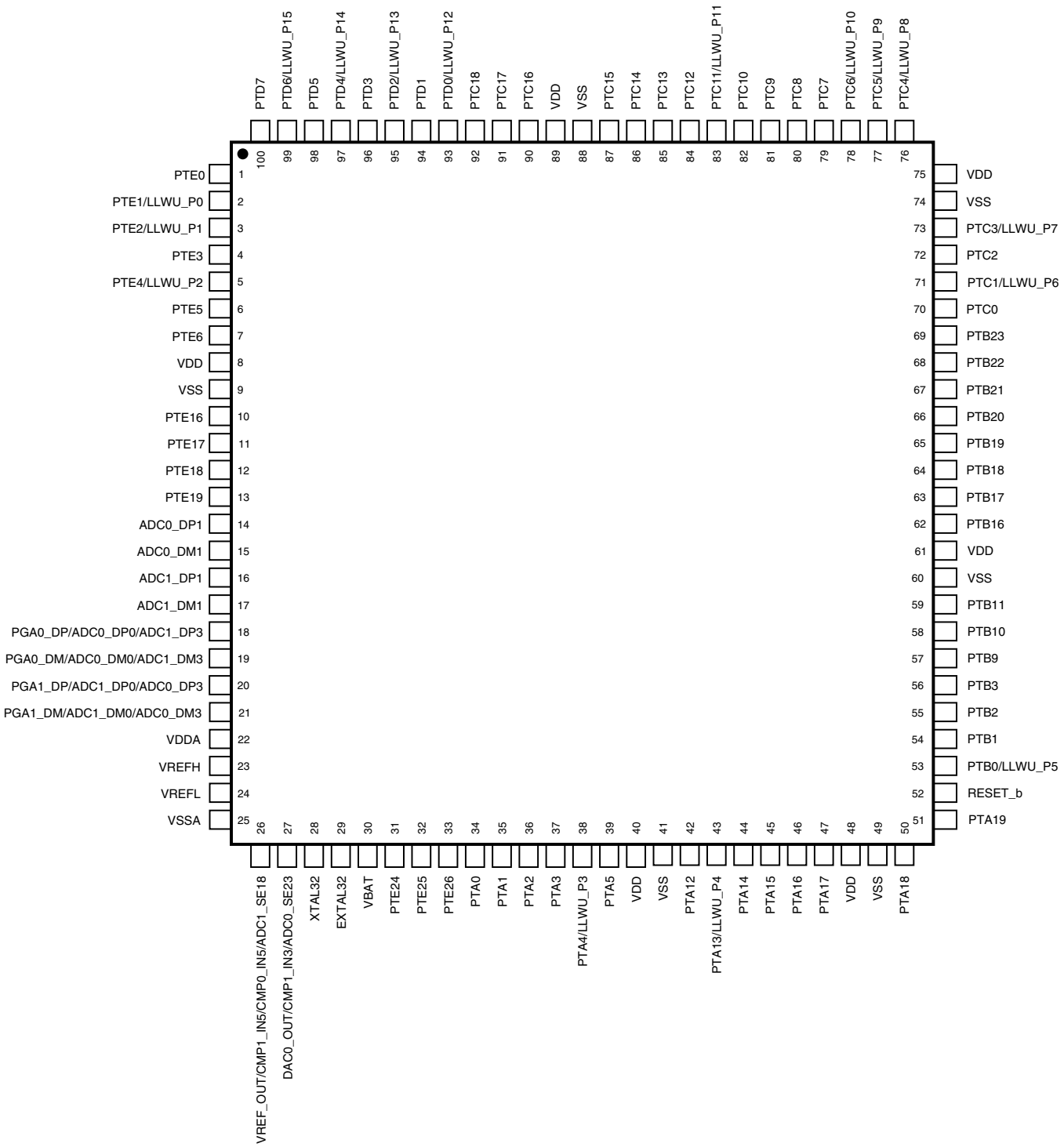



**Figure 29. K10 100 LQFP Pinout Diagram**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | PTD7 | PTD5 | PTD4/ LLWU_P14 | PTC19 | PTC14 | PTC13 | PTC8 | PTC4/ LLWU_P8 | NC | NC | NC | A |
| B | NC | PTD6/ LLWU_P15 | PTD3 | PTC18 | PTC15 | PTC12 | PTC7 | PTC3/ LLWU_P7 | PTC0 | PTB16 | NC | B |
| C | NC | NC | PTD2/ LLWU_P13 | PTC17 | PTC11/ LLWU_P11 | PTC10 | PTC6/ LLWU_P10 | PTC2 | PTB19 | PTB11 | NC | C |
| D | NC | NC | PTD1 | PTD0/ LLWU_P12 | PTC16 | PTC9 | PTC5/ LLWU_P9 | PTC1/ LLWU_P6 | PTB18 | PTB10 | PTB8 | D |
| E | NC | PTE2/ LLWU_P1 | PTE1/ LLWU_P0 | PTE0 | VDD | VDD | VDD | PTB23 | PTB17 | PTB9 | PTB7 | E |
| F | PTE16 | PTE17 | PTE6 | PTE3 | VDDA | VSSA | VSS | PTB22 | PTB21 | PTB20 | PTB6 | F |
| G | PTE18 | PTE19 | VSS | PTE5 | VREFH | VREFL | VSS | PTB3 | PTB2 | PTB1 | PTB0/ LLWU_P5 | G |
| H | ADC0_DP1 | ADC0_DM1 | NC | NC | PTE24 | PTE26 | PTE4/ LLWU_P2 | PTA1 | PTA3 | PTA17 | NC | H |
| J | ADC1_DP1 | ADC1_DM | NC | NC | PTE25 | PTA0 | PTA2 | PTA4/ LLWU_P3 | NC | PTA16 | RESET_b | J |
| K | PGA0_DP/ ADC0_DP0/ ADC1_DP3 | PGA0_DM/ ADC0_DM0/ ADC1_DM3 | NC | NC | DAC0_OUT/ CMP1_IN3/ ADC0_SE23 | VBAT | PTA5 | PTA12 | PTA14 | VSS | PTA19 | K |
| L | PGA1_DP/ ADC1_DP0/ ADC0_DP3 | PGA1_DM/ ADC1_DM0/ ADC0_DM3 | VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18 | XTAL32 | EXTAL32 | VSS | RTC_ WAKEUP_B | PTA13/ LLWU_P4 | PTA15 | VDD | PTA18 | L |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | |

**Figure 30. K10 121 MAPBGA Pinout Diagram**

# 9 Revision History

The following table provides a revision history for this document.

**Table 46. Revision History**

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| 1 | 3/2012 | Initial public release |

*Table continues on the next page...*

## Table 46. Revision History (continued)

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| 2 | 4/2012 | • Replaced TBDs throughout.<br>• Updated "Power consumption operating behaviors" table.<br>• Updated "ADC electrical specifications" section.<br>• Updated "VREF full-range operating behaviors" table.<br>• Updated "I2S/SAI Switching Specifications" section.<br>• Updated "TSI electrical specifications" table. |
| 3 | 11/2012 | • Updated orderable part numbers.<br>• Updated the maximum input voltage ($V_{ADIN}$) specification in the "16-bit ADC operating conditions" section. |

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