

DEMO9S12NE64

User's Manual

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User's Manual — DEMO9S12NE64 User's Manual

Section 1. General Information

1.1 Introduction

This user's manual explains connection and configuration of the Freescale DEMO9S12NE64. The DEMO9S12NE64 makes possible the development of code for target systems based on the MC9S12NE64 microcontroller unit (MCU). To set up and run the included demo program, please refer to the Quick Start guide supplied with the DEMO9S12NE64. There is also a soft copy of the quick start guide on the included resource CD.

1.2 System Requirements

An IBM PC or compatible running Windows® 98, Windows 2000, Windows NT® (version 4.0), or Windows® XP with at least 32MB of RAM an RS-232 serial port, and an Ethernet network card.

1.3 DEMO9S12NE64 Layout

- Figure 1-1 shows the case silk on the top of the DEMO9S12NE64
- Figure 1-2 and Figure 1-3 show the top and bottom side layout of the DEMO9S12NE64
- U1 is the MC9S12NE64 MCU in an LQFP 112 pin package
- S1 is user switch 1 (SW1) which is connected to I/O pin PE<0>. S2 is user switch 2 (SW2) which is connected to I/O pin PH<4>. S3 is the reset switch
- DS1 is user LED 1 which is connected to I/O pin PG<0>. DS2 is user LED 2 which is connected to I/O pin PG<1>. DS3 is the power LED and indicates 3.3 VDC out of the on-board voltage regulator.
- VR1 is a potentiometer that controls a variable voltage input to the Analog to Digital (ADC) input pin PAD<0>.

- J3 is the Background Debug Mode (BDM) header. It is a 2x3 100 mil center header compatible with BDM programming hardware such as P&E's Multilink.
- J50 is a 40-pin I/O connector that can be used to interface with other boards.
- J51 is the Ethernet connector that connects the DEMO9S12NE64 to the network card of a PC via the included Crossover Ethernet cable.
- J52 is barrel power socket that accepts a 6.3mm power supply plug. The center pin of this connector is positive.
- J53 is a DB-9 connector connected to the Serial Communication Interface (SCI) of the MC9S12NE64. This connector has a Data Carrier Equipment (DCE) pinout.

S50 is a slide switch (SW3) connected to I/O pin PG<4>. When this switch is in the 1 position PG<4> is pulled high to 3.3 VDC through a 10K ohm resistor. When S50 is in the 0 position PG<4> is tied directly to GND.

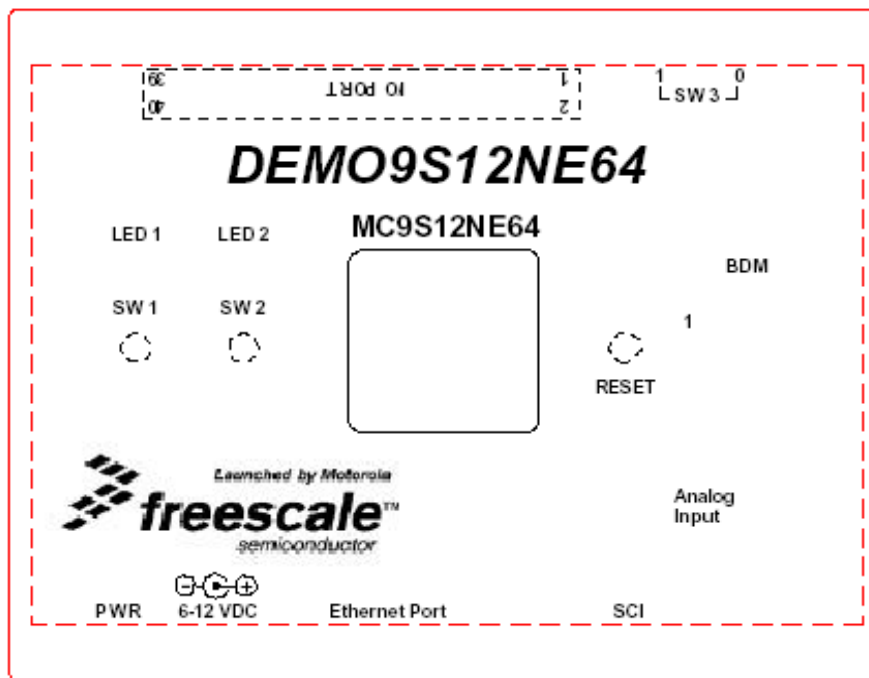


Figure 1-1 DEMO9S12NE64 Case Silk

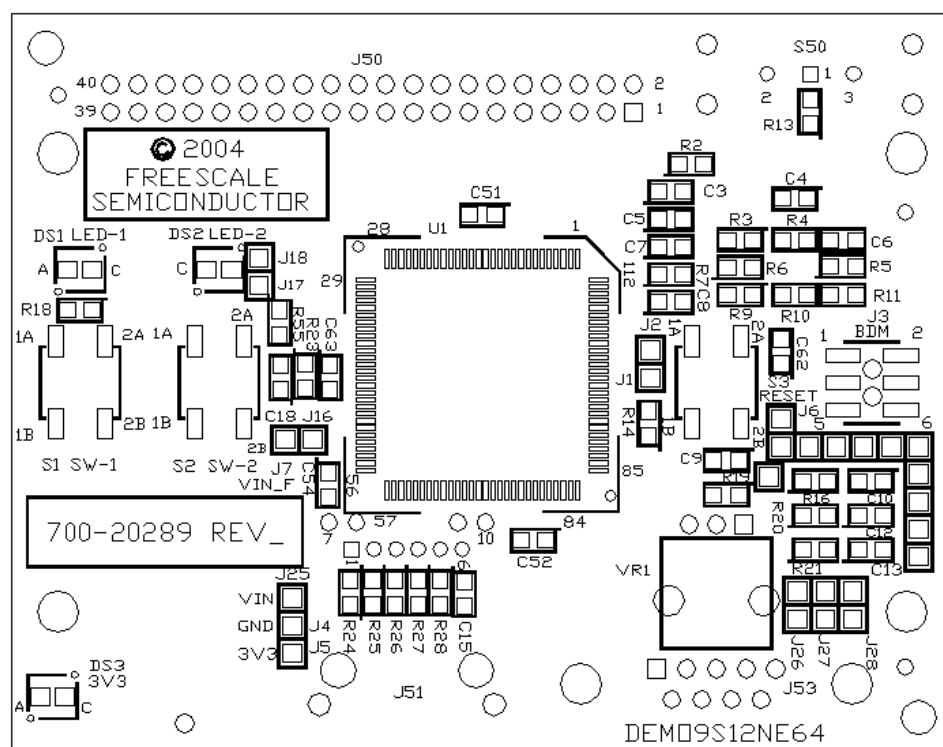


Figure 1-2 DEMO9S12NE64 Top Side

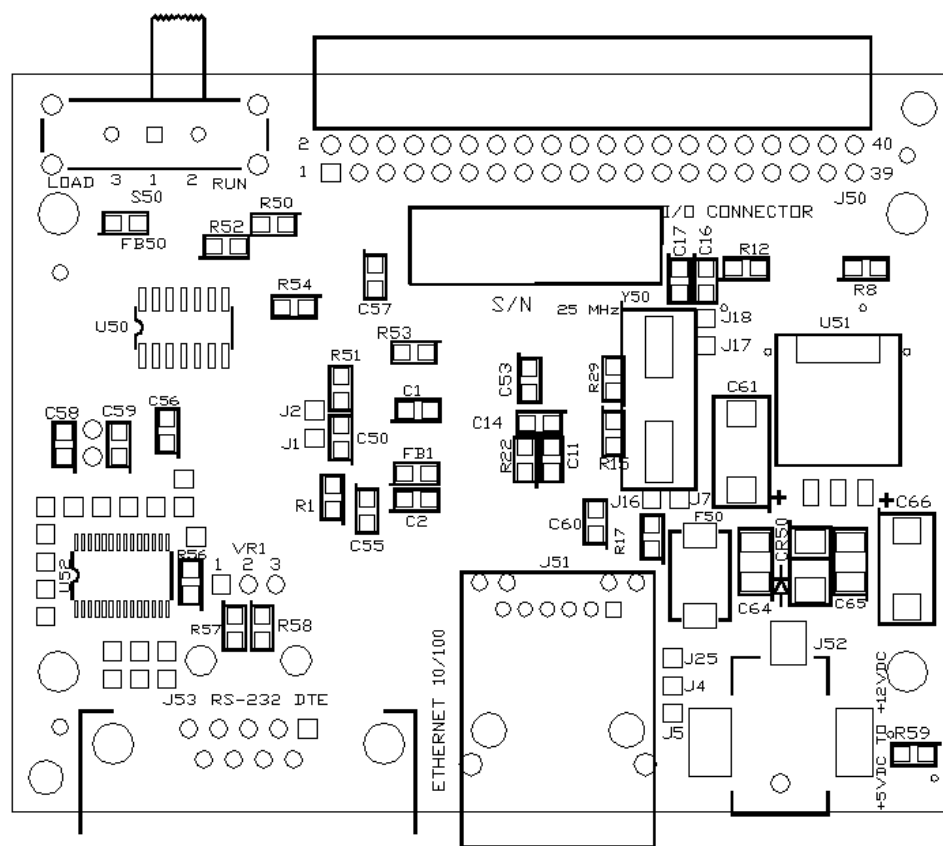


Figure 1-3 DEMO9S12NE64 Bottom Side

1.4 Specifications

Table 1-1 lists DEMO9S12NE64 specifications

Table 1-1 Specifications

| Characteristic | Specifications |
|-------------------------------------|---|
| Maximum Clock speed | 25-MHz at 3.3V (12.5-MHz bus) |
| Temperature operating storage | -10° to +50° C -40° to +85° C |
| MCU Extension I/O | HCMOS Compatible at 3.3V |
| Relative humidity | 0 to 90% (noncondensing) |
| Power requirements | 6 to 12 VDC 0.75 Amp supplied externally. A barrel type power plug is required with an outside diameter of 5.5mm and an inside diameter of 2.1mm. |
| Dimensions | 3.0 X 4.5 X 1.25 inches (76.2 x 114.3 x 31.7 mm) |



User's Manual — DEMO9S12NE64 User's Manual

Section 2. Support Information

2.1 Introduction

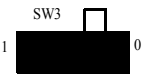
This section explains DEMO9S12NE64 preparation, how to set switches and how to make system connections. It also consists of connector pin assignments, connector signal descriptions, and other information that may be useful in your development activities.

CAUTION: ESD Protection

Freescall development tools contain static-sensitive components. These boards are subject to damage from electrostatic discharge (ESD). To prevent such damage, you must use static-safe work surfaces and grounding straps, as defined in ANSI/EOS/ESD S6.1 and ANSI/EOS/ESD S4.1. All handling of these boards must be in accordance with ANSI/EAI 625.

2.2 Configuring Board Components

Table 2-1 Configuration Components

| Component | Position | Effect |
|-------------|---|---|
| Switch, SW3 |  | <p>SW3: Controls the value of I/O pin PG<4>. In the 1 position (labeled in silk on the case) PG<4> is pulled high to 3.3 VDC through a 10K ohm resistor. In the 0 position, PG<4> is tied directly to GND.</p> <p>This switch is used by the serial monitor to put the monitor into Load or Run mode. To put the monitor into Load mode, set SW3 to the 0 position. To put the monitor into Run mode, set SW3 to the 1 position.</p> |

2.3 I/O Connector J50

Connector J50 is an I/O expansion connector that can be used to interface the DEMO9S12NE64 to other boards. Figure 2-1 and Table 2-2 give the pin assignments and signal descriptions for connector J50.

| J50 | | | | |
|-------|----|-----|----|---------|
| P3_3V | 1 | • • | 2 | IRQ_B |
| GND | 3 | • • | 4 | RESET_B |
| PS<1> | 5 | • • | 6 | PJ<0> |
| PS<0> | 7 | • • | 8 | PJ<1> |
| PH<4> | 9 | • • | 10 | PAD<0> |
| PH<5> | 11 | • • | 12 | PAD<1> |
| PT<4> | 13 | • • | 14 | PAD<2> |
| PT<5> | 15 | • • | 16 | PAD<3> |
| PS<5> | 17 | • • | 18 | PAD<4> |
| PS<4> | 19 | • • | 20 | PAD<5> |
| PS<6> | 21 | • • | 22 | PAD<6> |
| PS<7> | 23 | • • | 24 | PAD<7> |
| PG<0> | 25 | • • | 26 | PJ<6> |
| PG<1> | 27 | • • | 28 | PJ<7> |
| PG<2> | 29 | • • | 30 | PJ<2> |
| PG<3> | 31 | • • | 32 | PJ<3> |
| PG<4> | 33 | • • | 34 | PT<6> |
| PG<5> | 35 | • • | 36 | PT<7> |
| PG<6> | 37 | • • | 38 | PS<2> |
| PG<7> | 39 | • • | 40 | PS<3> |

Figure 2-1 I/O Connector (J50) Pin Assignments

Table 2-2 I/O Connector (J50) Signal Descriptions

| Pin | Label | Signal |
|-----|---------|--|
| 1 | P3_3V | 3.3 VDC supplied from the DEMO9S12NE64 |
| 2 | IRQ_B | IRQ_B, which is also PE1, is always an input and can always be read. This input is used for requesting an asynchronous interrupt to the MCU. When used as an interrupt pin, this signal is active-low |
| 3 | GND | GROUND |
| 4 | RESET_B | Active low bidirectional control signal that acts as an input to initialize the MCU to a known start-up state. It also acts as an open-drain output to indicate that an internal failure has been detected in either the clock monitor or COP watchdog circuit |
| 5 | PS<1> | PS1 is a general purpose input or output. When the Serial Communications Interface 0 (SCI0) transmitter is enabled the PS1 pin is configured as the transmit pin, TXD, of SCI0 |
| 6 | PJ<0> | PJ0 is a general purpose I/O pin. When the EMAC MII interface is enabled it becomes the management data clock(MII_MDC) signal |
| 7 | PS<0> | PS0 is a general purpose input or output. When the Serial Communications Interface 0 (SCI0) receiver is enabled the PS0 pin is configured as the receive pin RXD0 of SCI0 |
| 8 | PJ<1> | PJ1 is a general purpose I/O pin. When the EMAC MII interface is enabled it becomes the Management Data I/O (MII_MDIO) signal |
| 9 | PH<4> | PH4 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the transmit Clock (MII_TXCLK) signal |

Table 2-2 I/O Connector (J50) Signal Descriptions (Continued)

| Pin | Label | Signal |
|--------------------------------|----------------------------|---|
| 10, 12, 14, 16, 18, 20, 22, 24 | PAD<0> - PAD<7> | PAD[7:0] are the analog inputs for the analog to digital converter (ADC). They can also be configured as general purpose digital input |
| 11 | PH<5> | PH5 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the transmit Enabled (MII_TXEN) signal |
| 13, 15, 34, 36 | PT<4>, PT<5>, PT<6>, PT<7> | PT[7:4] are general purpose input or output pins. When the Timer system 1 (TIM1) is enabled they can also be configured as the TIM1 input capture or output compare pins IOC1[7-4] |
| 17 | PS<5> | PS5 is a general purpose input or output pin. When the Serial Peripheral Interface (SPI) is enabled PS5 is the master output (during master mode) or slave input (during slave mode) pin (MOSI) |
| 19 | PS<4> | PS4 is a general purpose input or output pin. When the Serial Peripheral Interface (SPI) is enabled PS4 is the master input (during master mode) or slave output (during slave mode) pin (MISO) |
| 21 | PS<6> | PS6 is a general purpose input or output pin. When the Serial Peripheral Interface (SPI) is enabled PS6 becomes the serial clock pin, SCK |
| 23 | PS<7> | PS7 is a general purpose input or output. When the Serial Peripheral Interface (SPI) is enabled PS7 becomes the slave select pin SS |
| 25 | PG<0> | PG6 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the receive data (MII_RXD0) signal |
| 26 | PJ<6> | PJ6 is a general purpose input or output pin. When the IIC module is enabled it becomes the Serial Data Line (IIC_SDL) for the IIC module (IIC) |
| 27 | PG<1> | PG1 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the receive data (MII_RXD1) signal |
| 28 | PJ<7> | PJ7 is a general purpose input or output pin. When the IIC module is enabled it becomes the serial clock line (IIC_SCL) for the IIC module (IIC) |
| 29 | PG<2> | PG2 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the receive data (MII_RXD2) signal |
| 30 | PJ<2> | PJ2 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the carrier sense (MII_CRS) signal |
| 31 | PG<3> | PG3 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the receive data (MII_RXD3) signal |
| 32 | PJ<3> | PJ3 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the collision (MII_COL) signal |
| 33 | PG<4> | PG4 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the receive clock (MII_RXCLK) signal |
| 35 | PG<5> | PG5 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the receive data valid (MII_RXDV) signal |
| 37 | PG<6> | PG6 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the receive error (MII_RXER) signal |
| 38 | PS<2> | PS2 is a general purpose input or output. When the Serial Communications Interface 1 (SCI1) receiver is enabled the PS2 pin is configured as the receive pin RXD of SCI1 |

Table 2-2 I/O Connector (J50) Signal Descriptions (Continued)

| Pin | Label | Signal |
|-----|-------|--|
| 39 | PG<7> | PG7 is a general purpose input or output pin. It can be configured to generate an interrupt(KWG7) causing the MCU to exit STOP or WAIT mode |
| 40 | PS<3> | PS3 is a general purpose input or output. When the Serial Communications Interface 1 (SCI1) transmitter is enabled the PS3 pin is configured as the transmit pin, TXD, of SCI1 |

2.4 SCI Connector J53

Connector J53 is the SCI connector which is pinned out according to the DCE format. Figure 2-2 and Table 2-3 give pin assignments and signal descriptions for connector J53.

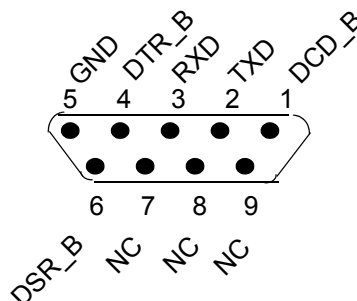


Figure 2-2 SCI Connector J53 Pin Assignments

Table 2-3 SCI Connector J53 Signal Descriptions

| Pin | Label | Signal |
|---------|---------------------|--|
| 1, 4, 6 | DCD_B, DTR_B, DSR_B | Pins 1, 4 and 6 are the active-low Data Carrier Detect, Data Terminal Ready, and Data Set Ready signals. These pins are connected together through zero ohm resistors. To disconnect pin 1 from pin 4, remove R58. To disconnect pin 6 from pin 4, remove R57 |
| 2 | TXD | Pin 2 is the transmit data pin. It is connected to PS<1> of the MC9S12NE64 through a MAX3243 RS-232 Line Driver |
| 3 | RXD | Pin 3 is the receive data pin. It is connected to PS<0> of the MC9S12NE64 through a MAX3243 RS-232 Line Driver |
| 5 | GND | GROUND |
| 7, 8, 9 | NC | Pins 7, 8, and 9 can be used as active-low Request to Send (RTS_B), Clear to Send (CTS_B), and Ring Indicator (RI_B) pins. These pins on J53 are not connected on the DEMO9S12NE64. If these pins need to be utilized, they can be accessed through the unpopulated one pin headers J28, J27, and J26 respectively |

2.5 BDM Connector J3

Connector J3 is the BDM connector. Figure 2-3 and Table 2-4 give the pin assignments and signal descriptions for this connector. You can connect hardware such as P&E’s BDM Multilink to this connector for debugging purposes.

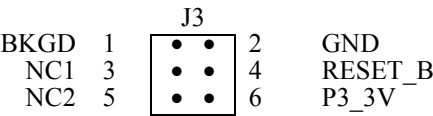


Figure 2-3 BDM Connector J3 Pin Assignments

Table 2-4 BDM Connector J3 Signal Descriptions

| Pin | Label | Signal |
|------|---------|---|
| 1 | BKGD | Background pin used as a pseudo-open-drain pin for background debug communication |
| 2 | GND | GROUND |
| 3, 5 | NC | No connection |
| 4 | RESET_B | Active low bidirectional control signal that acts as an input to initialize the MCU to a known start-up state |
| 6 | P3_3V | 3.3 VDC supplied from the DEMO9S12NE64 |

2.6 Power Connector J52

Connector J52 is the PWR connector. Figure 2-4 and Table 2-5 give the pin assignments and signal descriptions for this connector. This connector accepts a center positive barrel type power plug with an outside diameter of 5.5mm and an inside diameter of 2.1mm. The power circuit accepts input voltages from 6 VDC to 12 VDC and currents up to 0.75 amps.

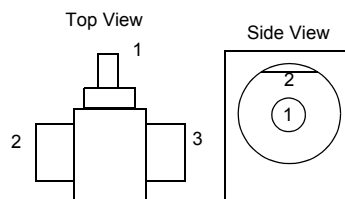


Figure 2-4 Power Connector J52 Pin Assignments

Table 2-5 Power Connector J52 Signal Descriptions

| Pin | Label | Signal |
|-------------|--------|---------------------------------|
| 1 (Center) | VIN | Voltage In, 6-12 VDC, 0.75 Amps |
| 2 (Outside) | SLEEVE | GROUND |
| 3 (Outside) | P_NC | No connection |

2.7 Troubleshooting

When using your DEMO9S12NE64 there are several issues you may run into. Some of these issues and possible solutions are listed below. It may be helpful to refer to the schematic and bill of materials located on the included resource CD.

Issue: I am having trouble running code that performs Ethernet Auto Negotiation

Answer: The DEMO9S12NE64 currently does not support Ethernet Auto Negotiation. The demo code shipped with the DEMO9S12NE64 includes Auto Negotiation code however this feature is turned off. The option for enabling this code is in the file etherinit.h in the line:

```
#define AUTO_NEG 0
```

Setting this definition to 1 will enable Auto Negotiation

Issue: I am having trouble getting the DEMO9S12NE64 to communicate over the ethernet.

Answer: The demo code shipped in the DEMO9S12NE64 has a non IEEE compliant MAC address for example only. If you have more than one DEMO9S12NE64 connected to your network, they will both have the same MAC address and there could be an ethernet conflict. You can change the MAC address in the demo or connection programs by changing the variable hard_address in the file address.c

Issue: I can not get the DEMO9S12NE64 to power up

Answer: Make sure you are using a power supply that is between + 6 VDC and + 12 VDC. It should have a center positive barrel type connector with an inside diameter of 2.1mm and an outside diameter of 5.5mm. When power is connected correctly the green LED marked "PWR" will light up denoting + 3.3 VDC out of the on-board regulator. There is a resettable 0.75A fuse on the DEMO9S12NE64. If you plug in a power supply with the wrong polarity or exceed 0.75A, remove power from the DEMO9S12NE64 for 1 minute before attempting to power up the DEMO9S12NE64 again.

Issue: When trying to program the part through the serial monitor I have the board hooked up correctly but still get a message that says "Could Not Connect to Hardware"

Answer: Make sure you do not have another program, such as a terminal program, using the com port you are trying to program the DEMO9S12NE64 through.

Issue: I have connected the Ethernet port of my DEMO9S12NE64 to my computer, or Local Area Network (LAN), but I am not seeing the correct Ethernet output in the demo program.

Answer: If you are connecting the DEMO9S12NE64 directly to your computer, make sure you are using an Ethernet crossover cable. An Ethernet crossover cable is supplied with your DEMO9S12NE64. If you are connecting the DEMO9S12NE64 to your LAN, you need to use a straight through Ethernet cable.

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